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1983

AMENDEMENT 1
AMENDMENT 1

1987-02

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Amendement 1

Résistances fixes utilisées dans les équipements électroniques

Sixième partie:
Spécification intermédiaire: Réseaux de résistances fixes à résistances mesurables individuellement

Amendment 1

Fixed resistors for use in electronic equipment

Part 6:
Sectional specification: Fixed resistor networks with individually measurable resistors

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PRICE CODE C

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PRÉFACE

La présente modification a été établie par le Comité d'Etudes N° 40 de la CEI: Condensateurs et résistances pour équipements électroniques.

Le texte de cette modification est issu des documents suivants:

Règle des Six Mois	Rapport de vote
40(BC)606	40(BC)648

Pour de plus amples renseignements, consulter le rapport de vote mentionné dans le tableau ci-dessus.

Le numéro QC qui figure sur la page de couverture de la présente publication est le numéro de spécification dans le système CEI d'assurance de la qualité des composants électroniques (IECQ).

Page 2

Ajouter après la Section Trois:

ANNEXE A — Schémas normalisés et identification des sorties pour réseaux de résistances fixes 34

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Ajouter le texte suivant:

ANNEXE A

SCHÉMAS NORMALISÉS ET IDENTIFICATION DES SORTIES POUR RÉSEAUX DE RÉSISTANCES FIXES

A1. Schémas pour les configurations «Simple en ligne»:

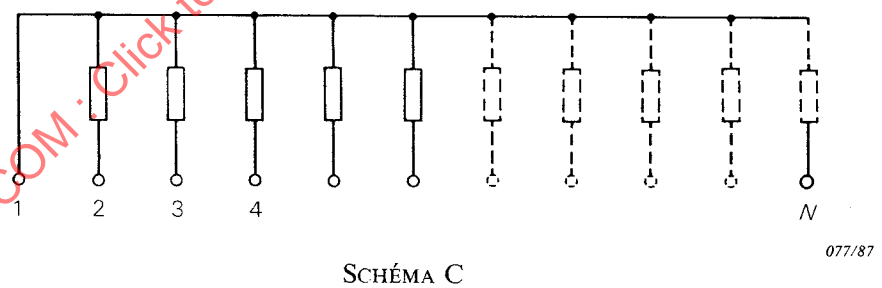

SCHÉMA C

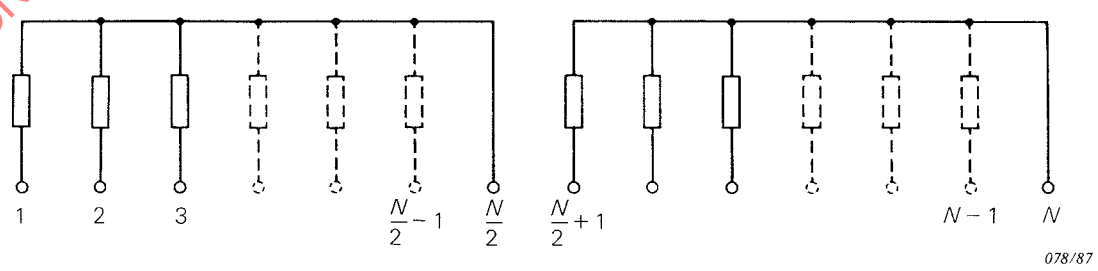

SCHÉMA D

N = nombre de sorties.

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PREFACE

This amendment has been prepared by IEC Technical Committee No. 40: Capacitors and Resistors for Electronic Equipment.

The text of this amendment is based upon the following documents:

Six Months' Rule	Report on Voting
40(CO)606	40(CO)648

Further information can be found in the relevant Report on Voting indicated in the table above.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

Page 3

Add after Section Three:

APPENDIX A — Standardized schematic diagrams and pin identifications for fixed resistor networks 35

Page 35

Include the following text:

APPENDIX A

STANDARDIZED SCHEMATIC DIAGRAMS AND PIN IDENTIFICATIONS FOR FIXED RESISTOR NETWORKS

A1. **Diagrams for "Single-In-Line" configurations:**

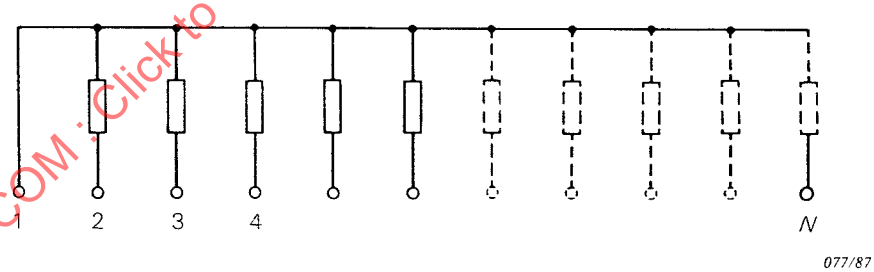

DIAGRAM C

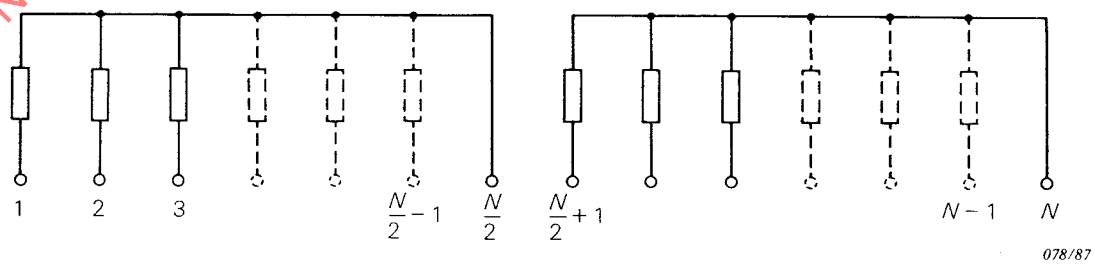

DIAGRAM D

N = number of terminations.

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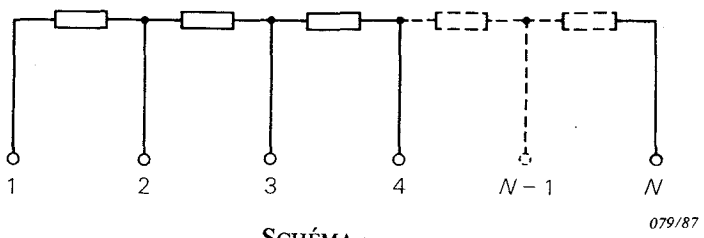

SCHÉMA
DIAGRAM F

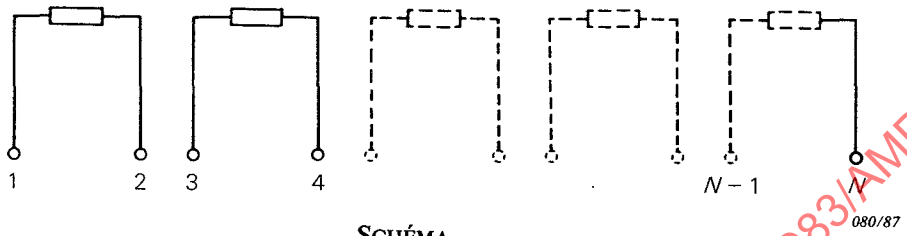

SCHÉMA
DIAGRAM G

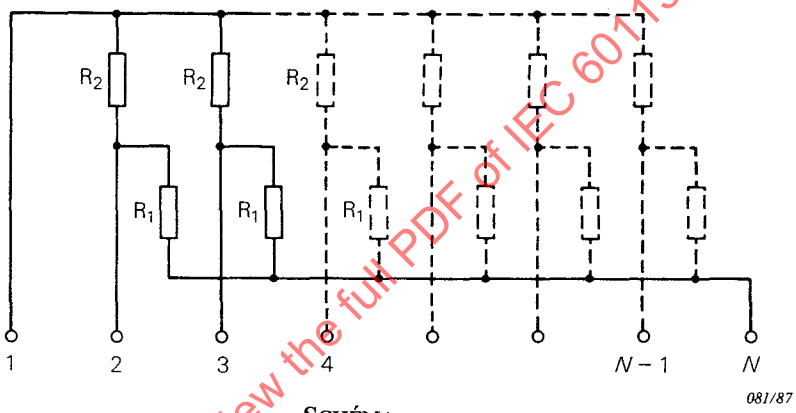

SCHÉMA
DIAGRAM H

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A2. **Schémas pour les configurations «Double en ligne» et «Boîtier plat»:**
Diagrams for "Dual-In-Line" and "Flat Pack" configurations:

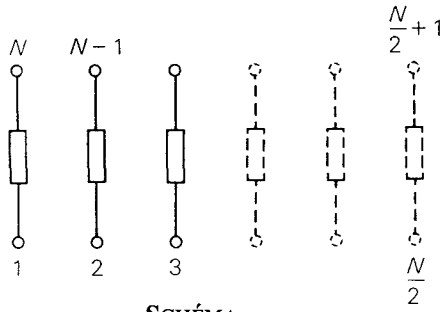

SCHÉMA
DIAGRAM A

N = nombre de sorties
number of terminations

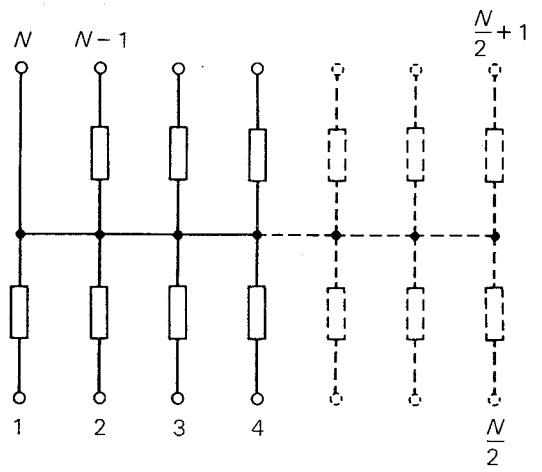

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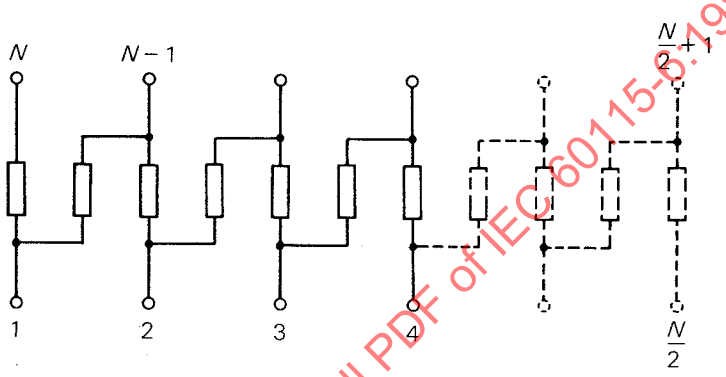
SCHÉMA B
DIAGRAM B



084/87

SCHÉMA E
DIAGRAM E

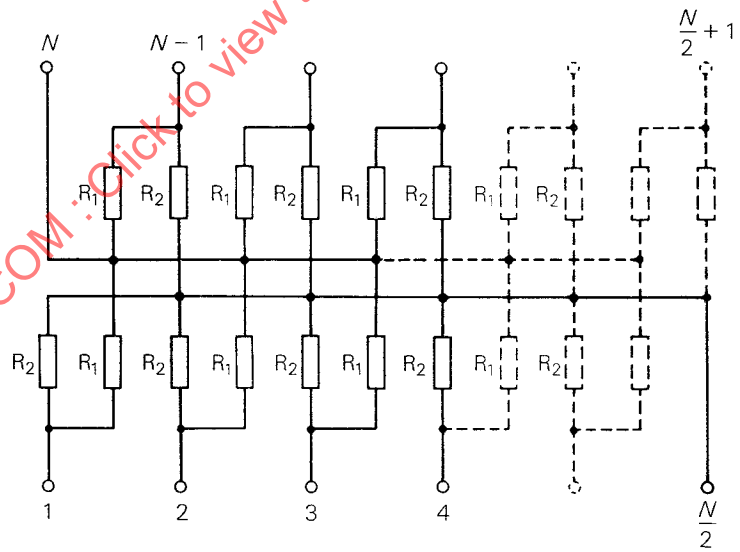


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SCHÉMA J
DIAGRAM J

N = nombre de sorties
number of terminations

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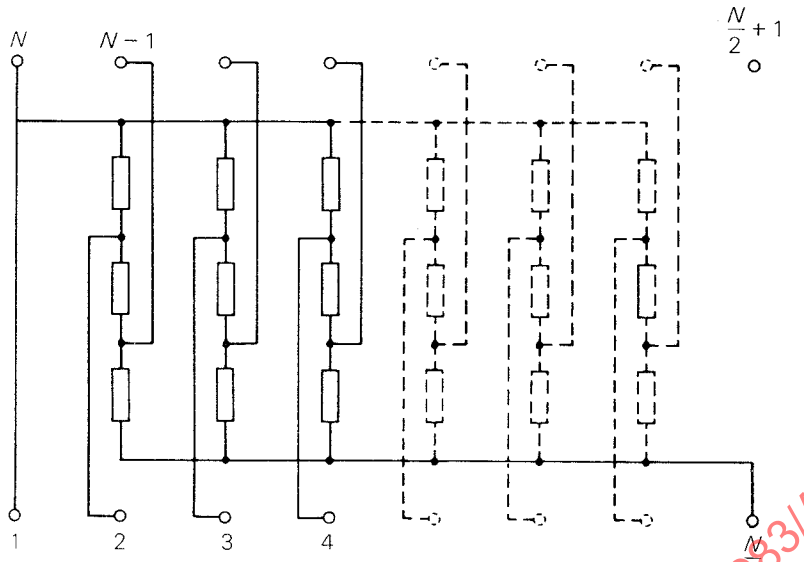

SCHÉMA K
DIAGRAM K

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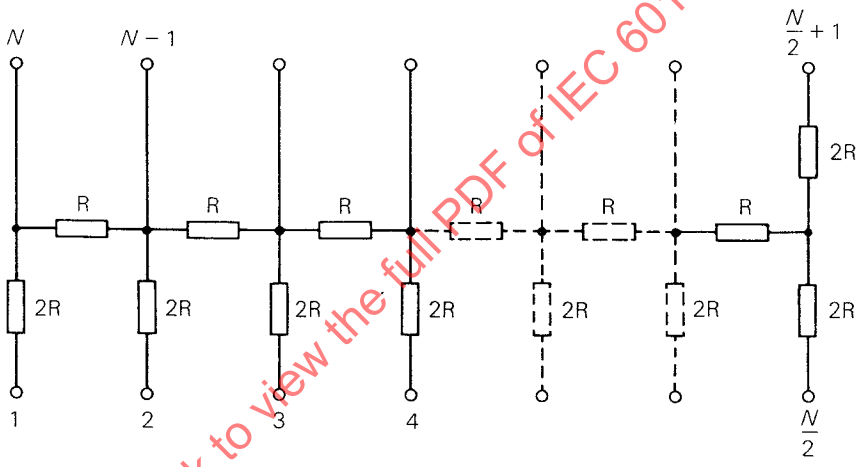

SCHÉMA L
DIAGRAM L

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N = nombre de sorties
number of terminations

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