

INTERNATIONAL STANDARD



**Printed boards design, manufacture and assembly – Vocabulary –
Part 2: Common usage in electronic technologies as well as printed board and
electronic assembly technologies**

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**PRINTED BOARDS DESIGN, MANUFACTURE
AND ASSEMBLY – VOCABULARY –****Part 2: Common usage in electronic technologies as well
as printed board and electronic assembly technologies**

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International Standard IEC 60194-2 has been prepared by IEC technical committee 91: Electronics assembly technology.

This first edition, together with IEC 60194-1, will cancel and replace IEC 60194:2015. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to IEC 60194:2015:

- a) exclusion of 32 general terms better served by other TCs;
- b) exclusion of 47 terms no longer used by the electronics assembly industry;
- c) inclusion of 13 new terms related with device embedded substrate technology;
- d) removal of identification codes for terms as well as annexes.

The text of this International Standard is based on the following documents:

CDV	Report on voting
91/1442/CDV	91/1473/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

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PRINTED BOARDS DESIGN, MANUFACTURE AND ASSEMBLY – VOCABULARY –

Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies

1 Scope

This part of IEC 60194 covers terms and definitions related to printed board and electronic assembly technologies as well as other electronic technologies.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of electronics assembly technology, the terms and definitions in 3.1 to 3.24 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1 A

3.1.1

abrasive trimming

adjustment of the value of a film component by notching it with a finely adjusted stream of an abrasive material against the resistor surface

3.1.2

accelerated ageing

accelerated life test

test in which the parameters such as voltage and temperature are increased above normal operating values to obtain observable or measurable deterioration in a relatively short period of time

3.1.3

accelerated test

test to check the life expectancy of an electronic component or electronic assembly in a short period of time by applying a physically severe condition(s) to the unit under test

3.1.4

acceleration factor

AF

ratio of stress in reliability testing to the normal operating condition

3.1.5

acceptance inspection

<criterion> inspection that determines conformance of a product to design specifications as the basis for acceptance

3.1.6

acceptance quality level

AQL

number of defects (in %) within a population (lot) at which the lot has the chance to be accepted with an acceptance probability of about 90 % when testing a sample

3.1.7

acceptance tests

tests deemed necessary to determine the acceptability of a product as agreed to by both purchaser and vendor

3.1.8

accuracy

degree to which the result of a measurement or calculation agrees with the true value

3.1.9

active device

electronic component whose basic character changes while operating on an applied signal

Note 1 to entry: This includes diodes, transistors, thyristors, and integrated circuits that are used for the rectification, amplification, switching, etc., of analogue or digital circuits in either monolithic or hybrid form.

3.1.10

add-on component

discrete or integrated packaged or chip components that are attached to a film circuit in order to complete the circuit's function

3.1.11

adhesive

non-metallic materials that can join solids by surface bonding and internal strength (adhesion and cohesion)

Note 1 to entry: In surface mounting, an epoxy adhesive is used to adhere SMDs to the substrate.

[SOURCE: IEC 60050-212:2010, 212-15-44]

3.1.12

all metal package

hybrid circuit package made solely of metal, without glass or ceramic

3.1.13

allowable temperature

temperature range in which an electronic circuit or component can perform its intended functions

3.1.14

alphanumeric, adj

pertaining to data that contain the letters of an alphabet, the decimal digits, and may contain control characters, special characters and the space character

3.1.15

alpha particle

He⁴ nucleus generated from a nuclear decay that is capable of generating hole-electron pairs in microelectronic devices and switching cells, causing soft errors in some devices

3.1.16**alternating current****AC**

electric current that is a periodic function of time with a zero direct component or, by extension, a negligible direct component

Note 1 to entry: For the qualifier AC, see IEC 60050-151.

[SOURCE: IEC 60050-131:2002, 131-11-24]

3.1.17**ambient**

surrounding environment coming into contact with the system or component in question

3.1.18**amplitude**

<voltage> maximum value of a voltage of an alternating voltage within one period

3.1.19**analogue circuit**

electrical circuit that provides a continuous relationship between its input and output

3.1.20**anisotropy**

condition for a substance having differing values for properties, such as permittivity, depending on the direction within the material

3.1.21**anode**

electrode capable of emitting positive charge carriers to and/or receiving negative charge carriers from the medium of lower conductivity

Note 1 to entry: The direction of electric current is from the external circuit, through the anode, to the medium of lower conductivity.

Note 2 to entry: In some cases (e.g. electrochemical cells), the term "anode" is applied to one or another electrode, depending on the electric operating condition of the device. In other cases (e.g. electronic tubes and semiconductor devices), the term "anode" is assigned to a specific electrode.

[SOURCE: IEC 60050-151:2001, 151-13-02]

3.1.22**application-specific integrated circuit****ASIC**

integrated circuit designed for specific applications

[SOURCE: IEC 60050-521:2002, 521-11-18]

3.1.23**area array package**

package that has terminations arranged in a grid on the bottom of the package and contained within the package outline

3.1.24**assembly****assembled board**

number of parts, subassemblies or combinations thereof joined together

Note 1 to entry: This term can be used in conjunction with other terms listed herein, for example, "printed board assembly".

3.1.25

attenuation

decrease of the energy of an electromagnetic wave during its propagation, represented quantitatively by the ratio of the power flux densities at two specified points

Note 1 to entry: Attenuation is generally expressed in decibels.

[SOURCE: IEC 60050-705:1995, 705-02-05]

3.2 B

3.2.1

backfill

filling a hybrid circuit package with a dry inert gas prior to hermetic sealing

3.2.2

backplane

backpanel

interconnection device used to provide point-to-point electrical interconnections

Note 1 to entry: It is usually a printed board that has discrete wiring terminals on one side and connector receptacles on the other side.

3.2.3

backward crosstalk

near-end crosstalk

noise induced into an adjacent line, as seen at that end of the adjacent line which is closest to the signal source, when this line has been placed near an active line

Note 1 to entry: See also "forward crosstalk".

3.2.4

balanced transmission line

transmission line that has distributed inductance, capacitance, resistance, and conductance elements that are equally distributed between its conductors

3.2.5

ball

raised metal (or other conductive material) feature on a package substrate used to facilitate bonding to the next level of interconnect

3.2.6

ball grid array

BGA

surface-mount package wherein the bumps for terminations are formed in a grid on the bottom of a package

SEE: Figure 1.

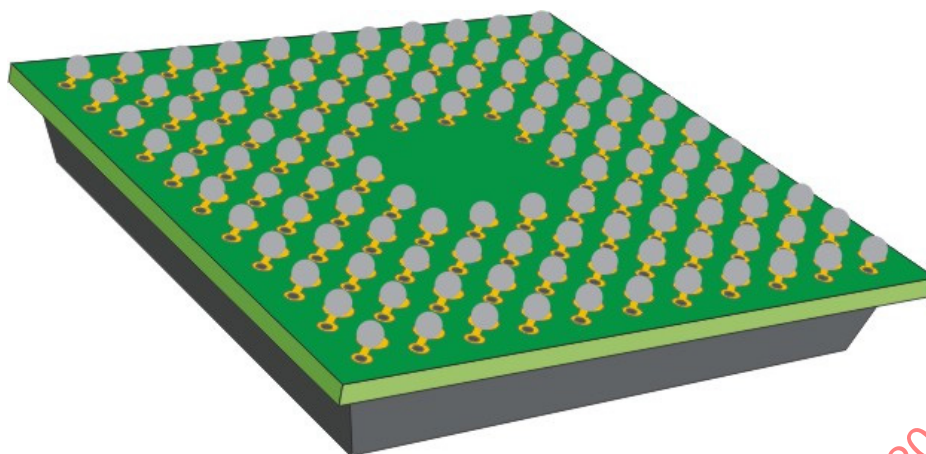


Figure 1 – Ball grid array (BGA)

3.2.7

barcode

linear arrangement of bars and spaces in a predetermined pattern

3.2.8

barcode marking

identification code consisting of a pattern of vertical bars whose width and spacing identifies the item marked

3.2.9

barcode symbol

print of photographically reproduced barcode composed of parallel bars and spaces of various widths

Note 1 to entry: A barcode symbol contains a leading quiet zone, a start character, data characters, a stop character, and a trailing quiet zone; in some cases, a check character is included.

3.2.10

bare die

unpackaged discrete semiconductor or integrated circuit with pads on the upper surface suitable for interconnection to the substrate or package

3.2.11

base film

<flexible circuits> film that is the base material for the flexible printed wiring board and on the surface of which the conductive pattern can be formed

Note 1 to entry: When the heat resistance is required, polyimide film is mostly used, and polyester film is usually used when the heat resistance is not required.

3.2.12

base material

substrate

insulating material upon which a conductive pattern may be formed

Note 1 to entry: The base material may be rigid or flexible, or both. It may be a dielectric or insulated metal sheet.

3.2.13

base material thickness

thickness of the base material excluding conductive foil or material deposited on the surfaces

3.2.14

base plane

plane that includes the lowest point of the mounting surface of the package, except for packages using stand-offs

3.2.15

basic specification

BS

document that describes the common elements for a set, family or group of products, materials, or services

3.2.16

bending resistance

ability of a material to withstand repeated bending to specified parameters without producing cracks and breaks in excess of the specification allowance

3.2.17

bias

<fabric> filling yarn that is off-square with the warp ends of a fabric

3.2.18

bipolar device

device in which both majority and minority carriers are present

Note 1 to entry: Bipolar and metal-oxide semiconductor (MOS) are the two most common device types.

3.2.19

bond

interconnection that performs a permanent electrical and/or mechanical function

3.2.20

bond pads

metallised areas on the die that are used for temporary or permanent electrical connection (bonding)

3.2.21

bond strength

pull strength

force perpendicular to a board's surface required to separate two adjacent layers of the board

Note 1 to entry: Bond strength is expressed as force per unit area.

3.2.22

bonding pad

<IC> area of metallization on an integrated circuit die that permits connection of fine wires or a circuit element to the die

3.2.23

bonding wire

gold or aluminium wire used for making electrical connections between lands, lead frames, and terminals

3.2.24

bow

warp

<fabric> filling yarn that lies in an arc across the width of a fabric

3.2.25**break-down voltage**

voltage at which the insulation between two conductors ruptures

3.2.26**bridging**

<electrical> unintentional formation of a conductive path between conductors

3.2.27**bulk packaging**

method for packaging loose parts, into a bag or case

3.2.28**bumped die**

semiconductor die with raised metal features that facilitate inner-lead bonding

SEE: Figure 2.

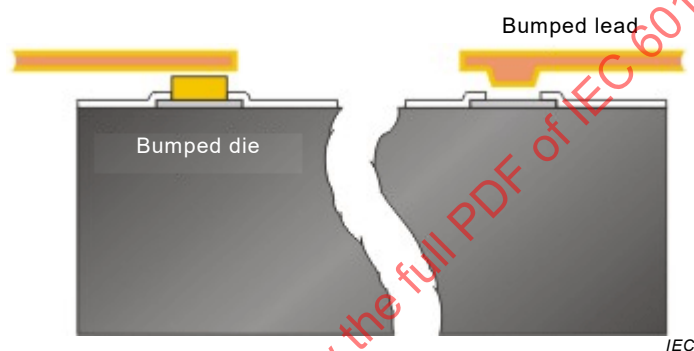


Figure 2 – Bumped die

3.2.29**burn-in**

<test> process of electrically stressing a device at an elevated temperature, for a sufficient amount of time to cause the failure of marginal devices (infant mortality)

3.2.30**burn-in**

<dynamic> burn-in at high temperatures that simulates the effects of actual or simulated operating conditions

3.2.31**burn-in**

<static> burn-in at high temperatures with unvarying voltage, either forward or reverse bias

3.3 C**3.3.1****capacitance**

measure of the ability of two adjacent conductors separated by an insulator to hold a charge when a voltage is impressed between them

[SOURCE: IEC 60050-131:2008, 131-12-13]

3.3.2**capacitive coupling**

electrical interaction between two conductors that is caused by the capacitance between them

3.3.3

ceramic dual in-line package

CERDIP

dual in-line package that has a package body of ceramic material and is hermetically sealed by a glass

Note 1 to entry: See also "dual in-line package".

3.3.4

ceramic pin grid array

ceramic PGA

pin grid array package (PGA) made of a ceramic material, hermetically sealed by metal, with leads formed on a grid extending from the bottom of the package

3.3.5

ceramic quad flat package

CQFP

quad flat package (QFP) made of a ceramic material, hermetically sealed by metal, with leads extending from all four sides

3.3.6

certification

verification that specified training or testing has been performed and that required proficiency or parameter values have been attained

3.3.7

characteristic impedance

quantity defined for a mode of propagation at a given frequency in a specific uniform transmission line or uniform waveguide by one of the three following relations:

$$Z_1 = S/|I|^2$$

$$Z_2 = |U|^2/S$$

$$Z_3 = U/I$$

where

Z is the complex characteristic impedance,

S is the complex power, and

U and I are the values, usually complex, respectively of a voltage and a current conventionally defined for each type of mode by analogy with transmission line equations.

EXAMPLE 1 For a parallel-wire transmission line, U and I can be uniquely defined and the three equations are consistent. If the transmission line is lossless, the characteristic impedance is real.

EXAMPLE 2 For a waveguide, the conventional definitions for U and I depend on the type of mode and generally lead to three different values of the characteristic impedance.

EXAMPLE 3 For a circular waveguide in the dominant mode TE₁₁, U = RMS voltage along the diameter where the magnitude of the electric field strength vector is a maximum, I = the r.m.s. longitudinal current.

EXAMPLE 4 For a rectangular waveguide in the dominant mode TE₁₀, U = the RMS voltage between midpoints of the two conductor faces normal to the electric field strength vector, I = the RMS longitudinal current following on one surface normal to the electric field strength vector.

[SOURCE: IEC 60050-726:1982, 726-07-01]

3.3.8**chemical vapour deposition**

process in which vapours and gases react chemically to produce deposits at the surface of a substrate

[SOURCE: IEC 60050-841:2004, 841-22-07]

3.3.9**chip**

SEE: "die".

Note 1 to entry: Common parlance for die.

3.3.10**chip carrier**

low-profile, usually square, surface-mount component semiconductor package whose die cavity or die mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package

Note 1 to entry: It can be leaded or leadless.

3.3.11**chip-on-board****COB**

printed board assembly technology that places unpackaged semiconductor dice and interconnects them by wire bonding or similar attachment techniques

SEE: Figure 3.

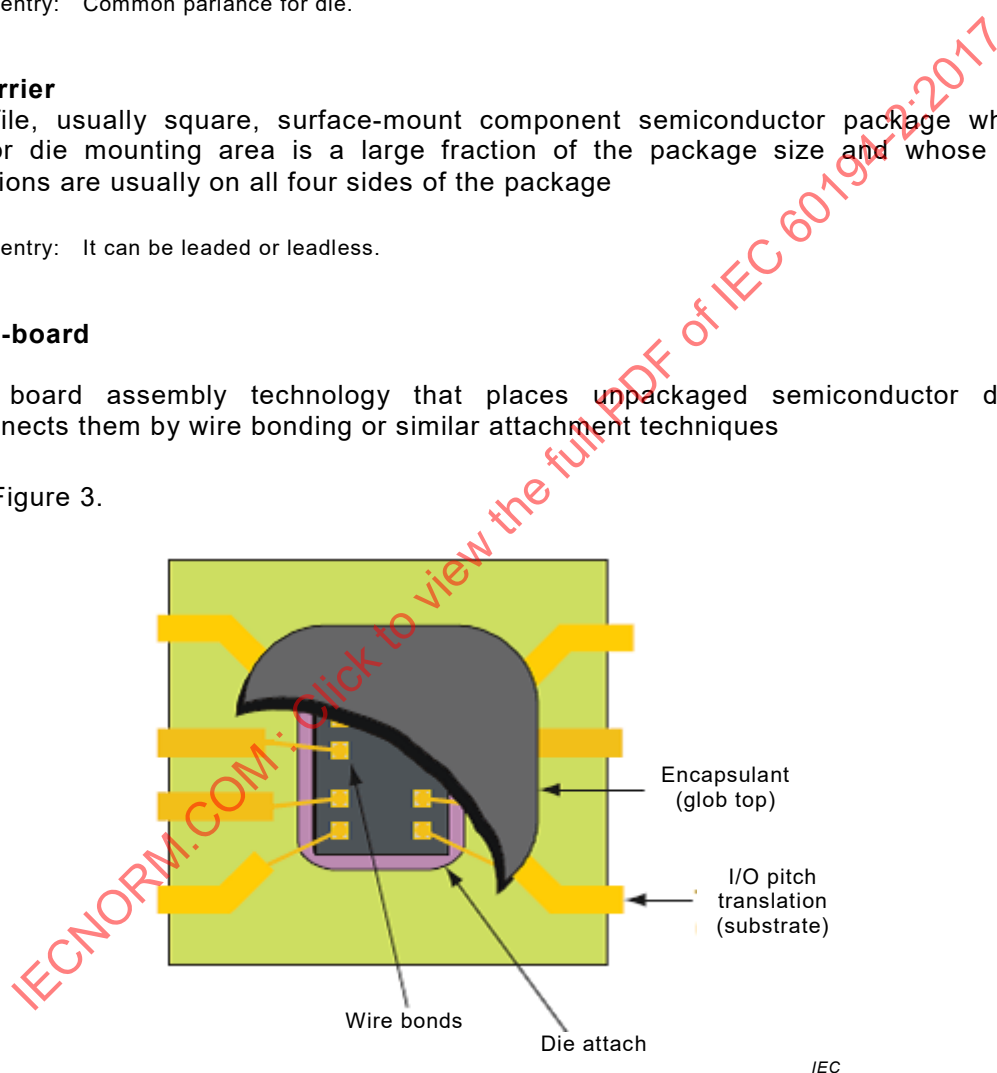


Figure 3 – Chip on board (COB)

Note 1 to entry: The silicon area density is usually smaller than the density of the printed board.

Note 2 to entry: A mounting and attachment technique where the die is mounted onto a substrate, often a printed-circuit board.

3.3.12**chip-on-flex****COF**

semiconductor chip mounted directly onto a flexible printed board

3.3.13

chip-on-glass

COG

assembly technology that uses an unpackaged semiconductor die mounted directly on a glass substrate such as a glass plate for liquid crystal displays (LCD)

3.3.14

chip scale package

CSP

generic term for packaging technologies that result in a packaged part that is only marginally larger than the internal die

3.3.15

circuit

number of electrical elements and devices that have been interconnected to perform a desired electrical function

3.3.16

CMOS

complementary metal-oxide semiconductor

fabrication technology that results in the creation of both NMOS and PMOS FET devices

3.3.17

coaxial cable

cable in the form of a central wire surrounded by a conductor tubing or sheathing that serves as a shield and return

3.3.18

compensation circuit

electrical circuit that alters the functioning of another circuit to which it is applied to achieve a desired performance

3.3.19

component

individual part or combination of parts that, when together, perform (a) design function(s)

Note 1 to entry: See also "discrete component".

3.3.20

component mounting site

location on a packaging and interconnecting structure (P&I) that consists of a land pattern and conductor fan-out to additional lands for testing, or vias that are associated with the mounting of a single component

3.3.21

compression seal

tight joint made between a component package and its leads that is formed as heated metal cools and shrinks around a glass insulator

3.3.22

computer-aided design

CAD

interactive use of computer systems, programs, and procedures in the design process wherein the decision-making activity rests with the human operator and a computer provides the data manipulation function

3.3.23**conditioning**

subsection of a specimen for a specified duration to specific climatic conditions (usually a specified temperature and a specified relative humidity) or to an atmosphere of specified relative humidity or to complete immersion in water or other liquid

[SOURCE: IEC 60050-212:2010, 212-12-01]

3.3.24**conductance**

for a resistive two-terminal element or two-terminal circuit with terminals A and B, quotient of the electric current i in the element or circuit by the voltage u_{AB} (IEC 60050-131:2013, 131-11-56) between the terminals

$$G = \frac{i}{u_{AB}}$$

where the electric current is taken to be positive if its direction is from A to B and negative if its direction is from B to A

Note 1 to entry: The conductance of an element or circuit is the inverse of its resistance.

Note 2 to entry: The term "conductance" is also a short term for "conductance to alternating current" (IEC 60050-131:2013, 131-12-53).

Note 3 to entry: The coherent SI unit of conductance is siemens, S.

[SOURCE: IEC 60050-131:2013, 131-12-06]

3.3.25**conductive ink**

liquid medium with a suspended powder of an electrically conductive material

3.3.26**conductive medium**

material with a suspended powder of an electrically conductive material

3.3.27**conductive pattern****conductor pattern**

configuration formed by the electrically conductive material of a printed board

[SOURCE: IEC 60050-541:1990, 541-01-04]

3.3.28**conductivity**

<electrical> ability of a substance or material to conduct electricity

3.3.29**conductivity**

<thermal> ability of a substance or material to conduct heat

3.3.30

conductor

trace

conductor line

conductor path

conductor track

line

electrical path

track

single conductive path in a conductive pattern

[SOURCE: IEC 60050-541:1990, 541-01-20]

3.3.31

constraining core

supporting plane that is internal to a packaging and interconnecting structure

3.3.32

controlled collapse soldering

controlled collapse

<component connection> technique for soldering a component (i.e., flip chip, chip scale package, BGA) to a substrate, where the component connection surface tension forces of the liquid solder support the weight of the component and controls the height of the joint

3.3.33

coplanar leads

flat beam leads of a component package that have been formed so that they can simultaneously contact one plane of a base material

3.3.34

corona

electrical discharge brought on by the ionization of a liquid surrounding a conductor, which occurs when the potential gradient exceeds a certain value, but conditions are insufficient to cause complete electrical breakdown or arcing

3.3.35

creel

device used as a yarn package rack to hold warp ends for a section beam

3.3.36

critical defect

anomaly specified as being unacceptable

3.3.37

crosstalk

spurious signal

undesirable transfer of electrical energy between neighbouring conductors (coupling) by mutual inductance and capacitance

Note 1 to entry: See also "backward crosstalk" and "forward crosstalk".

3.3.38

cupping

<BGA> condition of a ball grid array package after reflow where the corners turn up and away from the printed board laminate surface

Note 1 to entry: This condition in the worst case causes the balls on the outside row to be in tension and the balls in the centre to be in compression.

Note 2 to entry: Opposite of "doming <BGA>".

3.3.39**current**

flow or movement of electrons in a conductor as the result of a voltage difference between the ends of the conductive path

3.3.40**current-carrying capacity**

maximum electrical current that can be carried continuously by a conductor, under specified conditions, without causing objectable degradation of electrical and mechanical properties of the product

3.3.41**customer detail specification****CDS**

document that establishes the specific requirements, identified in a detailed specification, in order to tailor these to meet the needs of a custom product, material, or service

3.4 D**3.4.1****damage**

result of an event that degrades a product, for example a component, printed board, or module, beyond the form, fit and function limits of the governing document

3.4.2**data capture**

automatic collection of information from a given machine or other information source

3.4.3**database**

comprehensive collection of information that is structured in such a way that some or all of its data may be used to create queries about related items contained within it

3.4.4**dead-bug, adj**

orientation of a package with the terminations facing up

3.4.5**decoupling**

absorption of noise pulses in power supply lines, which are generated by switching logic devices, so as to prevent the lines from disturbing other logic devices in the same power-supply circuit

3.4.6**defect**

non-conformance or other risk factors as identified by the manufacturer

Note 1 to entry: A process and/or material non-conformance that could result in a reduction of functional capability, design life or reliability.

3.4.7**degradation**

undesired departure in the operational performance of any device, equipment or system from its intended performance

Note 1 to entry: The term "degradation" can apply to temporary or permanent failure.

[SOURCE: IEC 60050-161:1990, 161-01-19]

3.4.8

detail specification

detailed written description of a part or a process

3.4.9

dice

two or more die

3.4.10

dicing

separating of semi-conductor wafers into individual die

3.4.11

die

chip

leadless device

separated part (or whole) of a wafer intended to perform a function or functions in a device

[SOURCE: IEC 60050-521:2002, 521-05-30]

3.4.12

die bonding

attachment of a die to base material

3.4.13

die device

bare die, with or without connection structures, or a minimally packaged die

3.4.14

dielectric strength

maximum voltage that a dielectric can withstand under specified conditions without a voltage breakdown

Note 1 to entry: Dielectric strength is usually expressed as volts per unit dimension.

3.4.15

digital circuit

electrical circuit that provides two (binary) or three distinct relationships (states) between its input and output

3.4.16

direct current

DC

electric current that is time-independent or, by extension, periodic current, the direct component of which is of primary importance

Note 1 to entry: For the qualifier DC, see IEC 60050-151.

[SOURCE: IEC 60050-131:2002, 131-11-22]

3.4.17

discrete component

separate part of a printed board assembly that performs a circuit function (for example, a resistor, a capacitor, a transistor)

3.4.18

doming

<BGA> condition of a ball grid array package after reflow where the corners turn down and toward the printed board laminate surface

Note 1 to entry: This condition in the worst case causes the balls on the outside row to be compressed and the balls in the centre to be in tension.

Note 2 to entry: Opposite of "cupping BGA".

3.4.19

doping

addition of a specific impurity to a slice of silicon monocrystal to alter the conductivity of the crystal in a specified manner in order to produce semiconductor devices from this crystal

3.4.20

double-sided assembly

packaging and interconnecting structure with components mounted on both the primary and secondary sides

Note 1 to entry: See also "single-sided assembly".

3.4.21

dry pack

container that maintains the moisture content of the packages of die devices within specified limits

3.4.22

dual in-line package

DIP

basically rectangular component package that has a row of leads extending from each of the longer sides of its body that are formed at right angles to a plane and parallel to the base of its body

3.5 E

3.5.1

edge-transmission attenuation

loss of a logic signal's switching-edge sharpness that has been caused by the absorption of the highest-frequency components by the transmission line

Note 1 to entry: See also "attenuation".

3.5.2

electrical characteristics

distinguishing electrical traits or properties of a component or assembly

3.5.3

electromagnetic compatibility

EMC

ability of a device to function properly in its operating environment without causing electromagnetic interference to other equipment, or itself being susceptible to external interference

3.5.4

electromagnetic interference

EMI

degradation of the performance of a piece of equipment, transmission channel or system caused by an electromagnetic disturbance

Note 1 to entry: In French, the terms "perturbation électromagnétique" and "brouillage électromagnétique" designate respectively the cause and the effect, and should not be used indiscriminately.

Note 2 to entry: In English, the terms "electromagnetic disturbance" and "electromagnetic interference" designate respectively the cause and the effect, but they are often used indiscriminately.

[SOURCE: IEC 60050-161:1990, 161-01-06]

3.5.5

electrostatic discharge

ESD

transfer of electric charge between bodies of different electrostatic potential in proximity or through direct contact

[SOURCE: IEC 60050-161:1990, 161-01-22]

3.6 F

3.6.1

farad

unit of electrical capacitance

3.6.2

far-end crosstalk

SEE: "forward crosstalk".

3.6.3

fault

condition that causes a device or circuit to fail to operate in a proper manner

3.6.4

film conductor

conductor formed in place on a base material by depositing a conductive material using screening, plating or evaporating techniques

3.6.5

film network

electrical network composed of thin-film and/or thick-film components on a base material

3.6.6

final inspection

delivery inspection

evaluation of quality characteristics relating to a standard, specification, or design drawing prior to shipping to the customer

3.6.7

final seal

manufacturing process that completes the enclosure of a microcircuit so that further internal processing cannot be performed without removing a lid or otherwise disassembling the package

3.6.8

fine leak

leak in a sealed package that is less than 0,000 01 cm³/s at 1 atm of differential air pressure

3.6.9

fine pitch QFP

quad flat pack (QFP) package whose lead pitch centres at 0,635 mm or less

3.6.10

flat pack

rectangular component package that has a row of leads extending from each of the longer sides of its body that are parallel to the base of its body

3.6.11**flexible double-sided printed board****double-sided flexible printed wiring board**

double-sided printed board using a flexible base material only

[SOURCE: IEC 60050-541:1990, 541-01-14]

3.6.12**flexible material interconnect construction****FMIC**

integration of passive and active components with mechanical components (including switches and connectors) on a flexible or thin base material, i.e., flexible printed board, in order to produce an electronic assembly

3.6.13**flexible multilayer printed board**

multilayer printed board using a flexible base material only

Note 1 to entry: Different areas of the flexible multilayer printed board may have different numbers of layers and different thicknesses and consequently different flexibility.

[SOURCE: IEC 60050-541:1990, 541-01-05]

3.6.14**flexible printed board**

printed board using a flexible base material only

Note 1 to entry: It can be partially provided with electrically non-functional stiffeners and/or coverlayers.

[SOURCE: IEC 60050-541:1990, 541-01-12]

3.6.15**flexible printed circuit**

patterned arrangement of printed circuitry and components that uses a flexible base material with or without a flexible coverlayer

3.6.16**flexible printed wiring**

patterned arrangement of printed wiring that uses a flexible base material with or without flexible coverlayer

3.6.17**flexible single-sided printed board**

single-sided printed board using a flexible base material only

[SOURCE: IEC 60050-541:1990, 541-01-13]

3.6.18**flex-rigid double-sided printed board**

SEE: "rigid-flex double-sided printed board".

3.6.19**flex-rigid printed board**

SEE: "rigid-flex printed board".

3.6.20**flip chip**

leadless monolithic circuit element structure that electrically and mechanically interconnects to a printed board by conductive bumps

SEE: Figure 4.

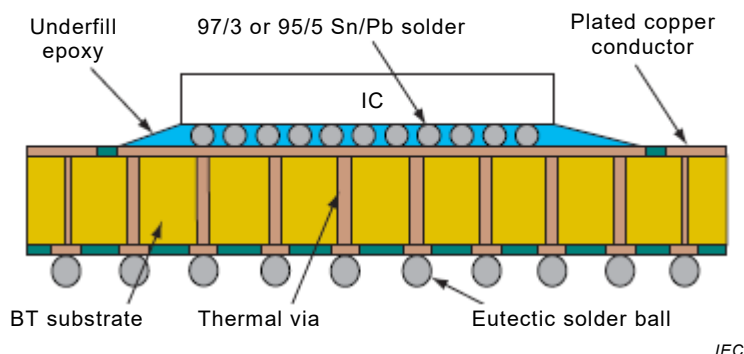


Figure 4 – Flip chip

3.6.21

forward crosstalk

far-end crosstalk

noise induced into a adjacent line, as seen at the end of the adjacent line that is the farthest from the signal source, because the adjacent line has been placed next to an active line

Note 1 to entry: See also "backward crosstalk".

3.6.22

frequency

<electrical current> number of cycles (hertz) or completed alterations per second

3.6.23

fully additive process

fully electroless process

additive process wherein the entire thickness of electrically isolated conductors is obtained by the use of electroless deposition

Note 1 to entry: See also: "semi-additive process".

3.7 G

3.7.1

generic specification

GS

document that describes as many general requirements as possible, pertaining to a set, family or group of products, materials, or services

3.7.2

go/no-go test

testing process that yields only a pass or a fail condition

3.7.3

gross leak

leak in a sealed package that is greater than 0,000 01 cm³/s at 1 atm of differential air pressure

3.7.4

ground

common reference point for electrical circuit returns, shielding, or heat sinking

3.7.5**ground plane**

conductor layer, or portion thereof, that serves as a common reference for electrical circuit returns, shielding, or heat sinking

3.8 H**3.8.1****header**

<module> base of an electronic component package that contains leads

3.8.2**heatsink****thermal shunt**

mechanical device that is made of a high thermal conductivity and low specific heat material that dissipates heat generated by a component or assembly

3.8.3**hermetic**

<sealing> condition of sealing a component from incoming gases to a specific of inward diffusion normally less than $1 \times 10^{-6} \text{ cm}^3/\text{s}$

3.8.4**histogram**

graph that depicts values that were obtained by dividing the range of a data set into equal intervals and that plots the number of data points in each interval

SEE: Figure 5.

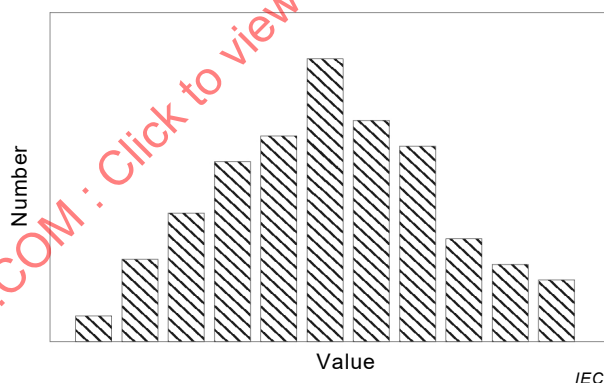


Figure 5 – Histogram

3.8.5**horn**

cone-shaped object that transmits ultrasonic energy from a transducer to a bonding tool

3.8.6**hybrid circuit**

circuit comprising insulating base material with various combinations of interconnected film conductors, film components, semiconductor die/dice, passive components and bonding wire

Note 1 to entry: See also "multi-chip module" and "multi-chip package".

3.8.7

hybrid integrated circuit

circuit comprising insulating base material with various combinations of interconnected film conductors, film components, semiconductor dice, passive components and bonding wire that perform the same function as a monolithic semiconductor integrated circuit

3.8.8

hybrid microcircuit

circuit comprising insulating base material with various combinations of interconnected film conductors, film components, semiconductor dice, passive components and bonding wire

3.9 I

3.9.1

immersion conditions

test conditions resulting when surface-mounting device package leads are immersed into a solder bath to check their resistance to soldering temperatures

3.9.2

impedance

resistance set against the flow of a current in a conductor, represented by an electrical network of combined resistance, capacitance and inductance, as seen by an AC source of time-varying voltage

Note 1 to entry: The unit for impedance is ohm, and in principle, it is equal to the square root of the sum of the squares of resistance, reactance and inductance.

3.9.3

inductance

property of a conductor that allows it to store energy in a magnetic field induced by a current flowing through it

Note 1 to entry: The unit of measure is the henry (H).

3.9.4

input vector

set of logic values to be applied to the complete set of input test points at any one point in time

3.9.5

insertion loss

ratio of transmitted electromagnetic power to incident power

Note 1 to entry: This loss of power includes losses by conversion to heat in the dielectric and in the conductors.

Note 2 to entry: The insertion loss is usually expressed in decibels (dB).

3.9.6

inspection lot

collection of product units that are identified and treated as a unique entity from which a sample is drawn and inspected in order to determine conformance with acceptability criteria

3.9.7

integrated circuit

combination of inseparable associated circuit elements that are formed in place and interconnected on or within a single base material to perform a particular electrical function

3.9.8

integrated passive component

multiple passive components that share a substrate and package

Note 1 to entry: Integrated passive components may be housed inside the layers of the primary interconnect substrate, and thus become embedded passive components. Alternatively, these components may be on the surface of a separate substrate that is then placed in an enclosure and surface-mounted on the primary interconnect substrate, thus becoming passive arrays or passive networks.

3.9.9

interconnection

joining of electrical devices to complete a circuit

3.10 J

3.10.1

jisso

total solution for interconnecting, assembling, packaging, mounting, and integrating system design

Note 1 to entry: A Japanese term.

3.10.2

J-leads

preferred surface mount lead form used on PLCCs (plastic leaded chip carrier), so named because the lead departs the package body near its Z-axis centreline, is formed down then rolled under the package

Note 1 to entry: Leads so formed are shaped like the letter "J".

3.10.3

junction temperature

temperature of the region of a transition between the p-type and n-type semiconductor material in a transistor or diode element during operation

3.11 K

3.11.1

known good die

KGD

die-form semiconductor product that provides assurance of equivalent quality and reliability as that found in its conventionally packaged counterparts

3.11.2

known tested die

KTD

die-form semiconductor product functionally verified by probing tests equal to the expected performance of the packaged product, without full quality assurance by supplier(s)

Note 1 to entry: The testing requirements are AABUS.

3.12 L

3.12.1

land grid array

LGA

square package with termination lands located in a grid pattern on the bottom of the package

3.12.2

large-scale integration

LSI

integrated circuit with over 100 gates

3.12.3

lay-up

process of combining one or more inner layers, and pre-preg or adhesive layer(s) into a lamination package

Note 1 to entry: The package can consist of inner layers, outer layers and copper foil.

3.12.4

lead frame

metallic portion of the device package on which the integrated circuit die is mounted and connected from the die or dice bonding sites to the structure that becomes the outer leads of the package

3.12.5

lead-free solder

alloy that does not contain more than 0,1 % lead (Pb) by weight and that is used for joining components to substrates or for coating surfaces

3.12.6

leadless chip carrier

chip carrier whose external connections consist of leads that are around and down the side of the package

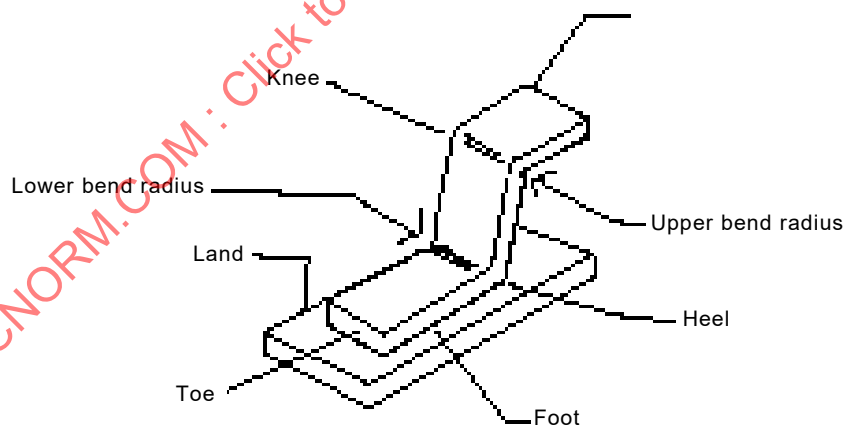
Note 1 to entry: See also "leadless chip carrier".

3.12.7

leadless surface-mount component

surface-mount component for which external connections consist of leads that are around and down the side of the package

SEE: Figure 6.



IEC

Figure 6 – Leadless surface-mount component – Gull wing-shaped lead

Note 1 to entry: See also "leadless surface-mount component".

3.12.8

leadless surface-mount component

leadless component

leadless device

surface-mount component whose external connections consist of metallized terminations that are integral parts of the component body

Note 1 to entry: See also "leadless surface-mount component".

3.12.9**leakage current**

undesired flow of an electrical current at the surface or through the inside of an insulator

3.12.10**line coupling**

interaction between two transmission lines that is caused by their mutual inductance and capacitance

3.12.11**load capacitance**

capacitance seen by the output of a logic circuit or other signal source

3.12.12**logic circuit**

functional digital circuits used to perform computational functions

3.12.13**logic diagram**

drawing that depicts the multistate device implementation of logic functions with logic symbols and supplementary notations that show the details of signal flow and control, but not necessarily the point-to-point wiring

3.12.14**logic family**

collection of logic functions using the same form of electronic circuit, for example, emitter-coupled logic (ECL), transistor-transistor logic (TTL), complementary metal-oxide semiconductor logic (CMOS)

3.12.15**lot accept number**

maximum number of devices that may fail a sample test without causing rejection of the lot

3.12.16**lot reject number**

number of failed devices that will cause lot rejection in a sample test

3.12.17**lot size****batch size**

collection of units produced in one continuous, uninterrupted fabrication run

3.12.18**luminance****brightness**

quantity defined by the formula

$$L_v = \frac{d\Phi_v}{dA \cos\theta d\Omega}$$

where:

$d\Phi_v$ is the luminous flux transmitted by an elementary beam passing through the given point and propagating in the solid angle $d\Omega$ containing the given direction;

dA is the area of a section of that beam containing the given point;

θ is the angle between the normal to that section and the direction of the beam

unit: $\text{cd} \cdot \text{m}^{-2} = \text{lm} \cdot \text{m}^{-2} \cdot \text{sr}^{-1}$

[SOURCE: IEC 60050-845:1987, 845-01-35]

3.12.19

luminous energy

time integral of the luminous flux

Note 1 to entry: Luminous energy is measured in lms (lumen second).

3.12.20

luminous flux

magnitude defined by

$$\Phi = K_m \int_0^{\infty} V(\lambda) P(\lambda) d\lambda$$

where:

$P(\lambda)$ is the power spectral density radiated by the source at wavelength λ ;

$V(\lambda)$ is the spectral luminous efficiency for photopic vision;

K_m is a constant

Note 1 to entry: In the SI system of units, where $P(\lambda)$ is expressed in watts per metre, the luminous flux Φ is expressed in lumens, and $K_m = 683 \text{ lm/W}$.

[SOURCE: IEC 60050-723:1997, 723-08-27]

3.13 M

3.13.1

major defect

defect that is likely to result in a failure of a unit or product or that materially reduces its usability for its intended purpose

3.13.2

metal-oxide semiconductor

MOS

fabrication technology, resulting in the creation of FET devices

3.13.3

microcircuit

relatively high-density combination of equivalent circuit elements that are interconnected so as to perform as an indivisible electronic circuit component

3.13.4

microcircuit module

combination of microcircuits and discrete components that are interconnected so as to perform as an indivisible circuit assembly

3.13.5

microelectronics

area of electronic technology with, or applied to, the realization of electronic systems from extremely small electronic elements, devices or parts

3.13.6

microwave integrated circuit

integrated circuit that performs at microwave frequencies

3.13.7**microwaves**

radio waves in the frequency range of 1 GHz to 100 GHz

Note 1 to entry: The term "microwave" generally refers to the frequency range where circuits and device interconnects are described as distributed elements instead of lumped elements.

3.13.8**minimally-packaged die****MPD**

die to which some exterior packaging medium and interconnection structure has been added for protection purposes and ease of handling

Note 1 to entry: This definition includes such packaging technologies as chip scale packages (CSP) in which the area of the package is not significantly greater than the area of the bare die.

3.13.9**minor defect**

defect that is not likely to result in a failure of a unit or product or that does not materially reduce its usability for its intended purpose

3.13.10**mixed component mounting technology**

component mounting technology that uses both through-hole and surface-mounting technologies on the same packaging and interconnecting structure

3.13.11**module**

separable unit in a packaging scheme

3.13.12**moisture barrier bag****MBB**

bag that is safe from electrostatic discharge (ESD) and is designed to restrict the ingress of water vapour used to package moisture-sensitive devices

3.13.13**monolithic integrated circuit**

integrated circuit in the form of a monolithic structure

3.13.14**moulded interconnection device**

combination of moulded plastic substrate and conductive patterns that provide both the mechanical and electrical functions of an electronic interconnection package

3.13.15**multi-chip module****MCM**

<structure> module that contains two or more dice and/or minimally packaged dice

Note 1 to entry: Also see "hybrid" and "multi-chip package".

3.13.16**multi-chip package****MCP**

package that contains two or more dice and/or minimally-packaged dice

Note 1 to entry: Also see "hybrid" and "multi-chip package".

3.13.17

multichip module

MCM

multichip integrated circuit

multichip microcircuit

<silicone efficiency> microchip module consisting primarily of closely-spaced integrated circuit dies that have a silicon area density of 30 % or more

3.14 N

3.14.1

nominal

design target dimension for a physical characteristic of a product or a feature to which a tolerance may be applied that establishes the limits of variation from the target that are acceptable

3.14.2

nominal value

centre value between a minimum and maximum allowance

3.15 O

3.15.1

output vector

set of logic values, either expected or measured, for all output points at a particular test step of a unit under test

3.16 P

3.16.1

package

total assembly, which protects one or more electronic components from mechanical, environmental and electrical damage throughout its operational life and which provides means of interconnection

3.16.2

package cap

cuplike package cover

3.16.3

package cover

cover that encloses the contents in the cavity of a package in the final sealing operation

3.16.4

package lid

flat package cover

3.16.5

packaging

process of assembling one or more electronic components into a package

Note 1 to entry: The use of "packaging" as a participle (for example "When packaging ICs into dual-in-line packages ...") is deprecated.

3.16.6

packaging and interconnecting assembly

assembly that has components mounted on one or both sides of a packaging and interconnecting structure

Note 1 to entry: "Packaging and interconnecting assembly" is a general term.

3.16.7**package cracking**

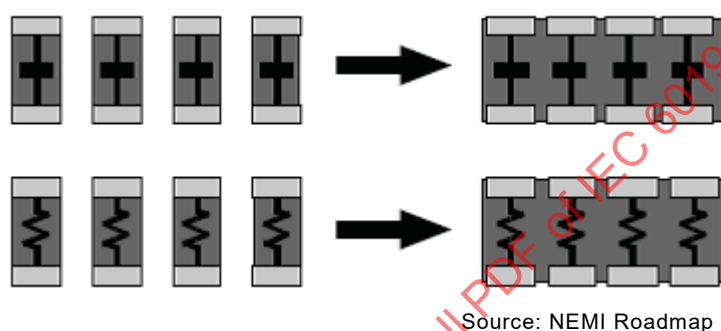
cracks in a plastic integrated circuit package caused by stress that results from exposure to reflow solder temperature

Note 1 to entry: These cracks may propagate from the die or die pad to the surface of the package, or only extend part way to the surface of lead fingers.

3.16.8**passive array**

multiple passive components of similar function, which are formed on the surface of a separate substrate and packaged in a single SMT case and mounted on the primary interconnect substrate

SEE: Figure 7.



Source: NEMI Roadmap

IEC

Figure 7 – Passive array

Note 1 to entry: Examples include an array of capacitors or resistors.

3.16.9**passive component**

<element> discrete electronic device whose basic character does not change while it processes an applied signal

Note 1 to entry: Passive components include components such as resistors, capacitors, and inductors.

3.16.10**passive network**

multiple passive components that have more than one function and are formed on the surface of a separate substrate and packaged in a single SMT case

Note 1 to entry: The case is then mounted on the primary interconnected substrate of the system.

Note 2 to entry: Passive networks typically have several internal connections to form simple functions such as terminations or filters.

3.16.11**peak package body temperature** **T_p**

highest temperature that an individual package body reaches during moisture sensitivity level (MSL) classification

3.16.12**perimeter sealing area**

surface on the perimeter of a package cavity that is used as an attachment to the package cover

3.16.13

photometry

light measurement where the luminous intensity is compared with that of the light source to be measured by measurable attenuation

Note 1 to entry: Photometry comprises visual, physical and photographic photometry. For the visual photometry, the eye is the receiver.

3.16.14

pick-up force

force required to pick up a surface-mount component from its packaging medium for placement on a substrate

3.16.15

pick-up tool

tool used to pick up surface-mount components from a packaging medium for placement on a substrate and which may be hand activated or a part of a pick-and-place machine

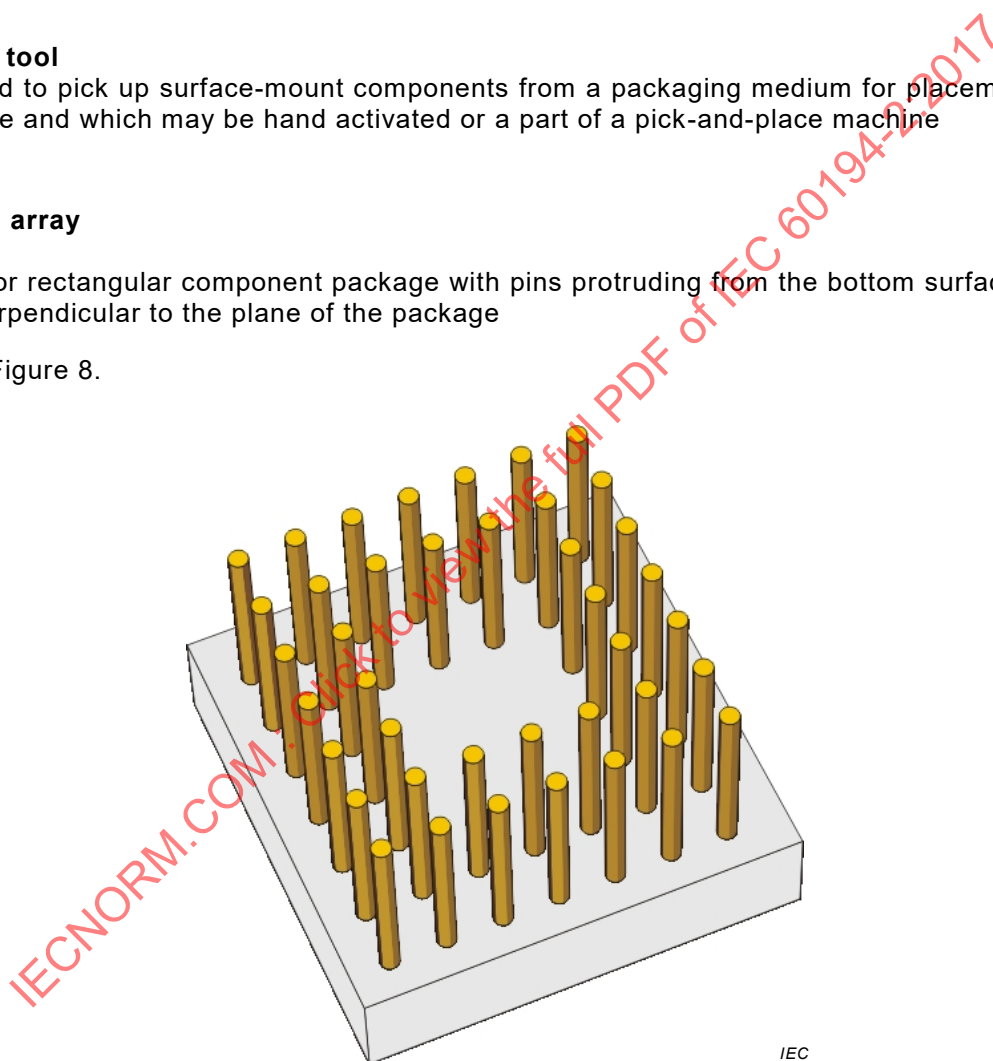
3.16.16

pin grid array

PGA

square or rectangular component package with pins protruding from the bottom surface with a pitch perpendicular to the plane of the package

SEE: Figure 8.



IEC

Figure 8 – Pin grid array

3.16.17

plastic ball grid array

PBGA

polymer-based package with interconnects formed of tin-lead solder spheres

Note 1 to entry: The solder interconnects are located in an array area on board side of package.

3.16.18

plastic device

semiconductor component wherein the package or encapsulant is plastic

3.16.19**plastic leaded chip carrier****PLCC**

surface-mount family of integrated circuit packages with leads exiting from all four sides of the package, generally with a 1,27 mm lead-to-lead pitch

3.16.20**plastic quad flat pack****PQFP**

surface-mount family of integrated circuit packages, bounded on all four sides by bumpers, with leads exiting from all four sides of the package and formed into a "gull-wing" lead format

3.16.21**power dissipation**

energy used by an electronic device in the performance of its function

3.16.22**power plane inductance**

inductance in response to AC noise, seen on a DC backplane system

primary side**component side**

side of a packaging and interconnecting structure that is defined as such on the master drawing

Note 1 to entry: It is usually the side that contains the most complex or the highest number of components.

3.16.23**printed board****PB****board**

card

circuit card

finished board

completely processed printed circuit and printed wiring configurations

Note 1 to entry: This includes single-sided, double-sided and multilayer boards with rigid, flexible, and rigid-flex base materials.

Note 2 to entry: "Printed board" is a general term.

3.16.24**printed board assembly**

assembly that uses a printed board for component mounting and interconnecting purposes

Note 1 to entry: "Printed board assembly" is a general term.

3.16.25**printed circuit****circuit board**

conductive pattern that is composed of printed components, printed wiring, discrete wiring, or a combination thereof, that is formed in a predetermined arrangement on a common base

Note 1 to entry: This is also a generic term that is used to describe a printed board that is produced by any of a number of techniques.

3.16.26**printed circuit board**

printed board that provides both point-to-point connections and printed components in a predetermined arrangement on a common base

Note 1 to entry: See also "printed wiring board".

3.16.27

printed component

part (such as an inductor, resistor, capacitor, or transmission line) that is formed as part of the conductive pattern of a printed board

3.16.28

printed component

<conductive inks> component (for example, printed inductor, resistor, capacitor or transmission line) forming part of the pattern of a printed circuit

3.16.29

printed contact

portion of a conductive pattern that serves as one part of a contact system

3.16.30

printed electronics sheet board

sheet (board) forming electronically functional pattern and/or devices on a large-scale by printing of conductive materials

Note 1 to entry: Applications of a printed electronics sheet can include sensors of various types including image and pressure, thin film secondary battery, smart card, RF-IC, etc.

3.16.31

printed wiring

conductive pattern that provides point-to-point connections but not printed components in a predetermined arrangement on a common base

Note 1 to entry: See also "printed circuit".

3.16.32

printed wiring board

printed board that provides point-to-point connections but not printed components in a predetermined arrangement on a common base

Note 1 to entry: See also "printed circuit board".

3.16.33

printing

act of reproducing a pattern on a surface by any process

3.16.34

propagation delay

time from output to input required for a signal to travel along a transmission line, or the time required for a logic device to receive an input stimulus, perform its function, and present a signal at its output

3.16.35

pulse

<digital> logic signal that switches from one digital state to the other and back again in a short period of time, and that remains in the original state for most of the time

3.17 Q

3.17.1

QFP with bumper

BQFP

QFP package with a guarding bumper

3.17.2**quad flat J-lead****QFJ**

generic rectangular component package, containing an electronic device, with leads on all four sides that are formed in a "J" shape

3.17.3**quad flat no-lead****QFN**

generic rectangular component package outline wherein the metal pad terminations are formed on four sides of the bottom of a package

3.17.4**quad flat pack****QFP****plastic QFP****PQFP**

generic square or rectangular component package, containing a semiconductor die, with leads on all four sides that are formed in a "gullwing" shape

3.17.5**qualification testing**

demonstration of the ability to meet all of the requirements specified for a product

3.17.6**quality conformance testing**

qualification testing that is performed on a regularly scheduled basis in order to demonstrate the continued ability of a product to meet all of the quality requirements specified

3.18 R**3.18.1****radiant flux**

power emitted, transmitted or received in the form of radiation

Note 1 to entry: Radiant flux is measured in W.

[SOURCE: IEC 60050-845:1987, 845-01-24, modified – Note to entry added.]

3.18.2**radiant intensity****power of source**

quotient of the radiant flux $d\Phi_e$ leaving the source and propagated in the element of solid angle $d\Omega$ containing the given direction, by the element of solid angle

$$I_e = \frac{d\Phi_e}{d\Omega}$$

Note 1 to entry: Radiant intensity is measured in $W \cdot sr^{-1}$.

[SOURCE: IEC 60050-845:1987, 845-01-30, modified – Note to entry added.]

3.18.3**radiation**

<infrared> thermal radiation emitted in the infrared region of the electromagnetic spectrum

3.18.4

radiation

<long wave infrared> infrared energy that is radiated at a wavelength that is between 5 microns and 100 microns

3.18.5

radiation

<medium wave infrared> infrared energy that is radiated at a wavelength that is between 2,5 microns and 5 microns

3.18.6

radiation

<re-emitted infrared> portion of thermal energy absorbed by a media that is in turn emitted in the infrared portion of the electromagnetic spectrum

3.18.7

radiation

near infrared radiation

<short wave infrared> infrared energy that is radiated at a wavelength that is between 0,78 microns and 2,5 microns

3.18.8

radiometry

measurement of radiation in the optical spectrum

Note 1 to entry: This includes infrared (IR), ultraviolet (UV), and visible.

3.18.9

random sample

set of individuals that is taken from a population in such a way that each possible individual in the population has an equal chance of being selected

3.18.10

reflection

<signal propagation> fraction of a propagating signal that is reflected back toward its source after the signal has encountered a discontinuity in the electrical impedance of the transmission line on which it is travelling

3.18.11

reflection coefficient

ratio of the power or voltage of a microwave signal reflected from a load resistance that is attached to a circuit or transmission line to the power of the incoming signal

3.18.12

relative permittivity

ϵ_r

ratio of the permittivity of a material to that of free space

3.18.13

reliability

probability that a component, device, or assembly functions properly for a definite period of time under the influence of specific environmental and operational conditions

3.18.14

return loss

level of the reflected signal, which is a result of a mismatch between a load and a source

Note 1 to entry: It is usually expressed as the ratio of reflected power to incident power in dB.

3.18.15**rigid-flex double-sided printed board****flex-rigid double-sided printed board**

flex-rigid printed board with conductive patterns on two sides comprising one conductive pattern on the flexible base material and the other on the rigid base material

[SOURCE: IEC 60050-541:1990, 541-01-17]

3.18.16**rigid-flex printed board****flex-rigid printed board****flex-rigid printed wiring board**

printed board using a flexible base material and a combination of flexible and rigid base materials in different areas

Note 1 to entry: Both the flexible and the rigid base material bear conductive patterns which are normally interconnected in the combined area.

[SOURCE: IEC 60050-541:1990, 541-01-16]

3.18.17**rise time**

interval of time between the instants at which the instantaneous value of a pulse first reaches a specified lower value and then a specified upper value

Note 1 to entry: Unless otherwise specified, the lower and upper values are fixed at 10 % and 90 % of the pulse magnitude.

[SOURCE: IEC 60050-161:1990, 161-02-05]

3.19 S**3.19.1****sampling plan**

statistically derived set of sample sizes, accept numbers, and/or reject number which will confirm that a given lot of materials meets established AQLs or LTPDs

3.19.2**schematic diagram**

drawing that shows, by means of graphic symbols, the electrical connections, components and functions of a specific circuit arrangement

3.19.3**screen printing****silkscreening**

transferring of an image to a surface by forcing a suitable screen printing ink with a squeegee through an imaged-screen mesh

3.19.4**secondary side**

side of a packaging and interconnecting structure that is opposite the primary side

Note 1 to entry: It is the same as the "solder side" on printed boards for through-hole mounting technology.

Note 2 to entry: See also "primary side".

3.19.5**section beam**

flanged cylinder onto which yarn is drawn and accumulated from the yarn bobbins or packages

3.19.6

sectional specification

SS

document that describes the specific requirements pertaining to a portion of a set, family, or group of products, materials, or services

3.19.7

semiconductor

solid material, such as silicon, that has a resistivity that is midway between that of a conductor and of a resistor

3.19.8

semiconductor carrier

package for a semiconductor die

3.19.9

sheet resistance

electrical resistance of a planar film of a resistive material with uniform thickness as measured across opposite sides of a unit square pattern

Note 1 to entry: Sheet resistance is expressed in ohms per square.

3.19.10

shelf life

duration of the time interval a raw material or semi-finished product may be stored under specified conditions without changing any important properties

[SOURCE: IEC 60050-212:2010, 212-13-15]

3.19.11

shielding

<electronic> physical barrier, that is usually electrically conductive, that reduces the interaction of electric or magnetic fields upon devices, circuits, or portions of circuits

3.19.12

shrink sop

SSOP

family of component packages with four sizes, each having the ability to provide lead pitches between 0,625 mm (0,002 5 in) and 0,3 mm (0,012 in)

3.19.13

signal

electrical impulse of a predetermined voltage, current, polarity and pulse form representing information to be transmitted

3.19.14

signal conductor

individual conductor that is used to transmit an impressed electrical signal

3.19.15

signal line

conductor used to transmit a logic signal from one part of a circuit to another

silicon on insulator

SOI

fabrication technology that uses an insulating material as the bulk material instead of silicon, which may be sapphire (SOS)

Note 1 to entry: Silicon on insulator is a general term.