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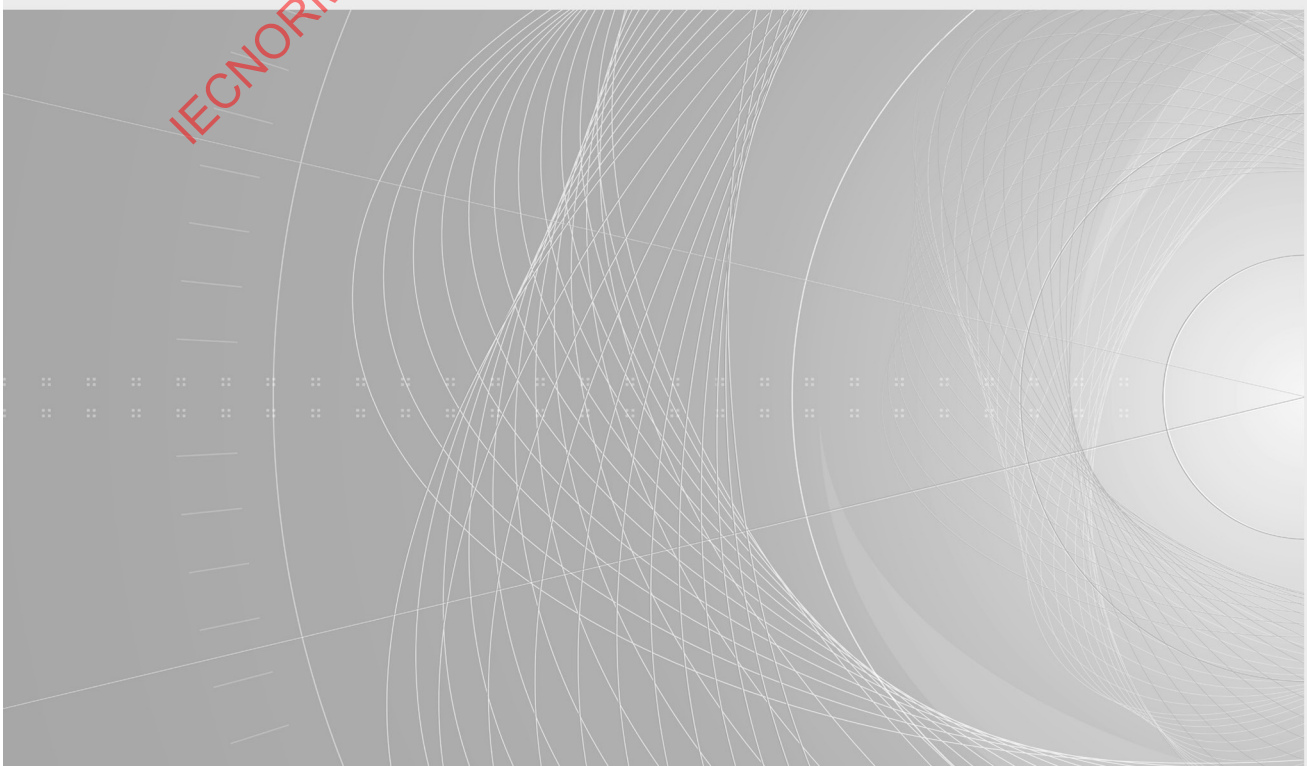
INTERNATIONAL STANDARD

Electronic assembly, design and circuit boards – Vocabulary – Part 2: Common usage in electronic technologies as well as electronic assembly technologies



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Electronic assembly, design and circuit boards – Vocabulary – Part 2: Common usage in electronic technologies as well as electronic assembly technologies

INTERNATIONAL ELECTROTECHNICAL COMMISSION

ICS 31.180; 31.190

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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ELECTRONIC ASSEMBLY, DESIGN AND CIRCUIT BOARDS – VOCABULARY –

Part 2: Common usage in electronic technologies as well as electronic assembly technologies

FOREWORD

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IEC 60194-2 has been prepared by IEC technical committee 91: Electronics assembly technology. It is an International Standard.

This second edition cancels and replaces the first edition published in 2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) exclusion of 116 terms transferred to IEV;
b) inclusion of 9 new terms related to printed electronics and packaging technology;
c) revision of definitions of 23 terms reflecting current technology;

d) three "printed wiring" terms were removed;

e) reintroduction of identification codes for terms.

The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1996/FDIS	91/2014/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 60194 series, published under the general title *Electronic assembly, design and circuit boards*, can be found on the IEC website.

Future documents in this series will carry the new general title as cited above. Titles of existing documents in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

ELECTRONIC ASSEMBLY, DESIGN AND CIRCUIT BOARDS – VOCABULARY –

Part 2: Common usage in electronic technologies as well as electronic assembly technologies

1 Scope

This part of IEC 60194 covers terms and definitions related to circuit board and electronic assembly technologies as well as other electronic technologies.

The terms have been classified according to the decimal classification code (DCC) and this DCC number appears just below the defined term. The DCC numbering is fully explained in Annex A.

A list of terms in alphabetical order with code number is provided in Annex B.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

In order to avoid two ID numbers, the usual practice of numbering every paragraph (every term and definition) in front of the paragraph has not been followed in this document. The official IEC number is the number which follows the DCC and the period (e.g., 21.xxxx).

3.1 Engineering and design for electronic packaging

3.1.1
ground plane
20.1413
conductor layer, or portion thereof, that serves as a common reference for electrical circuit returns, shielding, or heat sinking

Note 1 to entry: See also "signal plane" and "voltage plane" in IEC 60194-1:2021.

3.1.2
analogue circuit
21.0037
electrical circuit that provides a continuous relationship between its input and output

3.1.3
attenuation
21.0061
decrease of the energy of an electromagnetic wave during its propagation, represented quantitatively by the ratio of the power flux densities at two specified points

Note 1 to entry: Attenuation is generally expressed in decibels.

[SOURCE: IEC 60050-705:1995, 705-02-05]

3.1.4
capacitive coupling
21.0174
electrical interaction between two conductors that is caused by the capacitance between them

3.1.5
characteristic impedance
21.0194
capacitive coupling quantity defined for a mode of propagation at a given frequency in a specific uniform transmission line or uniform waveguide by one of the three following relations:

$$Z_1 = S / | I |^2 \quad (1)$$

$$Z_2 = | U |^2 / S \quad (2)$$

$$Z_3 = U / I \quad (3)$$

where

Z is the complex characteristic impedance,

S is the complex power, and

U and I are the values, usually complex, respectively of a voltage and a current conventionally defined for each type of mode by analogy with transmission line equations.

EXAMPLE 1 For a parallel-wire transmission line, *U* and *I* can be uniquely defined, and the three equations are consistent. If the transmission line is lossless, the characteristic impedance is real.

EXAMPLE 2 For a waveguide, the conventional definitions for U and I depend on the type of mode and generally lead to three different values of the characteristic impedance.

EXAMPLE 3 For a circular waveguide in the dominant mode TE_{11}, U = the RMS voltage along the diameter where the magnitude of the electric field strength vector is a maximum, I = the RMS longitudinal current.

EXAMPLE 4 For a rectangular waveguide in the dominant mode TE_{10}, U = the RMS voltage between midpoints of the two conductor faces normal to the electric field strength vector, I = the RMS longitudinal current following on one surface normal to the electric field strength vector.

[SOURCE: IEC 60050-726:1982, 726-07-01]

3.1.6
circuit
21.0213
number of electrical elements and devices that have been interconnected to perform a desired electrical function

3.1.7
compensation circuit
21.0231
electrical circuit that alters the functioning of another circuit to which it is applied to achieve a desired performance

3.1.8
crosstalk
21.0327
spurious signal
21.1006
undesirable transfer of electrical energy between neighbouring conductors (coupling) by mutual inductance and capacitance

Note 1 to entry: See also "backward crosstalk" and "forward crosstalk".

3.1.9
digital circuit
21.0380
electrical circuit that provides two (binary) or three distinct relationships (states) between its input and output

3.1.10
electromagnetic compatibility
EMC
21.0427
ability of equipment or a system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment

[SOURCE: IEC 60050-161:1990, 161-01-07]

3.1.11
electromagnetic interference
EMI
21.0431
degradation of the performance of a piece of equipment, transmission channel or system caused by an electromagnetic disturbance

Note 1 to entry: In French, the terms "perturbation électromagnétique" and "brouillage électromagnétique" designate respectively the cause and the effect and should not be used indiscriminately.

Note 2 to entry: In English, the terms "electromagnetic disturbance" and "electromagnetic interference" designate respectively the cause and the effect, but they are often used indiscriminately.

[SOURCE: IEC 60050-161:1990, 161-01-06]

3.1.12
electrostatic discharge
ESD
21.1716
transfer of electric charge between bodies of different electrostatic potential in proximity or through direct contact

[SOURCE: IEC 60050-161:1990, 161-01-22]

3.1.13
electrostatic discharge sensitive device
21.0441
device with known sensitivity or susceptibility to ESD

3.1.14
far-end crosstalk
21.0473
forward crosstalk
21.1406
noise induced into a adjacent line, as seen at the end of the adjacent line that is the farthest from the signal source, because the adjacent line has been placed next to an active line

3.1.15
leakage current
21.0699
electric current in an unintended conductive path under normal conditions

[SOURCE: IEC 60050-161:1990, 195-05-15]

3.1.16
line coupling
21.0711
interaction between two transmission lines that is caused by their mutual inductance and capacitance

3.1.17
load capacitance
21.0713
capacitance seen by the output of a logic circuit or other signal source

3.1.18
microwave integrated circuit
21.0762
integrated circuit that performs at microwave frequencies

3.1.19
near-end crosstalk
21.0795
backward crosstalk
21.1332
noise induced into an adjacent line, as seen at that end of the adjacent line which is closest to the signal source, when this line has been placed near an active line

3.1.20
logic circuit
21.1005
functional digital circuit used to perform computational functions

3.1.21
conductor
22.0254
electrical path
20.0837
single conductive path in a conductive pattern

[SOURCE: IEC 60050-161:1990, 541-01-20]

3.1.22
printed contact
22.0915
element of a conductive pattern that serves as one part of a contact system

3.1.23
signal conductor
22.0934
individual conductor that is used to transmit an impressed electrical signal

3.1.24
signal line
22.0935
conductor used to transmit a signal from one part of a circuit to another

3.1.25
conductive pattern
22.1362
configuration formed by the electrically conductive material of a circuit board

3.1.26
primary side
22.1484
side of a packaging and interconnecting structure that is defined as such on the master drawing

3.1.27
secondary side
22.1517
side of a packaging and interconnecting structure that is opposite the primary side

3.1.28
base material thickness
22.1604
thickness of the base material excluding conductive foil or material deposited on the surfaces

3.1.29
termination
22.1773
end of a conductor that connects the conductor to a terminal, distributing frame, switch or matrix

3.2 Components for electronic packaging

3.2.1
active device
30.0016
electronic component whose basic character changes while operating on an applied signal

Note 1 to entry: This includes diodes, transistors, thyristors, and integrated circuits that are used for the rectification, amplification, switching, etc., of analogue or digital circuits in either monolithic or hybrid form.

3.2.2
add-on component
30.0019
discrete or integrated packaged or chip components that are attached to a film circuit in order to complete the circuit's function

3.2.3
package cover
30.0053
cover that encloses the contents In the cavity of a package in the final sealing operation

3.2.4
CMOS
complementary metal oxide semiconductor
30.0221
complementary metal oxide semiconductor devices wherein N type and P type transistors are connected together for switching

3.2.5
discrete component
30.0392
separate part of a circuit board assembly that performs a circuit function

EXAMPLE resistor, capacitor, transistor.

3.2.6
heatsink
30.0594
mechanical device that is made of a high thermal- conductivity and low specific- heat material that dissipates heat generated by a component or assembly

3.2.7
microcircuit
30.0727
relatively high-density combination of equivalent circuit elements that are interconnected so as to perform as an indivisible electronic circuit component

3.2.8
microelectronics
30.0759
field of science and engineering that deals with highly miniaturized electronic circuits and their use

[SOURCE: IEC 60050-161:1990, 521-10-01]

3.2.9
monolithic integrated circuit
30.0777
integrated circuit in the form of a monolithic structure

3.2.10
package cap
30.0821
cuplike package cover

3.2.11
package lid
30.0822
flat package cover

3.2.12
perimeter sealing area
30.0844
surface on the perimeter of a package cavity that is used as an attachment to the package cover

3.2.13
semiconductor
30.1289
solid material, such as silicon, that has a resistivity that is midway between that of a conductor and of a resistor

3.2.14
quad flat J-lead
QFJ
30.1400
generic rectangular component package, containing an electronic device, with leads on all four sides that are formed in a "j" shape

3.2.15
quad flat no-lead
QFN
30.1402
generic rectangular component package outline wherein the metal pad terminations are formed on four sides of the bottom of a package

3.2.16
integrated circuit
30.1426
combination of inseparable associated circuit elements that are formed in place and interconnected on or within a single base material to perform a particular electrical function

3.2.17
passive component
30.1468
<element> discrete electronic device whose basic character does not change while it processes an applied signal

3.2.18
very large scale integration
VLSI
30.1559
integrated circuits with more than 80 000 transistors on a single die that are interconnected with conductors that are 1 µm or less in width

3.2.19
wafer level packaging
30.1564
technique of partial encapsulation and protection of die while still on the wafer and before the wafer is divided into singulated dies

3.2.20
hermetic
30.1867
<sealing> condition of sealing a component from incoming gases to a specific of inward diffusion normally less than 1×10^{-6} cm^3/s

3.2.21
base plane
30.2011
plane that includes the lowest point of the mounting surface of the package, except for packages using stand-offs

3.2.22
through hole package
THP
31.0858
electronic package for pin insertion assembly type of components or devices

3.2.23
single-inline package
SIP
31.0942
component package with one straight row of pins or wire leads

3.2.24
leaded chip carrier
31.1224
chip carrier whose external connections consist of leads that are around and down the side of the package

Note 1 to entry: See also "leadless chip carrier".

3.2.25
dual inline package
DIP
31.1387
basically, rectangular component package that has a row of leads extending from each of the longer sides of its body that are formed at right angles to a plane and parallel to the base of its body

3.2.26
ceramic dual inline package
CERDIP
31.1611
package that has a body of ceramic material, is hermetically sealed by a glass and that has two parallel rows of pins

3.2.27
ceramic pin grid array
ceramic PGA
31.1612
pin grid array package (PGA) made of ceramic material, hermetically sealed by metal that has pin-type leads in a matrix of rows and columns; terminals may be missing from some row-column intersection

3.2.28
pin grid array
PGA
31.1965
square or rectangular component package with pins protruding from the bottom surface with a pitch perpendicular to the plane of the package

SEE: Figure 1

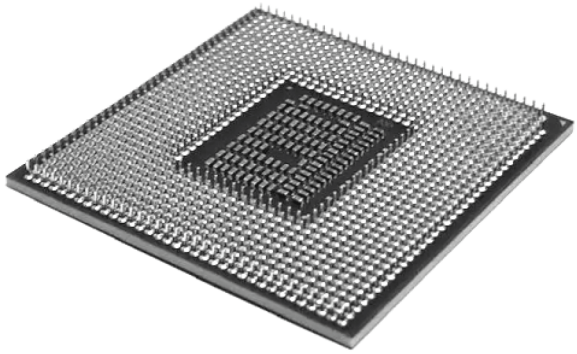

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Figure 1 – Pin grid array

3.2.29
passive array
32.1295
multiple passive components of similar function mounted on the primary interconnect substrate

SEE: Figure 2

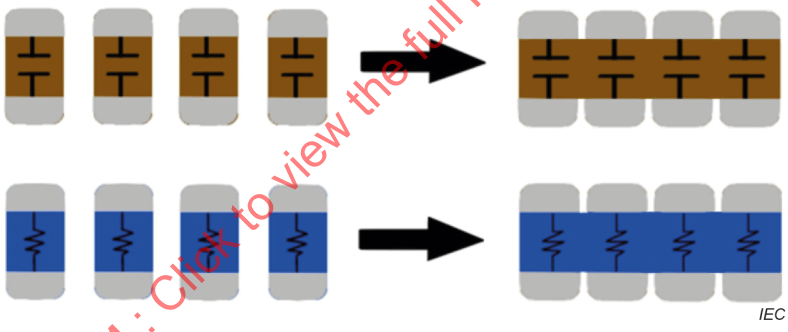

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Figure 2 – Passive array

Note 1 to entry: Examples include an array of capacitors or resistors.

3.2.30
chip carrier
33.0208
low-profile, usually square, surface-mount component semiconductor package whose die cavity or die mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package

3.2.31
coplanar leads
33.0295
flat beam leads of a component package that have been formed so that they can simultaneously contact one plane of a base material

3.2.32
flat pack
33.0523
rectangular component package that has a row of leads extending from each of the longer sides of its body that are parallel to the base of its body

3.2.33
metal package
33.0579
hybrid circuit package made mainly of metal

3.2.34
leadless device
33.0694
separated part (or whole) of a wafer intended to perform a function or functions in a device

3.2.35
known tested die
KTD
33.0910
die-form semiconductor product functionally verified by probing tests equal to the expected performance of the packaged product, without full quality assurance by supplier(s)

Note 1 to entry: The testing requirements are according to the agreement between trading partners.

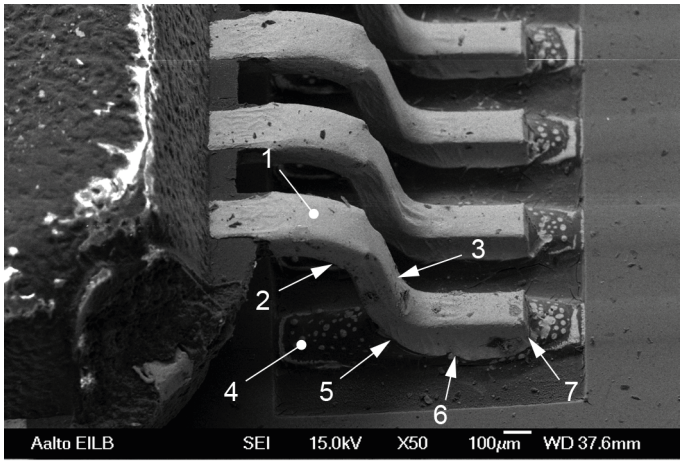
3.2.36
multichip module
MCM
33.1110
<structure> module that contains two or more dice and/or minimally packaged dice

Note 1 to entry: Also see "hybrid circuit" and "multi-chip package".

3.2.37
multi-chip package
MCP
33.1112
package that contains more than one dice and/or minimally packaged dice

3.2.38
leaded surface-mount component
33.1435
surface-mount component for which external connections consist of leads that are around and down the side of the package

SEE: Figure 3



Key

1 Knee
2 Upper bend radius
3 Lower bend radius
4 Land
5 Heel
6 Foot
7 Toe

Figure 3 – Leaded surface-mount component – Gull wing shaped lead (Courtesy of Aalto University)

Note 1 to entry: See also "leadless surface-mount component" in IEC 60194-1:2021.

3.2.39
leadless chip carrier
33.1435
chip carrier whose external connections consist of metallized terminations that are an integral part of the component body

3.2.40
bipolar device
33.1573
device in which both majority and minority carriers are present

3.2.41
bonding pad
33.1585
<IC> area of metallization on an integrated circuit die that permits connection of fine wires or a circuit element to the die

3.2.42
ceramic quad flat package
CQFP
33.1613
quad flat package (QPF) made of a ceramic material, hermetically sealed by metal, with leads extending from all four sides

3.2.43
QFP with bumper
BQFP
33.1835
QFP package with a guarding bumper

3.2.44
quad flat pack
QFP
33.1836
generic square or rectangular component package, containing a semiconductor die, with leads on all four sides that are formed in a "gullwing" shape

3.2.45
fine pitch QFP
33.1837
quad flat pack (QFP) package whose lead pitch centres at 0,65 mm or less

3.2.46
chip scale package
CSP
33.1838
generic term for packaging technologies that result in a packaged part that is only marginally larger than the internal die

3.2.47
land grid array
LGA
33.1891
square package with termination lands located in a grid pattern on the bottom of the package

3.2.48
plastic ball grid array
PBGA
33.1971
polymer-based BGA

3.2.49
plastic leaded chip carrier
PLCC
33.1972
surface-mount family of integrated circuit plastic packages with leads exiting from all four sides of the package

3.2.50
plastic quad flat pack
PQFP
33.1974
surface-mount family of integrated circuit packages, bounded on all four sides by bumpers, with leads exiting from all four sides of the package and formed into a "gullwing" lead format

3.2.51
single chip package
SCP
33.2034
integrated circuit package containing only one semiconductor die

3.2.52
small outline J-lead
SOJ
33.2040
generic rectangular component package, whose chip cavity or mounting area occupies a major portion of the package area, with leads on two opposite sides that are formed in a "J" shape

3.2.53
small outline no-lead
SON
33.2050
generic rectangular component package outline wherein the metal pad terminations are formed on two sides of the bottom of the package

3.2.54
small outline package
SOP
33.2060
generic rectangular component package, whose chip cavity or mounting area occupies a major portion of the package area, with leads or metal pad surfaces on two opposite sides

3.2.55
system in package
SiP
33.2070
multi-chip package (MCP) that performs a system function

3.2.56
system on a chip
SoC
33.2072
active die that functions as a complete system aside from power delivery and second level memory

Note 1 to entry: Second level memory are different forms of on-die memory additional to traditional registers and cache/SRAM; newer memory types such as ReRAM, MRAM, hybrid D/PC-RAM or integrated HBM are possible.

3.2.57
tape carrier package
TCP
33.2077
semiconductor package that has the TAB connection and is coated with a resin

3.2.58
wafer-level package
33.2110
<chip-scale package> chip-scale package whose size is generally equal to the size of the semiconductor device it contains and that is formed by processing on a complete wafer rather than on an individual device

Note 1 to entry: Because of the wafer-level processing, the size of a wafer-level package may be defined by finer dimensions and tighter tolerances than those for a similar non-wafer-level package.

Note 2 to entry: The package size will change with changes in the size of the die.

3.2.59
area array package
34.0811
package that has terminations arranged in a grid on the bottom of the package and contained within the package outline

3.2.60
ball grid array
BGA
34.1096
surface mount package that has solder balls attached to one side of a substrate in a matrix of rows and columns; terminals may be missing from some row-column intersections

[SOURCE: IEC 60191-6-18:2018]

SEE: Figure 4

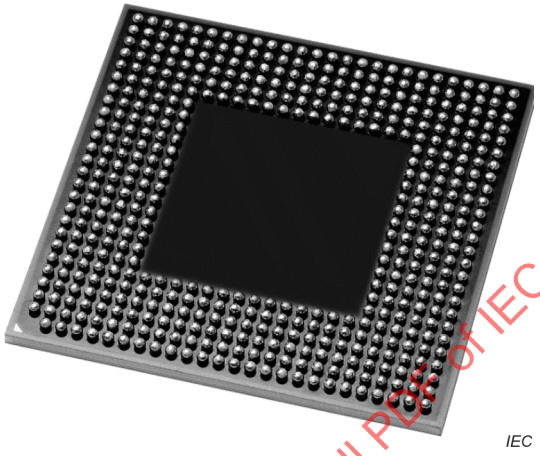


Figure 4 – Ball grid array (BGA)

3.2.61
cupping
34.1801
<BGA> condition of a ball grid array package after reflow where the corners turn up and away from the circuit board laminate surface

Note 1 to entry: This condition in the worst case causes the balls on the outside row to be in tension and the balls in the centre to be in compression.

Note 2 to entry: Opposite of "doming <BGA>".

3.2.62
doming
34.2011
<BGA> condition of a ball grid array package after reflow where the corners turn down and toward the circuit board laminate surface

Note 1 to entry: This condition in the worst case causes the balls on the outside row to be compressed and the balls in the centre to be in tension.

Note 2 to entry: Opposite of "cupping <BGA>".

3.2.63
bare die
35.0111
unpackaged discrete semiconductor or integrated circuit with pads on the upper surface suitable for interconnection to the substrate or package

3.2.64
bond pads
35.0121
metallised areas on the die that are used for temporary or permanent electrical connection (bonding)

3.2.65
chip
35.0205
SEE: "die".

3.2.66
dice
35.0373
more than one die

3.2.67
die
35.0375
separated part (or whole) of a wafer intended to perform a function or functions in a device

3.2.68
die device
35.0381
bare die, with or without connection structures, or a minimally packaged die

3.2.69
junction temperature
35.0666
temperature of the region of a transition between the p-type and n-type semiconductor material in a transistor or diode element during operation

3.2.70
known good die
KGD
35.0846
die-form semiconductor product that provides assurance of equivalent quality and reliability as that found in its conventionally packaged counterparts

3.2.71
probed die
PD
35.0912
semiconductor die evaluated by probing tests, but without quality assurance by supplier(s)

3.2.72
uncased device
35.1122
component without a package

3.2.73
wafer
35.1145
slice or a flat disc, either of semiconductor material or of such a material deposited on a substrate, in which one or more circuits or devices can be processed

3.2.74
dicing
35.1685
separating of wafers into individual die

3.2.75
wire bond
35.2130
completed wire connection that provides electrical continuity between the die and a terminal

3.2.76
backfill
36.0075
filling a hybrid circuit package with a dry inert gas prior to hermetic sealing

3.2.77
compression seal
36.0243
tight joint made between a component package and its leads that is formed as heated metal cools and shrinks around a glass insulator

3.2.78
support ring
36.1033
ring made of a dielectric material that is used to hold beam leads in place relative to one another outside of a packaged device

3.2.79
J-leads
36.1752
preferred surface mount lead form used on PLCCs (plastic leaded chip carrier), so named because the lead the lead has J shape, departs the package body near its Z-axis centreline, is formed down then rolled under the package

Note 1 to entry: Leads so formed are shaped like the letter "J."

3.2.80
lead frame
36.1902
metallic portion of the device package on which the integrated circuit die is mounted and connected from the die or dice bonding sites to the structure that becomes the outer leads of the package

3.2.81
coaxial cable
37.0220
cable in the form of a central wire surrounded by a conductor tubing or sheathing that serves as a shield and return

3.2.82
metal oxide semiconductor
MOS
39.1050
fabrication technology, resulting in the creation of FET devices

3.2.83
passive network
39.1275
multiple passive components that have more than one function and are formed on the surface of a separate substrate and packaged in a single SMD case

Note 1 to entry: The case is then mounted on the primary interconnected substrate of the system.

Note 2 to entry: Passive networks typically have several internal connections to form simple functions such as terminations or filters.

3.2.84
silicon on insulator
SOI
39.1410
fabrication technology that uses an insulating material as the bulk material instead of silicon, which may be sapphire (SOS)

Note 1 to entry: Silicon on insulator is a general term.

3.2.85
silicon on sapphire
SOS
39.1450
specific fabrication technology that uses sapphire, a variety of corundum (Al_2O_3), as the bulk material instead of silicon

3.3 Materials for electronic packaging

3.3.1
conductivity
40.0250
<electrical> ability of a substance or material to conduct electricity

3.3.2
conductivity
40.0261
<thermal> ability of a substance or material to conduct heat

3.3.3
anisotropy
40.0685
condition for a substance having differing values for properties, such as permittivity, depending on the direction within the material

3.3.4
printed electronics sheet board
40.1276
sheet (board) of forming an electronically functional pattern and/or devices on a large-scale by printing of conductive materials

3.3.5
base material
40.1334
insulating material upon which a conductive pattern may be formed

3.3.6
bias
44.0105
<fabric> filling yarn that is off-square with the warp ends of a fabric

3.3.7
constraining core
44.0273
supporting plane that is internal to a packaging and interconnecting structure

3.3.8
creel
44.0315
device used as a yarn package rack to hold warp ends for a section beam

3.3.9
supporting plane
44.1032
planar structure that is a part of a packaging and interconnecting structure in order to provide mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical characteristics

Note 1 to entry: It may be either internal or external to the packaging and interconnecting structure.

Note 2 to entry: See also "constraining core".

3.3.10
chemical vapour deposition
45.0202
process in which vapours and gases react chemically to produce deposits at the surface of a substrate

[SOURCE: IEC 60050-841:2004, 841-22-07]

3.3.11
conductive ink
45.0235
conductive fluid in which chemical precursors, polymers, or particles are dissolved or dispersed

[SOURCE: IEC 62899-101:2019]

3.3.12
conductive medium
45.0261
material with a suspended powder of an electrically conductive material

Note 1 to entry: See also conductive paints, inks, pastes.

3.3.13
film conductor
45.0501
conductor formed in place on a base material by depositing a conductive material using screening, plating or evaporating techniques

3.4 Assembly process for interconnection structures

3.4.1
bridging
70.0149
<electrical> unintentional formation of a conductive path between conductors

3.4.2
mixed component mounting technology
70.1452
<circuit board assembly> component mounting technology that uses both through-hole and surface-mounting technologies on the same packaging and interconnecting structure

3.4.3
component mounting site
70.1632
location on a packaging and interconnecting structure (P&I) that consists of a land pattern and conductor fan-out to additional lands for testing or vias that are associated with the mounting of a single component

3.4.4
flexible material interconnect construction
FMIC
70.1846
integration of passive and active components with mechanical components (including switches and connectors) on a flexible or thin base material, i.e., flexible circuit board, in order to produce an electronic assembly

3.4.5
pick-up tool
73.1759
tool used to pick up surface-mount components from a packaging medium for placement on a substrate and which may be hand activated or a part of a pick-and-place machine

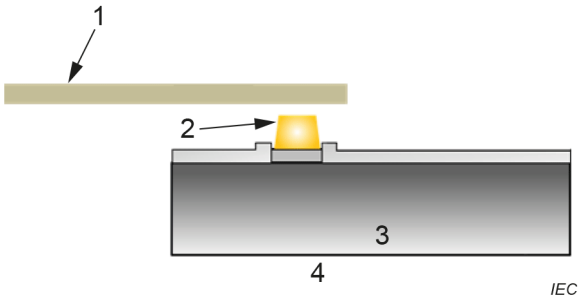
3.4.6
pick-up force
73.1760
force required to pick up a surface-mount component from its packaging medium for placement on a substrate

3.4.7
bonding wire
74.0132
gold, copper, silver, aluminium and alloy wire used for making electrical connections between lands, lead frames, and terminals

3.4.8
bumped die
74.0160
interconnection with a package or another device

SEE: Figure 5

Note 1 to entry: Use of the word bonding implied a bonding process is used which is not always the case.



Key

1 Inner-lead

2 Bump

3 Semiconductor chip

4 Bumped die

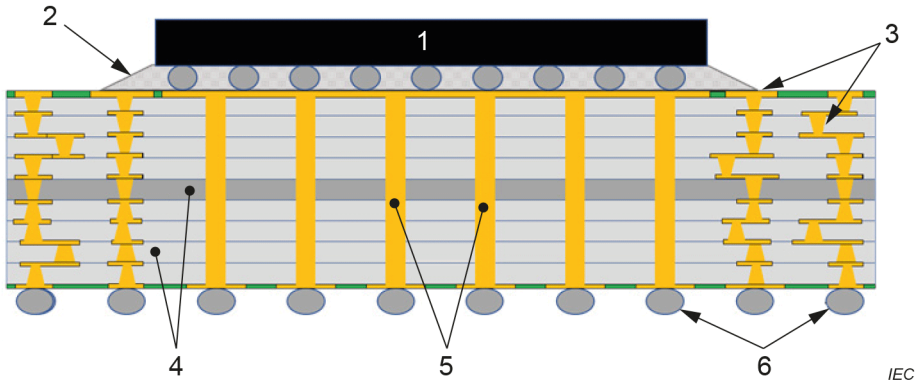
Figure 5 – Bumped die with inner lead

3.4.9
dead-bug, adj
74.0351
orientation of a package with the terminations facing up

3.4.10
die bonding
74.0376
attachment of a die to base material

3.4.11
flip chip
74.0530
leadless monolithic circuit element structure that electrically and mechanically interconnects to a circuit board by conductive bumps and solder balls

SEE: Figure 6



Key

1 IC

2 Underfill epoxy

3 Copper conductors and microvia connections

4 Substrate

5 Thermal vias

6 Eutectic solder balls

Figure 6 – Flip chip

3.4.12
semiconductor carrier
74.1290
package for a semiconductor die

3.4.13
chip-on-flex
COF
74.1619
semiconductor chip mounted directly onto a flexible circuit board

3.4.14
chip-on-glass
COG
74.1620
assembly technology that uses an unpackaged semiconductor die mounted directly on a glass substrate such as a glass plate for liquid crystal display (LCD)

3.4.15
solderability
75.0958
ability of the lead, termination or electrode of a component to be wetted by solder at the temperature of the termination or electrode, which is assumed to be the lowest temperature in the soldering process within the applicable temperature range of the solder

3.4.16
lead-free solder
75.1904
alloy that does not contain more than 0,1 % lead (Pb) by mass and that is used for joining components to substrates or for coating surfaces

3.4.17
peak package body temperature
Tp
75.1958
highest temperature that an individual package body reaches during moisture sensitivity level (MSL) classification

3.4.18
final seal
76.1397
manufacturing process that completes the enclosure of a microcircuit so that further internal processing cannot be performed without removing a lid or otherwise disassembling the package

3.5 Fabrication process for interconnection structures

3.5.1
printed component
52.0914
element (such as an inductor, resistor, capacitor, antenna, contact or interconnect line) that is formed as part of the printed pattern

3.5.2
screen printing
52.1204
transferring of an image to a surface by forcing a suitable screen-printing ink with a squeegee through an imaged-screen mesh

3.5.3
film network
53.0502
electrical network composed of thin-film and/or thick-film components on a base material

3.5.4
abrasive trimming
54.1318
adjustment of the value of a film component by notching it with a finely adjusted stream of an abrasive material against the resistor surface

3.5.5
lay-up
55.1900
process of combining one or more inner layers, and prepreg or adhesive layer(s) into a lamination package

Note 1 to entry: The package may consist of inner layers, outer layers and copper foil.

3.5.6
passivation
57.0832
top or final processing and covering on a die, usually of semiconductor oxide or nitride, that protects and seals the active areas of the die from further external chemical or mechanical contamination

3.6 Types and performance of interconnecting structures for electronic packaging

3.6.1
hybrid circuit board
60.0461
circuit board fabricated by combining subtractive and additive process technologies

3.6.2
interconnection
60.0782
joining of electrical devices to complete a circuit

3.6.3
packaging and interconnecting assembly
60.0823
assembly that has components mounted on one or both sides of a packaging and interconnecting structure

Note 1 to entry: "Packaging and interconnecting assembly" is a general term.

3.6.4
Jisso
60.0841
total solution for interconnecting, assembling, packaging, mounting, and integrating system design

Note 1 to entry: A term from Japanese.

3.6.5
circuit board
printed circuit
60.1625
conductive pattern that is composed of printed components, printed wiring, discrete wiring, or a combination thereof, that is formed in a predetermined arrangement on a common base

Note 1 to entry: This is also a generic term that is used to describe a circuit board that is produced by any of a number of techniques.

3.6.6
flexible circuit
flexible printed circuit
62.0525
patterned arrangement of circuitry and components that uses a flexible base material with or without a flexible coverlayer

flexible circuit board
flexible printed board
62.1579
circuit board using a flexible base material only

Note 1 to entry: It may be partially provided with electrically non-functional stiffeners and/or coverlayers.

[SOURCE: IEC 60050-541:1990, 541-01-14]

3.6.7
flexible single-sided circuit board
flexible single-sided printed board
62.1580
single-sided circuit board using a flexible base material only

Note 1 to entry: See also "flexible double-sided circuit board"

3.6.8
flexible double-sided circuit board
flexible double-sided printed board
62.1581
double-sided circuit board, either printed circuit or printed wiring, using a flexible base material only

Note 1 to entry: See also "flexible single-sided circuit board"

[SOURCE: IEC 60050-541:1990, 541-01-14]

3.6.9
flexible hybrid circuit board
62.1575
circuit board fabricated by combining traditional circuit board technology with printed electronics technology on conformable or stretchable substrates

3.6.10
flexible multilayer circuit board
flexible multilayer printed board
62.1582
multilayer circuit board using a flexible base material only

Note 1 to entry: Different areas of the flexible multilayer circuit board may have different numbers of layers and different thicknesses and consequently different flexibility.

[SOURCE: IEC 60050-541:1990, 541-01-05]

3.6.11
flex-rigid circuit board
flex-rigid printed board
63.0524
SEE: "rigid-flex circuit board".

3.6.12
flex-rigid double-sided circuit board
flex-rigid double-sided printed board
63.1570
SEE: "rigid-flex double sided circuit board".

3.6.13
moulded interconnection device
67.1926
combination of moulded plastic substrate and conductive patterns that provide both the mechanical and electrical functions of an electronic interconnection package

3.7 Types and performance of assemblies for electronic assembly

3.7.1
double-sided assembly
80.0401
packaging and interconnecting structure with components mounted on both the primary and secondary sides

Note 1 to entry: See also "single-sided assembly".

3.7.2
module
80.0775
separable unit in a packaging scheme

3.7.3
circuit board assembly
printed board assembly
80.0911
assembly that uses a circuit board for component mounting and interconnecting purposes

Note 1 to entry: "Printed board assembly" is a general term.

3.7.4
single-sided assembly
80.0944
packaging and interconnecting structure with components mounted only on one side

Note 1 to entry: See also "double-sided assembly".

3.7.5
assembly
assembled board
80.1327
number of parts, subassemblies or combinations thereof joined together

Note 1 to entry: This term can be used in conjunction with other terms listed herein, for example, "circuit board assembly".

3.7.6
thick-film circuit
83.1073
microcircuit in which passive components of a ceramic-metal composition are formed on a base material by screening and firing

3.7.7
thin-film hybrid circuit
83.1076
hybrid circuit with thin-film components and interconnections

Note 1 to entry: See also "hybrid circuit".

3.7.8
thin-film integrated circuit
83.1077
hybrid integrated circuit comprised only of thin-film components and interconnections

3.7.9
hybrid circuit
83.1417
circuit comprising insulating of base material with various combinations of interconnected film conductors, film components, semiconductor die(s), passive components and bonding wire

Note 1 to entry: See also "multi-chip module" and "multi-chip package".

3.7.10
hybrid integrated circuit
83.1418
circuit comprising insulating base material with various combinations of interconnected film conductors, film components, semiconductor dice, passive components and bonding wire that perform the same function as a monolithic semiconductor integrated circuit

3.7.11
hybrid microcircuit
83.1419
circuit comprising insulating base material with various combinations of interconnected film conductors, film components, semiconductor dice, passive components and bonding wire

3.7.12
in-mould electronics
IME
84.0614
manufacturing technology of integrating printed decorations and electronic circuitry with thermoforming and moulding

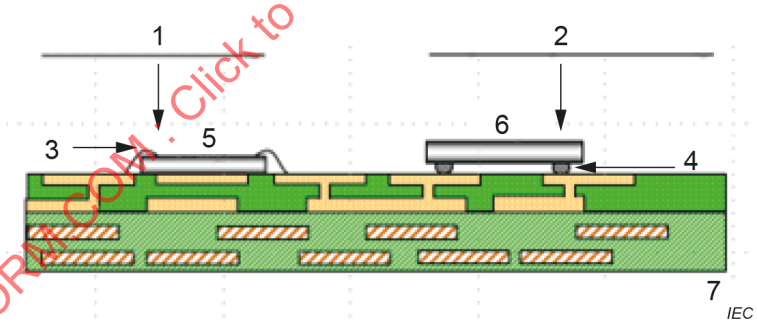
3.7.13
backplane
backpanel
85.1331
interconnection device used to provide point-to-point electrical interconnections

Note 1 to entry: It is usually a circuit board that has discrete wiring terminals on one side and connector receptacles on the other side.

Note 2 to entry: See also "mother board".

3.7.14
chip-on-board
COB
86.0207
circuit board assembly technology that places unpackaged semiconductor dice and interconnects them by wire bonding or similar attachment techniques

SEE: Figure 7



Key

1 Wire bonding
2 Flip-chip bonding
3 Bonding wire
4 Bump
5 Chip
6 Chip
7 Circuit board

Figure 7 – Chip on board (COB)

Note 1 to entry: The silicon area density is usually smaller than the density of the circuit board.

Note 2 to entry: A mounting and attachment technique where the die is mounted onto a substrate, often a circuit board.

3.7.15
integrated passive component
86.0700
multiple passive components that share a substrate and package

Note 1 to entry: Integrated passive components may be housed inside the layers of the primary interconnect substrate, and thus become embedded passive components. Alternatively, these components may be on the surface of a separate substrate that is then placed in an enclosure and surface mounted on the primary interconnect substrate, thus becoming passive arrays or passive networks.

3.7.16
microcircuit module
86.1446
combination of microcircuits and discrete components that are interconnected so as to perform as an indivisible circuit assembly

3.8 Quality and reliability, fabrication and assembly

3.8.1
sheet resistance
92.1525
electrical resistance of a planar film of a resistive material with uniform thickness as measured across opposite sides of a unit square pattern

Note 1 to entry: Sheet resistance is expressed in ohms per square.

3.8.2
bending resistance
92.1565
ability of a material to withstand repeated bending to specified parameters without producing cracks and breaks in excess of the specification allowance

3.8.3
substrate bending test
92.1771
test applied to a substrate to determine its resistance to bending and the effects of bending to the substrate and any components mounted on the substrate

3.8.4
burn-in
95.0164
<test> electrical and environmental test at elevated temperature, elevated voltage for a sufficient time that is used to screen out extrinsic and latent defects (infant mortality)

3.8.5
fine leak
95.0504
leak in a sealed package that is less than 1 μPa·m^3/s of differential air pressure

3.8.6
gross leak
95.0580
leak in a sealed package that is greater than 1 μPa·m^3/s of differential air pressure

3.8.7
package cracking
95.1945
cracks in a plastic integrated circuit package caused by stress that results from exposure to reflow solder temperature

Note 1 to entry: These cracks may propagate from the die or die pad to the surface of the package, or only extend part way to the surface of lead fingers.

Annex A
(informative)

Principles and use of the classification code

A.1 Background

The Decimal Classification Code (DCC) used in this document builds on the principles of widely acknowledged concepts that have been internationally accepted. The CC allows for the arrangement of terms according to various topics related to the elements and practices needed to produce electronic products.

Specifically intended to accommodate interconnecting structure design, fabrication, assembly and test, the primary emphasis is on circuit board and circuit board assembly products used in electronic packaging disciplines. Also included are the terminology for the processes, the materials, and component description, along with business administration issues, necessary to adequately define the products and services being performed.

The decimal classification code is divided into nine segments which are subdivided into topics.

1) Administration (topics 10-19)
2) Engineering and design for electronic packaging (topics 20-29)
3) Components for electronic packaging (topics 30-39)
4) Materials for electronic packaging (topics 40-49)
5) Fabrication performance of interconnection structures for electronic packaging (topics 50-59)
6) Types and processes for interconnecting structures (topics 60-69)
7) Assembly processes for interconnecting structures for electronic packaging (topics 70-79)
8) Types and performance of interconnecting structures assemblies for electronic packaging (topics 80-89)
9) Quality and reliability for electronic packaging, fabrication and assembly (topics 90-99)

The first part of the DCC Code consists of three digits which are available for categorizing terminology and information related to the nine segments. The first two digits describe the topic with a particular segment. The third digit is not standardized and is optional for users of the system and allows for a more detailed description of a particular topic.

Thus, a Classification Code of "44X" Signifies:

44 = topic 44 in segment 4 (Materials for Electronic Packaging/Reinforcement/Constraining)

X = a number optional at the discretion of the user

The second part of the DCC numbering scheme is a four-digit number that is assigned to a specific term and its definition, and which is unique to that term. These numbers are assigned in sequence of need, starting with the number 0001. For example, a complete number would be "44.0001". Terms are assigned to a Segment and Topic without duplication of the unique identification number. If a general term is used in the industry which can be applied to more than one Topic or Segment, the definition shall be enhanced to make it clear that the term belongs to only one Segment Topic.

An example is the term "void". This term might have three unique numbers and definitions. One is for a void in circuit board laminate, one is for a void in artwork emulsion, and one is for a void in solder joint.

The number assigned to each term is this standard shall be designated by the two-digit segment/topic descriptor, followed by a period(.), followed by a four-digit number that is assigned as the unique descriptor for each term; i.e., 44.0173, 56.2574, etc.

If a term is applicable to several areas, it is assigned a two-digit general topic/segment designator (i.e., 20,30)

The system has the capability of identifying almost ten thousand terms and their definitions. If the number is exceeded at some time in the future, the four-digit field will be increased by one digit by adding a zero (0) at the front of each existing number.

A.2 List of codes

A.2.1 Administration

10) General (administration issues)
11) Data processing
12) Personnel
13) Facilities
14) Environmental
15) Financial/purchasing
16) Inventory/shipping
17) Customer/vendor relations
18) <Reserved for future expansion>
19) Other (administration issues)

A.2.2 Engineering and design for electronic packaging

20) General (engineering and design issues)
21) Engineering
22) Circuit board and circuit board assembly design
23) Subassembly design
24) Photo tool generation and photographic processes
25) Electronic production data generation
26) Technical documentation
27) < Reserved for future expansion >
28) < Reserved for future expansion >
29) Other (engineering and design issues)

A.2.3 Components for electronic packaging

30) General (Component description issues)
31) Discrete and IC through-hole component packages
32) Discrete surface mount component packages
33) I/C package types for surface mounting
34) Grid array packages
35) Bare die and chip-scale components
36) Component and lead/termination properties
37) Components for wiring and cabling
38) < Reserved for future expansion >

39) Other (component description issues)

A.2.4 Materials for electronic packaging

40) General (material issues)
41) Rigid circuit board substrate materials (organic)
42) Flexible circuit board substrate materials (organic)
43) Inorganic substrates for interconnection structures
44) Reinforcement/constraining core/heat dissipation materials
45) Conductive materials (foil, film or plating)
46) Component attachment materials (conductive/non-conductive)
47) Coating and permanent masking materials
48) < Reserved for future expansion >
49) Other (material issues)

A.2.5 Fabrication process for interconnection structures

50) General (fabrication process for interconnection structures)
51) Mechanical processes
52) Imaging and application of resists and Inks
53) Metal deposition processes, including plating
54) Material removal processes, including etching
55) Lamination, sequential deposition, and moulding processes
56) Thermal cure/firing processes
57) Cleaning and chemical treatment processes
58) < Reserved for future expansion >
59) Other (interconnecting structure fabrication processes)

A.2.6 Types and performance of interconnecting structures for electronic packaging

60) General (interconnecting structure type and performance)
61) Rigid circuit boards (organic substrates)
62) Flexible circuit boards (organic substrates)
63) Flex-rigid circuit boards (organic substrates)
64) Discrete circuit boards (organic substrates)
65) Circuit boards (inorganic substrates)
66) Moulded structures (three dimensional)
67) Hybrid/multichip module interconnecting structures
68) < Reserved for future expansion >
69) Other (interconnecting structure type and performance issues)

A.2.7 Assembly process for interconnection structures

70) General (assembly process issues)
71) Component handling, storage and preparation
72) Through-hole mounting of components
73) Surface mounting of components
74) Bare chip placement and attachment
75) Joining techniques
76) Cleaning and conformal coating processes

77) Rework, repair and modification
78) < Reserved for future expansion >
79) Other (assembly process issues)

A.2.8 Types and performance of assemblies for electronic assembly

80) General (assembly type and performance issues)
81) Rigid circuit board assembly (organic substrates)
82) Flexible/rigid-flexible circuit board assembly (organic substrate)
83) Inorganic (ceramic, metal core, etc.) circuit board assemblies
84) Mounted or three dimensional circuit board assemblies
85) Backplanes
86) Multichip modules
87) < Reserved for future expansion>
88) < Reserved for future expansion>
89) Other (assembly type and performance issues)

A.2.9 Quality and reliability, fabrication and assembly

90) General (quality and reliability issues)
91) Process control/SPC
92) Inspection/testing
93) Component inspection, conditioning and evaluation
94) Quality management and assurance
95) Component quality and reliability
96) Interconnection structure quality and reliability
97) Electronic assembly/subassembly quality & reliability
98) < Reserved for future expansion>
99) Other (quality and reliability issues)

Annex B
(informative)

List of terms in alphabetical order with code number

B.1 A

abrasive trimming	54.1318
active device	30.0016
add-on component	30.0019
all metal package	33.0579
analog circuit	21.0037
anisotropy	40.0685
application specific integrated circuit	33.0692
area array package	34.0811
assembly	80.1327
attenuation	21.0061

B.2 B

backfill	36.0075
backplane	85.1331
backward crosstalk	21.1332
balanced transmission line	21.1333
ball grid array	34.1096
base material	40.1334
base material thickness	22.1604
base plane	30.2011
bending resistance	92.1565
bias	44.0105
bipolar device	33.1573
bond pads	35.0121
bonding pad	33.1585
bonding wire	74.0132
bow	60.0146
break-down voltage	21.1351
bridging, electrical	70.0149
bumped die	74.0160
burn-in	95.0164