IEC 60424-5

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INTERNATIONAL STANDARD

Ferrite cores – Guide on the limits of surface irregularities – Part 5: Planar-cores

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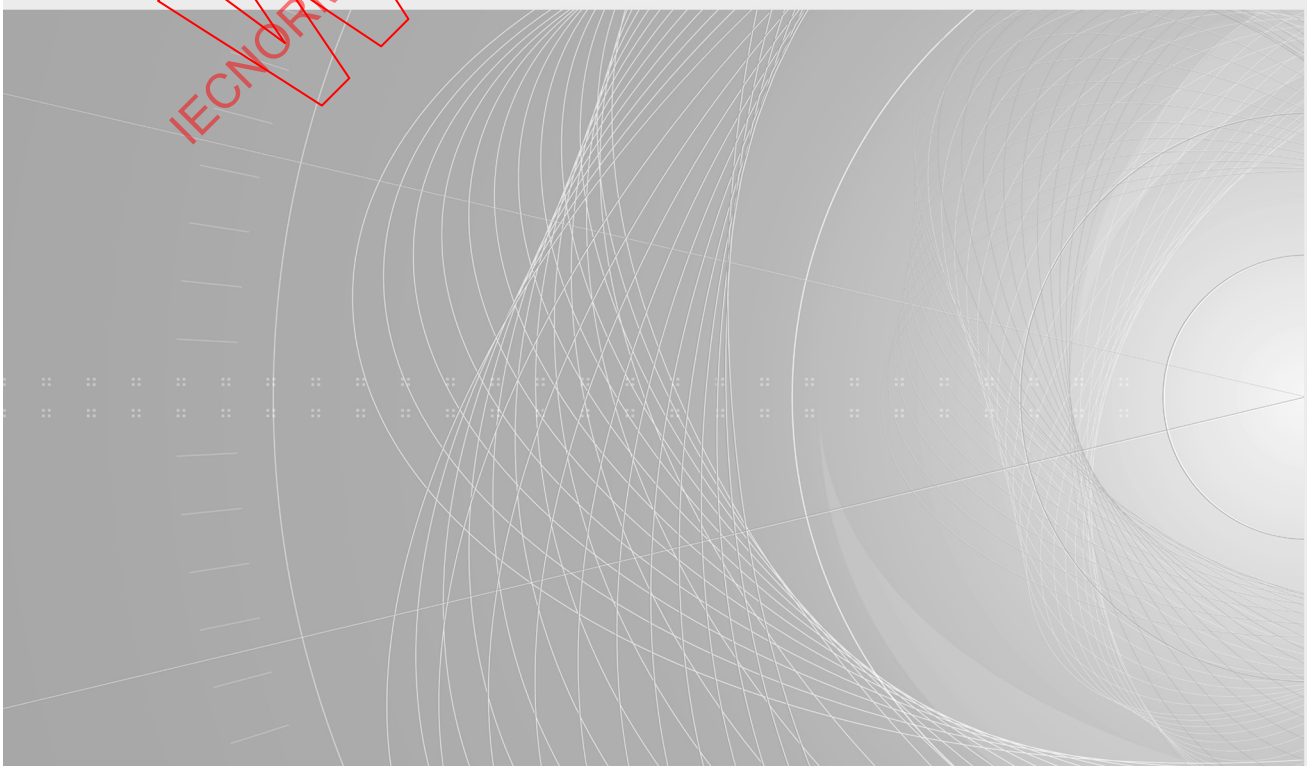

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FERRITE CORES – GUIDE ON THE LIMITS OF SURFACE IRREGULARITIES –

Part 5: Planar-cores

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International Standard IEC 60424-5 has been prepared by IEC technical committee 51: Magnetic components and ferrite materials.

The text of this standard is based on the following documents:

FDIS	Report on voting
51/947/FDIS	51/950/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of the IEC 60424 series, under the general title *Ferrite cores – Guide on the limits of surface irregularities*, can be found on the IEC website.

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The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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FERRITE CORES – GUIDE ON THE LIMITS OF SURFACE IRREGULARITIES –

Part 5: Planar-cores

1 Scope

This part of IEC 60424 gives guidance on allowable limits of surface irregularities applicable to planar-cores in accordance with the relevant generic specification defined in IEC 60424-1.

The relations between the main dimensions of planar E-, ER- and EL-cores differ from those of standard cores. For example, the width of planar cores is larger while the total height is much smaller. Also the thickness of the legs is in most cases smaller than compared to standard cores. Therefore the concept of fixed reference dimensions to determine the length of crack limits yield crack lengths which are not acceptable for this type of core. This part of IEC 60424 follows another concept which relates the crack length to dimensions of the surface on which the crack occurs.

Also the concept to determine the maximum area of chips based on the total mating surface fails in the case of planar cores. The outer legs of planar cores are much thinner than those of standard cores which makes overlapping and gluing much more difficult. A single chip of maximum size on the outer leg may risk the functionality of the core set. Therefore this standard uses as a reference the mating surface on which the chip occurs.

Windings of planar cores are often PCB's which are glued to the inner surfaces of the planar core. For this reason the inner surfaces of the planar cores need to have a better quality than the inner surfaces of standard cores. This was taken into account by reducing the maximum allowable area of pull outs in the inner surfaces.

This standard is considered as a sectional specification useful in the negotiation between ferrite core manufacturers and users about surface irregularities.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60424-1, *Ferrite cores – Guide on the limits of surface irregularities – Part 1: General specification*

IEC 62317-9, *Ferrite cores – Dimensions – Part 9: Planar-cores*

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3 Limits of surface irregularities

3.1 Chips and ragged edges

3.1.1 Chips and ragged edges on the mating surfaces (see Figures 1, 2 and 3)

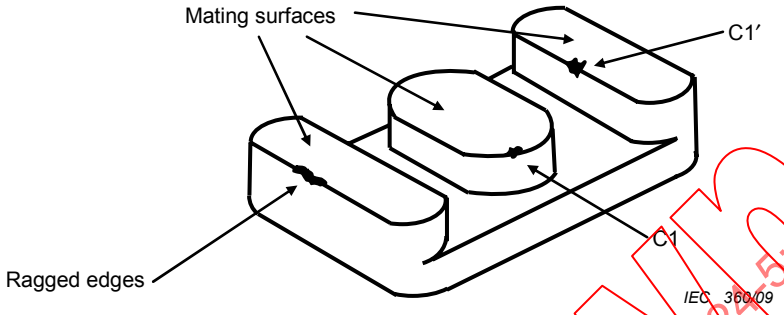

Figure 1 – Chip location for planar EL-core

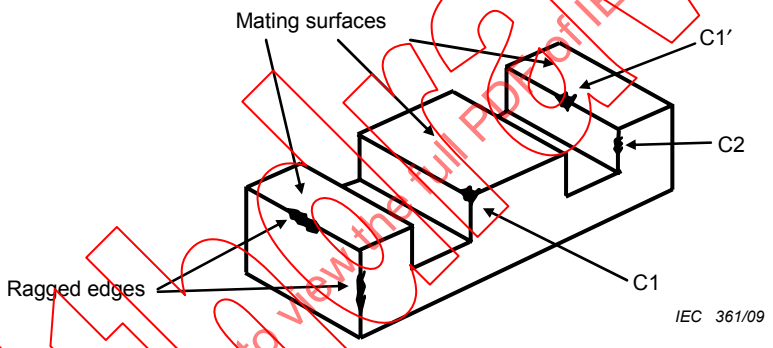

Figure 2 – Chip location for low profile E-core

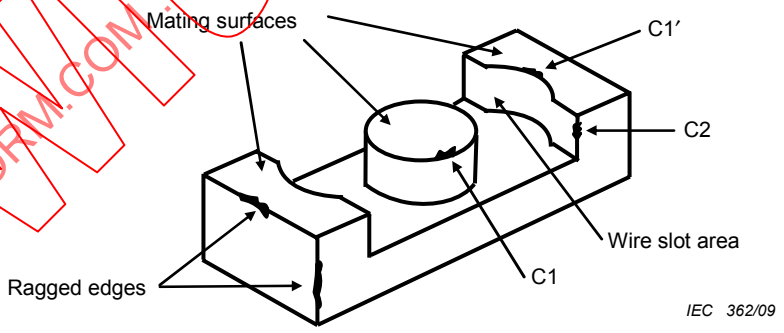

Figure 3 – Chip location for low profile ER-core

Areas of the chips located on the mating surfaces (C1 and C1' irregularities in Figures 1, 2 and 3) shall not exceed the following limits:

– the cumulative area of the chips shall be less than 4 % of the relevant mating surface. The mating surface of each outer leg and centre post is considered separately; the allowable areas are rounded to the figures in Table 4 (Area and length reference for visual inspection) and the minimum allowable area is taken as 0,5 mm^2 to be distinguishable to the naked eye;

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– the total area of all chips on all mating surfaces shall not exceed the value given for "overall chipping on the mating surface" in Tables 1, 2 or 3;

– the total length of the ragged edges shall be less than 25 % of the perimeter of the relevant mating surface.

3.1.2 Chips and ragged edges on other surfaces

– the allowable chipping areas are doubled as compared to the limits for the whole mating surfaces (see Table 1 for planar EL-corers, Table 2 for low profile E-cores, Table 3 for low profile ER-cores);

– the total length of the ragged edges shall be less than 25 % of the perimeter of the smaller adjoining surface;

– chips and ragged edges are not acceptable on the ridge of the clamping recess area;

– chips and ragged edges are not acceptable on the inner edges of wire slot area. (C2 irregularity in Figures 2 and 3)

The core sizes given in Tables 1, 2 and 3 correspond to the cores defined in IEC 62317-9, and area and length reference for visual inspection are given in Table 4.

Table 1 – Allowable areas of chips in mm^2 for planar EL-core

Core size	Chipping on mating surface of one outer leg	Chipping on mating surface of centre post	Overall chipping on mating surface	Other surfaces
EL 11 × 2,0	0,5	0,5	1,5	3,0
EL 11 × 3,0	0,5	0,5	1,5	3,0
EL 13 × 2,2	0,5	1,0	2,0	4,0
EL 13 × 3,2	0,5	1,0	2,0	4,0
EL 15,5 × 2,9	0,5	1,0	2,0	4,0
EL 15,5 × 4,4	0,5	1,0	2,0	4,0
EL 18 × 3,7	1,0	2,0	4,0	8,0
EL 18 × 5,7	1,0	2,0	4,0	8,0
EL 20 × 3,8	1,0	2,0	4,0	8,0
EL 20 × 5,8	1,0	2,0	4,0	8,0
EL 22 × 4,0	1,5	2,5	5,5	11,0
EL 22 × 6,0	1,5	2,5	5,5	11,0
EL 25 × 4,3	1,5	3,5	6,5	13,0
EL 25 × 6,3	1,5	3,5	6,5	13,0

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Table 2 – Allowable areas of chips in mm^2 for low profile E-core

Core size	Chipping on mating surface of one outer leg	Chipping on mating surface of centre post	Overall chipping on mating surface	Other surfaces
E 14 × 3,5 × 5	0,5	0,5	1,5	3,0
E 18 × 4 × 10	1,0	1,5	3,5	7,0
E 22 × 6 × 16	1,5	3,0	6,0	12,0
E 32 × 6 × 20	2,5	5,0	10,0	20,0
E 38 × 8 × 25	3,5	8,0	15,0	30,0
E 43 × 10 × 28	4,5	9,0	18,0	36,0
E 58 × 11 × 38	6,0	12,5	24,5	49,0
E 64 × 10 × 50	10,0	20,0	40,0	80,0
E 102 × 20 × 38	12,5	20,0	45,0	90,0

Table 3 – Allowable areas of chips in mm^2 for low profile ER-core

Core size	Chipping on mating surface of one outer leg	Chipping on mating surface of centre post	Overall chipping on mating surface	Other surfaces
ER 9,5 × 2,5 × 5	0,5	0,5	1,5	3,0
ER 11 × 2,5 × 6	0,5	0,5	1,5	3,0
ER 13 × 3 × 9	0,5	1,0	2,0	4,0
ER 14,5 × 3 × 7	0,5	1,0	2,0	4,0
ER 18 × 3 × 10	0,5	1,0	2,0	4,0
ER 20 × 6 × 14	1,5	2,0	5,0	10,0
ER 23 × 3,6 × 13	1,0	2,0	4,0	8,0
ER 23 × 5 × 13	1,0	2,0	4,0	8,0
ER 25 × 6 × 15	1,5	3,0	6,0	12,0
ER 30 × 8 × 20	2,5	4,0	9,0	18,0
ER 32 × 5 × 21	2,0	4,0	8,0	16,0
ER 32 × 6 × 25	2,5	5,0	10,0	20,0
ER 35 × 10 × 26	3,5	7,0	14,0	28,0
ER 40 × 10 × 28	4,0	7,0	15,0	30,0

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Table 4 – Area and length reference for visual inspection

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3.2 Cracks

Different cracks are shown in Figures 4, 5 and 6. In principle three different types of cracks can be distinguished.

a) Cracks which are parallel to the magnetic flux path (S1, S2, S5, S5', S5''). These cracks are magnetically not critical. The maximum length of a single crack is 33 % (1/3) of the dimension of the relevant surface which is parallel to the crack. In the case of multiple cracks the maximum cumulative length doubles.

b) Cracks which are perpendicular to the magnetic flux path (S3, S3', S3'', S4, S4'). These cracks are magnetically critical. They may reduce the relative cross section of the magnetic flux or add an additional air gap into the magnetic circuit. The maximum total length of cracks is 20 % (1/5) of the dimension of the relevant surface which is parallel to the crack.

c) Cracks which go from one edge to another edge (S6). These cracks may cause chipping during the operation in the circuit. The loose particles may cause malfunctions in the circuit. Therefore this type of crack is not acceptable in any case.

The limits for cracks are given in Tables 5, 6 and 7.

3.3 Flash

There shall be no flash extending from the core into the wire slot.

3.4 Pull-out

The pull-outs are applicable only for the inner surface where the PCB is seated (as shown in Figures 4, 5 and 6).

For planar EL-cores, low profile E-cores and low profile ER-cores, the cumulative area of pull-outs of the core shall be less than 20 % of the total respective surface area.

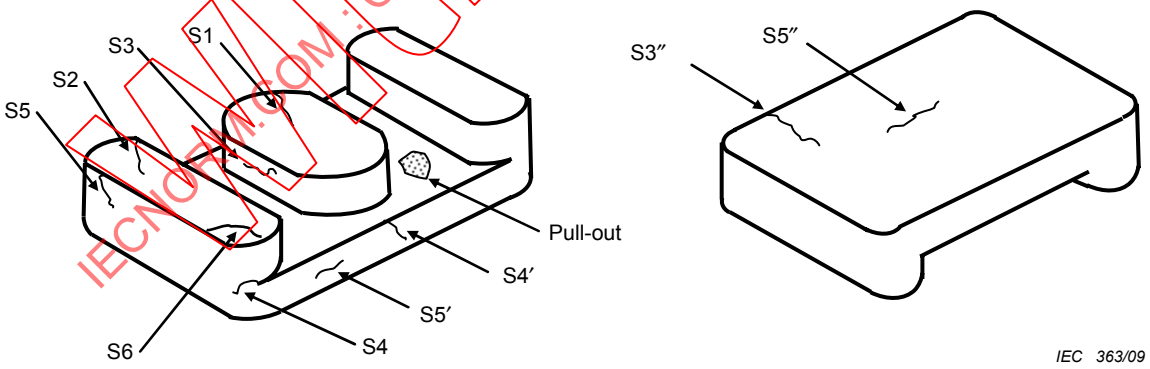

Figure 4 – Cracks and pull-out location for planar EL-core

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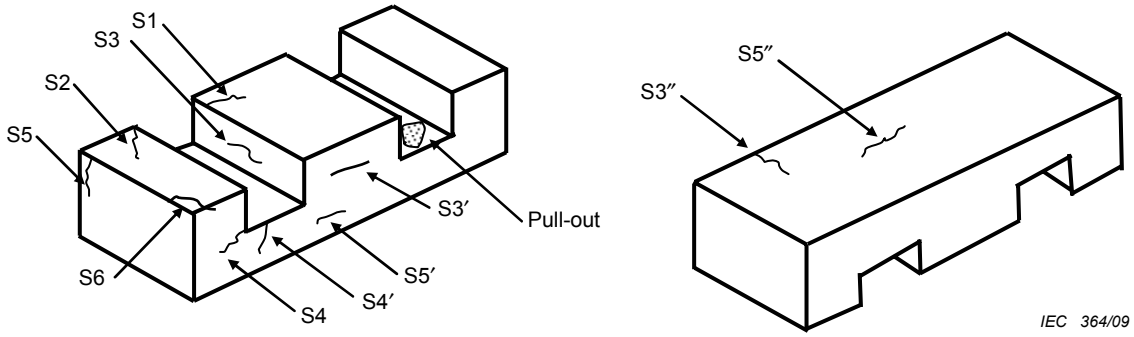

Figure 5 – Cracks and pull-out location for low profile E-core

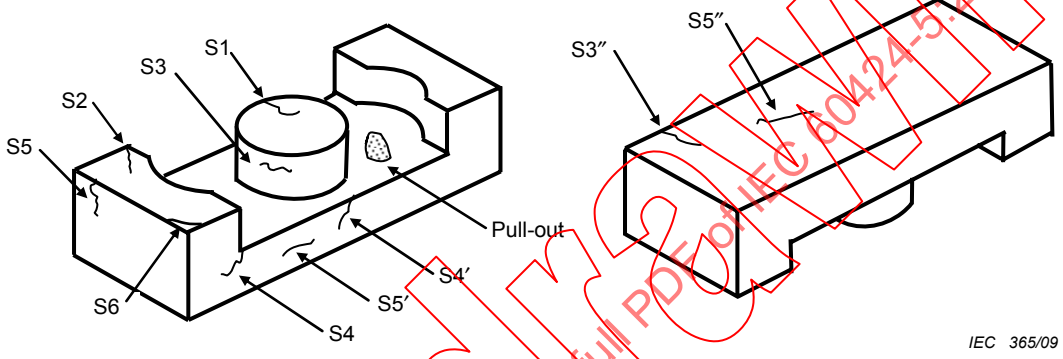

Figure 6 – Cracks and pull-out location for low profile ER-core

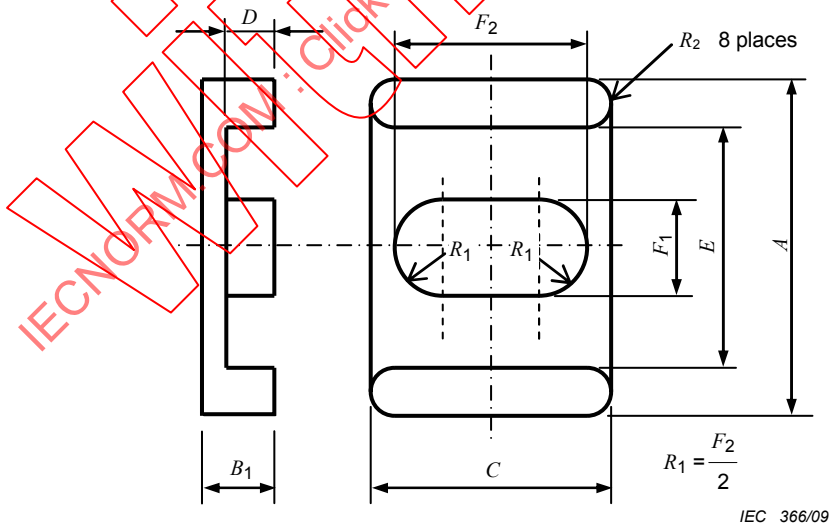

Figure 7 – Reference dimensions for EL-core

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Table 5 – Limits of cracks for planar EL-core

Type[1]	Reference dimension[2]	Limits for single crack	Limits for multiple cracks
S1	F_1	33 % (1/3) of reference dim.	66 % (2/3) of reference dim.
S2	$(A\text{-}E)/2$	33 % (1/3) of reference dim.	66 % (2/3) of reference dim.
S3	F_2	20 % (1/5) of reference dim.	20 % (1/5) of reference dim.
S3'	F_1	20 % (1/5) of reference dim.	20 % (1/5) of reference dim.
S3''	C	20 % (1/5) of reference dim.	20 % (1/5) of reference dim.
S4	$B_1 - D$	20 % (1/5) of reference dim.	20 % (1/5) of reference dim.
S4'	$B_1 - D$	20 % (1/5) of reference dim.	20 % (1/5) of reference dim.
S5	B_1	33 % (1/3) of reference dim.	66 % (2/3) of reference dim.
S5'	A	33 % (1/3) of reference dim.	66 % (2/3) of reference dim.
S5"	A	33 % (1/3) of reference dim.	66 % (2/3) of reference dim.
S6	Multiple edges	No cracks allowed	

[1] See Figure 4.

[2] See Figure 7.

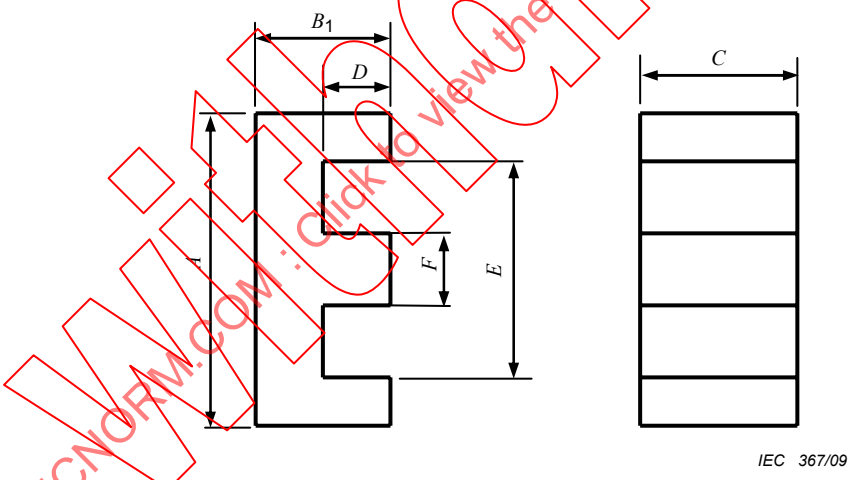

Figure 8 – Reference dimensions for E-core

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