

INTERNATIONAL STANDARD

IEC
60748-23-2

QC 165000-2

First edition
2002-05

Semiconductor devices – Integrated circuits –

Part 23-2:

Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests

*Dispositifs à semiconducteurs –
Circuits intégrés –*

Partie 23-2:

*Circuits intégrés hybrides et structures par films –
Certification de la ligne de fabrication –
Contrôle visuel interne et essais spéciaux*



Reference number
IEC 60748-23-2:2002(E)

Publication numbering

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PRICE CODE

XD

For price, see current catalogue

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –**Part 23-2: Hybrid integrated circuits and film structures –
Manufacturing line certification –
Internal visual inspection and special tests**

FOREWORD

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International Standard IEC 60748-23-2 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the European standard EN 165000-2 and the following documents:

FDIS	Report on voting
47A/639/FDIS	47A/650/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

IEC 60748-23-2 should be read in conjunction with Parts 23-1, 23-3 and 23-4.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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INTRODUCTION

This set of specifications prescribes a set of procedures to be used by users and manufacturers for the production and delivery of high-quality, special requirement hybrid integrated circuits and film structures with a specified level of quality and reliability.

This set of specifications prescribes reference criteria for the establishment, control, maintenance and development of a certified manufacturing line and represents a manufacturing line certification methodology.

The targeted level of quality and reliability is to be achieved by using best design and manufacturing practices. Examples of quality and reliability best practices for elimination of potential failure mechanisms and achievement of a targeted quality and reliability level include: material characterization for derivation of process design rules, in-process control, continuous improvement, etc.

Assessment (estimation) of the targeted quality and reliability level may be accomplished by:

- a) using data obtained from the material characterization, design and process control and improvement activities; or
- b) through the use of product assessment level schedule (PALS) tests.

Part 23-1 of this set of specifications provides general information.

Part 23-3 of this set of specifications provides a framework for use as an assessment/audit tool to assist the suppliers, customers or an independent organization to carry out an assessment of a certified manufacturing line of a hybrid manufacturing company.

Part 23-4 of this set of specifications provides a blank detail specification, which provides guidance to 'users' of hybrids for procurement purposes.

Part 23-5 of this set of specifications provides a means of quality assessment on the basis of qualification approval.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-2: Hybrid integrated circuits and film structures – Manufacturing line certification – Internal visual inspection and special tests

1 Scope

This part of IEC 60748 applies to high quality approval systems for hybrid integrated circuits and film structures.

The purpose of the tests is to perform visual inspections on the internal materials, construction and workmanship of hybrid, multichip and multichip module microcircuits and passive elements used for microelectronic applications including r.f./microwave.

These tests are for both Class H and Class K quality levels, SAW and film hybrid/multichip/multichip module microcircuits using substrates such as ceramic and silicon. Class K is applicable to all microcircuits released to product assessment level schedule 11 (e.g. for space applications – see IEC 60748-23-1). Class H is applicable to all other microcircuits released to this standard. The following types of microcircuits may be inspected:

- a) passive thin and thick film networks;
- b) active thin and thick film circuits;
- c) multiple circuits, including combinations, stacking or other interconnections of 1 a) and 1 b).

Where the deposited film has geometric features larger than 25 μm , the inspection criteria defined in clause 5 apply. In cases where deposited features are smaller than this (e.g. deposited integrated circuits) the inspection requirements of IEC 60747 shall be applied.

These tests will normally be used on microelectronic devices prior to capping or encapsulation to detect and eliminate devices with internal non-conformances that could lead to device failure in normal application. They may also be employed on a sampling basis to determine the effectiveness of the manufacturers' quality control and handling procedures.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050 (all parts), *International Electrotechnical Vocabulary*

IEC 60747-1:1983, *Semiconductor devices – Discrete devices – Part 1: General*¹

Amendment 3 (1996)

IEC 60748-1, *Semiconductor devices – Integrated circuits – Part 1: General*¹

IEC 60748-23-1:2002, *Semiconductor devices – Integrated circuits – Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification*

¹ Together with any other part of IEC 60747 or IEC 60748 relevant to the specific hybrid application, including terminology.

IEC 60748-23-3:2002, *Semiconductor devices – Integrated circuits – Part 23-3: Hybrid integrated circuits and film structures – Manufacturing line certification – Manufacturers' self-audit checklist and report*

IEC 60748-23-4:2002, *Semiconductor devices – Integrated circuits – Part 23-4: Hybrid integrated circuits and film structures – Manufacturing line certification – Blank detail specification*

IEC 61191-2:1998, *Printed board assemblies – Part 2: Sectional specification – Requirements for surface mount soldered assemblies*

IEC 61340-5-1:1998, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

EN 100012:1995, *Basic Specification: X-ray inspection of electronic components*

3 Definitions

For the purpose of this part of IEC 60748, the definitions given in IEC 60050, IEC 60747, IEC 60748-1 and IEC 60748-23-1, as well as the following definitions, shall apply.

3.1

active circuit area

includes all areas of functional circuit elements, operating metallization or connected combinations thereof excluding beam leads; in the case of resistors, includes all resistor material that forms a continuous path between two metallized areas (usually bonding pads)

3.2

add-on substrate

supporting structural material into and/or upon which glassivation, metallization and circuit elements are placed and the entire assembly is in turn placed on and attached to the main substrate

3.3

attachment medium

material used to effect the attachment of an element to an underlying surface (e.g. adhesive, solder, alloy)

3.4

blister, metallization

hollow bump that can be flattened

3.5

block resistor

solid, rectangularly shaped resistor, which, for purposes of trimming, is designed to be much wider than would be dictated by power density requirements

3.6

bonding pad

metallized area (usually located along the periphery of the element) at which an electrical connection is to be made by the user of the element

3.7

bonding site

metallized area on a substrate or element intended for a wire or ribbon interconnecting bond

3.8

bridging

complete connection between circuit features not intended to be connected

3.9

cold solder joint

solder joint whose appearance is "grainy" or "dull"

NOTE Where a "grainy" or "dull" appearance is characteristic of certain solder materials (e.g. AuSn, etc.), this criterion should not cause these materials to be rejected.

3.10

compound bond

one bond on top of another

3.11

conductive attach

process and materials used for the attachment that also provides an electrical contact or thermal dissipation path (e.g. solder, eutectic, solder-impregnated epoxy)

3.12

conductive substrate

substrate that can conduct electricity

NOTE Copper or doped silicon, for example, are conductive substrates while alumina and quartz are non-conductive (insulating) substrates.

3.13

contact window

opening (usually square) through the oxide (or insulating) layer for the purpose of allowing contact by deposited material to the substrate

3.14

controlled environment

environment that is in accordance with the requirements of the appropriate product assessment level schedules (PALS) in Annex A of IEC 60748-23-1 and with respect to cleanroom class and (where specified) temperature and relative humidity

3.15

corrosion

gradual wearing away of metal, usually by chemical action, with the subsequent production of a corrosion product

3.16

coupling (air) bridge

raised layer of metallization used for interconnection that is isolated from the surface of the element by an air gap or other insulating material

3.17

crazing

presence of numerous, minute, interconnected surface cracks

3.18

crossover

transverse crossing of metallization paths, without mutual electrical contact, achieved by the deposition of an insulating layer between the metallization paths in the area of crossing

3.19

detritus

fragments of original or trim-modified resistor or conductor material

3.20

dielectric

insulating material that does not conduct electricity but may be able to sustain an electric field

NOTE It can be used in crossovers, as a passivation or a glassivation, or in capacitors.

3.21**dielectric attach**

process and materials used for attachment that does not provide electrical contact or thermal dissipation

3.22**edge metallization**

metallization that electrically connects the metallization from the top surface to the opposite side of the substrate

3.23**element**

constituent of a hybrid microcircuit; such as integral deposited or screened passive elements, substrates, discrete or integrated electronic parts including dies, chips and other microcomponents; also mechanical piece parts such as cases and covers; all contributing to the operation of a hybrid microcircuit

3.24**electrically common**

satisfied when two or more conductive surfaces or interconnects are of equal d.c. voltage/signal potential

3.25**end terminated or wrap-around elements**

those elements which have electrical connections on the ends (sides) and/or base of their bodies

3.26**foreign material**

any material that is foreign to the element or microcircuit or any non-foreign material that is displaced from its original or intended position in the element or microcircuit package

NOTE It is considered attached when it cannot be removed by a nominal gas blow (approximately 138 kN/m²) (20 psig) or by an approved cleaning process. Conductive foreign material is any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles are considered to be embedded in glassivation when there is evidence of colour fringing around the periphery of the particle.

3.27**glassivation**

top layer(s) of transparent insulating material that covers the active circuit area, including metallization, but not bonding pads

NOTE Crazing is the presence of numerous minute cracks in the glassivation. Cracks are fissures in the glassivation layer resulting from stress release or poor adhesion. The cracks can form loops over metallized areas.

3.28**insulating layer**

dielectric layer used to isolate single or multilevel conductive and resistive material or to protect top level conductive resistive material

3.29**intermetallics (purple plague)**

one of several gold-aluminium compounds formed when bonding gold to aluminium and activated by re-exposure to moisture and high temperature (> 340 °C)

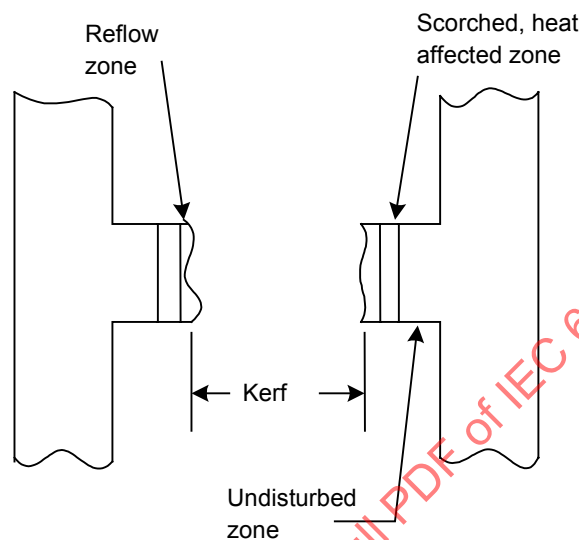
NOTE Purple plague is purplish in colour and is very brittle, potentially leading to time-based failure of the bonds. Its growth is highly enhanced by the presence of silicon to form ternary compounds.

3.30

kerf

clear area in a trimmed resistor resulting from the removal of resistor material by the trimming operation

NOTE In laser trimming, the kerf is bounded by the reflow zone (which is characterized by adherent, melted resistor material), the scorched heat-affected zone (which is characterized by discoloration of the resistor film without alteration of its physical form), and the undisturbed zone (see figure 1).



IEC 961/02

Figure 1 – Class H – Metallization scratch criteria

3.31

mar

non-tearing surface disturbance such as an indentation or a buff mark

3.32

mechanical strength tests

tests, such as mechanical shock or constant acceleration, which demonstrate adequate attachment processes and materials

3.33

metallization, multilevel (conductors)

alternate layers of metallization, or other material used for interconnection, that are isolated from each other by a grown or deposited insulating material. The term "overlying metallization" refers to any metallization layer on top of the insulating material

3.34

metallization, multilayered (conductors)

two or more layers of metallization, or other material used for interconnection, that are not isolated from each other by a grown or deposited insulating material

NOTE The term "underlying metallization" refers to any metallization layer below the top layer of metallization.

3.35

metallization, operating (conductors)

all metallization (gold, aluminium, or other material) used for interconnection

NOTE Bonding pads are considered to be operating metallization. Alignment markers, test patterns, and identification markings are not considered to be operating metallization.

3.36**narrowest resistor width**

narrowest portion of a given resistor prior to trimming; however, the narrowest resistor width for a block resistor may be specified in the approved manufacturer's design documentation

3.37**neck-down**

tapering of a resistor line at a metallization interface

NOTE Resistor material taper is typically equal on both sides of the line and is less abrupt than a void.

3.38**nicking (partial cut)**

incomplete or inadvertent trimming of a resistor adjacent to the one being trimmed or of the next ladder rung of the same resistor

3.39**nodule, metallization**

solid bump that cannot be flattened

3.40**non-monometallic compound bond**

two lead bonds, made of dissimilar metals, which are stacked one on top of the other, i.e. the interface between the two lead bonds is made up of dissimilar metals such as an aluminium lead bond stacked on top of a gold lead bond or vice-versa

3.41**non-planar element**

element that is essentially three-dimensional

3.42**operating metallization (conductors)**

metal or any other material used for interconnections except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads and identification markings

3.43**original design separation**

separation dimension or distance that is intended by design

3.44**original width**

width dimension or distance that is intended by design (e.g. original metal width, original diffusion width, original beam width, etc.)

3.45**oxide non-conformance**

irregularly shaped non-conformance in the oxide characterized by two or three coloured fringes at its edges

3.46**passivation**

silicon oxide, nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of the final metal layers

3.47**passivation step**

change in thickness of the passivation layer by design

3.48

passive elements

planar resistors, capacitors, inductors, and patterned substrates (both single-layer and multilayer), and non-planar chip capacitors, chip resistors, chip inductors, and transformers

3.49

patterned substrate

substrate on which conductors, and components such as resistors or capacitors, are formed using thick or thin film manufacturing techniques

3.50

pit

depression produced in a substrate surface typically by non-uniform deposition of metallization or by non-uniform processing such as excessively powered laser trim pulses

3.51

planar element

element that is essentially two-dimensional with all points in a common plane

3.52

protrusion

jutting-out of a circuit feature

NOTE Protrusion is typically caused by a photolithographic or screening non-conformance.

3.53

resistor ladder

resistor structure resembling a ladder in appearance that can be trimmed in incremental steps

NOTE A coarse ladder structure is one in which trimming of a rung results in a large incremental resistance change (one that can cause an out-of-tolerance condition to occur). A fine ladder structure is one in which trimming of a rung results in a small incremental resistance change (one that cannot cause an out-of-tolerance condition to occur).

3.54

resistor ladder rung

portion of a resistor ladder structure intended to be laser trimmed to result in an incremental change in resistance

3.55

resistor loop

resistor structure resembling a loop in appearance that can be trimmed

NOTE A coarse loop structure is one in which trimming results in a large resistance change (one that can cause an out-of-tolerance condition to occur). A fine loop structure is one in which trimming results in a small resistance change (one that cannot cause an out-of-tolerance condition to occur).

3.56

resistor material, self passivating

material on which a conformal insulating layer can be thermally grown (such as tantalum nitride on which tantalum pentoxide is grown)

3.57

scorching

discoloration of laser trimmed thin film resistor material without alteration of its physical form

3.58

scratch, metallization

any tearing non-conformance, including probe marks on the surface of the metallization

NOTE A mar on the metallization surface is not considered to be a scratch.

3.59**scratch, resistor**

any tearing non-conformance in the resistor film

NOTE A mar on the resistor surface is not considered to be a scratch.

3.60**sidebar**

portion of a resistor ladder structure to which rungs are attached

NOTE Sidebars are not intended to be laser trimmed.

3.61**string**

filamentary run-out or whisker of polymer material

3.62**surface acoustic wave (SAW) element**

planar element fabricated typically using thin film manufacturing techniques on various substrate materials

NOTE Size varies as a function of frequency and design features include interdigitated fingers.

3.63**thick film**

conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form

3.64**thin film**

conductive, resistive or dielectric material, usually less than 50,000 Å in thickness, that is deposited onto a substrate by vacuum evaporation, sputtering, or other means

3.65**tine**

individual lead of an edge connector lead frame that makes contact with an edge of a substrate

3.66**tuning**

adjustment of signals from an r.f./microwave circuit by altering lines or pads; adding, deleting or manipulating wires/ribbons; and/or changing resistance, inductance or capacitance values to meet specific electrical specifications

3.67**through-hole metallization**

metallization that electrically connects the metallization on the top surface of the substrate to the opposite surface of the substrate

3.68**underlying material**

any layer of material below the top-layer metallization. This includes metallization, resistor, passivation or insulating layers, or the substrate itself

3.69**unused component or unused deposited element**

one not connected to a circuit or one connected to a circuit path at one, and only one, point

NOTE A connection may be made by design or by visual anomaly.

3.70

via

opening in the insulating material in which a perpendicular conductive electrical connection from one metallization layer to another in a multilayer substrate is made

3.71

visible line

defined as 12,5 µm at 60× magnification

3.72

vitrification

conversion into glass or a glassy substance by heat and fusion

3.73

void

any region in the material (interconnects, bonding sites, etc.) where underlying material is visible that is not caused by a scratch

3.74

void, metallization

any missing metallization where the underlying material is visible (exposed)

NOTE Voids typically are caused by photolithographic, screen, or mask related non-conformances, not by scratches.

3.75

void, resistor

any missing resistor material where the underlying material is visible (exposed)

NOTE Voids typically are caused by photolithographic, screen, or mask related non-conformances, not by scratches.

3.76

wrap-around conductor

conductor which extends around the edge of the substrate by design

4 Apparatus

The apparatus for this test shall include optical equipment capable of the specified magnification(s) and visual standards/aids (gauges, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate means shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

5 Procedure

5.1 General

The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the specified test condition. If a specified visual inspection requirement is in conflict with element design, topology or construction, it shall be documented and specifically approved by the acquiring activity. Inspection for all of the visual non-conformance criteria in this test shall be performed on all elements to which they are applicable. Where a criterion is intended for a specific element type, process, or technology, it has been so indicated.

5.2 Sequence of inspection

The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Where obscuring mounting techniques (e.g. beam lead devices, stacked substrates, components mounting in holes or cutaways, flip chip devices, packaged devices, etc.) are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to mounting the element or substrate. The inspection criteria of clause 7 may be performed at the option of the manufacturer prior to element attachment.

5.3 Inspection control

In all cases, examination prior to final pre-seal inspection shall be performed under the same conditions that are required at the final pre-seal inspection station. If a microcircuit is electrostatic discharge (ESD) sensitive, then appropriate precautions shall be taken in accordance with IEC 61340-5-1. Devices examined according to the criteria of clauses 5 to 17 shall be inspected and prepared for sealing under the environmental conditions specified in the appropriate product assessment level schedules in annex A of IEC 60748-23-1, under "Process and packaging requirements".

5.4 Re-inspection

When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the acquisition document. Where sample inspection is used rather than 100 % re-inspection, the sampling plans defined in IEC 60748-23-1 shall apply.

5.5 Exclusions

Where conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.

5.6 Magnification

The magnification ranges to be used for inspection are specified at the start of each clause and are defined at the start of each major criteria grouping. "High magnification" inspection shall be performed perpendicular to the element with illumination normal to the element surface. Other angles at which the inspection can be performed, and at which the element can be illuminated, may be used at the option of the manufacturer if the visual presentation is the same as used in the originally specified conditions. "Low magnification" inspection shall be performed with either a monocular, binocular, or stereo microscope with the element under suitable illumination.

5.7 Format and conventions

For ease of understanding and comparison, visual criteria are presented side-by-side in a columnar format. Class H criteria are presented in the left column and class K criteria are presented in the right column. When there are differences, the applicable parts of the class H criterion are underlined, for ease of comparison and clarity, and the differences only are shown in the class K column. When there are similarities, the phrase "same as class H" is used with no underlining of the class H criterion. If a requirement is not applicable to either product class, this is indicated by "N/A". A note in the class H column is applicable to class K, unless otherwise specified in the class K column. A note in the class K column is applicable to class K only.

Two kinds of notes are used herein, regular notes (NOTE) and precautionary notes (PRECAUTIONARY NOTE). A regular note is an integral part of a criterion. A precautionary note is not an integral part of the criterion but serves to alert the user to a requirement of IEC 60748-23, Parts 1 to 5.

The phrases "except by design," "intended by design," "by design," or "unless otherwise specified by design" require that the element drawing be referenced to determine intent. For inspections performed at 100×, the criterion of "2,5 µm of passivation, separation, or metal" is satisfied by a "line of passivation, separation or metal." In the figures, cross-hatched areas represent metallization, blank areas represent resistor material and shaded areas represent exposed underlying material. The letters "x", "y", or "z" represent the dimension of interest and the letter "d" represents the original dimension. Most figures show the reject condition only.

5.8 Interpretations

References herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates that a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used to confirm that a reject condition does not exist, they shall be approved by the acquiring activity.

6 Thin film element inspection

Inspection for visual non-conformances described in this clause shall be conducted on each planar thin film passive element. The "high magnification" inspection shall be within the range of 100× to 200× for both class H and class K. The "low magnification" inspection shall be within the range of 30× to 60× for both class H and class K. Patterned substrates that have geometries of 50 µm or greater shall be inspected at 10× to 60× magnification.

6.1 Operating metallization non-conformances – "high magnification"

NOTE The metallization non-conformance criteria contained in this subclause apply to operating metallization only.

No element shall be acceptable that exhibits:

6.1.1 Metallization scratches

Class H

a) A scratch or probe mark in the metallization, excluding bonding pads, that both exposes underlying material anywhere along its length and leaves less than 50 % of the original metallization width undisturbed (see figure 2).

Class K

a) Same as Class H.

NOTE 1 This criterion does not apply to capacitors (see 6.1.1 e)).

NOTE 2 Underlying material does not have to be exposed along the full length of the scratch.

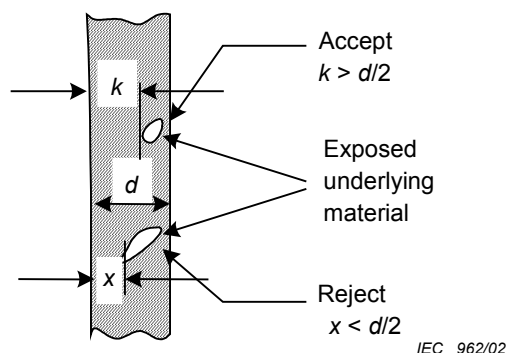


Figure 2 – Class H – Metallization scratch criterion

Class H

b) Scratch in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, and leaves less than 50 % of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 3).

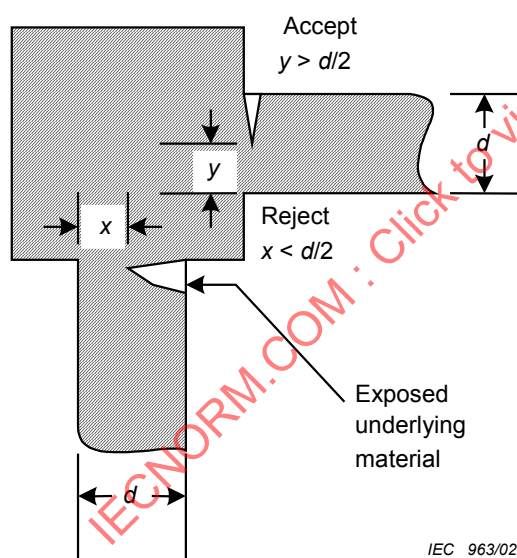


Figure 3 – Class H – Metallization width reduction at bonding pad criterion

Class K

b) Less than 75 % (see figure 4).

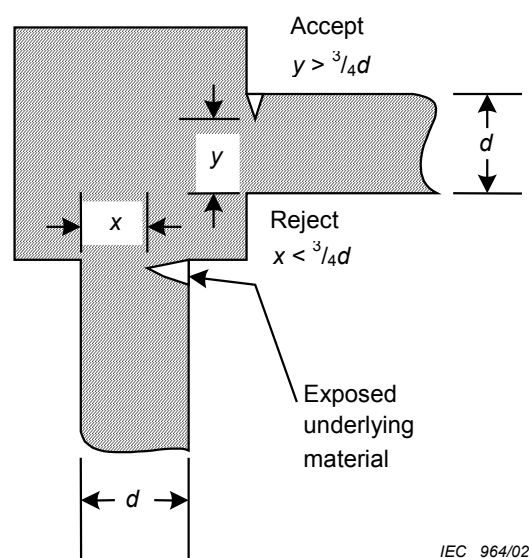


Figure 4 – Class K – Metallization width pad reduction at bonding pad criterion

c) Scratch that completely crosses metallization and damages the metallization on either side.

c) Not applicable.

d) Scratches or probe marks in the bonding pad area that expose underlying material over more than 25 % of the original unglassivated metallization area.

d) Same as Class H.

e) For capacitors only, a scratch in the metallization, other than in the bonding pad area, that exposes the dielectric material.

e) Same as Class H.

6.1.2 Metallization voids

Class H

Class K

a) Void(s) in the metallization, excluding bonding pads, that leave less than 50 % of the original metallization width undisturbed (see figure 5).

a) Same as Class H.

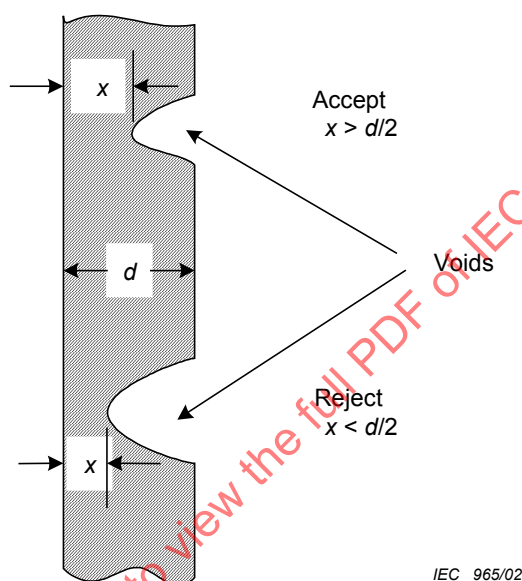


Figure 5 – Class H – Metallization void criterion

b) Void(s) in the bonding pad area that reduce the metallization path width, where it enters the bonding pad, to less than 50 % of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately.

b) Less than 75 %.

NOTE Figures 3 and 4 illustrate metallization width reduction at bonding pad criteria for scratches. Void criteria are similar.

c) Scratch that completely crosses void(s) in the bonding pad area that expose underlying material over more than 25 % of the original unglassivated metallization area.

c) Same as Class H.

NOTE For r.f./microwave elements on non-conductive substrates, a void created in the bonding pad area as a result of wire bond removal for performance optimization or tuning, is not rejectable provided that the void remains entirely visible.

d) For capacitors only, void(s) in metallization, other than in the bonding pad area, that reduce the metallization to an extent greater than an area equivalent to 25 % of the capacitor metallization.

e) For interdigitated capacitors only, void(s) in the metallization that leaves less than 50 % of the original metallization width undisturbed (see figure 6).

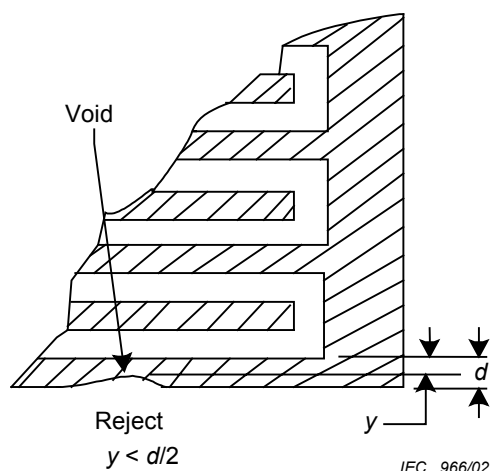


Figure 6 – Class H – Interdigitated capacitor metallization void criterion

d) Same as Class H.

e) Less than 75 % (see figure 7).

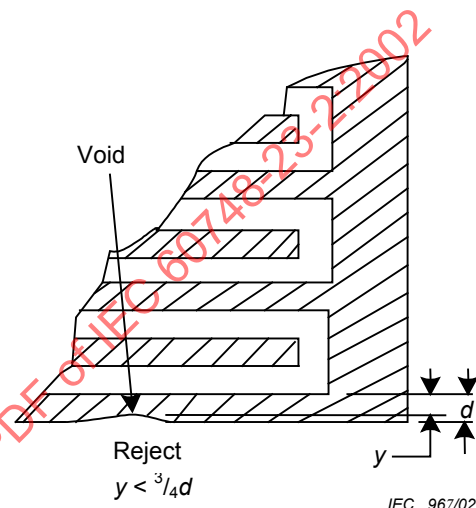


Figure 7 – Class K – Interdigitated capacitor metallization void criterion

6.1.3 Metallization corrosion

Class H

a) Any metallization corrosion

Class K

a) Same as Class H.

Metallization having any localized discoloured area shall be closely examined and rejected unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.

6.1.4 Metallization adherence

a) Any metallization lifting, peeling, or blistering.

a) Same as Class H.

NOTE 1 Nodules are acceptable. In order to determine if a bump in the metallization is a blister or a nodule, attempt to flatten the bump with a non-metallic instrument. If the bump flattens, then it is a blister.

NOTE 2 These criteria are not applicable to undercutting or separation induced anomalies (for example, metallization lifting due to scribe and break or diamond sawing) since these are not indicative of adhesion problems.

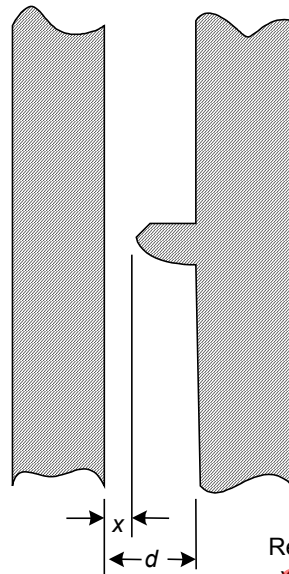
6.1.5 Metallization protrusion

Class H

a) Protrusion of metallization that reduces the original separation between adjacent operating metallization by more than 50 % (see figure 8).

Class K

a) Same as Class H.



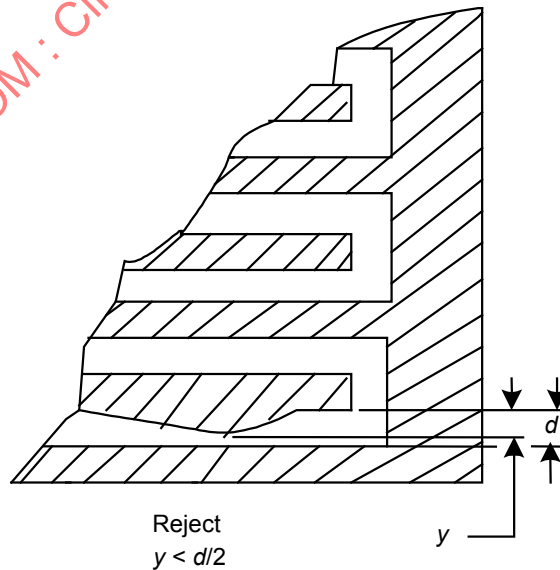
Reject
 $x < d/2$

IEC 968/02

Figure 8 – Class H – Operating metallization protrusion criterion

b) For interdigitated capacitors only, protrusion of metallization that reduces the original separation by more than 50 % (see figure 9).

b) Same as Class H.



Reject
 $y < d/2$

IEC 969/02

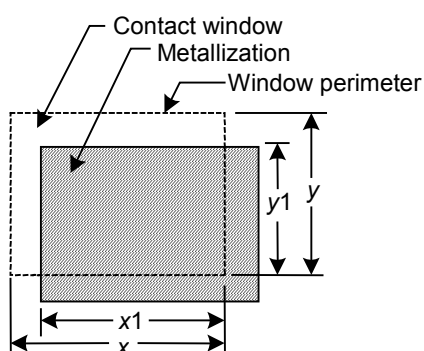
Figure 9 – Class H – Interdigitated capacitor metallization protrusion criterion

6.1.6 Metallization alignment

Class H

- a) A contact window that has less than 50 % of its area covered by metallization.
- b) A contact window that has less than a continuous 40 % of its perimeter covered by metallization (see figure 10).

NOTE When, by design, metallization is completely contained in a contact window, or does not cover the entire contact perimeter, 6.1.6 a), area coverage, or 6.1.6 b), perimeter coverage, can be deleted as applicable provided that the design criteria are satisfied.



Reject

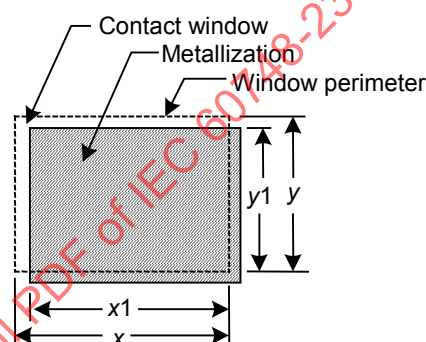
$$x1 + y1 < 0,4(2x + 2y)$$

IEC 970/02

Figure 10 – Class H – Metallization alignment criterion

Class K

- a) Less than 75 %.
- b) 50 % of its perimeter (see figure 11).



Reject

$$x1 + y1 < 0,5(2x + 2y)$$

IEC 971/02

Figure 11 – Class K – Metallization alignment criterion

- c) A metallization path not intended to cover a contact window that is separated from the window by less than 2,5 µm unless by design.

- c) Same as Class H.

6.1.7 Metallization bumps or indentations

- a) For capacitors only, a bump or indentation in the overlaying metallization.

- a) Same as Class H.

6.1.8 Metallized through-hole non-conformances – "high magnification"

No element shall be acceptable that exhibits:

- a) Through-hole metallization that is not perpendicularly continuous or that does not cover at least a continuous 50 % of the inside, circumferential surface area unless by design.

- a) Same as Class H.

6.1.9 Wrap-around connection non-conformances – "high magnification"

No element shall be acceptable that exhibits:

Class H

- a) Unmetallized area in the edges of wrap-around connections greater than 50 % of the largest dimension of the edge metallization (see figure 12).

Class K

- a) Same as Class H.

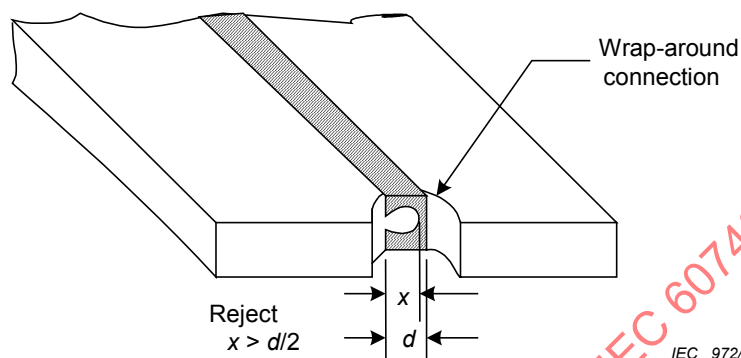


Figure 12 – Class H – Wrap-around connection unmetallized area criterion

6.2 Passivation non-conformances - "high magnification"

No element shall be acceptable that exhibits:

- a) Either multiple lines (colour fringing) or a complete absence of passivation visible at the edge and continuing under the metallization (see figure 13). A passivation non-conformance that exhibits a line of separation from the metallization is acceptable.

- a) Same as Class H.

NOTE 1 These criteria apply to conductive substrate elements only.

NOTE 2 Double or triple lines at the edge of the passivation non-conformance indicate it can have sufficient depth to penetrate down to the bare substrate.

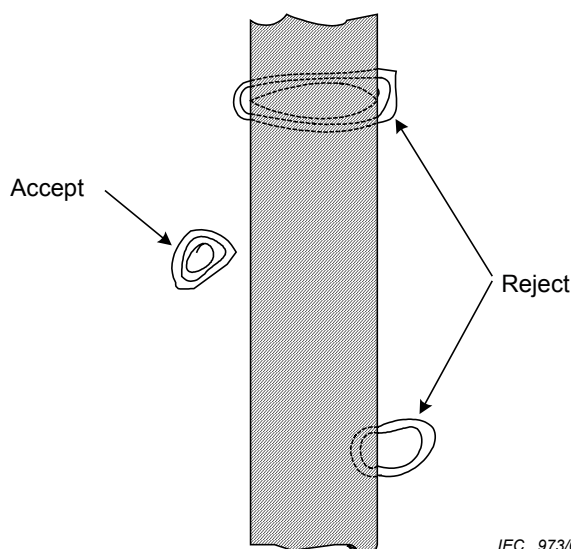


Figure 13 – Class H – Passivation non-conformance criteria

6.3 Glassivation non-conformances - "high magnification"

Class H

Class K

Criteria of 6.1.3 can be excluded when the non-conformances are due to laser trimming. In this case, the non-conformances outside the kerf due to laser trimming shall not be more than one half the remaining resistor width and shall leave a primary resistor path free of glassivation non-conformances, equal to or greater than 50 % of the narrowest resistor width, (see figure 14).

No device shall be acceptable that exhibits:

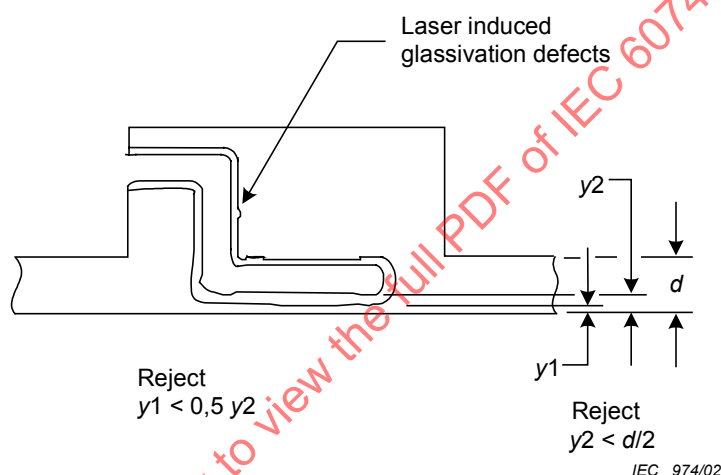


Figure 14 – Class H – Laser trimmed glassivation non-conformance criteria

a) Glass crazing or damage that prohibits the detection of visual criteria contained herein.

a) Same as Class H.

b) Any lifting or peeling of the glassivation.

b) Same as Class H.

NOTE Lifting or peeling of the glassivation is acceptable when it does not extend more than 25 μm from the designed periphery of the glassivation, provided that the only exposure of metallization is of adjacent bonding pads or of metallization leading from those pads.

c) A void in the glassivation that exposes two or more adjacent operating metallization paths, excluding bonding pad cut-outs, unless by design.

c) Same as Class H.

d) Unglassivated non-active circuit areas greater than 125 μm in any dimension, unless by design.

d) Same as Class H.

e) Unglassivated areas at the edge of a bonding pad exposing the conductive substrate.

e) Same as Class H.

Class H

- f) Glassivation covering more than 25 % of a bonding pad area.
- g) Crazing in glassivation over a resistor.
- h) Misalignment of the glassivation that results in incomplete coverage of a resistor, unless by design.
- i) Glassivation scratches or voids that expose any portion of a resistor or fusible link except for polycrystalline silicon links where the glassivation is opened by design.
- j) Scratches in the glassivation that disturb metallization and bridge metallization paths.
- k) Cracks (not crazing) in the glassivation that form a closed loop over adjacent metallization paths.

Class K

- f) Same as Class H.
- g) Same as Class H.
- h) Same as Class H.
- i) Same as Class H.
- j) Same as Class H.
- k) Same as Class H.

6.4 Substrate non-conformances - "high magnification"

No element shall be acceptable that exhibits:

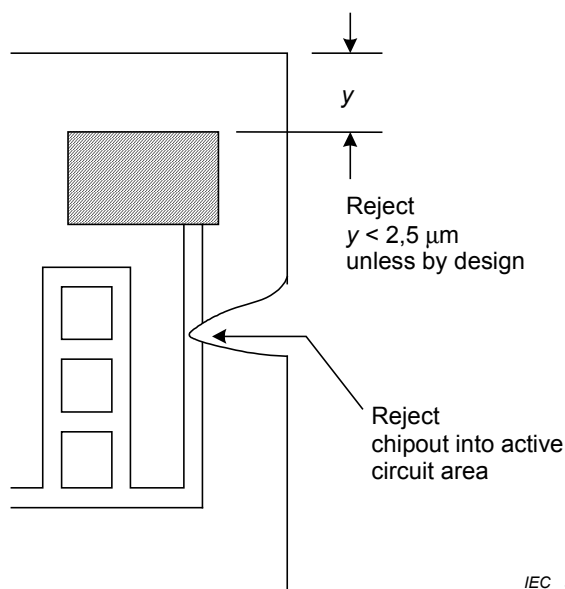
- a) Less than 2,5 µm of separation between the operating metallization and the edge of the element unless by design (see figure 15).

For elements containing wrap-around conductors or for bonding pads of r.f./microwave elements that are coincident with the element edge (as documented on the design drawing) this criterion does not apply. When bond pad metallization is coincident with the element edge, a minimum separation of 25 µm shall exist between the bonding pad metallization at the element edge and any non-common conductive surface.

- b) A chipout that extends into the active circuit area (see figure 15).

- a) Same as Class H.

- b) Same as class H.



IEC 975/02

Figure 15 – Class H – Separation and chipout criteria

Class H

- c) Any crack that exceeds $125\ \mu\text{m}$ in length (see figure 16).

NOTE For fused quartz or crystalline substrates, no cracking is allowed.

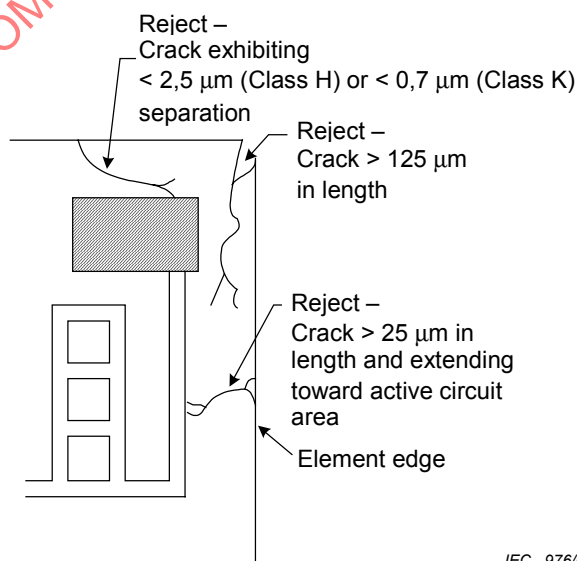
- d) Any crack that does not exhibit $2,5\ \mu\text{m}$ of separation from any active circuit area or operating metallization (see figure 16).
- e) Any crack exceeding $25\ \mu\text{m}$ in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 16).

Class K

- c) Same as Class H.

- d) $0,7\ \mu\text{m}$ (see figure 16).

- e) Same as Class H.



IEC 976/02

Figure 16 – Class H – Crack criteria

Class H

f) N/A.

Class K

f) Semicircular crack or combination of cracks along the element edge whose total length is equal to or greater than 75 % of the narrowest separation between any two bonding pads (see figure 17).

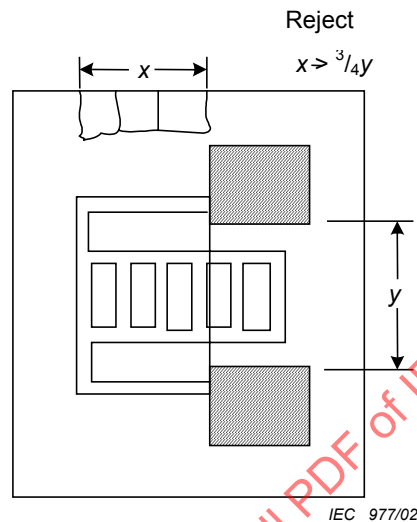


Figure 17 – Class K – Semicircular crack criterion

- | | |
|--|---------------------|
| g) An attached portion of an active circuit area from an adjacent element. | g) Same as Class H. |
| h) Any crack that does not originate at an edge. | h) Same as Class H. |
| i) Holes through the substrate, unless by design. | i) Same as Class H. |

6.5 Foreign material non-conformances - "low magnification"

No element shall be acceptable that exhibits:

- | | |
|---|---------------------|
| a) For mounted elements, unattached, conductive foreign material on the surface of the elements. For unmounted elements, unattached, conductive foreign material on the surface of the element that is large enough to bridge operating metallization paths, active circuitry, or any combination of these. | a) Same as Class H. |
|---|---------------------|

NOTE 1 If an element has an insulating layer (such as glassivation or self-passivation) that covers operating metallization paths, active circuitry, or any combination of these, then the presence of unattached, conductive foreign material, that is large enough to bridge these features, is acceptable since the features are protected by the insulating layer.

Class H

Class K

All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachment shall be accomplished by a light touch with an appropriate mechanical device (e.g. needle, probe, pick, etc.), or by a suitable cleaning process approved by the acquiring activity, or by a blow-off with a nominal gas blow (approximately 150 kN/m²).

NOTE 2 Removal of unattached foreign material may be attempted using the techniques for verification of attachment discussed above.

NOTE 3 Semiconductor particles are considered to be foreign material.

- b) Attached, conductive foreign material that bridges metallization paths, active circuitry, or any combination of these.
- c) Liquid droplets, ink drops, or chemical stains that appear to bridge any unglassivated or unpassivated active circuit areas.
- d) Attached foreign material that covers more than 25 % of a bonding pad area.

b) Same as Class H.

c) Same as Class H.

d) Same as Class H.

6.6 Thin film resistor non-conformances - "high magnification"

No element shall be acceptable that exhibits:

- a) Voids at the terminal that reduce the resistor width to less than 50 % of the original resistor width (see figure 18).

a) Same as Class H.

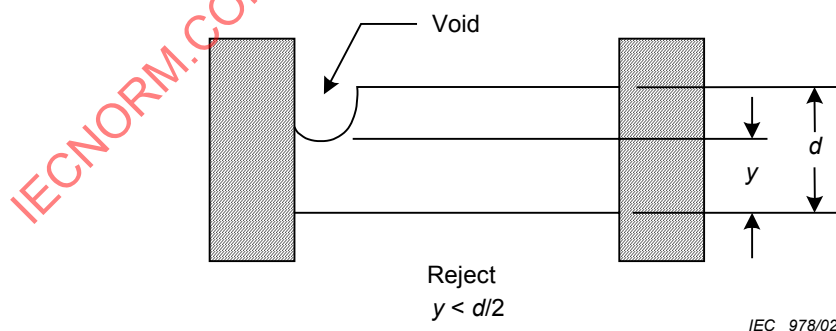


Figure 18 – Class H – Film resistor width reduction at terminal by voids criterion

Class H

- b) Neck-down at the terminal that reduces the resistor width to less than 75 % of the original resistor width (see figure 19).

Class K

- b) Same as Class H.

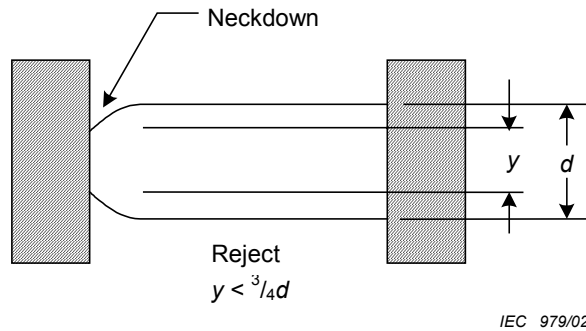


Figure 19 – Class H – Film resistor width reduction at terminal by necking criterion

- c) Any sharp (clearly defined) colour change within 2,5 µm of the terminal.

- c) Same as Class H.

NOTE A sharp colour change close to the terminal usually indicates an abrupt reduction of resistor film thickness. This colour change usually occurs in a straight line parallel to the terminal. A gradual colour change, or a non-uniform or mottled colour anywhere in the resistor, is not cause for rejection.

- d) Any resistor film lifting, peeling or blistering.

- d) Same as Class H.

- e) Reduction of resistor width, resulting from voids, scratches, or a laser trim kerf or a combination of these, that leaves less than 50 % of the narrowest resistor width (see figure 20).

- e) Same as Class H.

PRECAUTIONARY NOTE The maximum allowable current density requirement must not be exceeded.

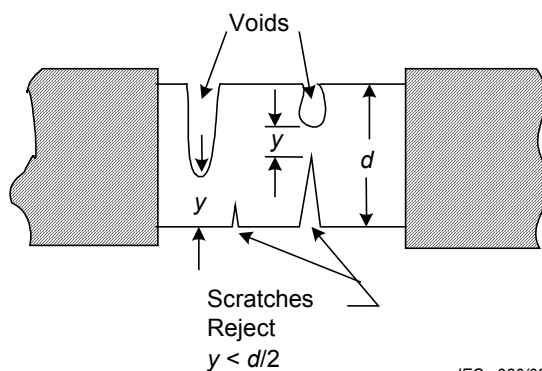


Figure 20 – Class H – Film resistor width reduction by voids and scratches criteria

Class H

- f) Contact overlap between the metalization and the resistor in which the width dimension "y" is less than 50 % of the original resistor width (see figure 21).

Class K

- f) Same as Class H.

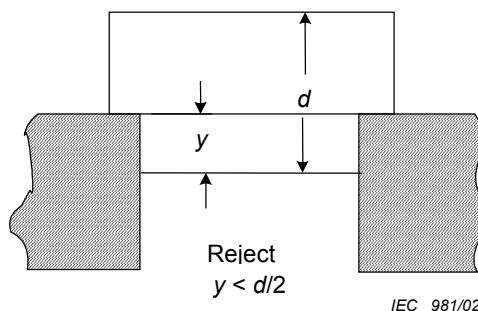


Figure 21 – Class H – Metal/resistor overlap criterion

- g) Contact overlap between the metalization and the resistor in which the length dimension "x" is less than 5 μm (see figure 22).

- g) Same as Class H.

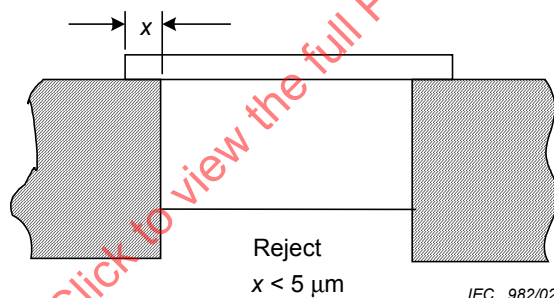


Figure 22 – Class H – Contact overlap criterion

- h) More than a 50 % reduction of the original separation, between any two different resistors, or a resistor and metallization not associated with it (see figure 23).

- h) Same as Class H.

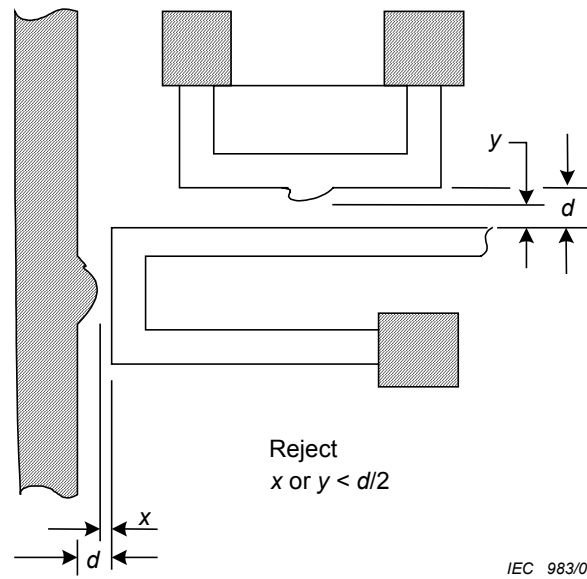


Figure 23 – Class H – Resistor separation criteria

Class H

- i) Any resistor that crosses a substrate irregularity (such as a void or scratch) (see figure 24).

NOTE This criterion is applicable to conductive substrates only.

Class K

- i) Same as Class H.

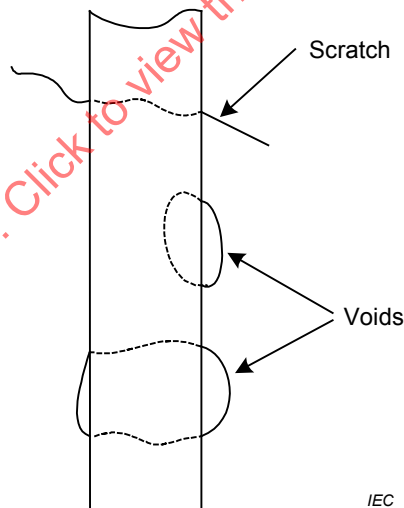


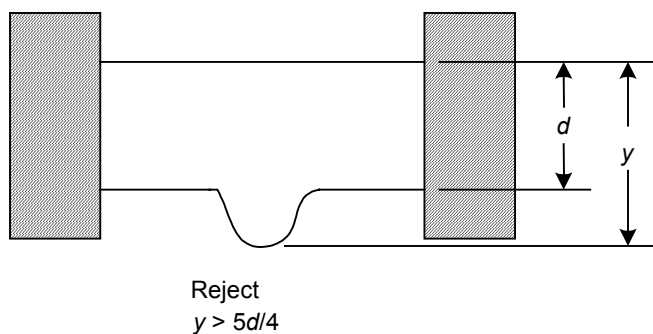
Figure 24 – Class H – Substrate irregularity criterion

Class H

- j) Any increase in resistor width of a block resistor greater than 25 % of the original resistor width (see figure 25).

Class K

- j) Same as Class H.



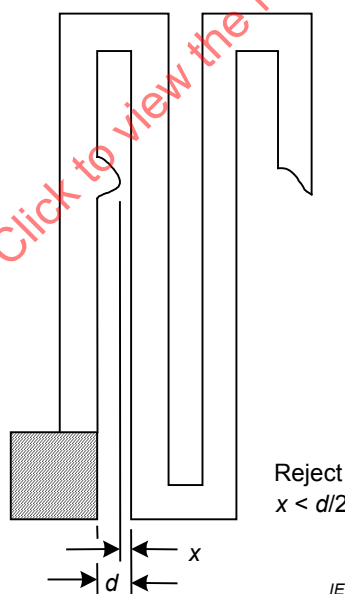
IEC 985/02

Figure 25 – Class H – Resistor width increase criterion

- k) Protruding resistor material within the same resistor structure that reduces the original separation to less than 50 % (see figure 26).

- k) Same as Class H.

NOTE This criterion applies to protrusion of resistor material resulting from a photolithographic non-conformance.



IEC 986/02

Figure 26 – Class H – Protrusion of resistor material criterion

Class H

- l) Bridging within the same resistor pattern where the width of the bridge is less than 50 % of the narrowest line being bridged (see figure 27).

Class K

- l) Same as class H.

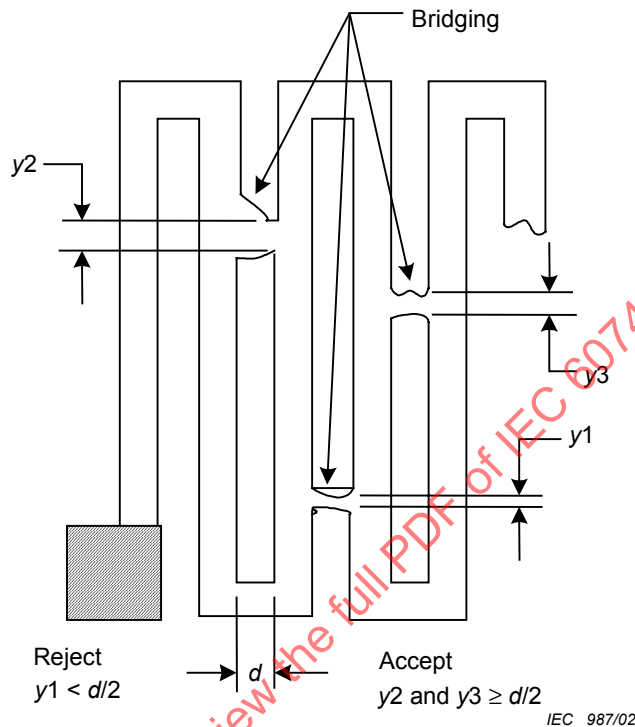


Figure 27 – Class H – Bridging of resistor material criteria

6.7 Laser trimmed thin film resistor non-conformances - "high magnification"

NOTE The laser trim non-conformance criteria contained in this subclause apply to active resistor areas only.

No element shall be acceptable that exhibits:

Class H

- a) A kerf width less than 2,5 μm (see figure 28).

Class K

- a) Same as Class H.

NOTE This does not apply to edge trimming.

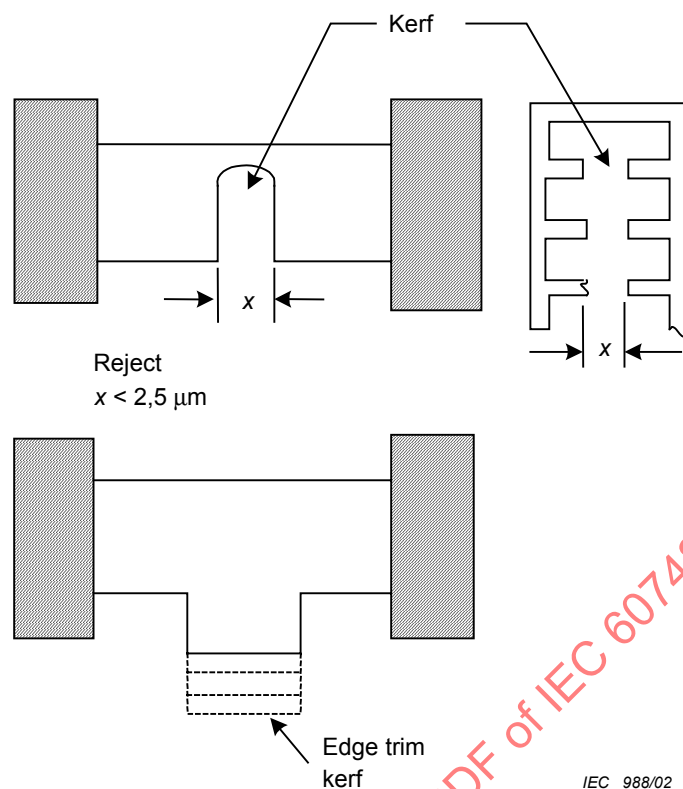


Figure 28 – Class H – Kerf width criteria

b) A kerf containing particles of detritus.

b) Same as Class H.

For resistor materials that are self-passivating (such as tantalum nitride), detritus in the kerf is allowed provided that a clear path of at least $2,5\ \mu\text{m}$ in width exists in the kerf. Such detritus shall be attached. Verification of attachment shall be accomplished using the techniques described in 6.5 a) (see figure 29).

NOTE This does not apply to edge trimming.

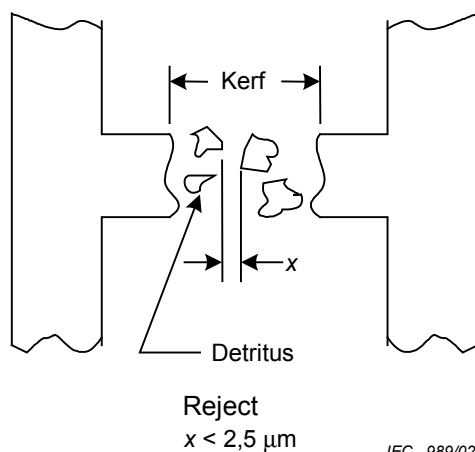


Figure 29 – Class H – Detritus criterion for self-passivating resistor materials

Class H

In the case of a resistor loop made with self-passivating resistor material which is similar in configuration to the one shown in figure 30, there shall be at least one kerf that contains a clear path of at least $2,5\text{ }\mu\text{m}$ in width; otherwise, the element shall be rejected.

Class K

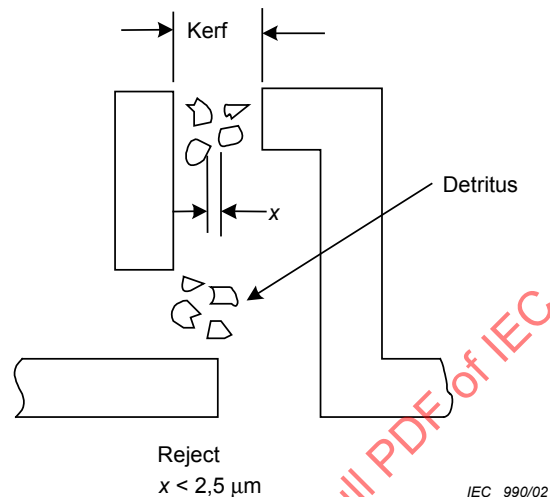


Figure 30 – Class H – Resistor loop element detritus criterion for self-passivating resistor materials

c) Bridging of detritus between rungs in the active area of a resistor ladder structure (see figure 31).

c) Same as Class H.

NOTE Bridging of detritus in inactive areas is acceptable.

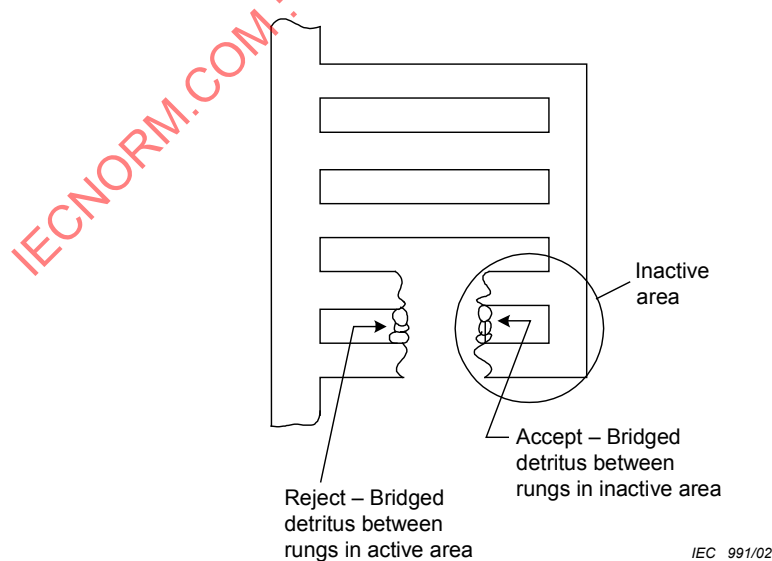


Figure 31 – Bridging of detritus between rungs in the active area of a resistor ladder structure criterion

Class H

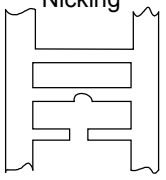
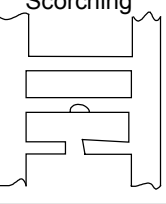
- d) No nicking or scorching is allowed except as permitted below.

NOTE 1 This does not apply to rungs in a fine resistor ladder structure (see figure 32).

NOTE 2 See 3.53 for a definition of coarse and fine resistor ladder structures. The element drawing must be referenced to determine if a given resistor ladder structure is coarse or fine.

Class K

- d) Same as Class H.

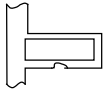
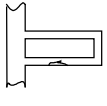
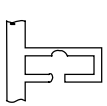
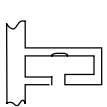
	Coarse ladders	Fine ladders
 Nicking	Reject	Accept
 Scorching	Reject	Accept

IEC 992/02

Figure 32 – Class H – Resistor ladder structure nicking and scorching criteria exceptions

NOTE 3 These criteria do not apply to the second rung of a resistor loop since the second rung is inactive. These criteria do not apply to a fine loop or to a resistor structure that consists of fine loops (see figure 33).

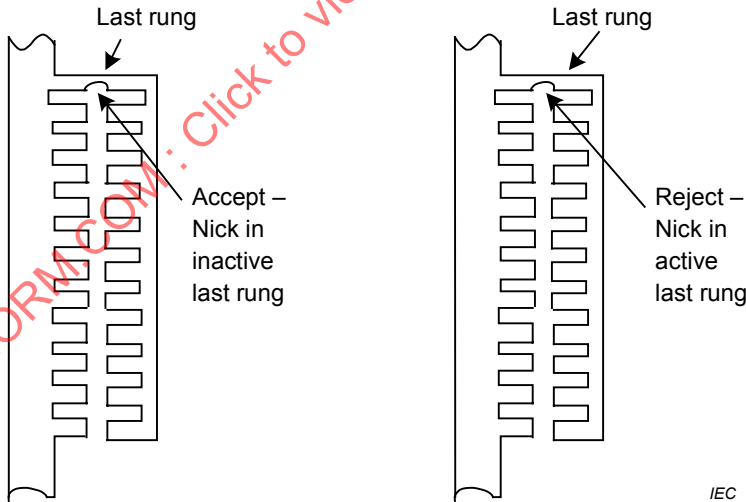
NOTE 4 See 3.55 for a definition of coarse and fine resistor loop structures. The element drawing must be referenced to determine if a given resistor loop structure is coarse or fine.

		Course loops	Fine loops
Nick in first (Active) rung		Reject	Accept
Scorch in first (Active) rung		Reject	Accept
Nick in second (Inactive) rung		Accept	Accept
Scorch in second (Inactive) rung		Accept	Accept

IEC 993/02

Figure 33 – Class H – Resistor loop nicking and scorching criteria exceptions

NOTE This criterion does not apply to the last rung of a resistor ladder if the last rung is inactive (see figure 34).



IEC 994/02

Figure 34 – Class H – Laser nicking criteria exception for the last rung of a resistor ladder

Class H

- e) A kerf or scorch which extends into a resistor ladder sidebar (see figure 35).

Class K

- e) Same as Class H.

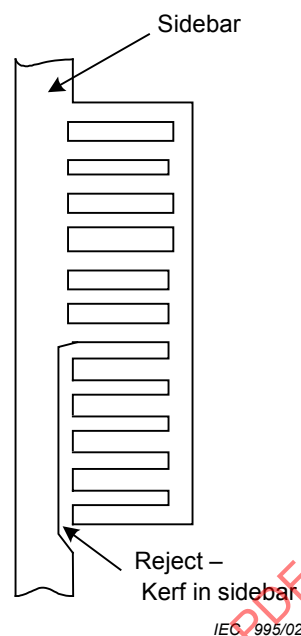


Figure 35 – Class H – Resistor ladder sidebar trim criterion

- f) Kerf or scorch misalignment (see figure 36).

- f) Same as Class H.

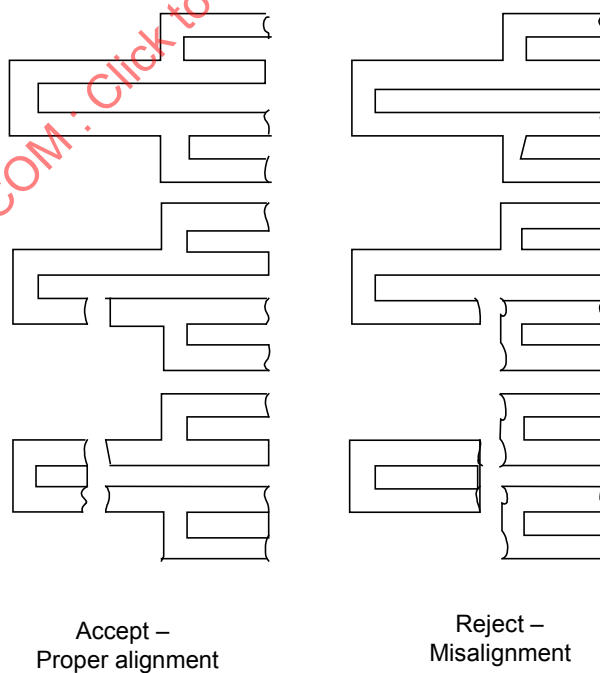


Figure 36 – Class H – Laser trim misalignment criteria

Class H

- g) A kerf which extends into metallization and leaves less than 75 % of the metallization width undisturbed (see figure 37).

NOTE Opening a metallization link by design is acceptable.

Class K

- g) Same as Class H.

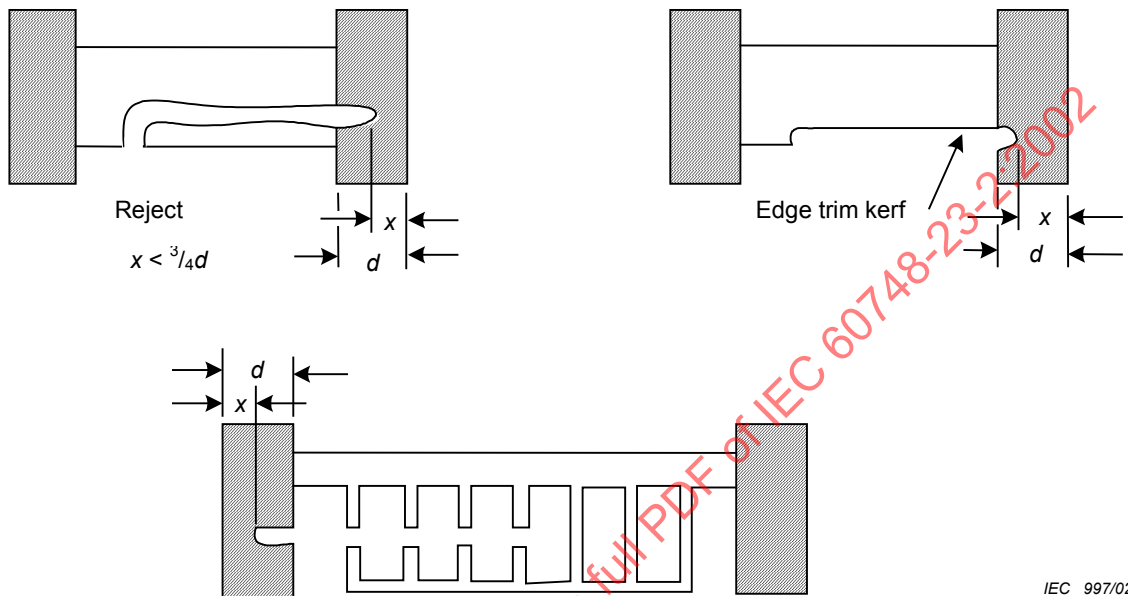


Figure 37 – Class H – Laser trim kerf extension into metallization criteria

Class H

- h) A kerf in a resistor, at the interface of the resistor material with the metallization, that leaves less than 50 % of the original resistor width, unless by design.

PRECAUTIONARY NOTE The maximum allowable current density requirement must not be exceeded. (see figure 38).

Class K

- h) Same as Class H.

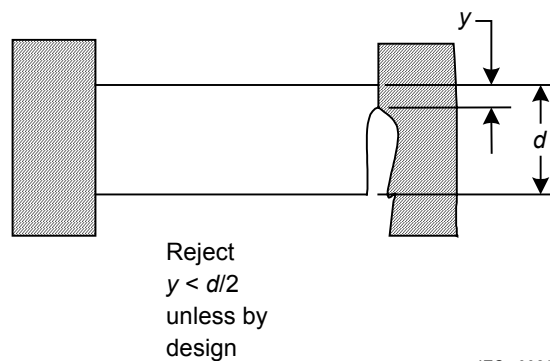


Figure 38 – Class H – Resistor width reduction at metallization interface criteria

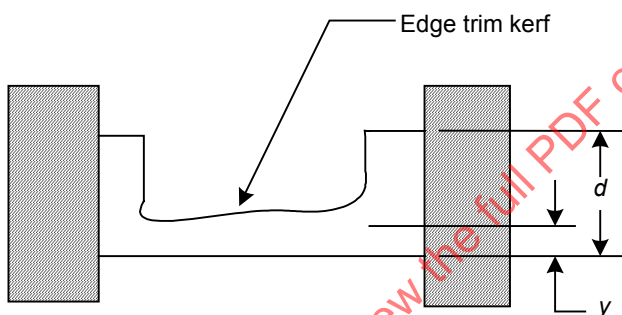
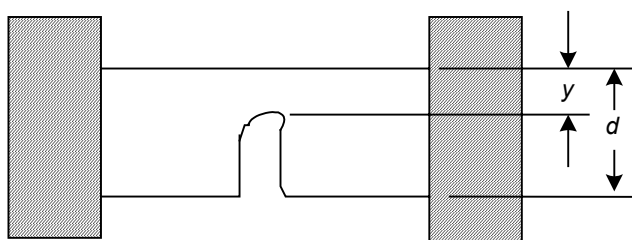
Class H

- i) A kerf in a resistor that leaves less than 50 % of the original resistor width, unless by design.

PRECAUTIONARY NOTE The maximum allowable current density requirement must not be exceeded (see figure 39).

Class K

- i) Same as Class H.



Reject
 $y < d/2$
 unless by
 design

IEC 999/02

Figure 39 – Class H – Resistor width reduction by trimming criteria

- j) A kerf in a resistor that leaves less than 50 % of the narrowest resistor width unless by design (see figure 40).

NOTE A floating kerf (one that is completely contained within the resistor) must meet this criterion.

PRECAUTIONARY NOTE The maximum allowable current density requirement must not be exceeded.

- j) Same as Class H.

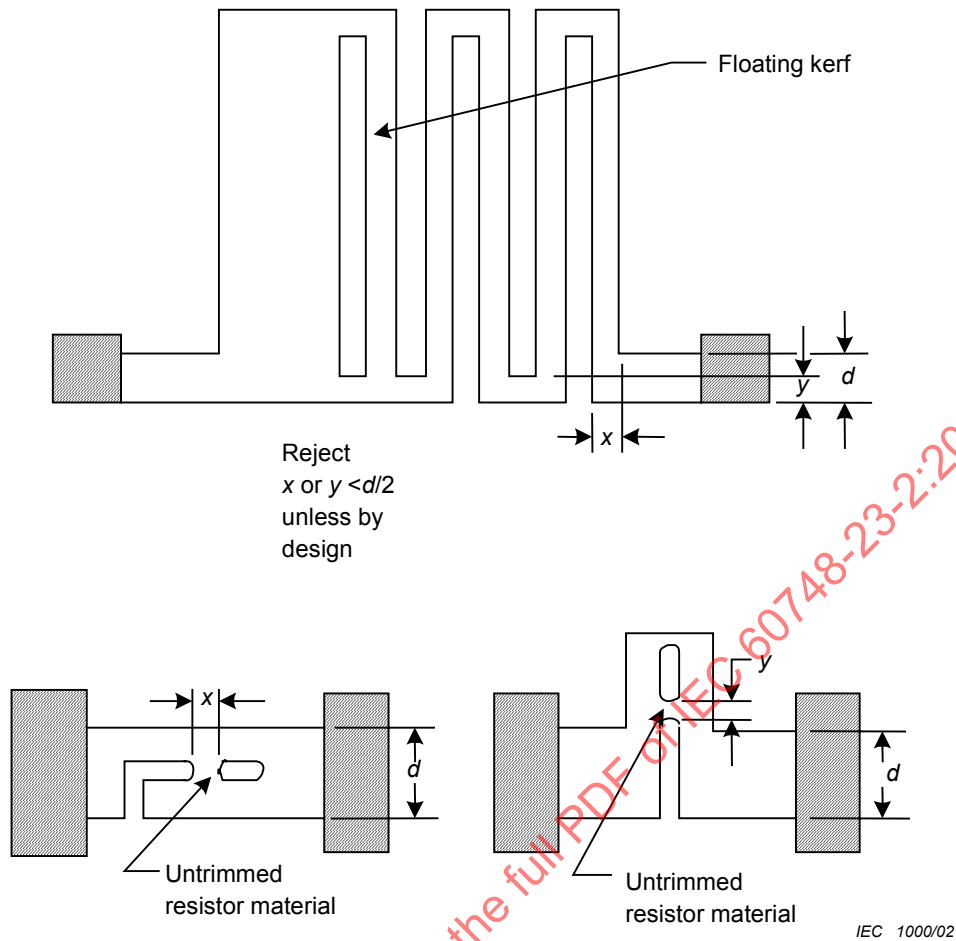


Figure 40 – Class H – Resistor width reduction and untrimmed resistor material criteria

k) Pits into the silicon dioxide of conductive substrate elements in the kerf which does not show a line of separation between the pit and the resistor material (see figure 41).

k) Same as Class H.

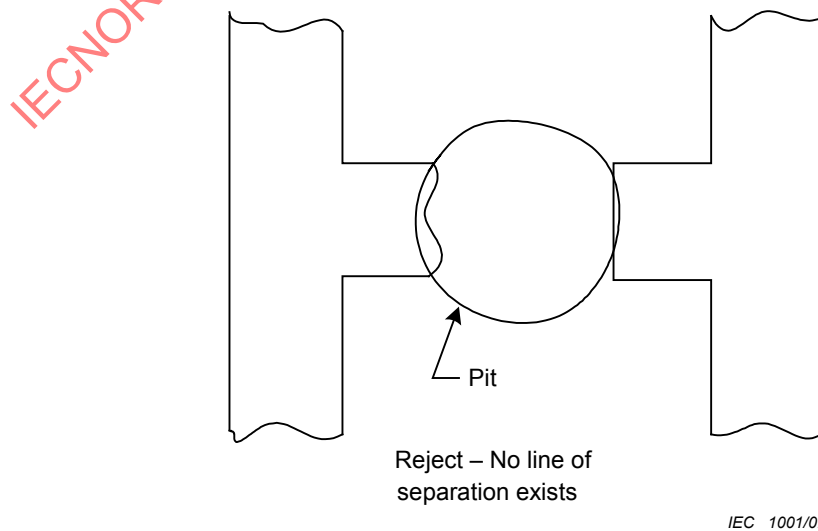


Figure 41 – Class H – Laser trim pitting criterion

6.8 Multilevel thin film non-conformances - "high magnification"

No element shall be acceptable that exhibits:

Class H

- a) Insulating material that does not extend beyond the width of the upper and lower metallization by 7,5 μm minimum (see figure 42).

Class K

- a) Same as Class H.

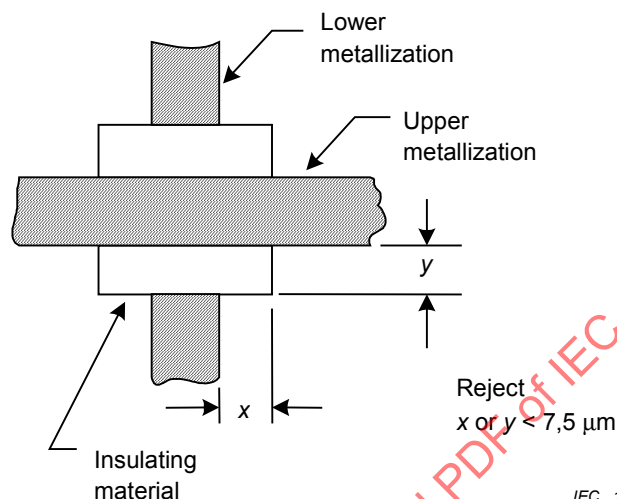


Figure 42 – Class H – Insulating material extension criteria

- b) Voids in the insulating material.

- b) Same as Class H.

- c) A bump or indentation in the upper (overlying) metallization.

- c) Same as Class H.

NOTE This criterion is not applicable to coupling (air) bridges.

- d) Scratch that completely crosses the metallization and damages the insulating material surface on either side.

- d) Same as Class H.

6.9 Coupling (air) bridge non-conformances - "high magnification"

No element shall be acceptable that exhibits:

- a) A void in the coupling (air) bridge metallization that leaves less than 50 % of the original metallization width undisturbed (see figure 43).

- a) Same as Class H.

- b) Nodules or bumps that are greater, in any dimension, than the original coupling (air) bridge metallization width (see figure 43).

- b) Same as Class H.

- c) Coupling (air) bridge that contacts underlying operating metallization (see figure 43).

- c) Same as Class H.

Class H

d) Attached, conductive foreign material that is greater, in any dimension, than 50 % of the original coupling (air) bridge metallization width.

e) No visible separation between the coupling (air) bridge and the underlying operating metallization.

NOTE This criterion is not applicable when an insulating material is used between the coupling (air) bridge and the underlying metallization (see figure 43).

f) Coupling (air) bridge metallization overhang over adjacent operating metallization, not intended by design, that does not exhibit a visible separation (see figure 43).

g) Mechanical damage to a coupling (air) bridge that results in depression (lowering) of coupling (air) bridge metallization over underlying operating metallization.

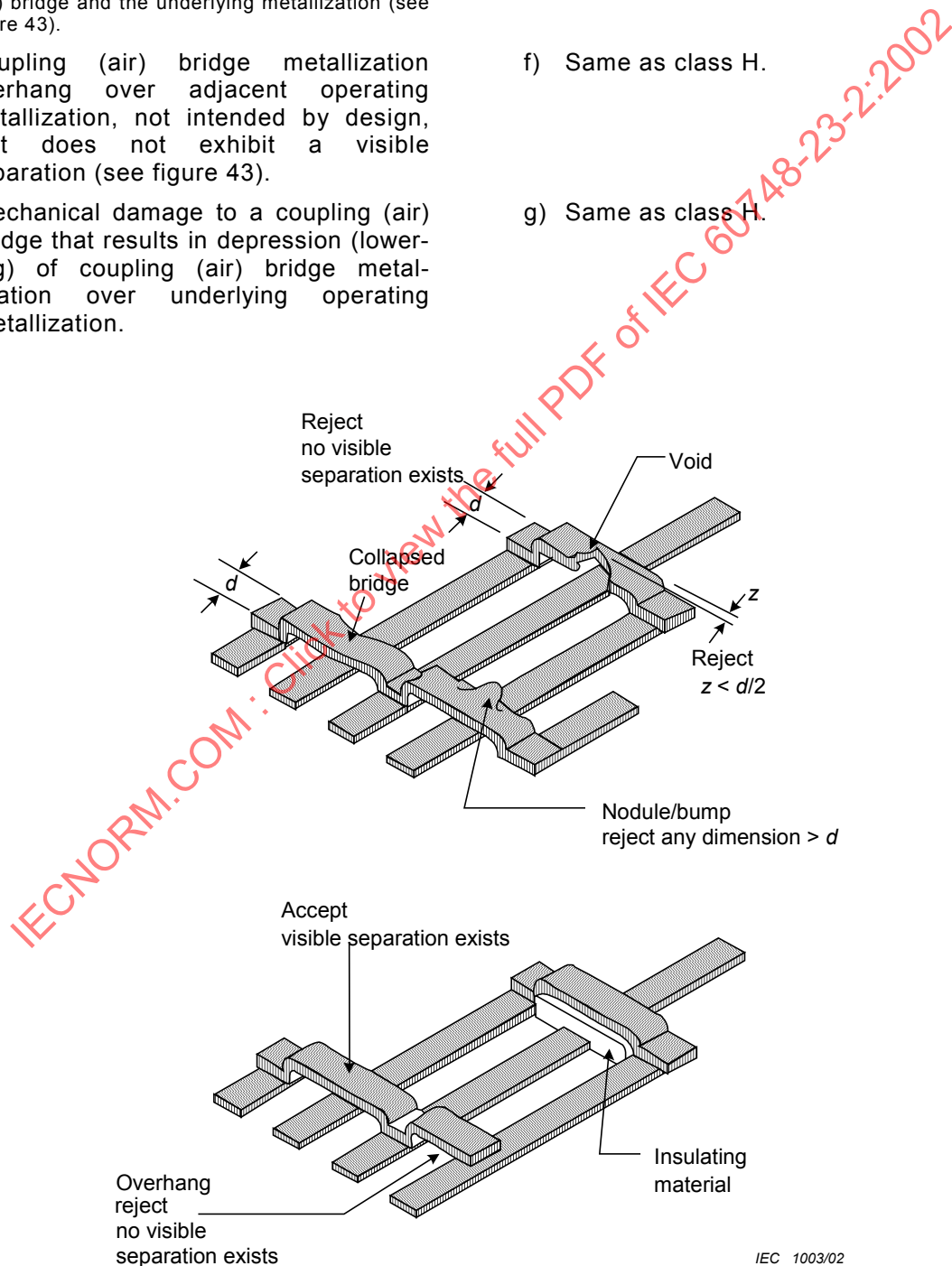
Class K

d) Same as Class H.

e) Same as Class H.

f) Same as class H.

g) Same as class H.



IEC 1003/02

Figure 43 – Class H and Class K – Coupling (air) bridge criteria

7 Planar thick film element inspection

Inspection for visual non-conformances described in this clause shall be conducted on each planar thick film passive element. All inspection shall be performed at "low magnification" within the range of 10× to 60× magnification for both class H and class K.

7.1 Operating metallization non-conformances - "low magnification"

NOTE The metallization non-conformance criteria contained in this subclause apply to operating metallization only.

No element shall be acceptable that exhibits:

7.1.1 Metallization scratches

Class H

- a) A scratch or probe mark in the metallization, excluding bonding pads, that both exposes underlying material anywhere along its length and leaves less than 50 % of the original metallization width undisturbed (see figure 44).

NOTE 1 Underlying material does not have to be exposed along the full length of the scratch.

NOTE 2 This criterion does not apply to capacitors.

Class K

- a) Same as Class H.

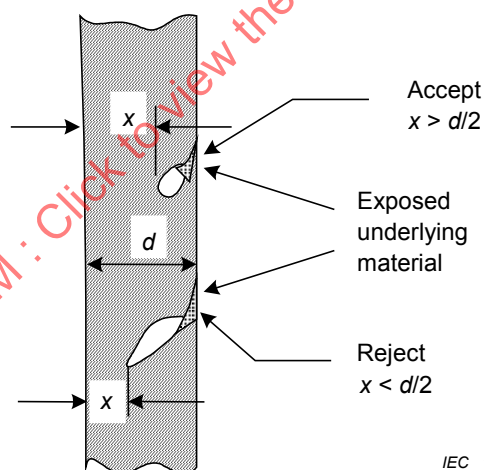


Figure 44 – Class H – Metallization scratch criteria

- b) Scratch in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, to less than 50 % of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 45).

- b) Less than 75 % (see figure 46).

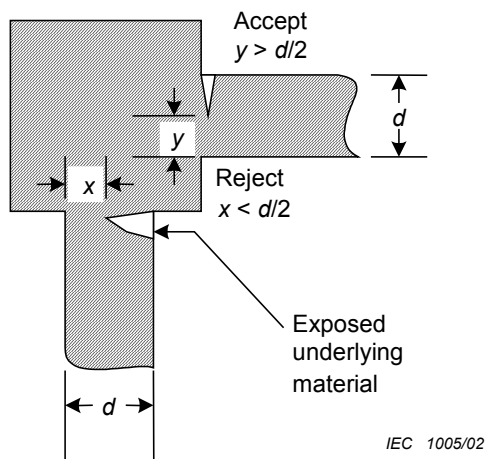


Figure 45 – Class H – Metallization width reduction at bonding pad criteria

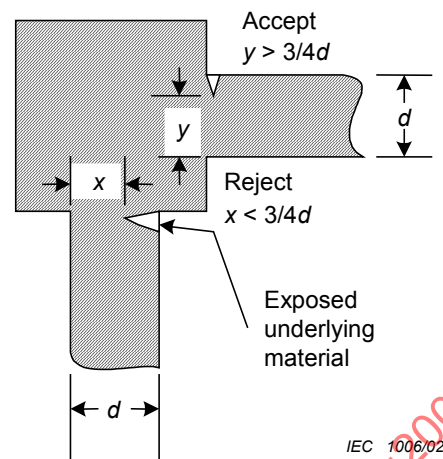


Figure 46 – Class K – Metallization width reduction at bonding pad criteria

- c) Scratch or probe marks in the bonding pad area that expose underlying material over more than 25 % of the original metallization area.

- c) Same as Class H.

7.1.2 Metallization voids

Class H

- a) Void(s) in the metallization, excluding bonding pads, that leaves less than 50 % of the original metallization width undisturbed (see figure 47).

Class K

- a) Same as Class H.

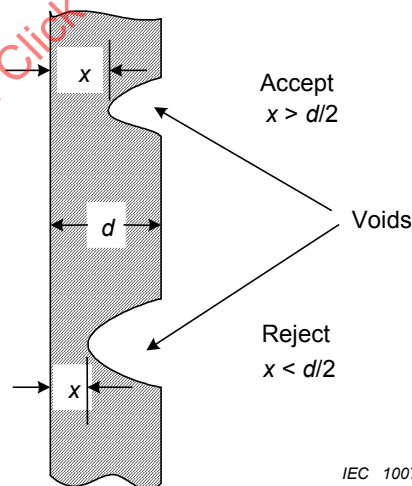


Figure 47 – Class H – Metallization void criteria

Class H

- b) Void(s) in the bonding pad area that reduce the metallization path width, where it enters the bonding pad, to less than 50 % of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately.

NOTE Figures 45 and 46 illustrate metallization width reduction at bonding pad criteria for scratches. Void criteria are similar.

- c) Void(s) in the bonding pad area that expose underlying material over more than 25 % of the original metallization area.

NOTE For r.f. microwave elements on non-conductive substrates, a void created in the bonding pad area as a result of wire bond removal for performance optimization or tuning, is not rejectable provided that the void remains entirely visible.

7.1.3 Metallization corrosion

- a) Any metallization corrosion.

7.1.4 Metallization adherence

- a) Any metallization lifting, peeling, or blistering.

NOTE 1 Nodules are acceptable. In order to determine if a bump in the metallization is a blister or a nodule, attempt to flatten the bump with a non-metallic instrument. If the bump flattens, then it is a blister.

NOTE 2 These criteria are not applicable to separation induced anomalies (for example, metallization lifting due to scribe and break or diamond sawing) since these are not indicative of adhesion problems.

7.1.5 Metallization protrusion

- a) More than 50 % reduction of the original design separation, between any protruding metallization and adjacent metallization paths (see figure 48).

Class K

- b) Less than 75 %.

- c) Same as Class H.

- a) Same as Class H.

- a) Same as Class H.

- a) Same as Class H.

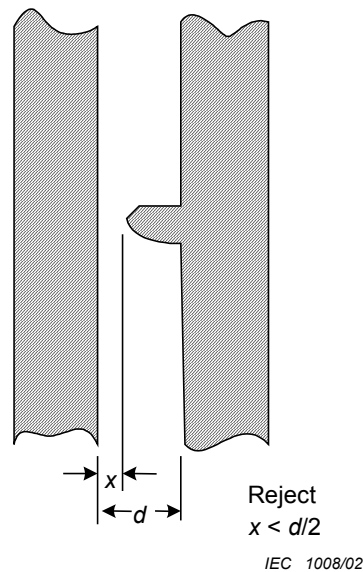


Figure 48 – Class H – Metallization protrusion criterion

7.1.6 Metallization overlap

Class H

- a) Contact overlap between the upper and lower metallizations that is less than 50 % of the designed contact overlap area (see figure 49).

NOTE The overlap area is that area in which the upper metallization actually contacts the lower metallization.

Class K

- a) Same as Class H.

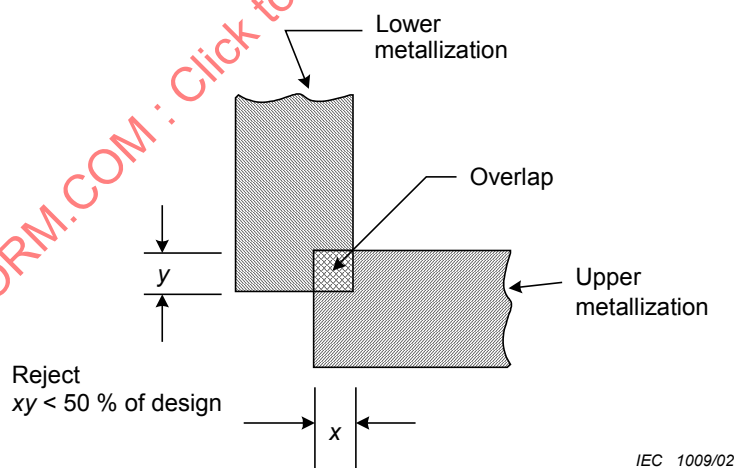


Figure 49 – Class H – Metallization overlap criterion

7.1.7 Metallized through-hole non-conformances - "low magnification"

No element shall be acceptable that exhibits:

- a) Through-hole metallization that is not perpendicularly continuous or that does not cover at least a continuous 50 % of the inside, circumferential surface area unless by design.
- a) Same as Class H.

7.1.8 Wrap-around connection non-conformances - "low magnification"

No element shall be acceptable that exhibits:

Class H

- a) Unmetallized area in the edges of wrap-around connections greater than 50 % of the largest dimension of the edge metallization (see figure 50).

Class K

- a) Same as Class H.

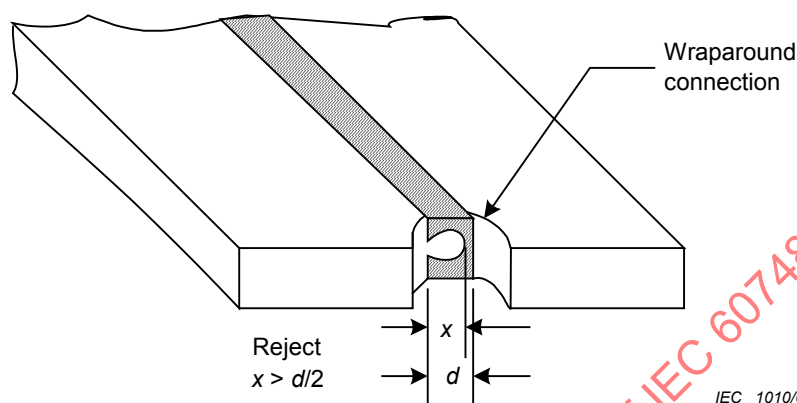


Figure 50 – Class H – Wrap-around connection unmetallized area criterion

7.2 Substrate non-conformances - "low magnification"

No element shall be acceptable that exhibits:

- a) Less than 2,5 μm separation between the operating metallization and the edge of the element unless by design (see figure 51).

- a) Same as Class H.

NOTE This criterion does not apply to substrates designed for wrap-around conductors.

- b) A chipout that extends into the active circuit area (see figure 51).

- b) Same as Class H.

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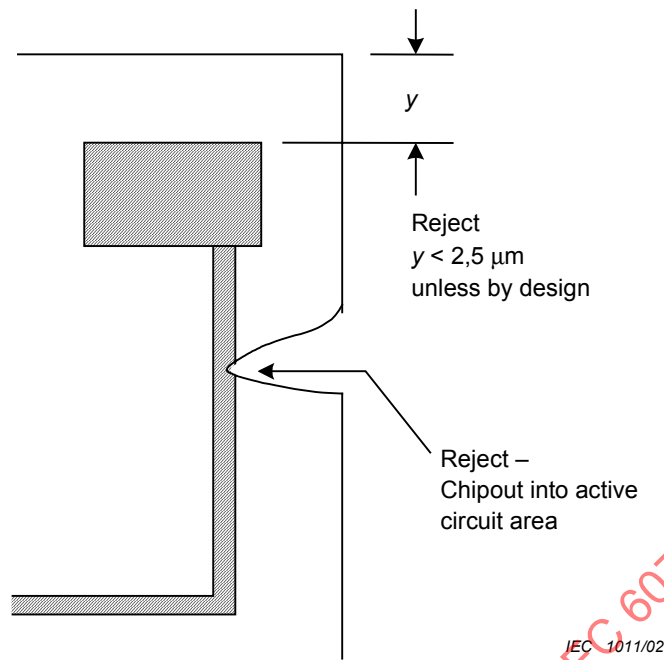


Figure 51 – Class H – Separation and chipout criteria

c) Any crack that exceeds 125 μm in length (see figure 52).

c) Same as Class H.

NOTE For fused quartz or crystalline substrates, no cracking is allowed.

d) Any crack that does not exhibit 25 μm of separation from any active circuit area or operating metallization (see figure 52).

d) Same as Class H.

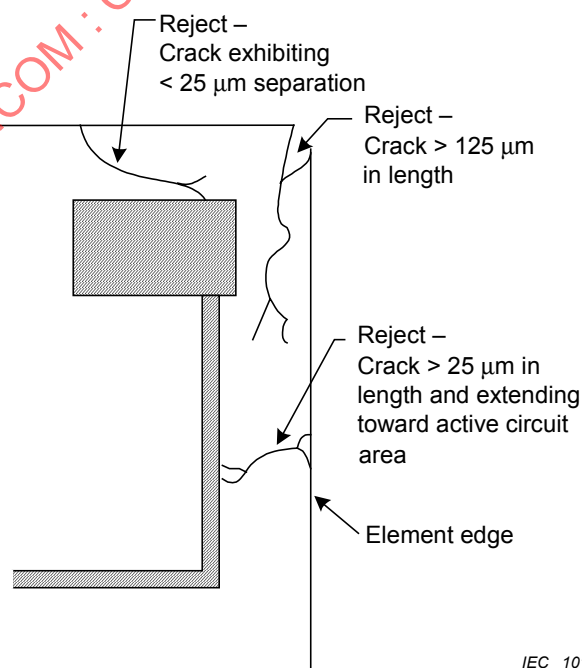


Figure 52 – Class H – Additional crack criteria

Class H

- e) Any crack exceeding 25 μm in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 52).
- f) N/A

Class K

- e) Same as Class H.
- f) Semicircular crack or combination of cracks along the element edge whose total length is equal to or greater than 75 % of the narrowest separation between any two bonding pads (see figure 53).

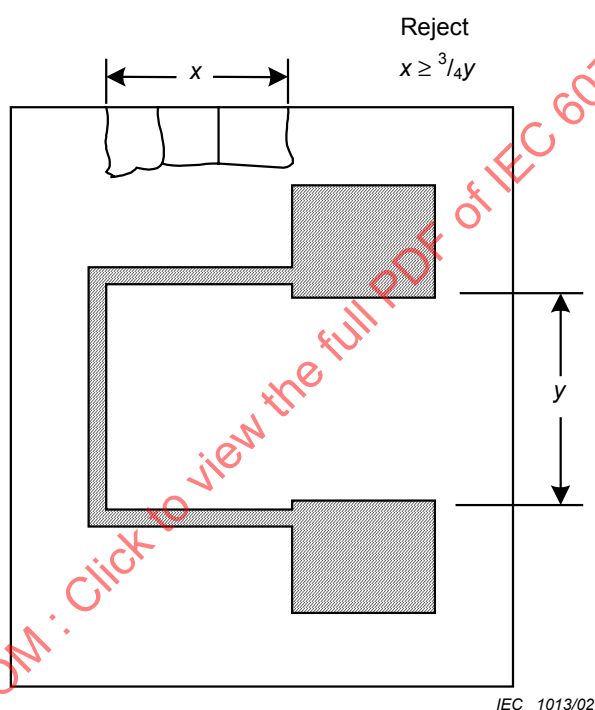


Figure 53 – Class K – Semicircular crack criterion

- g) An attached portion of a circuit area from an adjacent element.
- h) Any crack that does not originate at an edge.
- i) Holes through the substrate, unless by design.
- j) Patterned substrates having a section broken out around a substrate mounting hole(intended for substrate-to-post attachment) that is greater than 25 % of the mounting hole circumference.
- g) Same as Class H.
- h) Same as Class H.
- i) Same as Class H.
- j) Same as Class H.

7.3 Thick film resistor non-conformances - "low magnification"

No element shall be acceptable that exhibits:

Class H

- a) A reduction due to voids of the resistor at the terminal to less than 50 % of the original resistor width (see figure 54).

Class K

- a) Same as Class H.

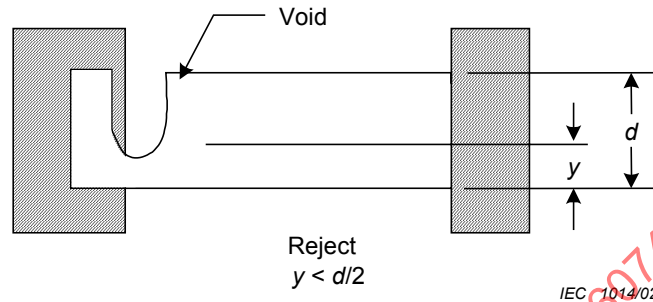


Figure 54 – Class H – Resistor width reduction at terminal caused by voids criterion

- b) Reduction due to neck-down of the resistor at the terminal, to less than 50 % of the original resistor width (see figure 55).

- b) Same as Class H.

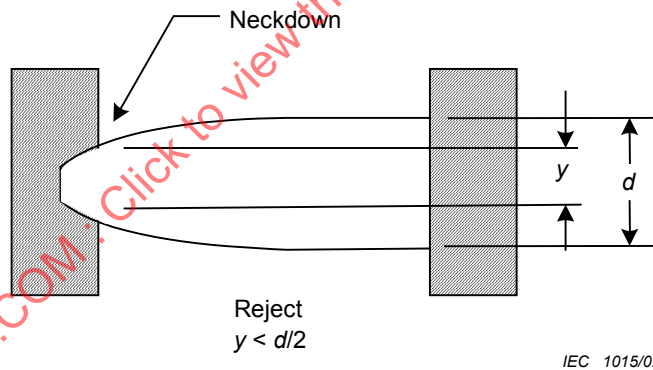


Figure 55 – Class H – Resistor width reduction at terminal by neck-down criterion

- c) Any resistor film lifting, peeling, or blistering.
- d) Crack in the resistor greater than 25 µm in length.

- c) Same as Class H.

- d) Same as Class H.

NOTE Irregularities such as fissures in resistor material that are created during firing, and that do not expose the underlying material, are not considered to be cracks.

- e) Evidence of resistor repair by over-printing or any other means.

- e) Same as Class H.

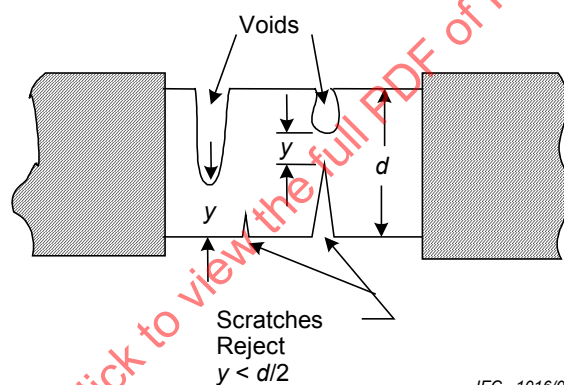
Class H

- f) Separation between any two resistors that is less than 50 % of the original separation.
- g) Separation between any resistor and conductor combination that is less than 50 % of the original separation.
- h) Increase in resistor width greater than 25 % of the original design width.
- i) Resistor that is closer than 25 μm to the edge of the substrate.
- j) Reduction of resistor width resulting from voids, scratches, or chipouts, or a combination of these, that leaves less than 50 % of the narrowest resistor width (see figure 56).

PRECAUTIONARY NOTE The maximum allowable current density requirement must not be exceeded.

Class K

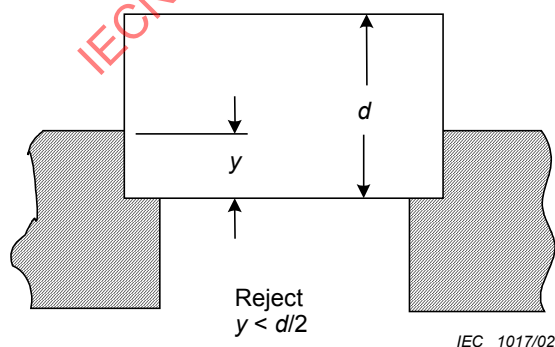
- f) Same as Class H.
- g) Same as Class H.
- h) Same as class H.
- i) Same as Class H.
- j) Same as Class H.



IEC 1016/02

Figure 56 – Class H – Resistor width reduction criteria

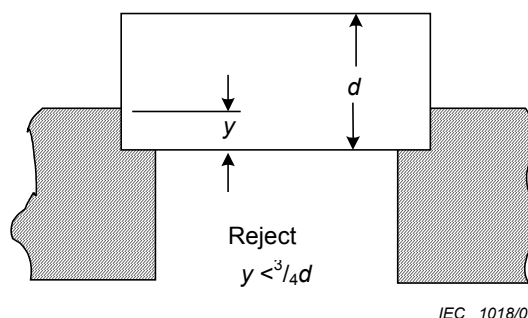
- k) Contact overlap between the metalization and the resistor in which the actual width dimension "y" is less than 50 % of the original resistor width (see figure 57).



IEC 1017/02

Figure 57 – Class H – Resistor overlap criterion

- k) Less than 75 % (see figure 58).



IEC 1018/02

Figure 58 – Class K – Resistor overlap criterion

Class H

- l) Contact overlap between the metalization and the resistor in which the length dimension "x" is less than $75\text{ }\mu\text{m}$ (see figure 59).

Class K

- l) Same as Class H.

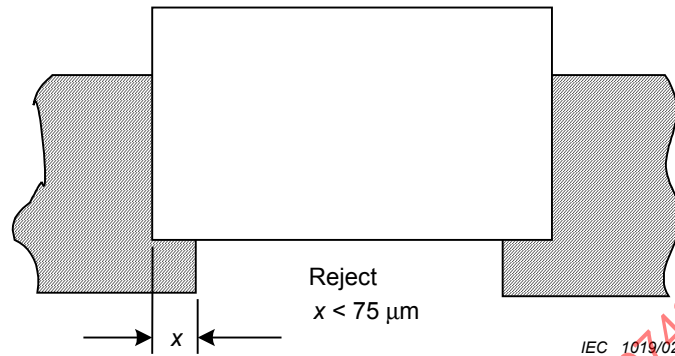


Figure 59 – Resistor overlap criterion

- m) Voids or misalignment of glassivation that results in less than 90 % coverage of the resistor area, unless by design.
n) Crazeing of glassivation over a resistor.
o) Glassivation scratches, lifting, or peeling that expose any portion of a resistor.

- m) Same as Class H.
n) Same as Class H.
o) Same as Class H.

7.4 Trimmed thick film resistor non-conformances - "low magnification"

NOTE The trim non-conformance criteria contained in this subclause apply to active resistor areas only.

No element shall be acceptable that exhibits:

- a) A kerf width less than $12,5\text{ }\mu\text{m}$ (see figure 60).

- a) Same as Class H.

NOTE This does not apply to edge trimming.

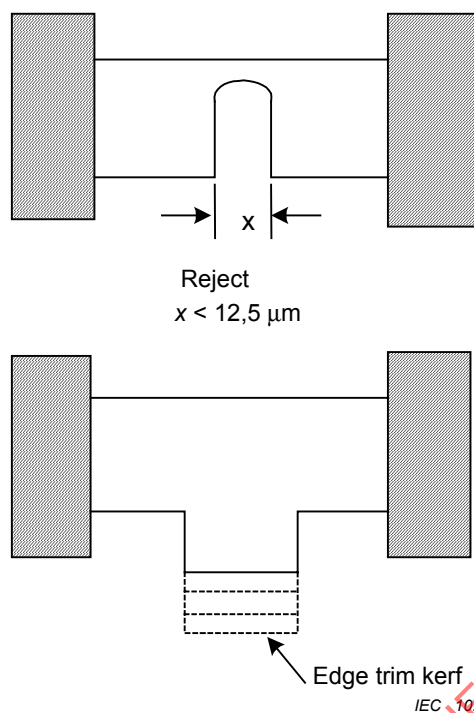


Figure 60 – Class H – Kerf width criteria

Class H

Class K

b) A kerf containing detritus.

b) Same as Class H.

c) A kerf which extends into metallization and leaves less than 75 % of the metallization width undisturbed (see figure 61).

c) Same as Class H.

NOTE Opening a metallization link by design is acceptable.

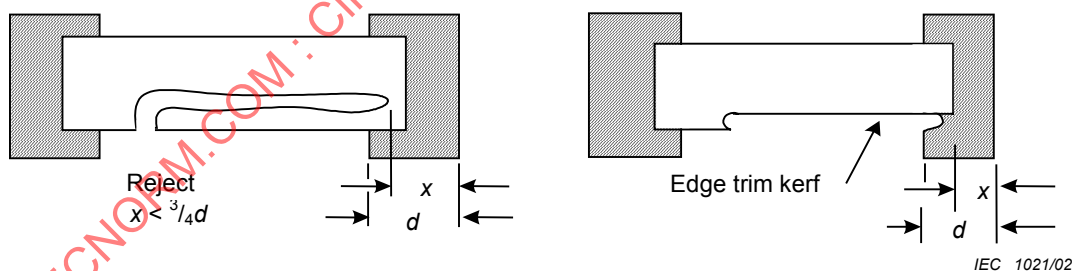


Figure 61 – Class H – Laser trim kerf extension into metallization criteria

d) A kerf that leaves less than 50 % of the original width of a resistor, unless by design (see figure 62).

d) Same as class H.

PRECAUTIONARY NOTE The maximum allowable current density requirement must not be exceeded.

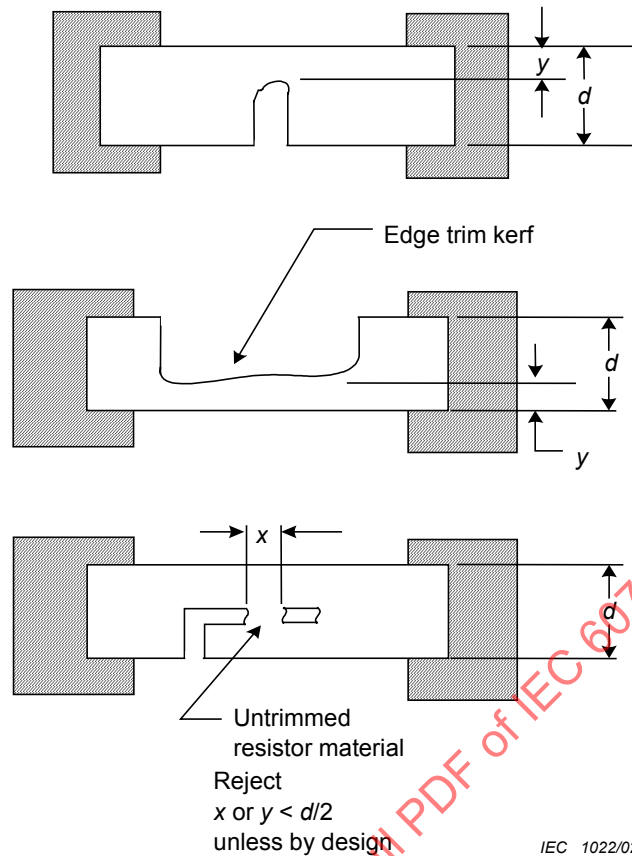


Figure 62 – Class H – Resistor width reduction and untrimmed resistor material criteria

Class H

- e) A trim that does not originate from the edge of the resistor.

Class K

- e) Same as Class H.

7.5 Multilevel thick film non-conformances - "low magnification"

No element shall be acceptable that exhibits:

- | | |
|--|---------------------|
| a) Any insulating material that does not extend beyond the width of the upper and lower metallization by 75 μm minimum (see figure 63). | a) Same as Class H. |
| b) Voids in the insulating material that expose underlying metallization. | b) Same as Class H. |
| c) Vias that are less than 50 % of the original design area. | c) Same as Class H. |
| d) Scratch that completely crosses the metallization and damages the insulating material surface on either side. | d) Same as Class H. |

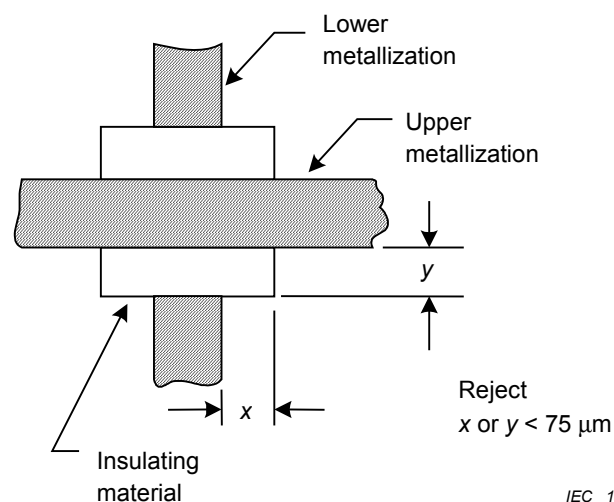


Figure 63 – Class H – Dielectric extension criteria

7.6 All thin film capacitors and overlay capacitors used in GaAs microwave devices - "low magnification"

No element shall be acceptable that exhibits:

- scratches that expose an underlying material;
- any peeling or lifting of the metallization;
- excess top metal which extend beyond the capacitor bottom metal;
- voids in the capacitor bottom metal which extend under the capacitor top metal;
- voids in the top metallization which leaves less than 75 % of the metallization area undisturbed.

8 Active and passive elements

All integrated circuit, transistor and semiconductor diode elements shall be examined in accordance with the visual inspection requirements of IEC 60747.

Passive elements (including substrates) shall be examined in accordance with clauses 5 and 6.

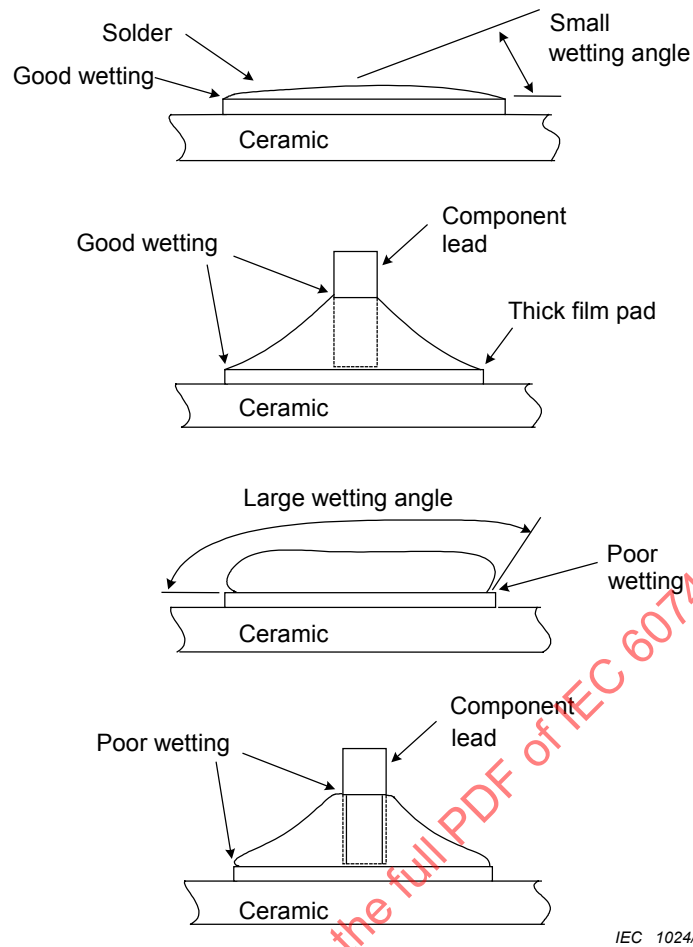
Soldered surface mounted assemblies shall be examined in accordance with IEC 61191-2.

9 Element attachment (assembly) - "magnification 10× to 60×"

9.1 Solder connections (general appearance)

No device will be acceptable that exhibits:

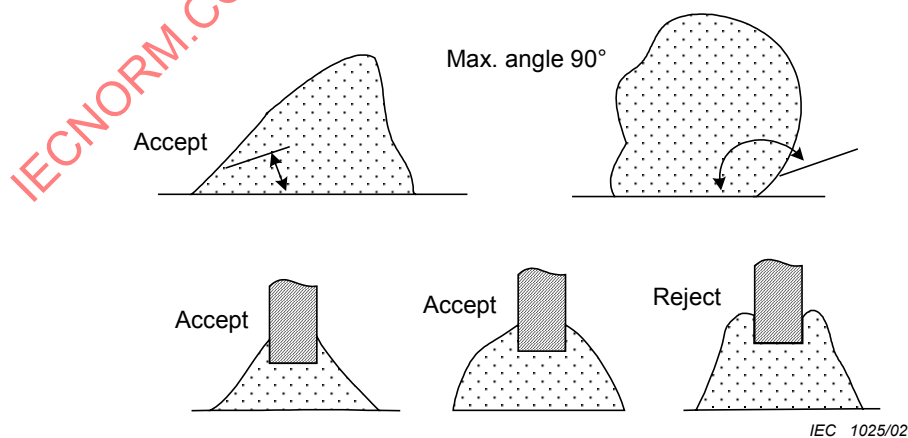
Soldered connections with poor wetting to either the film solder pad or the component termination. Good wetting is defined as when the wetting angle is less than 90° (see figure 64).



IEC 1024/02

Figure 64 – Solder wetting criteria

The degree of wetting of solder to a conductor is assessed by the contact angle between the two at their common interface perimeter. Contact angles greater than 90° shall be the cause of rejection (see figure 65).



IEC 1025/02

Figure 65 – Solder wetting contact angle

9.2 Element attachment requirements

Figure 66 gives examples of visual representations of attachment media types.

NOTE 1 Rejection criteria are not to be derived from these examples but rather from the specific criteria descriptions that follow.

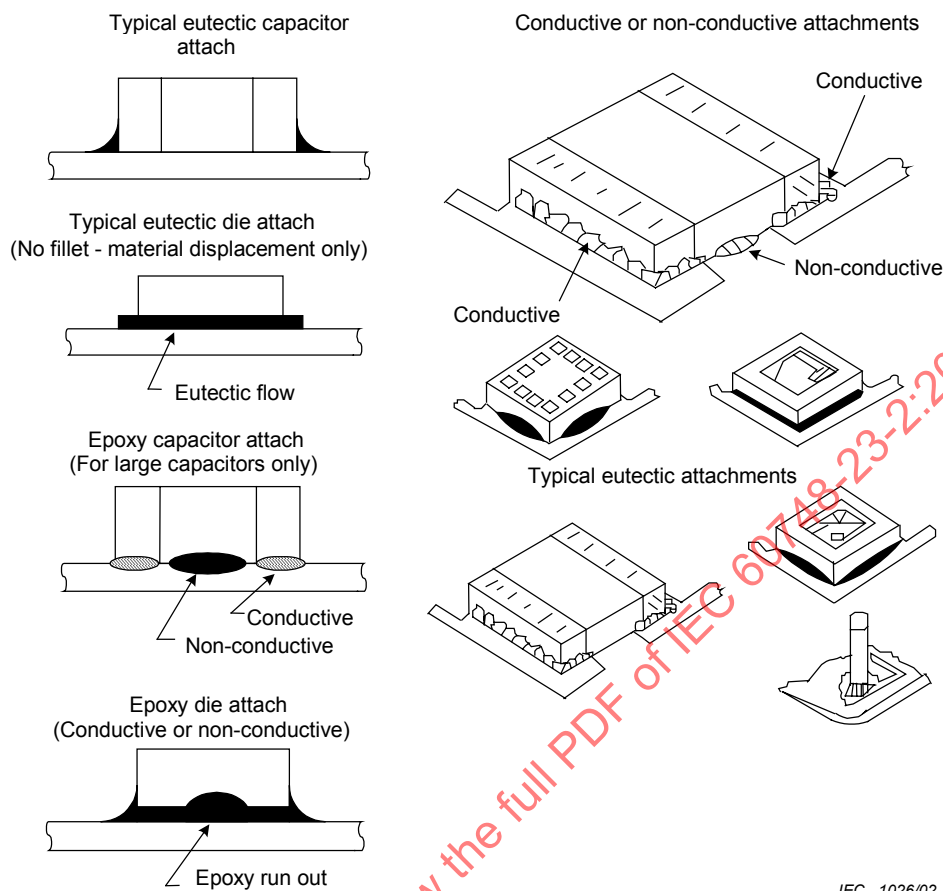


Figure 66 – Element attachments

Class H

NOTE 2 Mechanical strength or radiography may be used to verify attachment in lieu of visual criteria.

Class K

Dielectric attachment may be assessed through mechanical strength testing. For conductive attachment, the qualifying activity may approve alternative methods for verifying attachment integrity.

No device shall be acceptable that exhibits:

- a) For non-end-terminated elements, attachment media not visible around at least 50 % of the perimeter unless it is continuous on two full non-adjacent sides of the element.

NOTE 3 The criterion of 9.2 a) does not apply when attachment material is applied directly to more than 50 % of the element attach area by use of a method such as preforms or printing.

- b) End-terminated elements that do not have conductive attachment media visible around at least 50 % of the visible bonding pad perimeter on each end termination. For dielectric attachment of end-terminated elements (i.e. where the body of the element between the end terminations is attached), the criterion of a) above applies.

- b) End terminated elements that do not have conductive attachment media visible around at least 75 % of the visible bonding pad perimeter on each end termination. For dielectric attachment of end terminated elements (i.e. where the body of the element between the end terminations is attached), the criterion of a) above applies.

NOTE 4 These criteria do not apply when attachment material is applied directly to more than 50 % of the substrate attach area by use of a method such as printing. Mechanical strength of the attachment may be verified in lieu of visual criteria.

Class H

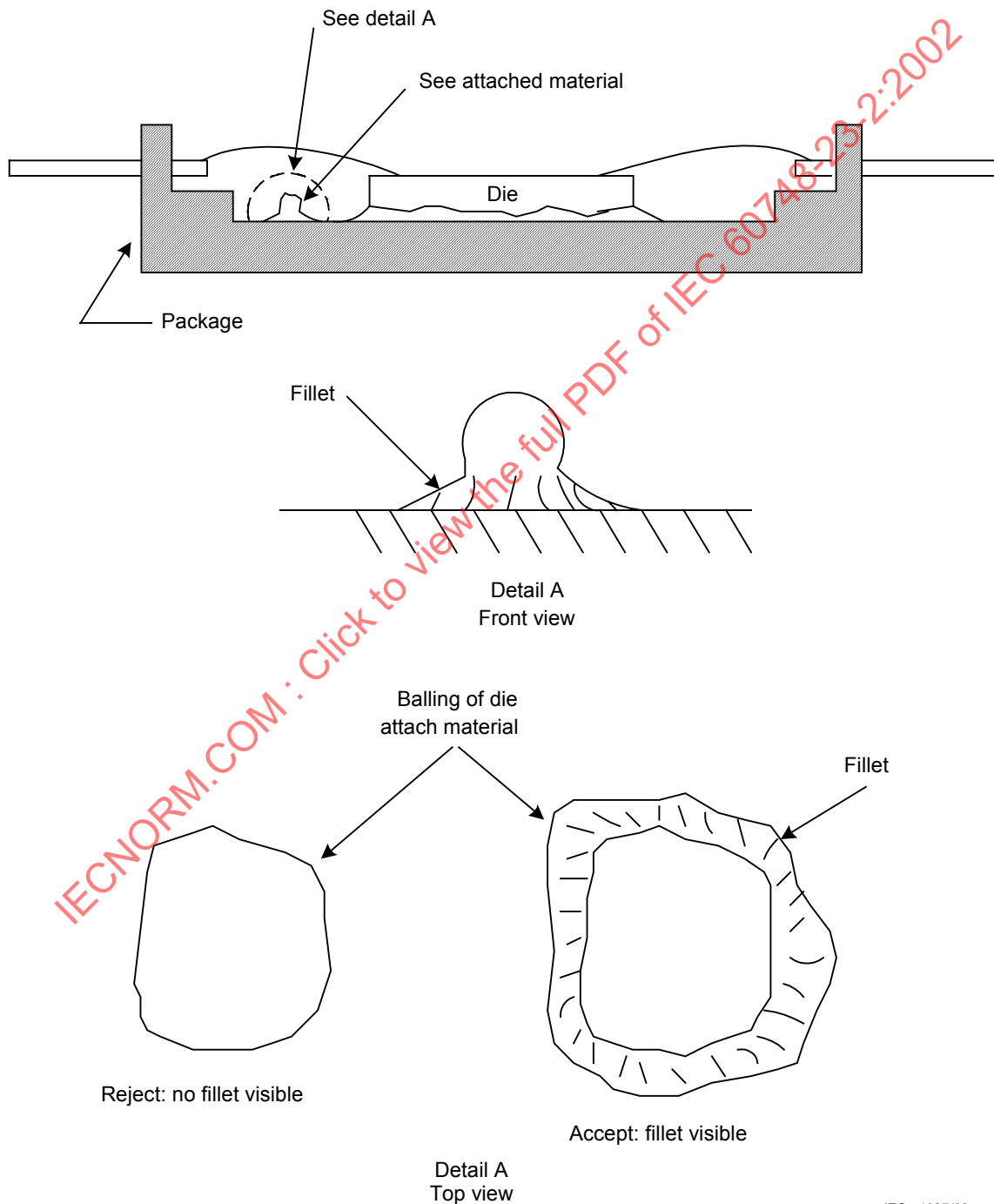
Class K

- c) Glass substrates or transparent die, when viewed from the bottom, which exhibit attach area less than 50 %.

NOTE 5 This criterion may be employed in lieu of that of 8.2 a).

- d) Flaking of the attachment media material.

- e) Balling of the solder or alloy material that does not exhibit a fillet (see figure 67).



IEC 1027/02

Figure 67 – Balling of die attach material

- f) Conductive attachment media which comes closer than $25\ \mu\text{m}$ to any functional metallization or element which is not electrically common.
- g) Cracks in the surface of the attachment media greater than $125\ \mu\text{m}$ in length or 10 % of the contact periphery, whichever is greater.

NOTE 6 Irregularities such as fissures or pullback at the edges of the adhesive are not considered cracks (see figure 68).

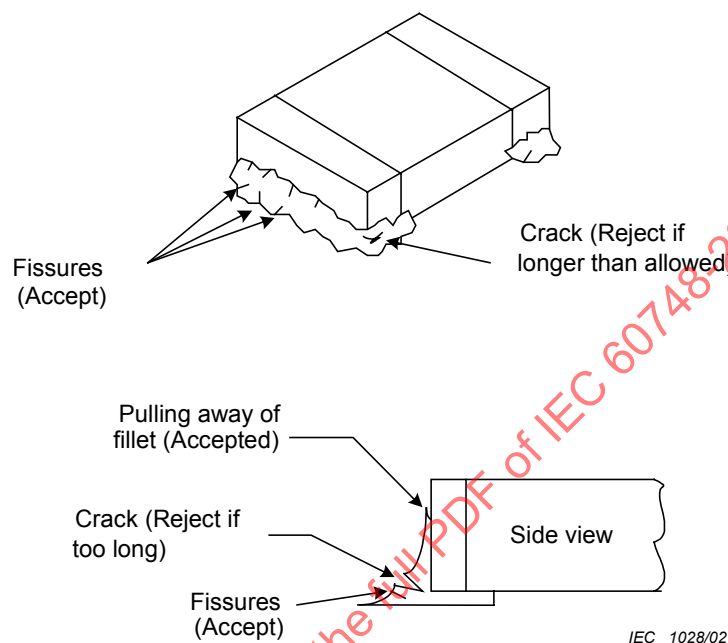


Figure 68 – Adhesive irregularities and cracks

- h) Adhesive strings where the diameter of the string at the point of attachment is less than 50 % of the maximum length of the string (see figure 69).

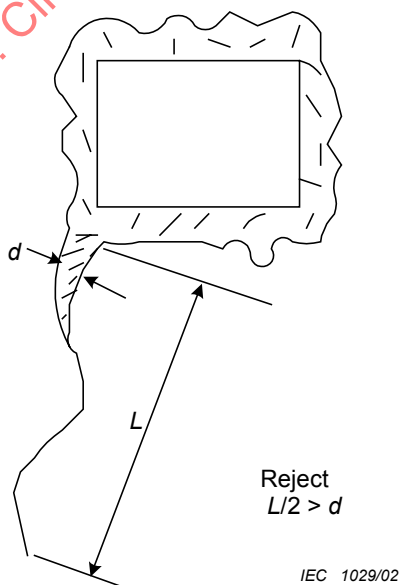
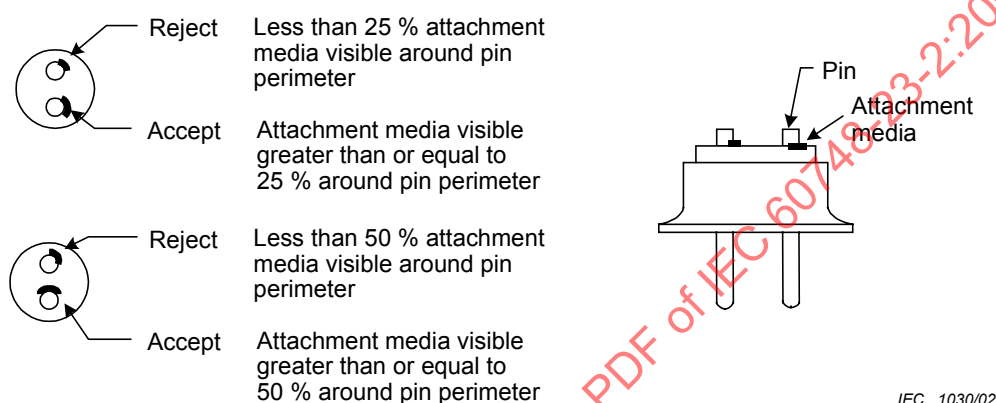


Figure 69 – Adhesive string criterion

- i) For element connection to a package post lead, attachment media visible for less than 25 % of the post perimeter. When the post also serves for substrate attachment, media shall be visible for no less than 50 % of the post perimeter (see figure 70).
- j) Cold solder joints.
- k) The width of a conductor shall not be reduced to less than 50 % of design through leaching or contamination.
- l) The area of a solder pad shall not be reduced more than 25 % of its designed area through leaching or contamination.
- m) Presence of any residual flux or flux residues (except, by design, ionically neutral flux).
- n) For thin film NiCr only, non-conductive adhesive material that covers more than 10 % of the active area of deposited resistor material.



IEC 1030/02

Figure 70 – Package post criteria

9.3 Leadless element attachment

Soldered surface mount components, pre-assembly, shall be examined in accordance with IEC 61191-2. Subclauses 9.4 to 9.6 give additional requirements.

9.4 Dual-in-line integrated circuit attachment (butt joints)

The following requirements apply to any component housed in a dual-in-line package (e.g. transistor/diode arrays, diode bridges) and other components, such as relays, connectors and transformers which do not have feet formed at the end of the leads and so make butt joints to the thick film pad.

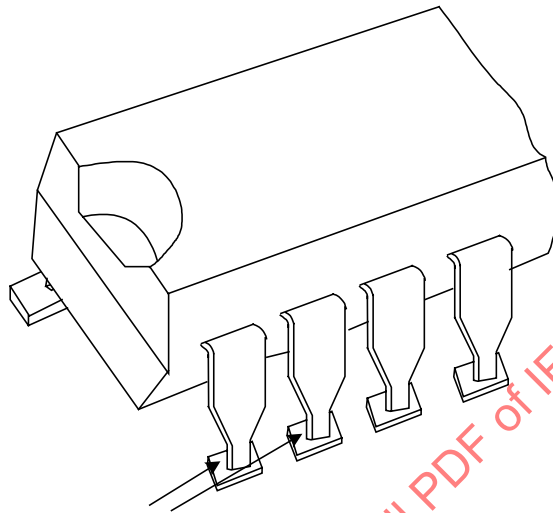
No device shall be acceptable that exhibits:

Class H

- a) A fillet of solder with inadequate wetting (see 9.1) of either lead or pad to less than 50 % of the available wetted area of a round or flat lead (see figure 71).

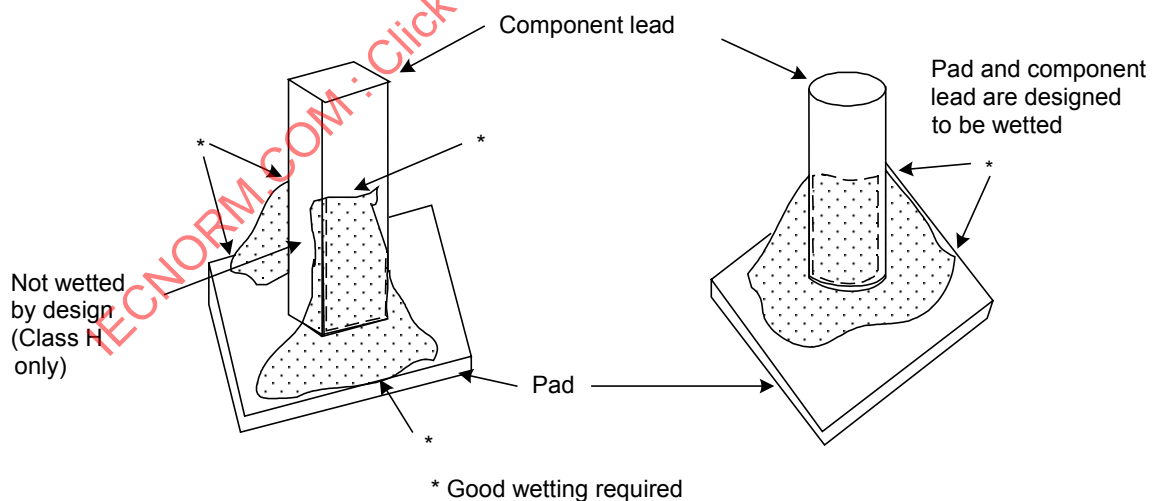
Class K

- a) A fillet of solder with inadequate wetting (see 9.1) of either lead or pad to less than the available wetted area of a round or flat lead (see figure 71).



Edges of leads may not solder due to lack of plating
(Edges not part of available wetted area) – Class K only.

Class K lead edges must be suitably tinned to enable wetting



IEC 1031/02

Figure 71 – Dual-in-line package leads solder wetting

Class H

- b) Less than 50 % registration of the lead to pad (the requirements of 9.1 shall nevertheless be met) (See figure 72).

Class K

- b) Less than 100 % registration of the lead to pad (the requirements of 9.1 shall nevertheless be met) (see figure 72).

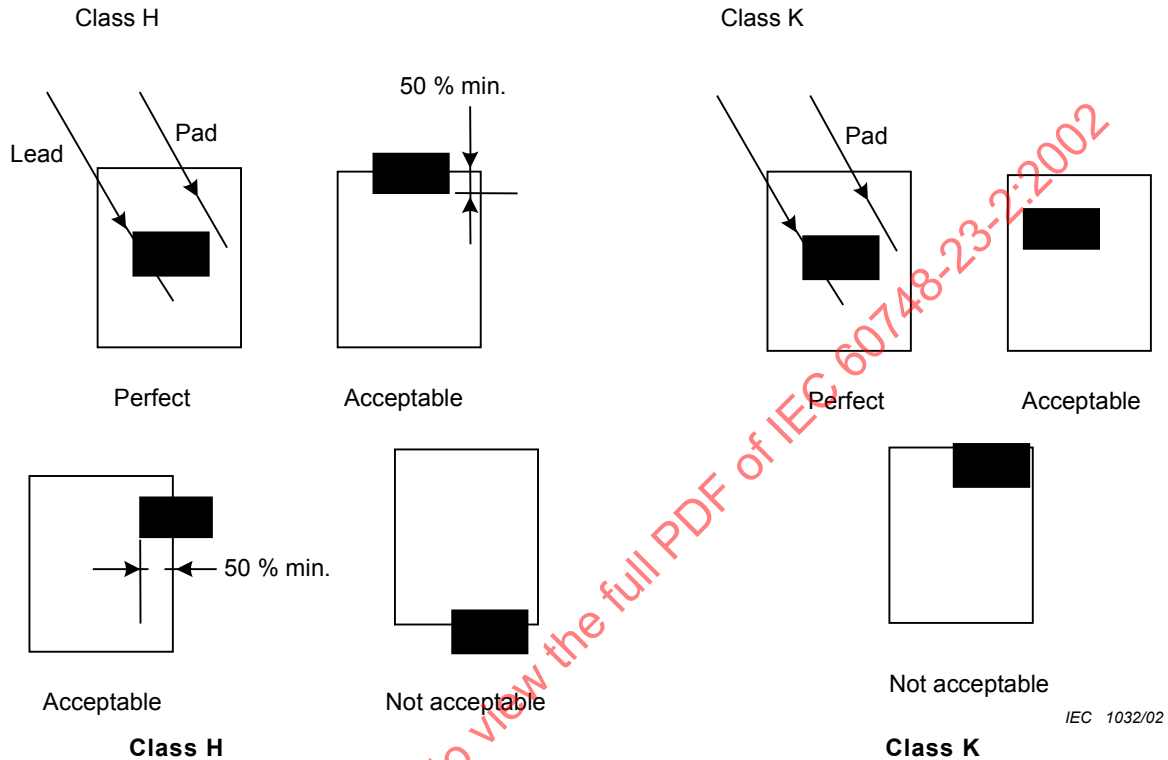


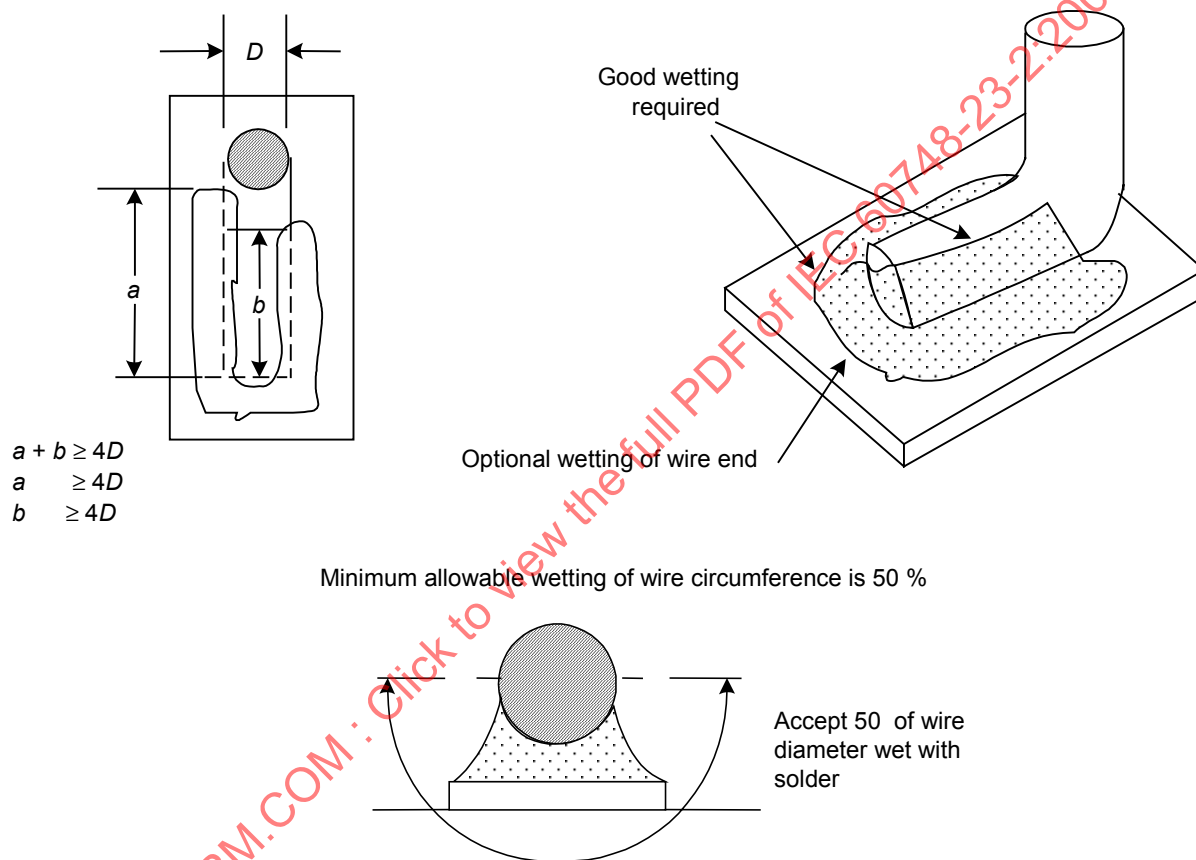
Figure 72 – Lead to pad registration

9.5 Axial and radial leaded components (lap joints)

The following requirements apply to any component or flying leads that are attached by lap joints.

No device shall be acceptable that exhibits:

- a) Solder wetting of less than four wire diameters on both sides of the length of circular cross-section leaded components adding together the visible length down each side but not including the end which does not need to be wetted. (Each side shall have at least one wire diameter's length of good wetting). The profile of the component termination shall be visible through the solder coating (see figure 73).



IEC 1033/02

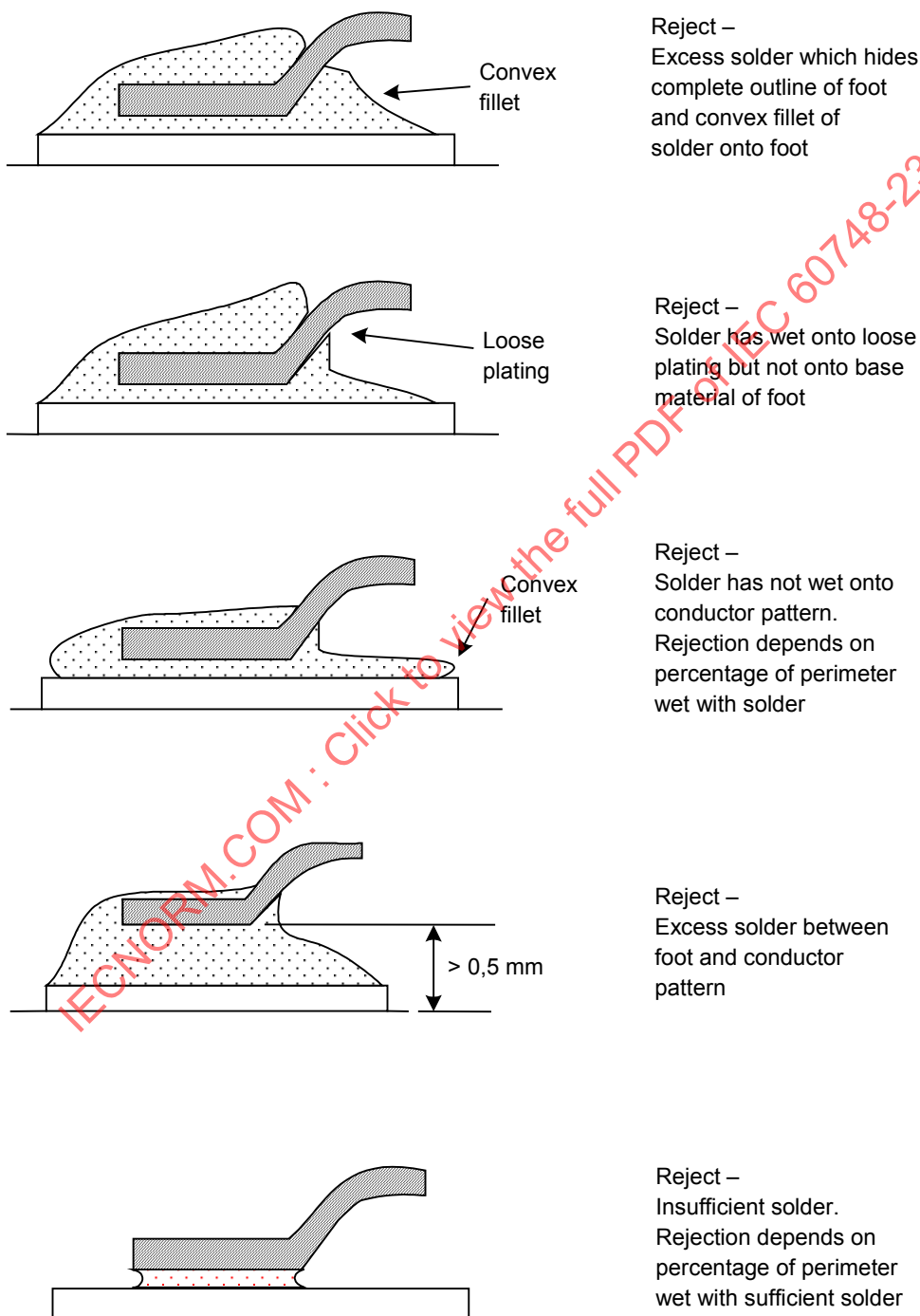
Figure 73 – Lap joint solder wetting

9.6 Components with feet (combined butt and lap joints)

The following requirements apply to components with ribbon tracks with formed feet such as SOT23 transistors, SO packaged ICs and leaded chip carriers. They also apply to larger components such as connectors and relays which have had feet formed on the end of their leads.

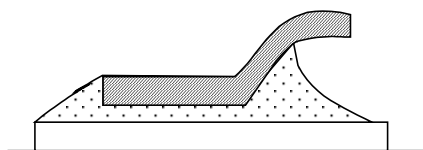
No device shall be acceptable that exhibits:

a) The fillet criteria depicted in figure 74 (acceptable joints are shown in figure 75).

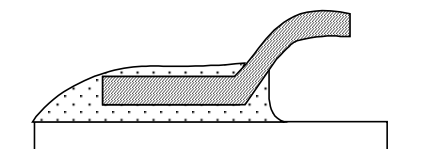


IEC 1034/02

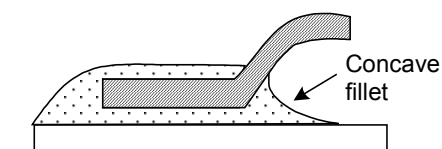
Figure 74 – Combined butt and lap joints solder wetting – Reject



Accept –
Ideal joint. Good
wetting and correct
amount of solder



Accept –
Typical joint with
outline of foot just
discernible. Good
wetting



Accept –
Excess solder which
hides complete outline
of foot but joint is
acceptable because of
concave fillet onto foot

IEC 1035/02

Figure 75 – Combined butt and lap joints solder wetting – Accept

Class H

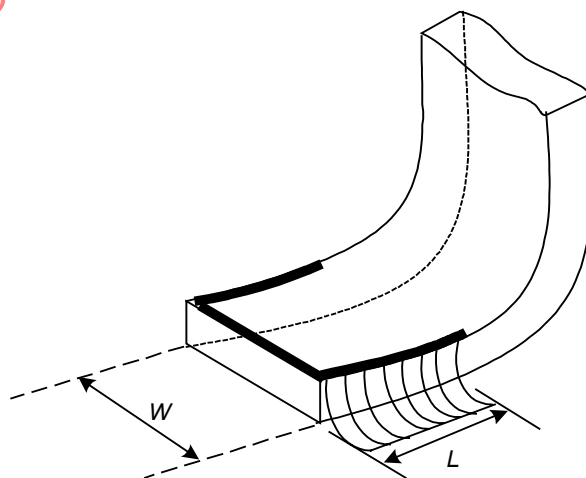
- b) Leads where the total solder fillet does not run along all faces solderable by design for a minimum of 75 % overall and a minimum of 50 % of each of these faces (see figure 76).

Class K

- b) Leads where the total solder fillet does not run along the whole of all faces solderable by design (see figure 76).

Class H

Solder fillet must run along 50 % (min.) of W and 50 % (min.) of L on both sides and 75 % overall. Edges, such as W which may have been cropped and do not solder due to lack of solderable plating, may be considered not to be solderable by design



Class K

Solder fillet must run along the whole of W and the whole of L on both sides

IEC 1036/02

Figure 76 – Solder fillet coverage criteria

9.7 Leadless chip carriers

No device shall be acceptable which exhibits:

Class H

- a) Package placement that reduces the isolation between adjacent pads to less than 250 μm or 50 % of the design space whichever is less (overhang of the chip carrier terminal to substrate pad shall not exceed 50 % of the lead out.
- b) Inadequate solder wetting (see 9.1) on either the substrate pad or the visible portion of the chip carrier package terminal (although the main solder terminal of the chip carrier is on the underside when attached to the substrate there shall still be a visible solder fillet between the substrate solder pad and the visible perpendicular chip carrier terminal).

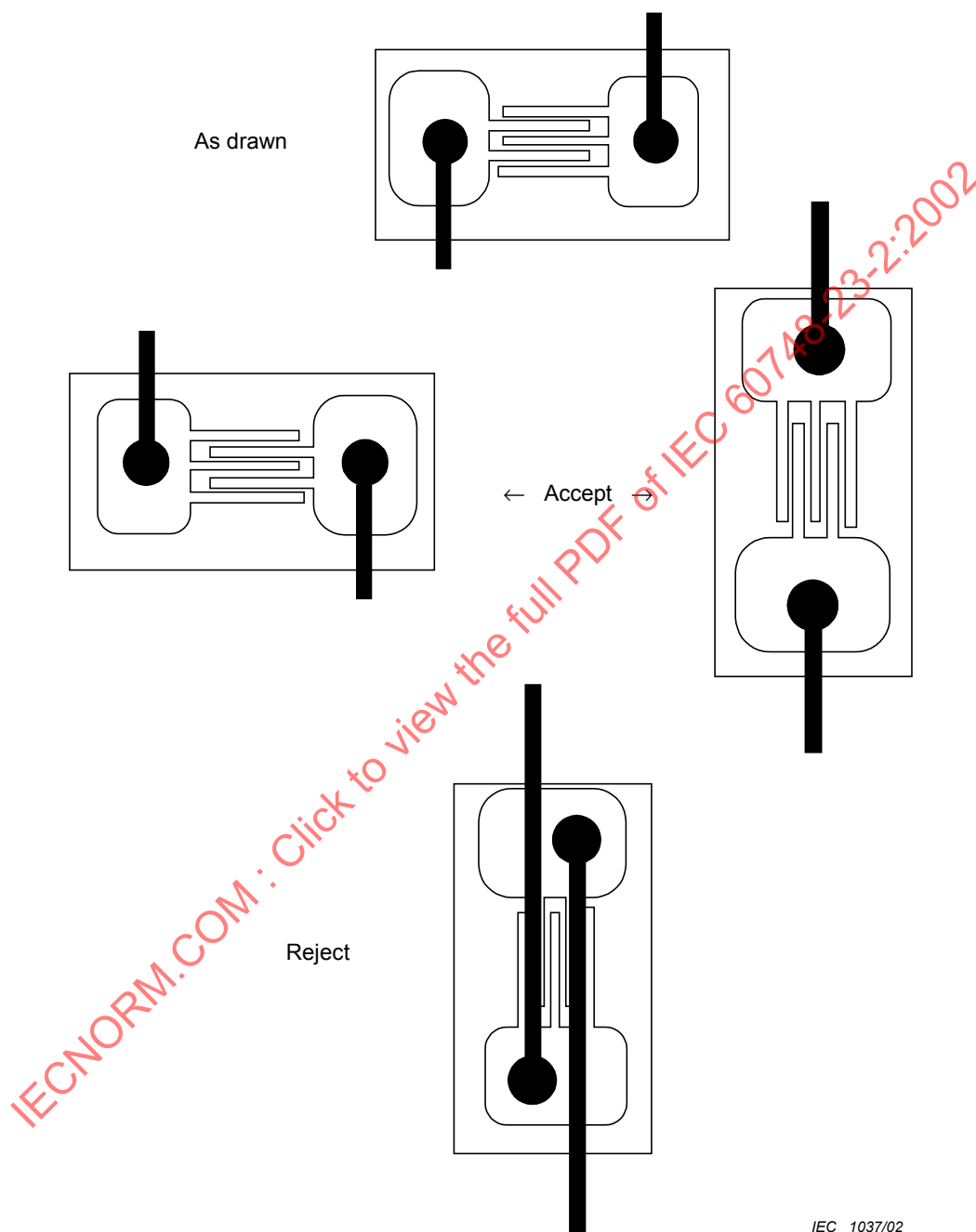
Class K

- a) Same as Class H.
- b) Inadequate solder wetting (see 9.1) on either the substrate pad or the visible portion of the chip carrier package terminal (although the main solder terminal of the chip carrier is on the underside when attached to the substrate there shall still be a visible solder fillet extending to at least 50 % of the available metallization path of each terminal).

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10 Element orientation

Elements not located or oriented in accordance with the applicable assembly drawing of the device are not acceptable. Elements whose bond and electrical configuration is symmetrical may be rotated unless otherwise stated in the assembly drawings (see figure 77).



IEC 1037/02

Figure 77 – Acceptable symmetrical element orientation

11 Separation

Elements shall not overhang the edge of the substrate. A minimum clearance of 25 μm shall be maintained between any uninsulated portion of the element and any non-common conductive surface.

12 Bond inspection, magnification 30× to 60×

The following shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above.

NOTE Wire tail is not considered part of the bond when determining physical bond dimensions.

12.1 Ball bonds

No device shall be acceptable that exhibits:

- a) ball bond diameter less than 2,0 times or greater than 5,0 times the wire diameter;
- b) ball bonds where the wire exit is not completely within the periphery of the ball;
- c) ball bonds where the wire centre exit is not within the boundaries of the bonding site.

12.2 Wire wedge bonds

No device shall be acceptable that exhibits (see figure 78):

- a) ultrasonic and thermosonic wedge bonds that are less than 1,0 times or greater than 3,0 times the wire diameter in width or less than 0,5 times the wire diameter in length or no evidence of tool impression;
- b) devices with thermocompression wedge bonds that are less than 1,2 times or greater than 3,0 times the wire diameter in width or less than 0,5 times the wire diameter in length or no evidence of tool impression.

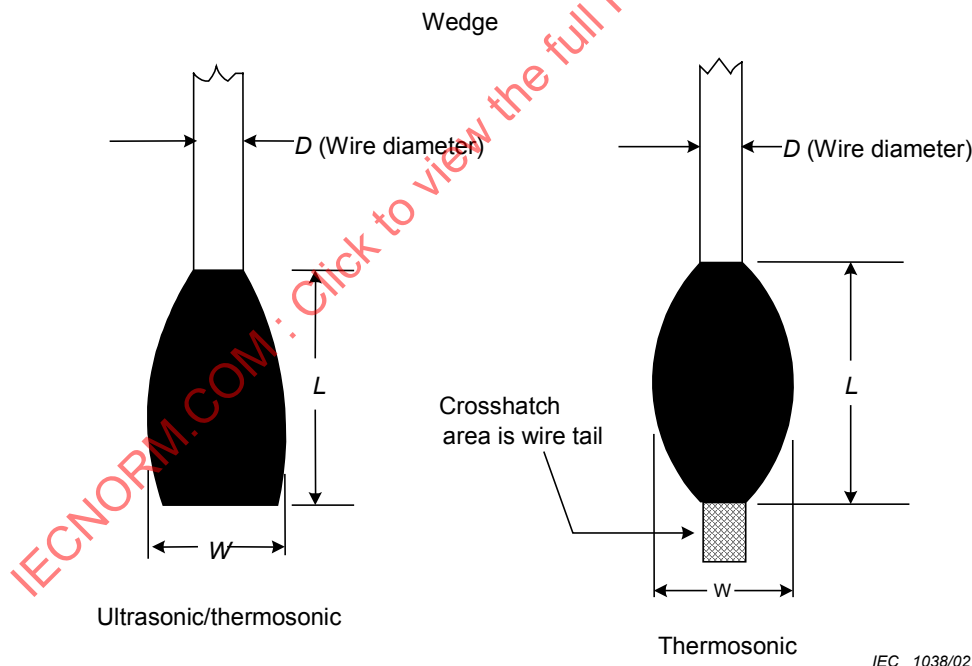


Figure 78 – Bond dimensions

NOTE 1 These criteria are not mandatory for wire bonds of diameters 100 µm and above which are used for applications such as power hybrids.

For wedge bonds of 100 µm diameter and above, the full impression of the bonding tool shall be evident on the surface of the bond.

NOTE 2 The heavy gauge wire used in power applications may use a wedge with an unconventional shape, which may affect the deformation characteristic of the wire during wire-bond operations.

12.3 Tailless bonds (crescent)

No device shall be acceptable that exhibits:

- tailless bonds that are less than 1,2 times or greater than 5,0 times the wire diameter in width (see figure 79);
- a tailless bond of a gold wire bonded on the aluminium pads of a die.

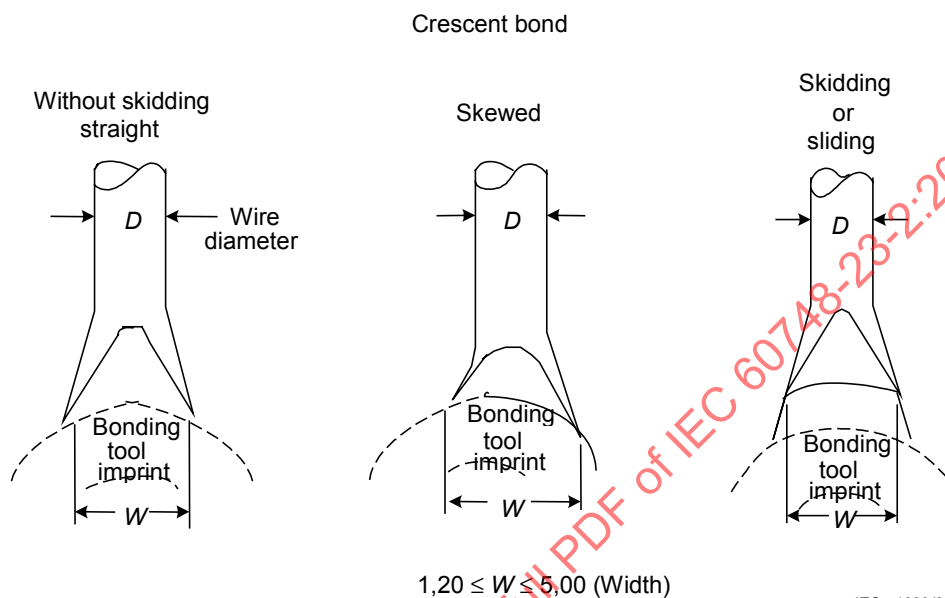


Figure 79 – Bond dimensions

12.4 Compound bond

No device shall be acceptable that exhibits the following:

- one bond used to secure two common wires (see figure 80);

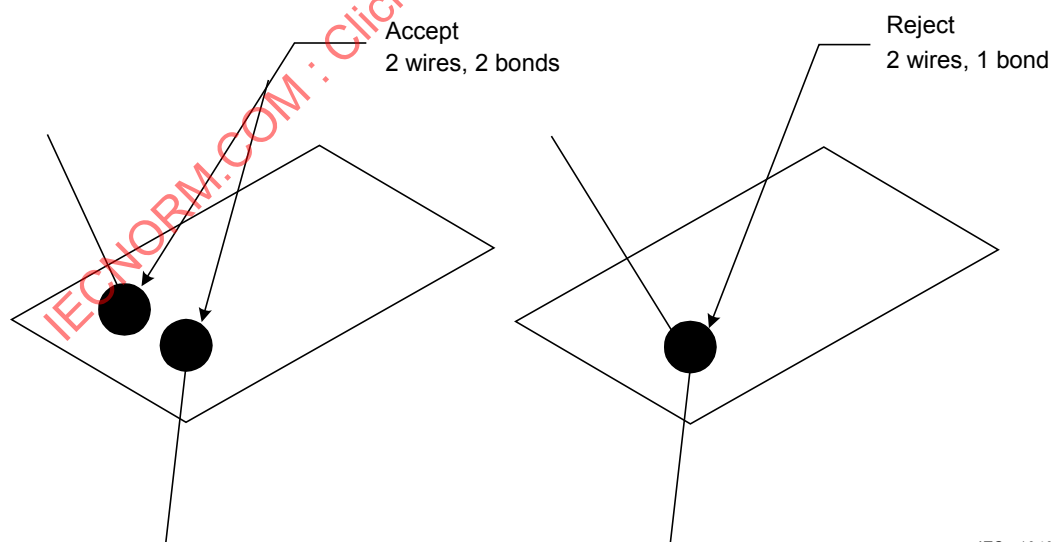


Figure 80 – One bond used to secure two common wires

- b) more than one bond on top of original bond;

NOTE When required by design and based on a justifiable technical need, and with the approval of the qualifying or acquiring activity, additional compound bonds may be allowed in addition to the limitations of a) and b) above. Demonstration of acceptable N+1 bond stacks (N = maximum number of compound bonds allowable by the manufacturer's process) and establishment of necessary process controls will be required for approval.

- c) compound bond where the contact area of the second bond with the original bond is less than 75 % of the bottom bond;
- d) non-monometallic compound bond (i.e. between dissimilar metals, excluding the bond pad metallization).

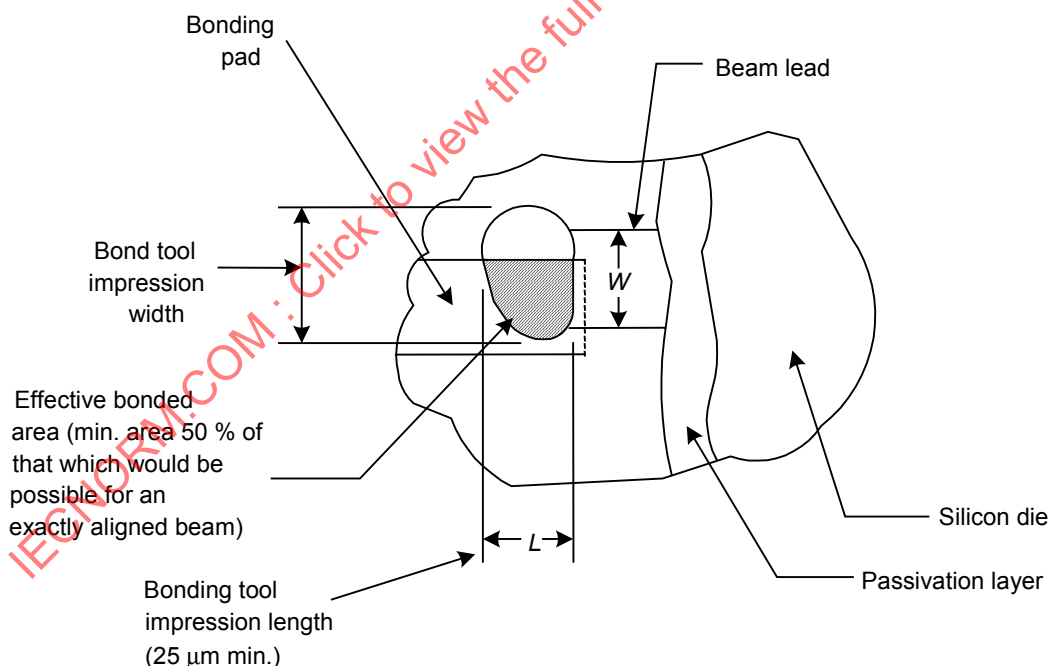
12.5 Beam lead

This inspection and criteria shall apply to the completed bond area made using direct tool contact. No device shall be acceptable that exhibits:

- a) bonds which do not exhibit 100 % bond/weld impression(s) across the width of the beam lead;

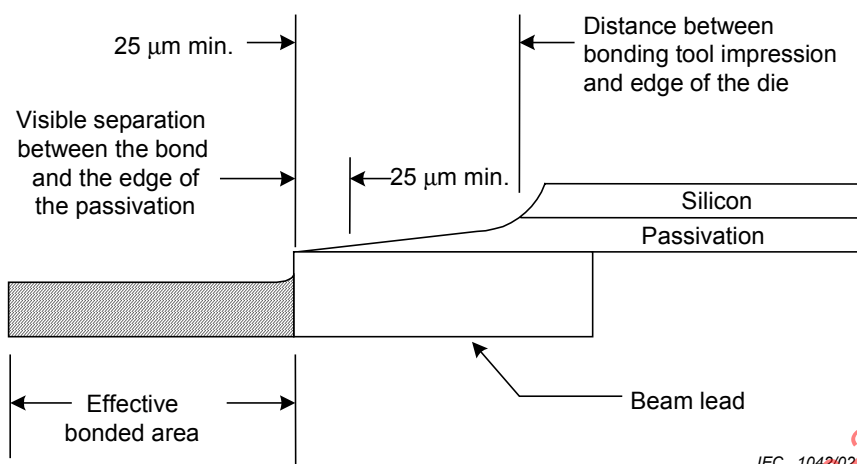
NOTE Gaps between bonds/welds on the beam lead caused by the natural footprint of a bond/weld tip (e.g. split tip, etc.), are acceptable provided the total of all gaps does not exceed 25 % of the beam lead width.

- b) complete or partial beam separation from the die;
- c) bonds on the substrate where the tool impression is not visible on the beam;
- d) beam lead width increased by greater than 60 % of the original beam width;
- e) bonds where the tool impression length is less than 25 μm (see figures 81a and 81b);

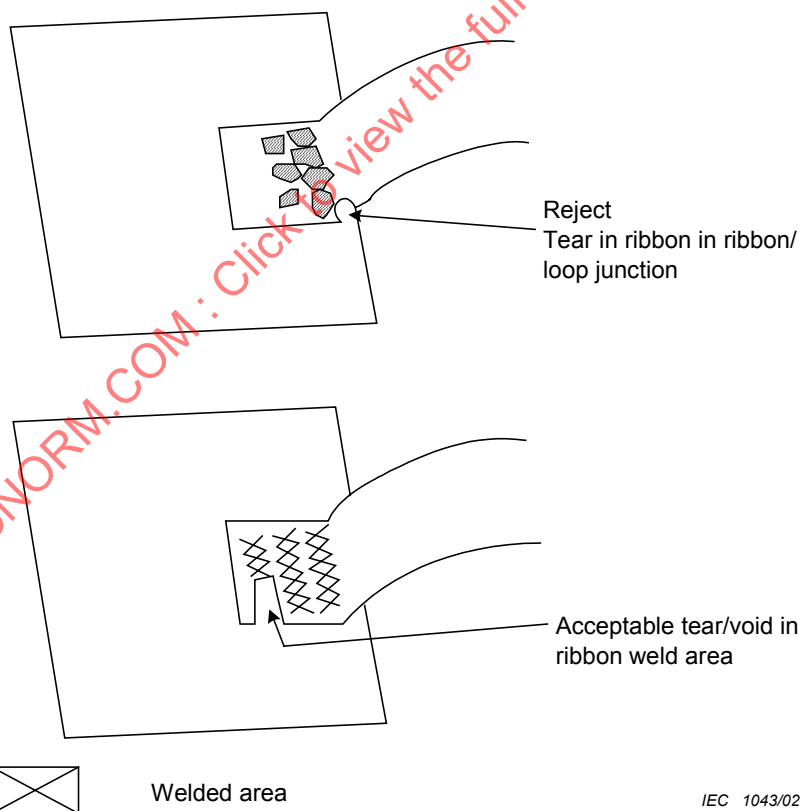


IEC 1041/02

Figure 81a – Beam lead area and location

**Figure 81b – Beam lead area and location****Figure 81 – Beam lead**

- f) bonding tool impression less than 25 µm from the die edge (see figures 81a and 81b);
- g) effective bonded area less than 50 % of that which would be possible for an exactly aligned beam (see figures 81a and 81b);
- h) any tears in the beam lead between the bond junction nearest the die body and the die or in the bonded area of the beam lead within a distance equal to 50 % of the beam lead width (see figure 82);

**Figure 82 – Acceptable/rejectable tears or voids in ribbon weld area**

- i) an absence of visible separation between the bond and the edge of the passivation layer (see figure 81b);
- j) an absence of visible separation between a beam lead and non-electrically-common metallization. This criterion applies for both glassivated and unglassivated metallization.

12.6 Mesh bonding

No device shall be acceptable that exhibits the following:

- less than 50 % of the bond is on substrate metallization;
- the number of continuous strands along the mesh is less than 50 % of lengthwise strands through each section (see figure 83);
- less than two continuous conducting paths through a bond (see figure 84).

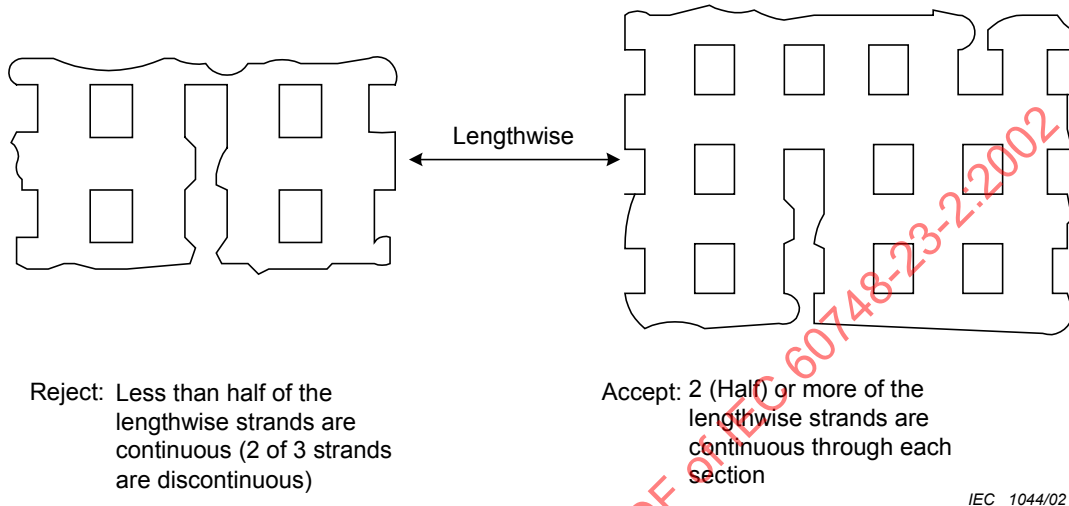


Figure 83 – Criterion for strands along the mesh

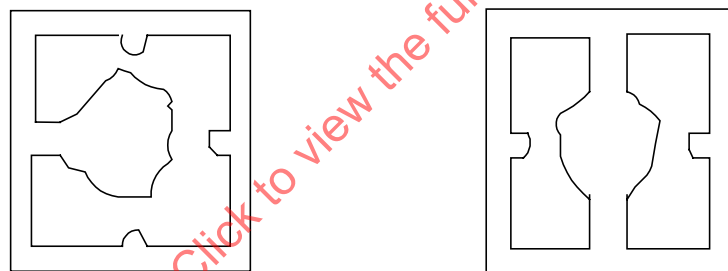


Figure 84 – Criterion for continuous conducting paths

12.7 Ribbon bonds

No device shall be acceptable that exhibits the following:

- any tears in the ribbon at the junction between the ribbon loop and bond/weld;
- bonds which do not exhibit 100 % bond/weld impression(s) across the width of the ribbon overlapping underlying metallization;

NOTE Gaps between welds on the ribbon caused by the natural footprint of a weld tip (e.g. split tip, etc.) are acceptable provided the total of all gaps does not exceed 25 % of the ribbon width.

- effective bonded area less than 50 % of that which would be possible for an exactly aligned ribbon;
- bond tails longer than one ribbon width or 250 μm , whichever is less, or bridging adjacent metallization;
- the unbonded end of a ribbon bond tuning stub longer than one ribbon width or 250 μm , whichever is less, that is not secured by polymer adhesive.

12.8 General

No device shall be acceptable that exhibits:

Class H

- a) Bonds on the die where less than 50 % of the bond is within the unglassivated bonding site.

Class K

Monometallic bonds on the die where less than 50 % of the bond is within the unglassivated bonding site. Bimetallic bonds on the die where less than 75 % of the bond is within the unglassivated bonding site.

- b) Bonds on the package post or substrate that are not completely within the bonding site.

NOTE For cases where the substrate bonding site is smaller than 1,5 times the minimum bond size, bonds on the substrate where less than 50 % of the bond is within the bonding site are not acceptable.

- c) Bonds placed so that the wire exiting from a bond crosses over another bond, except by design, in which case the clearance shall be 2,0 wire diameters minimum (common bonds are excluded from this criterion).
- d) An absence of a visible line of separation between non-electrically-common bonds.
- e) An absence of a visible line of separation between a bond and non-electrically-common metallization. This criterion applies to both glassivated and unglassivated metallization.
- f) Wire bond tails that extend over or make contact with any non-common, unglassivated active metal.
- g) Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.
- h) Bonds on element attach media or on contaminated or foreign material.
- i) Any lifted or peeling bond.
- j) Intermetallic formation extending completely around the metallic interface of any bond between dissimilar metals.
- k) Wedge or crescent bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe.

NOTE 1 The criterion of 12.8 k) can be excluded when the entering conductor is $>50\text{ }\mu\text{m}$ in width and the bond pad dimension on the entering conductor side is $>90\text{ }\mu\text{m}$.

NOTE 2 For Class H only, the requirements for a visible line of metal can be satisfied when an acceptable wire tail obscures the area of concern, provided the following condition exists:- the bond is located more than $0,25\text{ }\mu\text{m}$ from the intersecting line of the entering metallization stripe and the bonding pad and there is no visual evidence of disturbed pad metallization at the bond and wire tail interface.

NOTE 3 The criterion of 12.8 k) is not applicable to interdigitated (Lange) couplers or when the interface between a thermosonic/ultrasonic (i.e. non-thermocompression) bond and underlying metal is monometallic.

- l) Polymeric adhesive which may be material or residue as evidenced by discoloration within $125\text{ }\mu\text{m}$ of the outer periphery of a wire bond.
- m) Tearing at the junction of the wire and bond. The junction is the line of deformation of the wire at the bonding site.

13 Internal leads (e.g. wires, ribbons, beams, wire loops, ribbon loops, beams, etc.) – "magnification 10x to 60x"

No device shall be acceptable that exhibits:

- a) Within the first $125\text{ }\mu\text{m}$ of wire from the die surface for ball bonds, or $250\text{ }\mu\text{m}$ for wedge bonds, any wire that comes closer than $25\text{ }\mu\text{m}$ to any non-common conductive surface (e.g. unglassivated operating metallization, unpassivated edge of conductive die).

NOTE Insulated wires and electrically common wires are excluded from this criterion.

- b) After the first 125 μm of wire from the die surface for ball bond(s), or 250 μm for wedge bonds, any wire that comes closer than two wire diameters to any non-common, uninsulated conductive surface (e.g. unglassivated operating metallization, unpassivated edge of conductive die).

NOTE Insulated wires and electrically common wires are excluded from this criterion.

- c) Nicks, cuts, crimps, scoring, sharp bends, or neck-down in any lead that reduces the lead diameter/width by more than 25 %.
- d) Missing or extra lead(s) not in conformance with bonding diagram.

NOTE Leads designated for tuning on the bonding diagram are excluded.

- e) Any lead making a straight line run from bond to bond that has no arc, unless specifically allowed by the bonding diagram.

NOTE This exception also applies to wires of 100 μm diameter or greater, such as those used for power hybrids, where formation of an arc may not be possible.

- f) Wire(s) crossing wire(s) with a separation of less than two lead widths. Common or insulated conductors and insulated wires are excluded.
- g) Complete or partial separation of the lead from the body of the element.
- h) Excessive loop height such that the wire would contact the lid when it is installed.

14 Screw tabs and through-hole mounting - magnification 3 $\times$ to 10 $\times$

No device shall be acceptable that exhibits:

- a) misaligned tabs;
- b) missing or broken tabs;
- c) cracks emanating from mounting holes;
- d) loose substrates;
- e) missing or loose screws.

15 Connector and feedthrough centre contact soldering - magnification 10 $\times$ to 30 $\times$

No device shall be acceptable that exhibits:

- a) less than 50 % of centre contact overlaps onto metallized pattern (see figure 85);
- b) centre contact to substrate protrudes over onto circuit less than 1 diameter of a round pin or the width of a flat pin (see figure 86);
- c) voids in solder (see figure 87a);
- d) cracked solder joint (see figure 87b);
- e) poor adhesion of solder to centre contact or substrate (see figure 87d);
- f) insufficient or excess solder (see figures 87c through 87e);
- g) less than full coverage of solder along the length of the centre contact and the metallization.