IEC 60749-37

Edition 2.0 2022-10
REDLINE VERSION

INTERNATIONAL STANDARD

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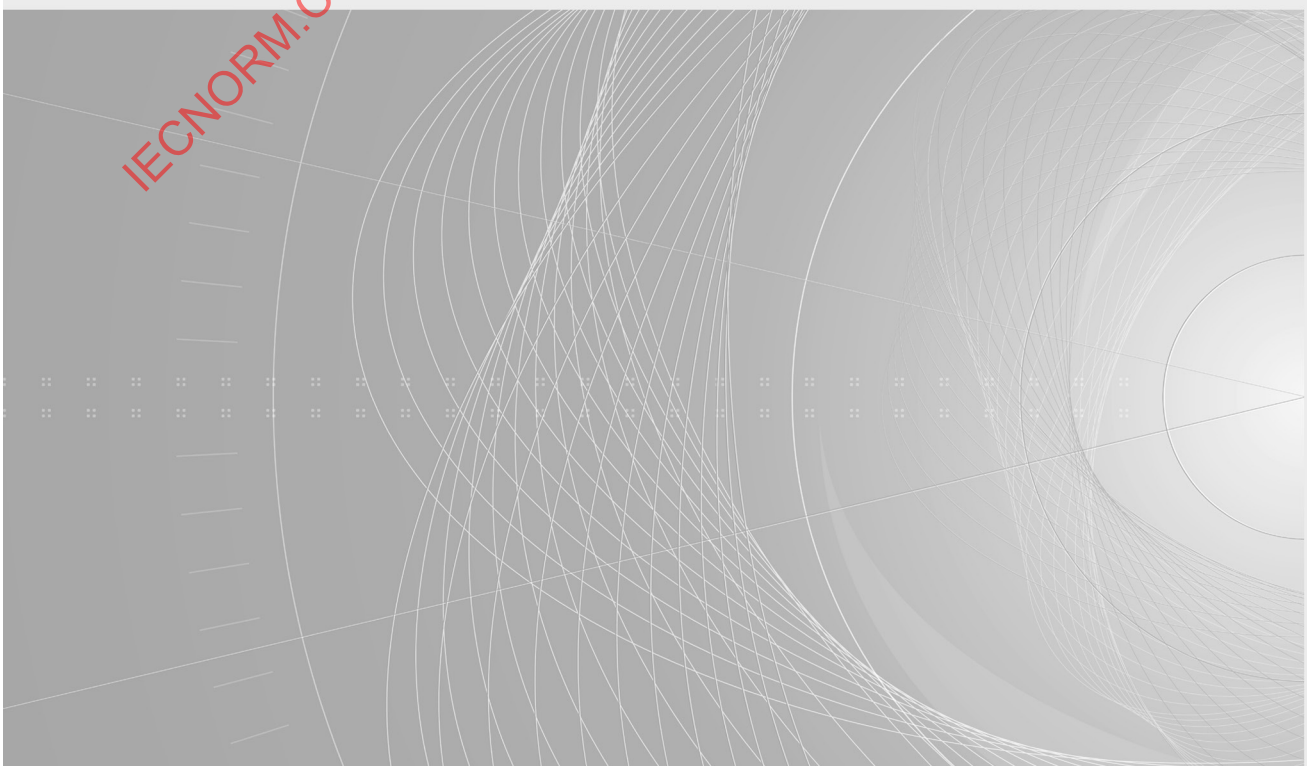
Semiconductor devices – Mechanical and climatic test methods – Part 37: Board level drop test method using an accelerometer



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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 37: Board level drop test method using an accelerometer

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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This redline version of the official IEC Standard allows the user to identify the changes made to the previous edition IEC 60749-37:2008. A vertical bar appears in the margin wherever a change has been made. Additions are in green text, deletions are in strikethrough red text.

IEC 60749-37 has been prepared by IEC technical committee 47: Semiconductor devices. It is an International Standard.

This second edition, based on JEDEC document JESD22-B111A, cancels and replaces the first edition published in 2008. It is used with permission of the copyright holder, JEDEC Solid State Technology Association. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) correction of a previous technical error concerning test conditions;

b) updates to reflect improvements in technology.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2651/CDV	47/2719/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts of the IEC 60749 series, under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found in the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

Handheld electronic products fit into the consumer and portable market segments. Included in handheld electronic products are cameras, calculators, cell phones, cordless phones, pagers, palm size PCs, personal computer memory card international association (PCMCIA) cards, smart cards, personal digital assistants (PDAs) and other electronic products that can be conveniently stored in a pocket and used while held in user's hand.

These handheld electronic products are more prone to being dropped during their useful service life because of their size and weight. This dropping event can not only cause mechanical failures in the housing of the device but also create electrical failures in the printed circuit board (PCB) assemblies mounted inside the housing due to transfer of energy through PCB supports. The electrical failures ~~may~~ sometimes result from various failure modes such as cracking of the circuit board, track cracking on the board, cracking of solder interconnections between the components and the board, and component cracks. The primary driver of these failures is excessive flexing of the circuit board due to input acceleration to the board created from dropping the handheld electronic product. This flexing of the board causes relative motion between the board and the components mounted on it, resulting in component, interconnect or board failures. The failure is a function of the combination of the board design, construction, material, thickness and surface finish; interconnect material and standoff height and component size.

Correlation between test and field conditions is not yet fully established. Consequently, the test procedure is presently more appropriate for relative component performance than for use as a pass/fail criterion. Rather, results ~~should~~ can be used to augment existing data or establish a baseline for potential investigative efforts in package/board technologies.

The comparability between different test sites, data acquisition methods, and board manufacturers has not been fully demonstrated by existing data. As a result, if the data are to be used for direct comparison of component performance, matching studies ~~must~~ will first be performed to prove that the data are in fact comparable across different test sites and test conditions.

This method is not intended to substitute for full characterization testing, which ~~might~~ could incorporate substantially larger sample sizes and increased number of drops. Due to limited sample size and number of drops specified here, it is possible that enough failure data ~~may~~ are not ~~be~~ generated in every case to perform full statistical analysis.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 37: Board level drop test method using an accelerometer

1 Scope ~~and object~~

This part of IEC 60749 provides a test method that is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface-mounted components while producing the same failure modes normally observed during product level test.

This document aims at prescribing a standardized test method and reporting procedure. This is not a component qualification test and is not meant to replace any system level drop test that ~~may be needed~~ is sometimes used to qualify a specific handheld electronic product. The standard is not meant to cover the drop test required to simulate shipping and handling-related shock of electronic components or PCB assemblies. These requirements are already addressed in test methods such as IEC 60749-10. The method is applicable to both area array and perimeter-leaded surface mounted packages.

This test method uses an accelerometer to measure the mechanical shock duration and magnitude applied which is proportional to the stress on a given component mounted on a standard board. The test method described in IEC 60749-40[1] uses strain gauge to measure the strain and strain rate of a board in the vicinity of a component. The ~~detailed~~ customer specification states which test method is to be used.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-10:~~2002~~2022, *Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock – Device and subassembly*

IEC 60749-20, *Semiconductor devices – Mechanical and climatic test methods – Part 20: Resistance of plastic-encapsulated SMDs to the combined effect of moisture and soldering heat*

IEC 60749-20-1, *Semiconductor devices – Mechanical and climatic test methods – Part 20-1: Handling, packing, labelling and shipping of surface-mount devices sensitive to the combined effect of moisture and soldering heat*[2]

[1] ~~Under consideration.~~

[2] ~~In preparation.~~

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

IEC Electropedia: available at https://www.electropedia.org/

ISO Online browsing platform: available at https://www.iso.org/obp

3.1
component
packaged semiconductor device

3.2
single-sided ~~PCB~~ assembly
printed circuit board assembly with components mounted on only one side of the board

3.3
double-sided ~~PCB~~ assembly
printed circuit board assembly with components mounted on top and bottom sides of the board

3.4
handheld electronic product
product that can conveniently be stored in a pocket (of sufficient size) and used when held in user's hand

Note 1 to entry: Handheld electronic products include cameras, calculators, cell phones, pagers, palm-size PCs (formerly called 'pocket organizers'), personal computer memory card international association (PCMCIA) cards, smart cards, mobile phones, personal digital assistants (PDAs) and other communication devices.

3.5
peak acceleration
maximum acceleration during the dynamic motion of the test apparatus

3.6
pulse duration
acceleration interval
time interval between the instant when the acceleration first reaches 10 % of its specified peak level and the instant when the acceleration first returns to 10 % of the specified peak level after having reached that peak level

3.7
table drop height
free-fall drop height of the drop table needed to attain the prescribed peak acceleration and pulse duration

3.8
event
electrical discontinuity of resistance greater than 1 000 Ω lasting for 1 µs or longer

3.9
event detector
continuity test instrument capable of detecting electrical discontinuity of resistance greater than 1 000 Ω lasting for 1 µs or longer

4 Test apparatus and components

4.1 Test apparatus

The shock-testing apparatus shall be capable of providing shock pulses up to a peak acceleration of 2 900 $m \cdot s^{-2}$ with a pulse duration between 0,3 ms and 8,0 ms to the body of the device and a velocity change of ~~710 $mm \cdot s^{-1}$~~ 1 250 $mm \cdot s^{-1}$ to 5 430 $mm \cdot s^{-1}$. For free-state testing, a velocity change of 1 250 $mm \cdot s^{-1}$ to 5 430 $mm \cdot s^{-1}$ and a pulse duration between 0,3 ms and 2,0 ms is sufficient. Conversely, for mounted-state testing, apparatus capable of a velocity change of 1 000 $mm \cdot s^{-1}$ to 5 430 $mm \cdot s^{-1}$ and a pulse duration between 5,0 ms and 8,0 ms to the body of the component is sufficient.

The acceleration pulse shall be a half-sine waveform with an allowable deviation from specified peak acceleration level not greater than ± ~~20 %~~ 10 % ~~of the specified peak acceleration~~. ~~This is determined by a transducer having a natural frequency 5 times the frequency of the shock pulse being established and measured through a low pass filter having a band width preferably at least 5 times the frequency of the shock pulse being established. It is very important that the transducer resonance does not approach the measured value. Filtering should not be used in lieu of good measurement set-up and procedure practices. The pulse duration shall be measured between the points at 10 % of the peak acceleration during rise time and 10 % of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be ±30 % of the specified duration. It is recommended that the test velocity change should be ±10 % of the specified level.~~ The test velocity change shall be ±10 % of the specified level. The pulse duration shall be measured between the points at 10 % of the peak acceleration during rise time and 10 % of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be ±15 % of the specified duration. The test equipment transducer shall have a natural frequency greater than 5 times the frequency of the shock pulse being established, and measured through a low-pass filter having a bandwidth greater than 5 times the frequency of the shock pulse being established. Filtering shall not be used in lieu of good measurement setup and procedure practices.

Appropriate equipment calibration shall be carried out prior to any testing.

4.2 Test components

This document covers all area arrays and perimeter-leaded surface-mountable packaged semiconductor devices such as ball grid arrays (BGA), land grid arrays (LGA), chip scale packages (CSP), thin small outline packages (TSOP) and quad flat no-lead packages (QFN) typically used in handheld electronic product. The maximum size of the component body covered in this document is 15 mm x 15 mm in general. A larger body size may be used for a special board layout as described in detail in 4.3. All components used for this testing ~~must~~ shall be daisy-chained. The daisy chain ~~should either be~~ is made at the die level or by providing daisy chain links at the lead-frame or substrate level. In case of non-daisy chain die, a mechanical dummy die shall be used inside the package to simulate the actual structure of the package. The die size and thickness ~~should~~ shall be similar to the functional die size to be used in application. The component materials, dimensions and assembly processes shall be representative of typical production device.

4.3 Test board

Since the drop test performance is a function of the test board used for evaluation, this document describes a preferred test board construction, dimensions, and material that is representative of those used in handheld electronic products. If another board construction/material better represents a specific application, the test board construction, dimensions and material ~~should~~ shall be documented. The test data generated using such a board shall be correlated at least once by generating the same data on the same component using the preferred board defined in this document (see Annex A for recommendations).

4.4 Test board assembly

Prior to board assembly, all devices shall be inspected for missing balls or bent leads. Board thickness, warpage and pad sizes shall also be measured using a sampling plan. A visual inspection shall be performed on all boards for solder mask registration, contamination and daisy chain connection. It is recommended that boards ~~should~~ be inspected and accepted in accordance with a relevant national or international standard. One board shall also be used to measure the mechanical properties (modulus and glass transition temperature, T_g) of the board at the component location using dynamic mechanical analysis (DMA) and thermomechanical analysis (TMA) methods. It is highly recommended that the coefficient of thermal expansion (CTE) of the board be also measured in X, Y and Z direction. The mechanical property measurements are not required for every board lot, unless the fabrication process, material or vendor is changed from lot to lot.

The components shall be baked according to IEC 60749-20 and ~~the future~~ IEC 60749-20-1 prior to board assembly. The test boards shall be assembled using best known methods of printed circuit assembly process, representative of production methods. At least one board shall be used to adjust the board mounting process such as paste printing, placement and reflow profile. All assemblies shall be single-sided only, unless the component is anticipated for use in mirror-sided board assemblies. In that case, the components shall be mounted on each side of the board.

A 100 % X-ray inspection is recommended on assembled units to check for voids, short-circuits and other abnormalities. Electrical continuity test shall also be performed on all mounted units to detect any open-circuits or short-circuits.

4.5 Number of components and sample size

~~The board design recommended in Annex A allows up to 15 locations for component mounting and it is preferred that components be mounted on all 15 locations. Since the drop performance is a function of component location on the board, testing with components mounted on all 15 locations will provide useful information to the users of this data in proper layout of their product board. With the board supported at four corners, these locations cover the worst case board curvature (U8 location), the effect of proximity to support locations (U1, U5, U11, and U15 locations) and various locations in between. Because of various designs for tests, and designs for failure analysis practices used in the industry, it is recognized that populating boards with all 15 locations may not leave enough room between components for a large number of test points to properly identify the exact failure location. Therefore, options are provided for mounting just 1 or 5 components on the board using the following locations:~~

~~– 1-component configurations: location U8~~

~~– 5-component configurations: locations U2, U4, U8, U12, and U14~~

The board design recommended in Annex A allows 4 locations for component mounting and is recommended that all 4 components are mounted. Since the board is designed with full symmetry, all 4 components are expected to be subjected to the same drop performance and hereby the test results are treated as one single group. Statistical analysis on the data equivalence is suggested to ensure that variability in the component performance is insignificant before comprehensive data or full qualification is pursued. In order to get good statistically meaningful results, a total of 6 boards or 24 components are recommended as a minimum quantity per each design.

Since the number and size of the components mounted on the board ~~may~~ can influence the dynamic response of the test board assembly during drop, it is required that additional data ~~are~~ be provided whenever ~~these 1-component or 5-component configurations are~~ the 1-component configuration is employed. The additional data shall directly compare the effect of optional component mounting (1 ~~or 5~~ component case) to the preferred ~~15~~ 4-component mounting configuration. This comparison shall be provided for a component similar in size (within 20 % in both length and width) to the component, which has been tested using 1 ~~or 5~~-component per board configuration only.

~~Depending on the number of components mounted per board, Table 1 shall be used to determine the minimum quantity of assembled boards required for testing and the total number of components to be tested. Sample sizes greater than specified in Table 1 can be used to generate statistically sufficient data. In case of rectangular components, the longer side of the component should be parallel to the longer side of the board when mounted.~~

In the case of 1 component mount on the board, Table 1 shall be used to determine the minimum quantity of assembled board required for testing and total number of components to be tested. Sample sizes greater than specified below can also be used to generate statistically sufficient data.

Table 1 – Quantity of test boards and components required for testing

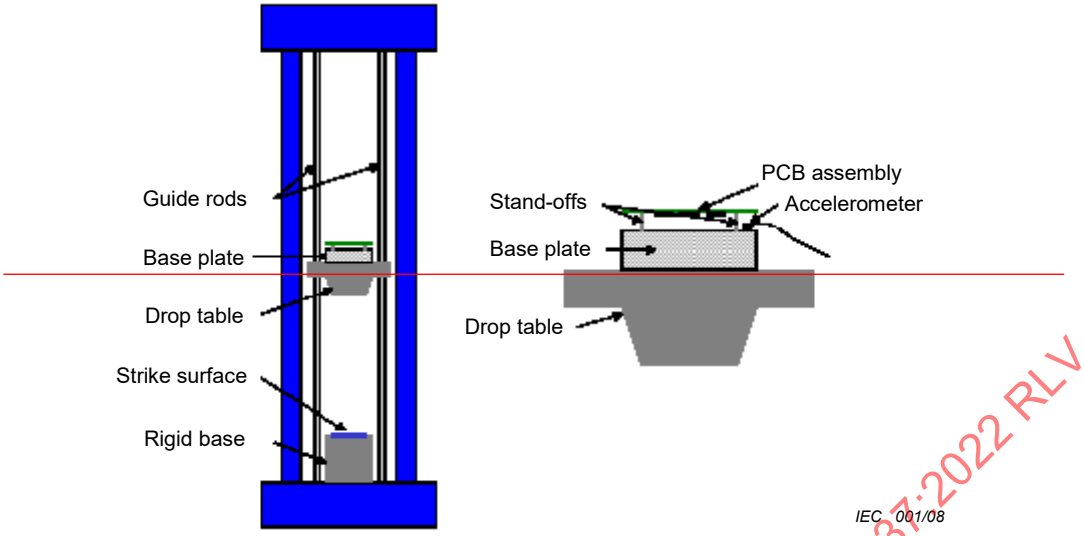
~~Number of components per board~~	~~Number of boards~~		~~Total number of components~~
	~~Side A assembly (via in pad)~~	~~Side B assembly (not via in pad)~~	
~~15~~	~~4~~	~~4~~	~~120~~
~~5~~	~~4~~	~~4~~	~~40~~
~~1~~	~~10~~	~~10~~	~~20~~

Number of components per board	Location	Number of boards		Total number of components
		Side A assembly (via in pad)	Side B assembly (not via in pad)	
4	U1, U2, U3 and U4	6	6	48
1	Centre of the board	16	16	32

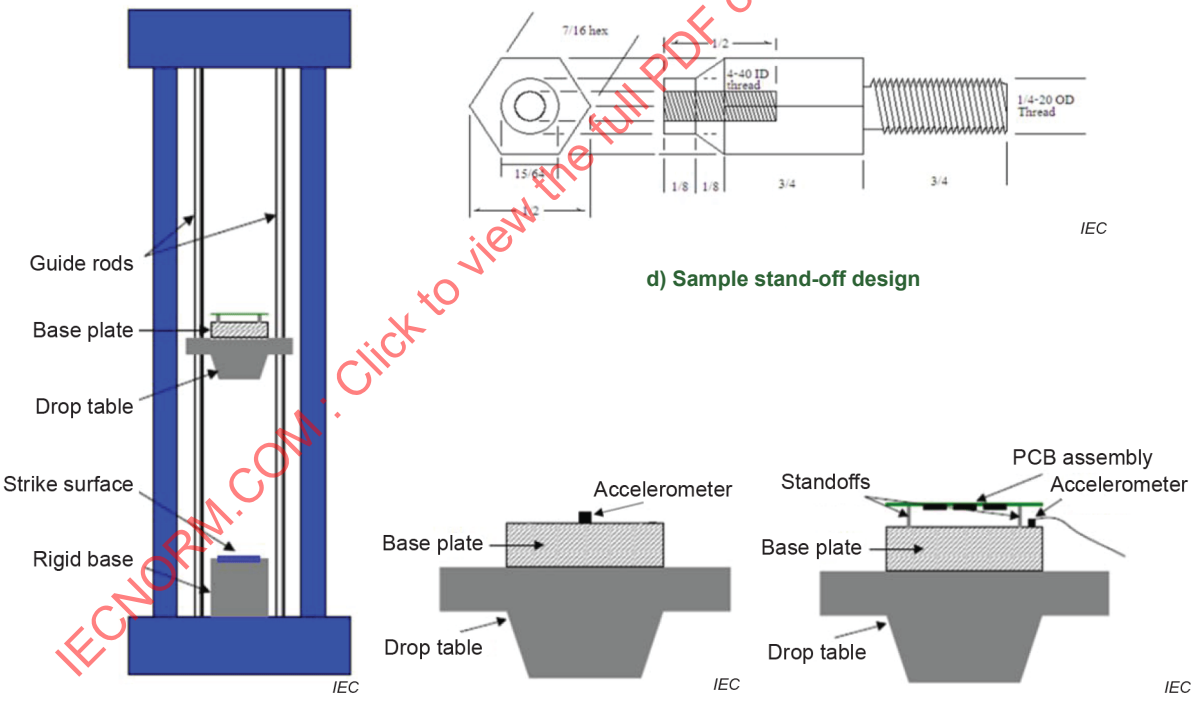
5 Test procedure

5.1 Test equipment and parameters

The shock testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and levelled before use. Means shall be provided in the apparatus (such as an automatic braking mechanism) to eliminate bounce and to prevent multiple shocks to the board. Figure 1 shows the typical drop test apparatus where the drop table travels down on guide rods and strikes the rigid fixture. The rigid fixture typically is covered with some form of material to achieve the desirable pulse and acceleration levels. The bottom of the drop table is usually rounded slightly to ensure a very small area of contact with the strike surface.



~~Figure 1 – Typical drop test apparatus and mounting scheme for PCB assembly~~



a) Typical drop test apparatus

d) Sample stand-off design

b) Pre-characterization set up without test board

c) Assembly set up with board

Figure 1 – Drop test apparatus detail

A base plate with suitable standoffs ~~(e.g. 6 mm hexagonal outside diameter / M3 × 0,5 inside diameter, 10 mm long)~~ shall be rigidly mounted on the drop table. The thickness and mounting locations of the base plate shall be selected such that there is no relative movement between the drop table and any part of base plate during drop testing. This plate will serve as the mounting structure for the PCB assemblies. This is pictorially shown in Figure 1. The PCB assembly shall be mounted to the base plate standoffs using four screws, one at each corner of the board. The board shall be mounted using four suitable precision shoulder screws (e.g. M3 × 0,5). Test data suggests that the variations in response acceleration and strain are

reduced significantly depending upon the choice of screw. Since the length of shoulder is nominal, a number of washers ~~should~~ shall be placed between the screw head and the top surface of the board (nominal 1,0 mm thick) to avoid any gap between the top of the standoffs and the bottom surface of the board. Due to tolerance stack up, a small gap is still possible but this gap shall not exceed 50 µm. The use of shoulder screw eliminates the need to re-tighten screws between drops. The screws shall be tightened in a diagonal pattern in the order of SW, NE, SE, and NW corners of the board. The screw shall be tightened until the shoulder of the screw bottoms out against the standoff. The number of washers used shall be the same for all four screws. A custom board jig may be used instead of mounting the board directly to the plate.

Experience with different board orientations has suggested that the horizontal board orientation with components facing down results in maximum PCB flexure and, thus, the worst orientation for failures. Therefore, this document requires that the board shall be horizontal in orientation with components facing in downward direction during the test. Drop testing using other board orientations is not required but may be performed if deemed necessary. However, this is an additional test option and not a replacement for testing in the required orientation.

This document requires test condition B (~~1 500~~ 15 000 m·s^{-2}, 0,5 ms duration, half-sine pulse), as listed in Table 1 of IEC 60749-10:2022, as the input shock pulse to the printed circuit assembly. This is the applied shock pulse to the base plate and shall be measured by accelerometer mounted at the centre of base plate or close to the support posts for the board. ~~Other shock conditions, such as 2 900 m·s^{-2}, 0,3 ms duration, in addition to the required condition can also be used.~~ The velocity change of the drop pulse shall be also controlled and maintained at 4,67 m/s. The calculation of the velocity change is defined by the effective pulse where the acceleration must be equal to or above 1 500 m·s^{-2} as shown in Figure 2. No rebounces are allowed in this calculation.

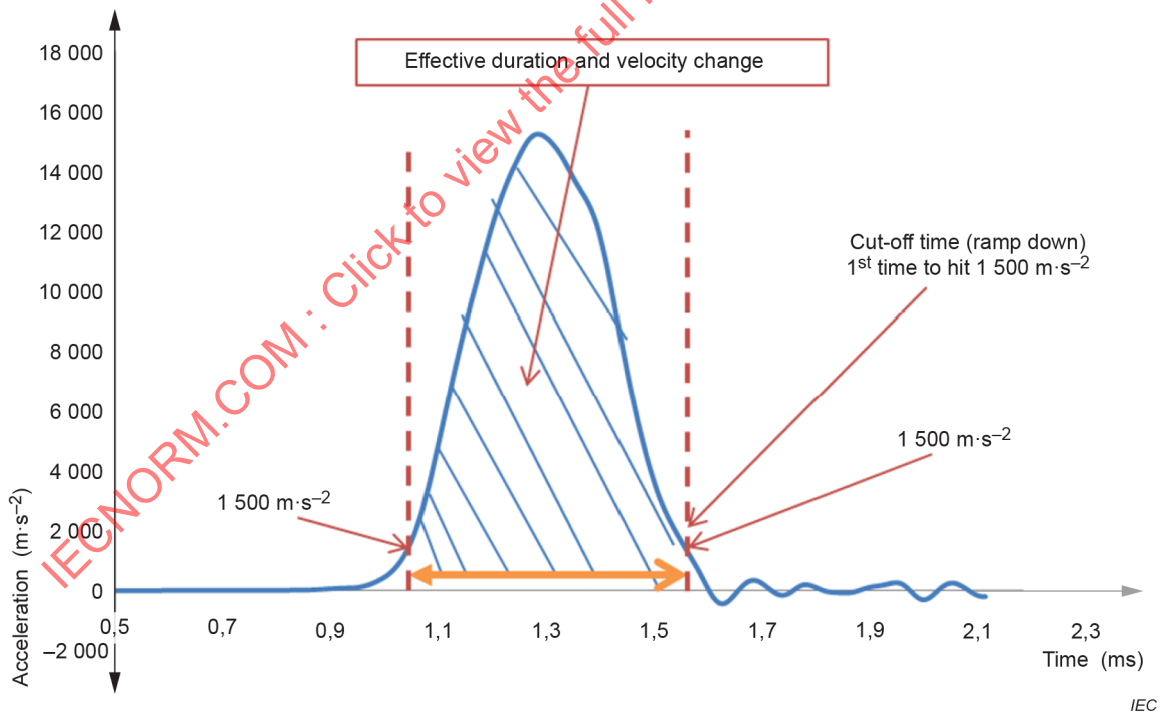


Figure 2 – Calculation of velocity change

5.2 Pre-test characterization

A set-up board with components mounted on it shall be used to adjust and characterize the drop test parameters and board response. ~~A lightweight accelerometer should be attached with beeswax (or equivalent adhesive) on top of the component located at position U8 to characterize the output acceleration response of the PCB assembly. It should be noted, however, that any additional mass will add significant dynamic weight to the board and may~~

~~alter its dynamic response. Therefore, it is recommended that this characterization should only be carried out on a set-up board. In addition, a 45 ° rectangular rosette strain gauge shall be mounted on this set-up board underneath position U8 on the other side (non-component) side of the board to characterize strains in the X and Y directions as well as the principal strain and principal strain angle.~~ A lightweight accelerometer is attached with (using suitable adhesive) in the centre of the mounting plate. Since the board weight is negligible as compared to mounting plate, setup characterization without a test board will not alter the results. Both the accelerometer and the strain gauge shall be connected to a data acquisition system capable of measuring at a scan frequency of 20 kHz and greater with a 16-bit signal width. Additional strain gauges ~~may~~ can also be mounted at different locations on the board to fully characterize the strain response of the assembly.

The board assembly shall then be mounted on the drop test fixture using four screws. The screws shall be tightened in diagonal pattern in the order of SW, NE, SE, and NW corners of the board. An additional accelerometer may also be mounted on the board assembly at or close to one of the support locations to ensure that the input pulse to the base plate is transmitted to the PCB without any distortion. The drop table shall then be raised to the height required to meet test condition B of Table 1 of IEC 60749-10:2022 and dropped on to the strike surface while measuring the G level, pulse duration, and pulse shape.

~~Multiple drops might be required whilst adjusting the drop height and strike surface to achieve the specified acceleration levels and pulse duration (1 500 m·s^{-2}, 0,5 ms half-sine pulse). It should be noted that the peak acceleration and the pulse duration is a function of not only the drop height but also the strike surface.~~ The acceleration pulse shall follow a half-sine curve with a peak acceleration of 1 500 m·s^{-2} during each drop as shown in Figure 2. Multiple drops can be required while adjusting the drop height and impact surface to achieve the specified peak acceleration and change of velocity (1 500 m·s^{-2}, 4,67 m/s respectively). The variations of the peak acceleration and change of velocity needs to be controlled within 10 % on each individual measurement and 5% tolerance on average when 20 repeating measurements. The change of velocity is the total area enclosed by the acceleration pulse and the time axis. An effective change of velocity shall be counted in which only an acceleration equal to or higher than 1 500 m·s^{-2} is considered and any rebounces after the acceleration dropping to below 1 500 m·s^{-2} from the peak shall be ignored in the calculation. The time duration for defining the area of effective change of velocity is called effective pulse duration and shall also be maintained at 0,5 ms within 15 % tolerance which is in accordance with IEC 60749-10. The test equipment and transducer shall have a natural frequency greater than 5 times the frequency of the shock pulse being established, and measured through a low-pass filter having a bandwidth greater than 5 times the frequency of the shock pulse being established, see detail in IEC 60749-10. However, both unfiltered and filtered acceleration profiles shall be reported for the comparison purposes. It shall be noted that these pulse parameters are function of not only the drop height but also the impact surface. Depending on the strike surface, the same drop height could result in different acceleration levels and pulse durations. Theoretically, the drop height needed to achieve the appropriate acceleration levels can be determined from Equations (1) and (2) and the associated Figure 3, where H is the drop height and C is the rebound co-efficient (1,0 for no rebound, 2,0 for full rebound). However, this equation does not include the strike surface effect.

Experiments with different strike surfaces ~~may~~ can be ~~needed~~ necessary to achieve the desired peak value and duration.

$$A(t) = A_0 \sin\left(\frac{\pi t}{t_w}\right) \tag{1}$$

$$\sqrt{2gH} = A_0 \sin\left(\frac{2A_0 t_w}{C\pi}\right) \tag{2}$$

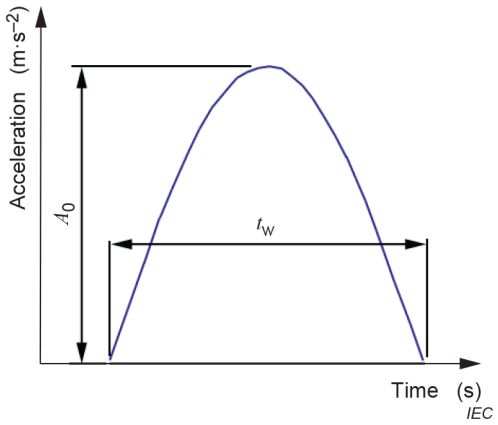


Figure 3 – Typical shock test half-sine pulse graphic and formulae

Once the specified drop parameters (acceleration level, duration and pulse shape) are achieved, the PCB response acceleration and strain shall be measured. The strain rate shall also be calculated by dividing the change in strain value by the time interval during which this change occurred. The characterized board response (acceleration, strain and strain rate) and its variation shall be documented and provided with the test data. Although it is recommended that this characterization be performed for previously untested components, this may not be required if such characterization data are available for a similar sized component.

5.3 Drop testing

With test parameters adjusted and PCB response characterized, the PCB assemblies shall be prepared for drop testing. This involves soldering cables to the plated-through holes on one end of the board, mounting the board on the drop fixture with components facing down, and connecting cables to the event detector/data logger. Since the dynamic response of the board can be affected by the mass and stiffening of the connector, it is recommended that no connectors are used and wires are directly soldered to the board.

The event detector's threshold resistance shall be set to no more than 1 000 Ω. The system used for such event detections shall have a 55 MHz scan rate or 0,2 µs (or lower) event detection window. Proper strain relief ~~should~~ shall also be provided to cables/wires to avoid a failure at wires to board interconnects. All cables shall be cleared from the drop path. The initial resistance of all nets for each assembly shall be measured and logged before conducting the first drop. The drop test shall be conducted by releasing the drop table from the pre-established height. The electrical resistance of each net shall be measured in situ during each drop and all failures shall be logged. The board shall be dropped a required maximum number of times or until a percentage of all devices has failed, whichever is earlier. The maximum number of drops or percentage of devices failing shall be consistent with the application. The maximum number of drops shall be irrespective of single or double-sided assembly. In the event that a shock condition in addition to the required condition B is used to conduct the test, the maximum number of drops shall be determined using the acceleration factor between the two conditions for similar sized components. This acceleration factor shall be reported with the test data.

During the test, the shock pulse shall be measured for each drop to ensure that the input pulse remains within the specified tolerance. Adjustments in drop height or replacement of strike surface shall be made if the pulse deviates from that specified.

Depending on the number of components per board, Table 1 shall be used to determine the number of boards to be tested per component type.

6 Failure criteria and failure analysis

In-situ electrical monitoring of daisy chain nets for failure is required during each drop. The electrical continuity of all nets ~~should~~ shall either be detected by an event detector or by a high-speed data acquisition system. The event detector ~~should~~ shall be able to detect any intermittent discontinuity of resistance greater than 1 000 Ω lasting for 1 µs or longer. The high-speed data acquisition system ~~should~~ shall be able to measure resistance with a sampling rate of 50,000 samples per second or greater.

Depending on the monitoring system used, the failure is defined as follows:

– **event detector**: the first event of intermittent discontinuity as defined above followed by 3 additional such events during 5 subsequent drops.

– **high speed data acquisition**: the first indication of resistance value of 100 Ω or 20 % increase in resistance from the initial resistance if initial resistance is greater than 85 Ω followed by 3 additional such indications during 5 subsequent drops.

A visible partial separation of component from the test board, even without a significant increase in resistance or intermittent discontinuity, shall also be considered as a failure. This can occur if the PCB tracks come off the board with the component while maintaining electrical continuity.

As wires soldered to the board for electrical continuity test can also come off during the test, it is highly recommended that all electrical connections be checked once a failure is indicated to ensure that the failure is due to a component to board interconnection failure.

All failures after each drop shall be logged. A sufficient number of components from the test lot shall be subjected to failure analysis to determine the root cause and to identify failure mechanism. The selection of components ~~should~~ shall cover different locations on the board. Different methods and equipment, such as visual inspection, cross-section, dye and pry, chemical etching, scanning electron microscopy, and scanning acoustic tomography can be employed to determine the root cause of failure. The failure site shall be clearly identified as ‘component failure’, ‘interconnect failure’ or ‘board failure’. For the purpose of this document, the “interconnect failure” is defined as any failure

a) on the package pad – joint interface or intermetallics,

b) through the joint material,

c) on the PCB pad joint interface or intermetallics.

The above criteria may always be overridden by an applicable procurement document.

Data analysis shall be conducted showing mean and standard deviation of failure data according to component groupings. Weibull and/or log normal analysis result ~~should~~ shall also be included if sufficient quantities have failed for such analyses. ~~Because of symmetric component design and support locations, grouping (see Table 2) can be used for data analysis for boards mounted with 15 components (refer to Figure A.1).~~

Table 2 – Component locations for test boards

Group	Number of components in the group	Component locations on the board	Sample size	
			Side A assembly	Side B assembly
A	4	U1, U5, U11, U15	8	8
B	4	U2, U4, U12, U14	8	8
C	2	U6, U10	4	4
D	2	U7, U9	4	4
E	2	U3, U13	4	4
F	1	U8	2	2

Failure data for components in group E and F can also be combined into one group as the PCB curvature underneath these components is expected to be very similar during the fundamental mode of vibration, as shown in Figure 3. The fundamental mode results in maximum displacements and is typically most damaging. Similarly, a larger group containing components in groups B and D may also exist. It is recommended first to analyse the component reliability data at individual locations without assuming any grouping. The failure data can only be pooled together when they have been proved to be statistically equivalent.

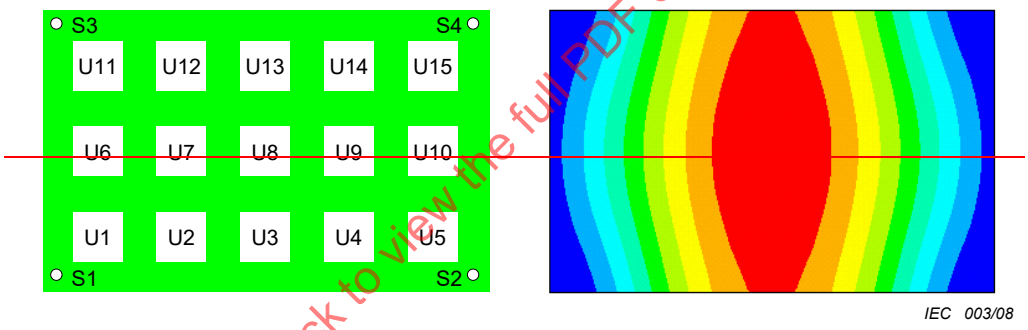


Figure 3 – Fundamental mode of vibration of PCB supported with four screws

For the cases where component design is not symmetric about the X- and Y-axis, the above grouping may not work. This may require additional boards to be tested to achieve the sample sizes given above.

7 Summary

All test reports shall include the following information:

a) number of packages per board;

a) package and PCB assembly weight;

b) package geometrical details including body size, lead size, ball size, layer thickness and die size;

c) package materials including mould compound, die attach, substrate;

d) PCB information, including materials, surface finishes, pad design type, board thickness, layer count and etc.;

e) board geometry, material and material properties such as thickness, pad size, modulus and T_g;

f) board assembly details including stencil thickness, apertures, stencil material, solder alloy and paste, reflow profile and other board assembly process details;

g) test details: drop height, strike surface, shock pulse profile;

h) board response (acceleration, strain and strain rate);

i) shock table response (shock parameter including peak acceleration, velocity change, time duration, number of spots/locations on table tested and repetitions, tolerance report of those measurements; filtering frequency for acceleration;

j) initial resistance of daisy chain nets;

k) failure detection equipment and failure criteria;

l) test results including the number of drops to failure for each location on each test board, failure mechanisms and representative pictures;

m) data analysis showing mean and standard deviation of failure data according to component groupings.

Annex A
(informative)

Preferred board construction, material, design and layout

A.1 Preferred board construction, material and design

The preferred test board should use built-up multilayer technology incorporating microvias using 1+6+1 stack-up. This is recommended because typical PCB assemblies used in handheld electronic systems are constructed using high density, build-up technology. The test board should have a nominal thickness of 1,0 mm. A thinner board (0,8 mm) can also be used but correlation between the drop test performance and the different board thicknesses needs to be established. Table A.1 provides the thickness, copper coverage and material for each layer. The dielectric materials should meet the mechanical properties ~~requirements~~ given in Table A.2. The PCB should have organic solderability preservatives (OSP) as surface finish to avoid any copper oxidation before component mounting. The glass transition temperature, T_g, of each dielectric material, as well as of the composite board, should be ~~125~~ 130 °C or greater. The modulus and T_g of the dielectric materials should be specified. The composite values (modulus and T_g) should be measured on at least one representative test board at the component mounting location. The boards should be symmetrical in construction about the mid-plane of the board, except for the minor differences in the top and bottom two layers.

Table A.1 – Test board stack-up and material

Board layer	Thickness µm	Copper coverage %	Material
Solder mask	20		LPI [a]
Layer 1	~~35~~ 25	Pads + ~~tracks~~traces (via in pad)	Copper
Dielectric 1-2	~~65~~ 60		~~RCC~~ FR4 [b,c]
Layer 2	~~35~~ 25	40 % 70 % including daisy chain links	Copper
Dielectric 2-3	~~130~~ 60		FR4 [c]
Layer 3	18	70 %	Copper
Dielectric 3-4	~~130~~ 100		FR4 [c]
Layer 4	18	70 %	Copper
Dielectric 4-5	~~130~~ 100		FR4 [c]
Layer 5	18	70 %	Copper
Dielectric 5-6	130		FR4 [c]
Layer 6	18	70 %	Copper
Dielectric 6-7	~~130~~ 100		FR4 [c]
Layer 7	~~35~~ 18	~~40~~ 70 %	Copper
Dielectric 7-8	~~65~~ 100		~~RCC [b]~~ FR4 [c]
Layer 8	18	70 %	Copper
Dielectric 8-9	60		FR4 [c]
Layer 9	25	70 %	Copper
Dielectric 9-10	60		FR4 [b,c]
Layer ~~8~~ 10	~~35~~ 25	Pads + ~~tracks~~traces + daisy chain links (no via in pad)	Copper
Solder mask	20		LPI [a]

[a] Liquid photo-imageable.

[b] Resin-coated copper; usage as an alternative to FR4 shall be documented.

[c] Details of the FR4 material shall be documented.

Table A.2 – Mechanical property requirements for dielectric materials

Property	Unit	FR4	RCC
Tensile strength	MPa	>100	>50
Tensile modulus	GPa	20 ± 2	2 ± 1
Tensile elongation	%	>3	>3
In-plane CTE (below T_g)	ppm/°C	~~15 ± 2~~ 14 ± 3	60 to 80
T_g	°C	>130	>130
Cu peel	N/mm	>1	>1

Since a typical product board may have a combination of microvias in pad and no vias in pad for area array packages for routing purposes, it is required that such components (BGAs, CSPs, etc.) be tested on boards with both microvia and non-microvia PCB pads. This should be accomplished by designing double-sided boards with mirror component footprints on each side (top and bottom) of the board. The board side A should have microvias in pads ("via in pad") on all component mounting pads while the board side B should have no microvias in pads ("no via in pads"). For board side A, the microvias in pads should be created with laser ablation with a via diameter of 110 µm. The vias should then be plated resulting in straight or near straight walls. The capture pad diameter should be at least 220 µm. Although two-sided boards should be designed, the component should only be mounted on one side at a time, resulting in two, single-sided assemblies ("side A assembly" and "side B assembly"), unless the component is anticipated for use in mirror-sided board assemblies. In that case, the components should be mounted on each side of the board.

As perimeter-leaded devices do not typically require microvia in pad, the test board for such devices (TSOP, quad flat pack, etc.) does not need to include microvias. The board should still be designed as double-sided with footprint of similar sized components on each side.

Although daisy-chain nets will typically not require plated-through holes (PTH) other than those required for manual probe pads and connectors, the test board should contain PTH in the component region (1,2 × the area covered by component) to approximate the mechanical effect of vias on actual application boards.

It is recommended that there should be 20 plated-through holes per square centimetre in the component region. The actual location and distribution of plated-through holes will depend on component size and I/O. The through holes should have a drill diameter of 300 µm and a finished plated hole diameter of 250 µm. The PTH pad diameters should measure 550 µm for the outer layer and 600 µm for the inner layers. It is recommended that the component mounting pads on the PCB be designed in accordance with the specification in Table A.3 for area array devices. The pad design for leaded and perimeter I/O devices should be in accordance with relevant national or international guidelines. All component attachment pads should be non-solder-mask-defined (NSMD) with solder mask clearance of 75 µm between the edge of the pad and the edge of solder mask. A smaller clearance can be used, as long as it does not cause any solder mask encroachment on pads due to mis-registrations.

Solder mask registration tolerance should not exceed 50 µm.

Table A.3 – Recommended test board pad sizes and solder mask openings

Component I/O pitch mm	PCB pad diameter mm	Solder mask opening mm
0,4	0,25	0,32
0,50	0,28	0,43
0,65	0,30	0,45
0,75 to 0,80	0,35	0,50
1,00	0,45	0,60

The track widths on the suggested test board should be 75 µm within the component area. This includes all tracks making contact with solder joint interconnect as well as with all internal layers. A track width of 100 µm should be used for all tracks outside of the component region. The board should have a matching daisy chain pattern such that one or multiple nets are formed through all interconnects after component mounting. Wherever necessary, additional test points within each net may be incorporated for failure location identification. Each additional test point should be clearly labelled using the row column format of the package. All routing and tracks within and just outside the component footprint should be done on layer 2 and layer 8 for area array packages and layer 1 and layer 8 for perimeter leaded packages.

The suggested test board should have component mounting features such as Pin 1 identification and global/local fiducials.

A.2 Preferred test board size, layout, and component locations

~~The board footprint and layout are shown in Figure A.1. The overall board size should be 132 mm × 77 mm such that it can accommodate up to 15 components of the same type in a 3 row by 5 column format. The preferred maximum component size is 15 mm in length or width and there should be at least a 5 mm and 8 mm gap between the components in X- and Y-direction, respectively. If larger components, up to 18 mm in length or width,are tested using this method, the gap between components cannot be less than 2 mm. All 15 sites on each side of the board (top and bottom) should have the same component footprint.~~

~~A "common" footprint for multiple components can also be used if daisy chain requirements, as specified in 5.2, are met. For example, a 9 × 9 pad array can be designed to accommodate suitably designed daisy chain components with 8 × 8, 7 × 7, 8 × 9, or any other ball array combination. However, a mix of different component sizes and styles should not be used on the same board, as this will affect the dynamic response of the board, making the results difficult to analyze. There should be four holes on the board to be used for mounting board on drop test fixture. The locations of these holes are shown in Figure A.1. All components should be located within the 95 mm × 61 mm box (shown by the dashed line in Figure A.1) defined by the outer edges of all outer components. The outer edges of out side components (U1 through U6 and U10 through U15) should align with the boundary of this box, guaranteeing a fixed diagonal distance of 4 mm between the outer edge of the screw head and the component's corner closest to the screw head (components U1, U3, U5, U11, U13, and U15) irrespective of component size. The X, Y location of the centre of each component location is listed in Table A.4, using the centre of the lower, left screw hole as datum.~~

~~The area of the board in the length direction outside of the components should be restricted for labelling, through holes, edge fingers, and any other fixtures, if needed. Plated through holes or edge fingers should be provided on each end of the board for soldering wires, one for each side (top and bottom) of the board.~~

Dimensions in millimetres

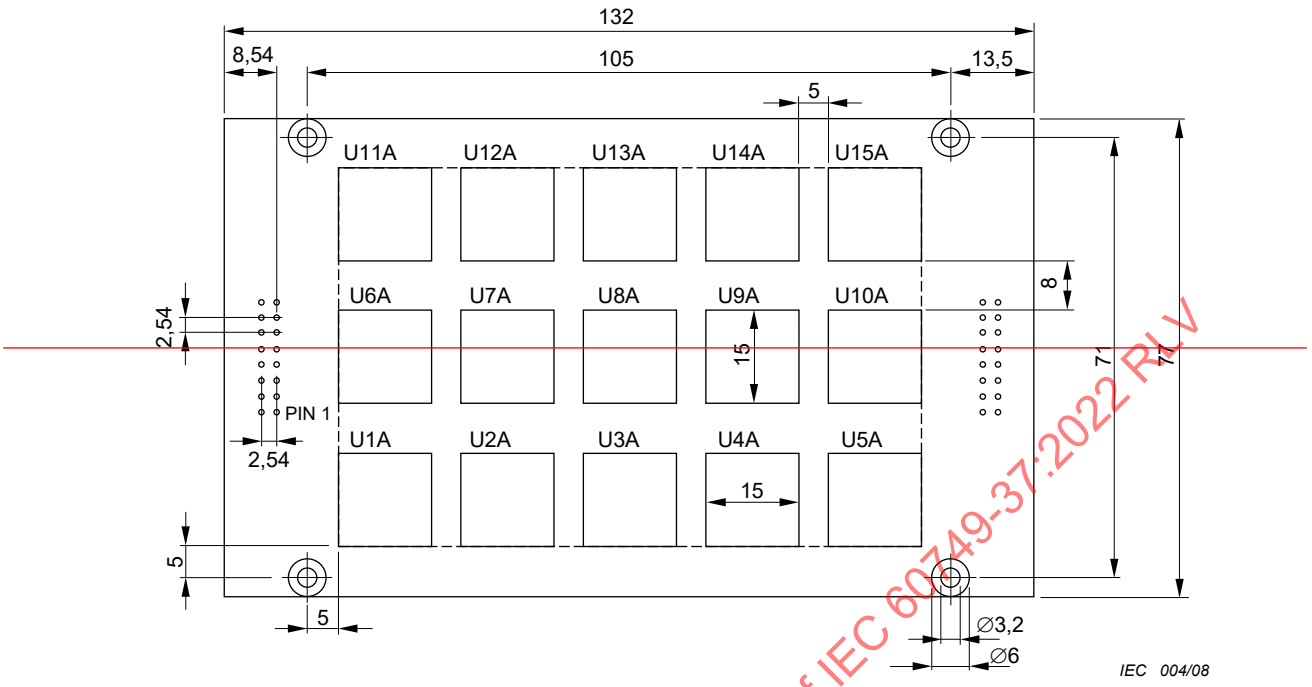


Figure A.1 – Recommended test board size and layout

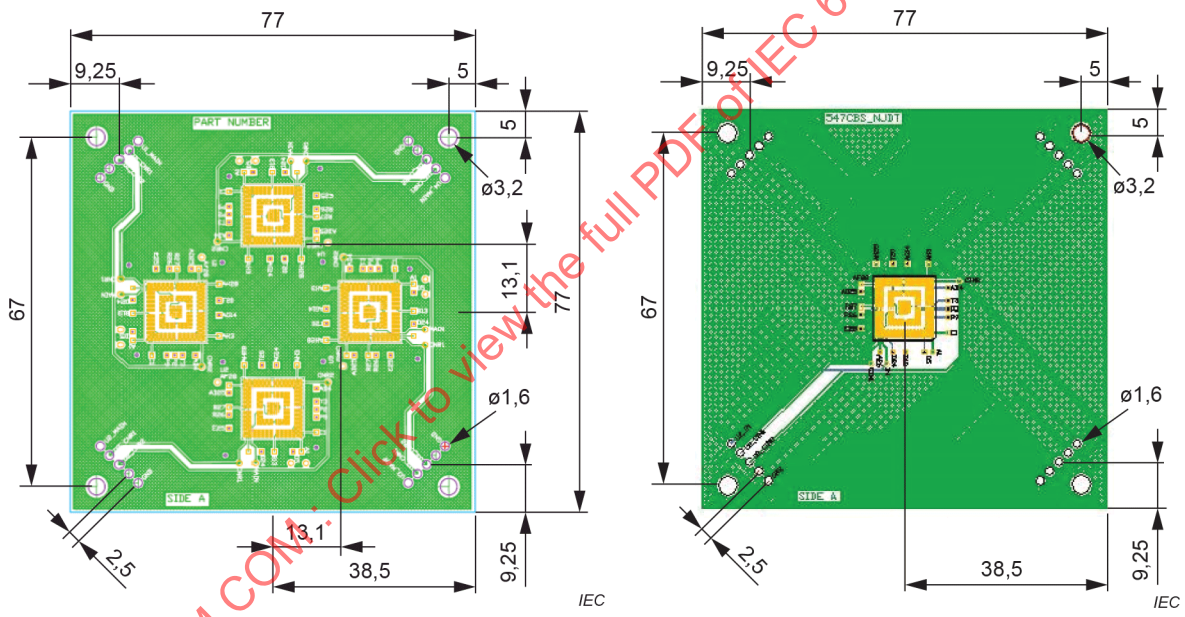
Table A.4 – X and Y locations for component's centre

Component ID	X location of component centre mm	Y location of component centre mm
U1	$5 + L_e/2$	$5 + W_e/2$
U2	$28{,}75 + L_e/4$	$5 + W_e/2$
U3	52,5	$5 + W_e/2$
U4	$76{,}25 - L_e/4$	$5 + W_e/2$
U5	$100 - L_e2$	$5 + W_e/2$
U6	$5 + L_e/2$	35,5
U7	$28{,}75 + L_e/4$	35,5
U8	52,5	35,5
U9	$76{,}25 - L_e/4$	35,5
U10	$100 - L_e/2$	35,5
U11	$5 + L_e/2$	$66 - W_e/2$
U12	$28{,}75 + L_e/4$	$66 - W_e/2$
U13	52,5	$66 - W_e/2$
U14	$76{,}25 - L_e/4$	$66 - W_e/2$
U15	$100 - L_e/2$	$66 - W_e/2$
L_e and W_e = component length and width.		
NOTE Centre of lower left screw hole as datum.		

The board footprint and layout is shown in Figure A.1. The overall board size is a 77 mm by 77 mm square board. The total number of components per board is 4 with an option of 1 component per board. In the case of four (4) components per board, these components are mounted orthogonally and totally symmetric with each other from the board center to the package edge with a distance of 13,10 mm. The maximum component size should be no more than 15 mm in length or width for the case of 4 components per board. All 4 sites on each side of the board (top and bottom) should have the same component footprint. A “common” footprint for multiple components can also be used if daisy chain requirements, as specified in 5.2, are met.

The daisy chain can be arranged as outer corner, inner corner and the main chain for each component. The outer corner chain contains the corner-most balls on the outer corners, i.e., these two corners are closer to the board edge. The inner corner chain contains the corner-most balls on two inner corners, i.e., these two corners are closer to the board centre. These corner balls should also be daisy-chained separately if the number of channel of monitoring is not limited. The remaining balls can be chained together and called main chain. All components should be the same and mix of different component sizes and styles should not be used on the same board, as this will affect the dynamic response of the board, making the results difficult to analyze.

Dimensions in millimetres



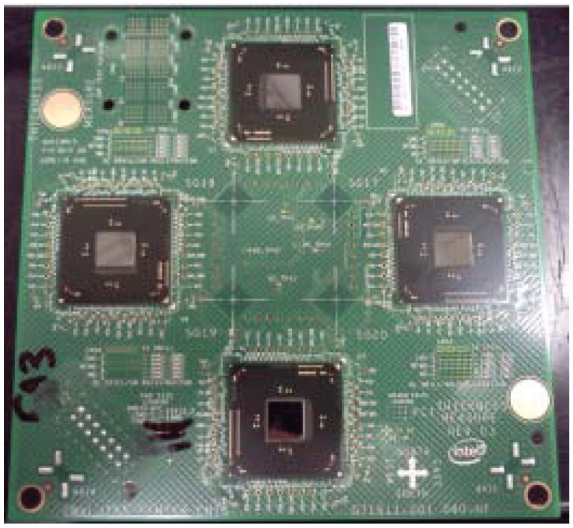
a) For 4 components b) For one component

Figure A.1 – Board footprint and BGA layout

The mounting board used on the drop test fixture is designed with four holes. The locations of these holes are shown in Figure A.1. In the case of 4 components, all components shall be located with a distance of 13,10 mm from the inner edge of the component to the board center. The four components are numbered as U1, U2, U3, and U4, which are located at 12, 3, 6, and 9 o’clock, respectively. The area of the board in the length direction outside of components is restricted for labeling, through holes, edge fingers, and any other fixtures, if needed. As illustrated in Figure A.1, there is a space for a 5-pin plated through hole (PTH) connector on each corner, even though the connector is not to be mounted. The minimum gap of these holes to the screw hole as well as to any component edge should be 5 mm. These plated through holes provide the solder wiring for functional continuity test which can be done on each side (top and bottom) of the board.

For the option of 1 component per board, the component is mounted in the center of the board as shown in Figure A.1 b). In this case, screw holes and 5-pins PTH holes should remain in every corner (the same as those in the 4-component case). This is to ensure the total symmetric

design for the board. This design may be used for a component with a larger body such as 17 mm. However, this should be clearly specified in the drop test report if one component per board is used. Figure A.2 provides an illustration that integrates both 4 component placement (primary board side) and option of single component (bottom site of board).



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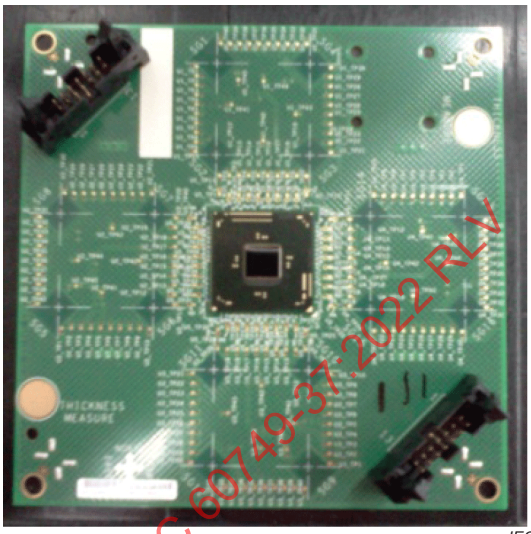

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Figure A.2 – Test vehicle with 4 component placement (top side – left) and 1 component at center location (bottom side – right).

Since the drop test performance is a function of the test board used for evaluation, this document defines a preferred test board construction, dimensions, and material that is representative of those used in handheld electronic products. If another board construction/material better represents a specific application, the test board construction, dimensions and material should be documented. The test data generated using such a board should be correlated at least once by generating the same data on same component using the preferred board defined in this document.

If materials or specifications are used other than those mentioned in this document, they should be clearly reported in the documentation.

Bibliography

IEC 60749-40, *Semiconductor devices – Mechanical and climatic test methods – Part 40: Board level drop test method using a strain gauge~~s~~*[3]

"Shock risk assessment of BGA components – Importance of physics based metrics"; Rahmani, H.; Vujosevic, M.; Pei, M, Proc. of ASME Int'l. Conf. on Nanochannels, Microchannels and Minichannels; San Francisco, CA; July 2015

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[3] ~~Under consideration.~~

IEC 60749-37

Edition 2.0 2022-10

INTERNATIONAL STANDARD

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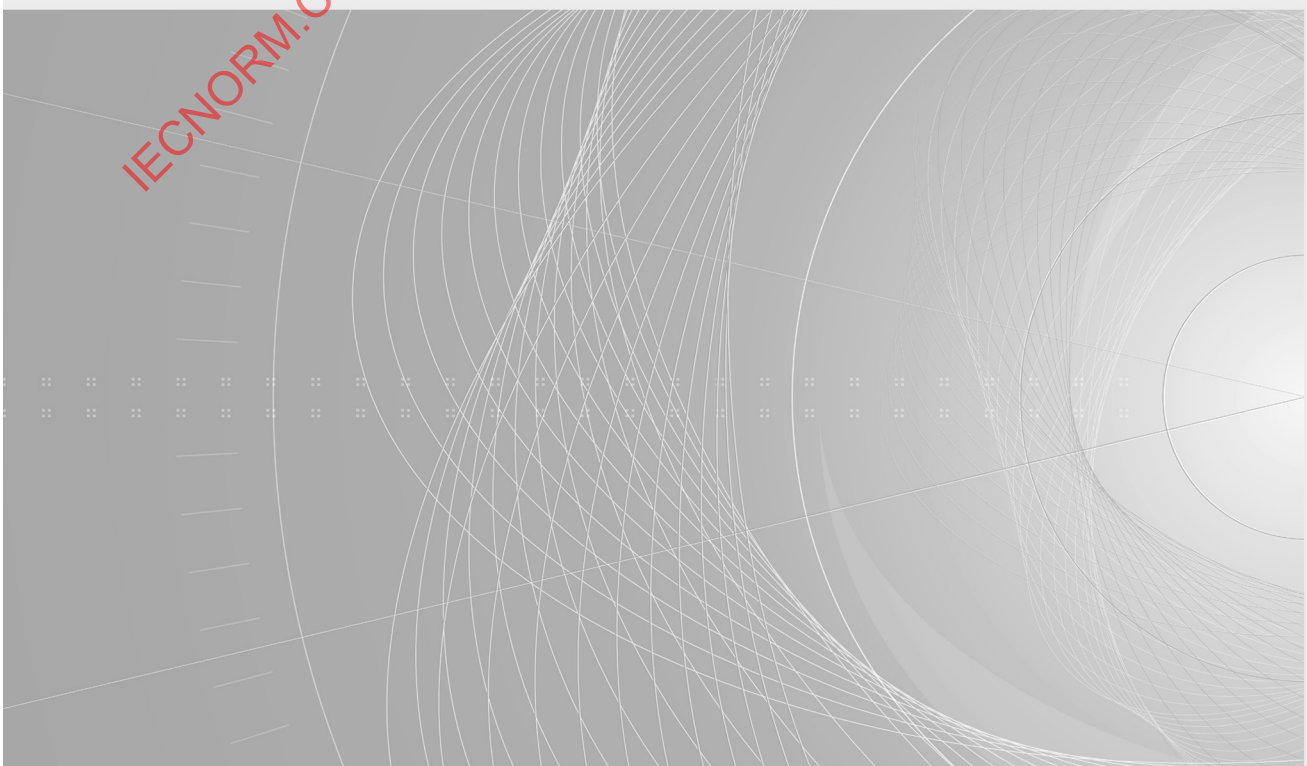
Semiconductor devices – Mechanical and climatic test methods – Part 37: Board level drop test method using an accelerometer

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 37: Méthode d'essai de chute au niveau de la carte avec utilisation d'un accéléromètre



IEC 60749-37:2022-10(en-fr)

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 37: Board level drop test method using an accelerometer

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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This edition includes the following significant technical changes with respect to the previous edition:

a) correction of a previous technical error concerning test conditions;
b) updates to reflect improvements in technology.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2651/CDV	47/2719/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts of the IEC 60749 series, under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found in the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

Handheld electronic products fit into the consumer and portable market segments. Included in handheld electronic products are cameras, calculators, cell phones, cordless phones, pagers, palm size PCs, personal computer memory card international association (PCMCIA) cards, smart cards, personal digital assistants (PDAs) and other electronic products that can be conveniently stored in a pocket and used while held in user's hand.

These handheld electronic products are more prone to being dropped during their useful service life because of their size and weight. This dropping event can not only cause mechanical failures in the housing of the device but also create electrical failures in the printed circuit board (PCB) assemblies mounted inside the housing due to transfer of energy through PCB supports. The electrical failures sometimes result from various failure modes such as cracking of the circuit board, track cracking on the board, cracking of solder interconnections between the components and the board, and component cracks. The primary driver of these failures is excessive flexing of the circuit board due to input acceleration to the board created from dropping the handheld electronic product. This flexing of the board causes relative motion between the board and the components mounted on it, resulting in component, interconnect or board failures. The failure is a function of the combination of the board design, construction, material, thickness and surface finish; interconnect material and standoff height and component size.

Correlation between test and field conditions is not yet fully established. Consequently, the test procedure is presently more appropriate for relative component performance than for use as a pass/fail criterion. Rather, results can be used to augment existing data or establish a baseline for potential investigative efforts in package/board technologies.

The comparability between different test sites, data acquisition methods, and board manufacturers has not been fully demonstrated by existing data. As a result, if the data are to be used for direct comparison of component performance, matching studies will first be performed to prove that the data are in fact comparable across different test sites and test conditions.

This method is not intended to substitute for full characterization testing, which could incorporate substantially larger sample sizes and increased number of drops. Due to limited sample size and number of drops specified here, it is possible that enough failure data are not generated in every case to perform full statistical analysis.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 37: Board level drop test method using an accelerometer

1 Scope

This part of IEC 60749 provides a test method that is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface-mounted components while producing the same failure modes normally observed during product level test.

This document aims at prescribing a standardized test method and reporting procedure. This is not a component qualification test and is not meant to replace any system level drop test that is sometimes used to qualify a specific handheld electronic product. The standard is not meant to cover the drop test required to simulate shipping and handling-related shock of electronic components or PCB assemblies. These requirements are already addressed in test methods such as IEC 60749-10. The method is applicable to both area array and perimeter-leaded surface mounted packages.

This test method uses an accelerometer to measure the mechanical shock duration and magnitude applied which is proportional to the stress on a given component mounted on a standard board. The test method described in IEC 60749-40 uses strain gauge to measure the strain and strain rate of a board in the vicinity of a component. The customer specification states which test method is to be used.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-10:2022, *Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock – Device and subassembly*

IEC 60749-20, *Semiconductor devices – Mechanical and climatic test methods – Part 20: Resistance of plastic-encapsulated SMDs to the combined effect of moisture and soldering heat*

IEC 60749-20-1, *Semiconductor devices – Mechanical and climatic test methods – Part 20-1: Handling, packing, labelling and shipping of surface-mount devices sensitive to the combined effect of moisture and soldering heat*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

IEC Electropedia: available at https://www.electropedia.org/

ISO Online browsing platform: available at https://www.iso.org/obp

3.1
component
packaged semiconductor device

3.2
single-sided assembly
printed circuit board assembly with components mounted on only one side of the board

3.3
double-sided assembly
printed circuit board assembly with components mounted on top and bottom sides of the board

3.4
handheld electronic product
product that can conveniently be stored in a pocket (of sufficient size) and used when held in user's hand

Note 1 to entry: Handheld electronic products include cameras, calculators, cell phones, pagers, palm-size PCs (formerly called 'pocket organizers'), personal computer memory card international association (PCMCIA) cards, smart cards, mobile phones, personal digital assistants (PDAs) and other communication devices.

3.5
peak acceleration
maximum acceleration during the dynamic motion of the test apparatus

3.6
pulse duration
acceleration interval
time interval between the instant when the acceleration first reaches 10 % of its specified peak level and the instant when the acceleration first returns to 10 % of the specified peak level after having reached that peak level

3.7
table drop height
free-fall drop height of the drop table needed to attain the prescribed peak acceleration and pulse duration

3.8
event
electrical discontinuity of resistance greater than 1 000 Ω lasting for 1 µs or longer

3.9
event detector
continuity test instrument capable of detecting electrical discontinuity of resistance greater than 1 000 Ω lasting for 1 µs or longer

4 Test apparatus and components

4.1 Test apparatus

The shock-testing apparatus shall be capable of providing shock pulses up to a peak acceleration of 2 900 $m \cdot s^{-2}$ with a pulse duration between 0,3 ms and 8,0 ms to the body of the device and a velocity change of 1 250 $mm \cdot s^{-1}$ to 5 430 $mm \cdot s^{-1}$. For free-state testing, a velocity change of 1 250 $mm \cdot s^{-1}$ to 5 430 $mm \cdot s^{-1}$ and a pulse duration between 0,3 ms and 2,0 ms is sufficient. Conversely, for mounted-state testing, apparatus capable of a velocity change of

1 000 mm·s^{-1} to 5 430 mm·s^{-1} and a pulse duration between 5,0 ms and 8,0 ms to the body of the component is sufficient.

The acceleration pulse shall be a half-sine waveform with an allowable deviation from specified peak acceleration not greater than ±10 %. The test velocity change shall be ±10 %of the specified level. The pulse duration shall be measured between the points at 10 % of the peak acceleration during rise time and 10 % of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be ±15 % of the specified duration. The test equipment transducer shall have a natural frequency greater than 5 times the frequency of the shock pulse being established, and measured through a low-pass filter having a bandwidth greater than 5 times the frequency of the shock pulse being established. Filtering shall not be used in lieu of good measurement setup and procedure practices.

Appropriate equipment calibration shall be carried out prior to any testing.

4.2 Test components

This document covers all area arrays and perimeter-leaded surface-mountable packaged semiconductor devices such as ball grid arrays (BGA), land grid arrays (LGA), chip scale packages (CSP), thin small outline packages (TSOP) and quad flat no-lead packages (QFN) typically used in handheld electronic product. The maximum size of the component body covered in this document is 15 mm x 15 mm in general. A larger body size may be used for a special board layout as described in detail in 4.3. All components used for this testing shall be daisy-chained. The daisy chain is made at the die level or by providing daisy chain links at the lead-frame or substrate level. In case of non-daisy chain die, a mechanical dummy die shall be used inside the package to simulate the actual structure of the package. The die size and thickness shall be similar to the functional die size to be used in application. The component materials, dimensions and assembly processes shall be representative of typical production device.

4.3 Test board

Since the drop test performance is a function of the test board used for evaluation, this document describes a preferred test board construction, dimensions, and material that is representative of those used in handheld electronic products. If another board construction/material better represents a specific application, the test board construction, dimensions and material shall be documented. The test data generated using such a board shall be correlated at least once by generating the same data on the same component using the preferred board defined in this document (see Annex A for recommendations).

4.4 Test board assembly

Prior to board assembly, all devices shall be inspected for missing balls or bent leads. Board thickness, warpage and pad sizes shall also be measured using a sampling plan. A visual inspection shall be performed on all boards for solder mask registration, contamination and daisy chain connection. It is recommended that boards be inspected and accepted in accordance with a relevant national or international standard. One board shall also be used to measure the mechanical properties (modulus and glass transition temperature, T_g) of the board at the component location using dynamic mechanical analysis (DMA) and thermomechanical analysis (TMA) methods. It is highly recommended that the coefficient of thermal expansion (CTE) of the board be also measured in X, Y and Z direction. The mechanical property measurements are not required for every board lot, unless the fabrication process, material or vendor is changed from lot to lot.

The components shall be baked according to IEC 60749-20 and IEC 60749-20-1 prior to board assembly. The test boards shall be assembled using best known methods of printed circuit assembly process, representative of production methods. At least one board shall be used to adjust the board mounting process such as paste printing, placement and reflow profile. All assemblies shall be single-sided only, unless the component is anticipated for use in mirror-

sided board assemblies. In that case, the components shall be mounted on each side of the board.

A 100 % X-ray inspection is recommended on assembled units to check for voids, short-circuits and other abnormalities. Electrical continuity test shall also be performed on all mounted units to detect any open-circuits or short-circuits.

4.5 Number of components and sample size

The board design recommended in Annex A allows 4 locations for component mounting and is recommended that all 4 components are mounted. Since the board is designed with full symmetry, all 4 components are expected to be subjected to the same drop performance and hereby the test results are treated as one single group. Statistical analysis on the data equivalence is suggested to ensure that variability in the component performance is insignificant before comprehensive data or full qualification is pursued. In order to get good statistically meaningful results, a total of 6 boards or 24 components are recommended as a minimum quantity per each design.

Since the number and size of the components mounted on the board can influence the dynamic response of the test board assembly during drop, it is required that additional data be provided whenever the 1-component configuration is employed. The additional data shall directly compare the effect of optional component mounting (1 component case) to the preferred 4-component mounting configuration. This comparison shall be provided for a component similar in size (within 20 % in both length and width) to the component, which has been tested using 1-component per board configuration only.

In the case of 1 component mount on the board, Table 1 shall be used to determine the minimum quantity of assembled board required for testing and total number of components to be tested. Sample sizes greater than specified below can also be used to generate statistically sufficient data.

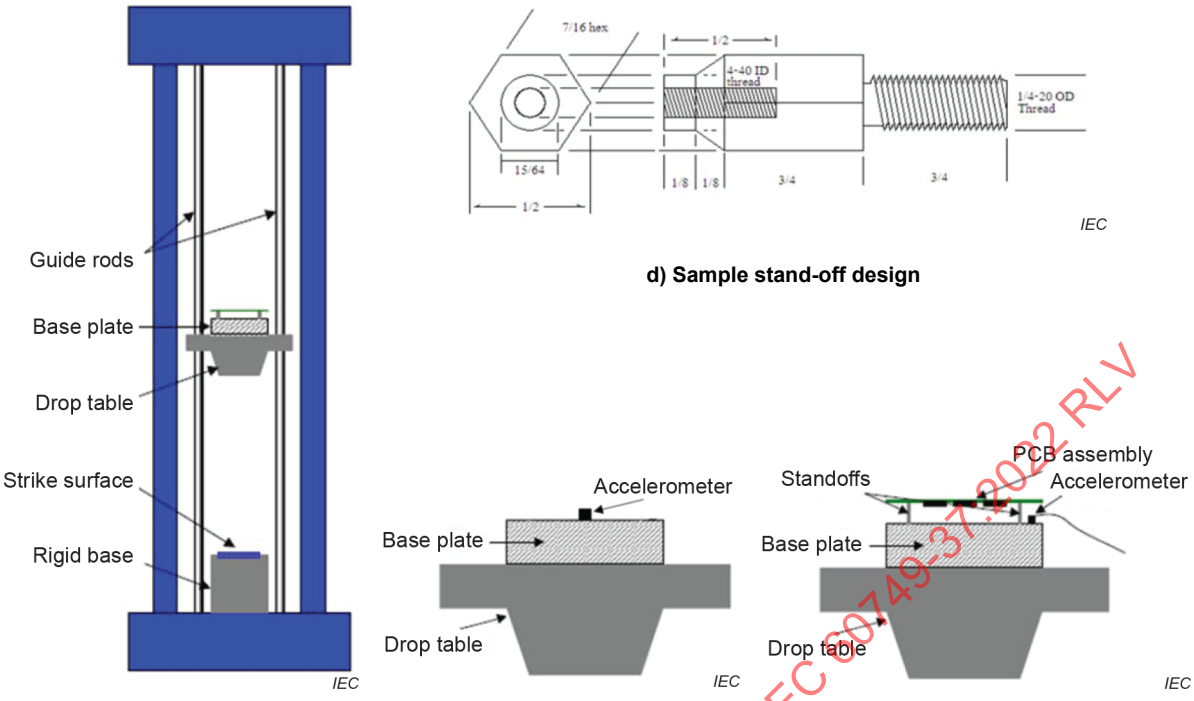
Table 1 – Quantity of test boards and components required for testing

Number of components per board	Location	Number of boards		Total number of components
		Side A assembly (via in pad)	Side B assembly (not via in pad)	
4	U1, U2, U3 and U4	6	6	48
1	Centre of the board	16	16	32

5 Test procedure

5.1 Test equipment and parameters

The shock testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and levelled before use. Means shall be provided in the apparatus (such as an automatic braking mechanism) to eliminate bounce and to prevent multiple shocks to the board. Figure 1 shows the typical drop test apparatus where the drop table travels down on guide rods and strikes the rigid fixture. The rigid fixture typically is covered with some form of material to achieve the desirable pulse and acceleration levels. The bottom of the drop table is usually rounded slightly to ensure a very small area of contact with the strike surface.



d) Sample stand-off design

a) Typical drop test apparatus

b) Pre-characterization set up without test board

c) Assembly set up with board

Figure 1 – Drop test apparatus detail

A base plate with suitable standoffs shall be rigidly mounted on the drop table. The thickness and mounting locations of the base plate shall be selected such that there is no relative movement between the drop table and any part of base plate during drop testing. This plate will serve as the mounting structure for the PCB assemblies. This is pictorially shown in Figure 1. The PCB assembly shall be mounted to the base plate standoffs using four screws, one at each corner of the board. The board shall be mounted using four suitable precision shoulder screws (e.g. M3 × 0,5). Test data suggests that the variations in response acceleration and strain are reduced significantly depending upon the choice of screw. Since the length of shoulder is nominal, a number of washers shall be placed between the screw head and the top surface of the board (nominal 1,0 mm thick) to avoid any gap between the top of the standoffs and the bottom surface of the board. Due to tolerance stack up, a small gap is still possible but this gap shall not exceed 50 µm. The use of shoulder screw eliminates the need to re-tighten screws between drops. The screws shall be tightened in a diagonal pattern in the order of SW, NE, SE, and NW corners of the board. The screw shall be tightened until the shoulder of the screw bottoms out against the standoff. The number of washers used shall be the same for all four screws. A custom board jig may be used instead of mounting the board directly to the plate.

Experience with different board orientations has suggested that the horizontal board orientation with components facing down results in maximum PCB flexure and, thus, the worst orientation for failures. Therefore, this document requires that the board shall be horizontal in orientation with components facing in downward direction during the test. Drop testing using other board orientations is not required but may be performed if deemed necessary. However, this is an additional test option and not a replacement for testing in the required orientation.

This document requires test condition B (15 000 $m \cdot s^{-2}$, 0,5 ms duration, half-sine pulse), as listed in Table 1 of IEC 60749-10:2022, as the input shock pulse to the printed circuit assembly. This is the applied shock pulse to the base plate and shall be measured by accelerometer mounted at the centre of base plate or close to the support posts for the board. The velocity change of the drop pulse shall be also controlled and maintained at 4,67 m/s. The calculation of the velocity change is defined by the effective pulse where the acceleration must be equal to or above 1 500 $m \cdot s^{-2}$ as shown in Figure 2. No rebounces are allowed in this calculation.

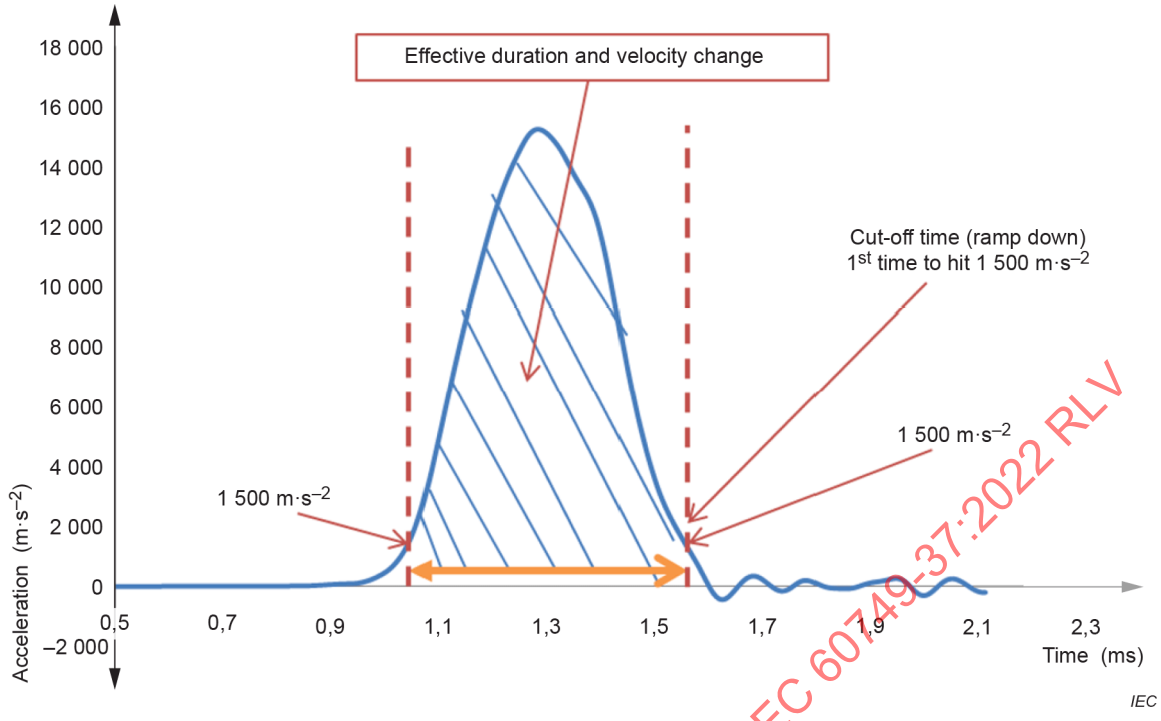


Figure 2 – Calculation of velocity change

5.2 Pre-test characterization

A set-up board with components mounted on it shall be used to adjust and characterize the drop test parameters and board response. A lightweight accelerometer is attached with (using suitable adhesive) in the centre of the mounting plate. Since the board weight is negligible as compared to mounting plate, setup characterization without a test board will not alter the results. Both the accelerometer and the strain gauge shall be connected to a data acquisition system capable of measuring at a scan frequency of 20 kHz and greater with a 16-bit signal width. Additional strain gauges can also be mounted at different locations on the board to fully characterize the strain response of the assembly.

The board assembly shall then be mounted on the drop test fixture using four screws. The screws shall be tightened in diagonal pattern in the order of SW, NE, SE, and NW corners of the board. An additional accelerometer may also be mounted on the board assembly at or close to one of the support locations to ensure that the input pulse to the base plate is transmitted to the PCB without any distortion. The drop table shall then be raised to the height required to meet test condition B of Table 1 of IEC 60749-10:2022 and dropped on to the strike surface while measuring the G level, pulse duration, and pulse shape.

The acceleration pulse shall follow a half-sine curve with a peak acceleration of 1 500 $m \cdot s^{-2}$ during each drop as shown in Figure 2. Multiple drops can be required while adjusting the drop height and impact surface to achieve the specified peak acceleration and change of velocity (1 500 $m \cdot s^{-2}$, 4,67 m/s respectively). The variations of the peak acceleration and change of velocity needs to be controlled within 10 % on each individual measurement and 5% tolerance on average when 20 repeating measurements. The change of velocity is the total area enclosed by the acceleration pulse and the time axis. An effective change of velocity shall be counted in which only an acceleration equal to or higher than 1 500 $m \cdot s^{-2}$ is considered and any rebounces after the acceleration dropping to below 1 500 $m \cdot s^{-2}$ from the peak shall be ignored in the calculation. The time duration for defining the area of effective change of velocity is called effective pulse duration and shall also be maintained at 0,5 ms within 15 % tolerance which is in accordance with IEC 60749-10. The test equipment and transducer shall have a natural frequency greater than 5 times the frequency of the shock pulse being established, and measured through a low-pass filter having a bandwidth greater than 5 times the frequency of the shock pulse being established, see detail in IEC 60749-10. However, both unfiltered and

filtered acceleration profiles shall be reported for the comparison purposes. It shall be noted that these pulse parameters are function of not only the drop height but also the impact surface. Depending on the strike surface, the same drop height could result in different acceleration levels and pulse durations. Theoretically, the drop height needed to achieve the appropriate acceleration levels can be determined from Equations (1) and (2) and the associated Figure 3, where H is the drop height and C is the rebound co-efficient (1,0 for no rebound, 2,0 for full rebound). However, this equation does not include the strike surface effect.

Experiments with different strike surfaces can be necessary to achieve the desired peak value and duration.

$$A(t) = A_0 \sin\left(\frac{\pi t}{t_w}\right) \quad (1)$$

$$\sqrt{2gH} = A_0 \sin\left(\frac{2A_0 t_w}{C\pi}\right) \quad (2)$$

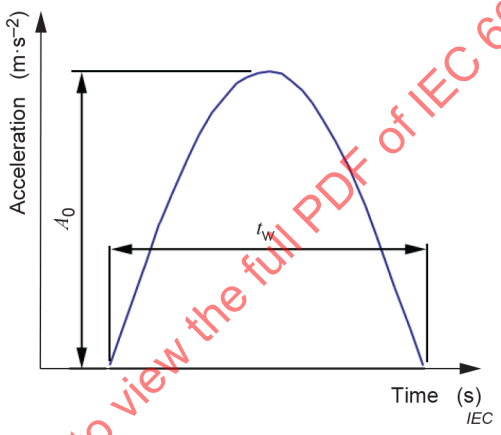


Figure 3 – Typical shock test half-sine pulse graphic and formulae

Once the specified drop parameters (acceleration level, duration and pulse shape) are achieved, the PCB response acceleration and strain shall be measured. The strain rate shall also be calculated by dividing the change in strain value by the time interval during which this change occurred. The characterized board response (acceleration, strain and strain rate) and its variation shall be documented and provided with the test data. Although it is recommended that this characterization be performed for previously untested components, this may not be required if such characterization data are available for a similar sized component.

5.3 Drop testing

With test parameters adjusted and PCB response characterized, the PCB assemblies shall be prepared for drop testing. This involves soldering cables to the plated-through holes on one end of the board, mounting the board on the drop fixture with components facing down, and connecting cables to the event detector/data logger. Since the dynamic response of the board can be affected by the mass and stiffening of the connector, it is recommended that no connectors are used and wires are directly soldered to the board.

The event detector's threshold resistance shall be set to no more than 1 000 Ω. The system used for such event detections shall have a 55 MHz scan rate or 0,2 µs (or lower) event detection window. Proper strain relief shall also be provided to cables/wires to avoid a failure at wires to board interconnects. All cables shall be cleared from the drop path. The initial resistance of all nets for each assembly shall be measured and logged before conducting the first drop. The drop test shall be conducted by releasing the drop table from the pre-established

height. The electrical resistance of each net shall be measured in situ during each drop and all failures shall be logged. The board shall be dropped a required maximum number of times or until a percentage of all devices has failed, whichever is earlier. The maximum number of drops or percentage of devices failing shall be consistent with the application. The maximum number of drops shall be irrespective of single or double-sided assembly. In the event that a shock condition in addition to the required condition B is used to conduct the test, the maximum number of drops shall be determined using the acceleration factor between the two conditions for similar sized components. This acceleration factor shall be reported with the test data.

During the test, the shock pulse shall be measured for each drop to ensure that the input pulse remains within the specified tolerance. Adjustments in drop height or replacement of strike surface shall be made if the pulse deviates from that specified.

Depending on the number of components per board, Table 1 shall be used to determine the number of boards to be tested per component type.

6 Failure criteria and failure analysis

In-situ electrical monitoring of daisy chain nets for failure is required during each drop. The electrical continuity of all nets shall either be detected by an event detector or by a high-speed data acquisition system. The event detector shall be able to detect any intermittent discontinuity of resistance greater than 1 000 Ω lasting for 1 µs or longer. The high-speed data acquisition system shall be able to measure resistance with a sampling rate of 50,000 samples per second or greater.

Depending on the monitoring system used, the failure is defined as follows:

– **event detector**: the first event of intermittent discontinuity as defined above followed by 3 additional such events during 5 subsequent drops.
– **high speed data acquisition**: the first indication of resistance value of 100 Ω or 20 % increase in resistance from the initial resistance if initial resistance is greater than 85 Ω followed by 3 additional such indications during 5 subsequent drops.

A visible partial separation of component from the test board, even without a significant increase in resistance or intermittent discontinuity, shall also be considered as a failure. This can occur if the PCB tracks come off the board with the component while maintaining electrical continuity.

As wires soldered to the board for electrical continuity test can also come off during the test, it is highly recommended that all electrical connections be checked once a failure is indicated to ensure that the failure is due to a component to board interconnection failure.

All failures after each drop shall be logged. A sufficient number of components from the test lot shall be subjected to failure analysis to determine the root cause and to identify failure mechanism. The selection of components shall cover different locations on the board. Different methods and equipment, such as visual inspection, cross-section, dye and pry, chemical etching, scanning electron microscopy, and scanning acoustic tomography can be employed to determine the root cause of failure. The failure site shall be clearly identified as ‘component failure’, ‘interconnect failure’ or ‘board failure’. For the purpose of this document, the “interconnect failure” is defined as any failure

a) on the package pad – joint interface or intermetallics,
b) through the joint material,
c) on the PCB pad joint interface or intermetallics.

The above criteria may always be overridden by an applicable procurement document.

Data analysis shall be conducted showing mean and standard deviation of failure data according to component groupings. Weibull and/or log normal analysis result shall also be included if sufficient quantities have failed for such analyses.

7 Summary

All test reports shall include the following information:

a) number of packages per board;

b) package and PCB assembly weight;

c) package geometrical details including body size, lead size, ball size, layer thickness and die size;

d) package materials including mould compound, die attach, substrate;

e) PCB information, including materials, surface finishes, pad design type, board thickness, layer count and etc.;

f) board geometry, material and material properties such as thickness, pad size, modulus and T_g;

g) board assembly details including stencil thickness, apertures, stencil material, solder alloy and paste, reflow profile and other board assembly process details;

h) test details: drop height, strike surface, shock pulse profile;

i) board response (acceleration, strain and strain rate);

j) shock table response (shock parameter including peak acceleration, velocity change, time duration, number of spots/locations on table tested and repetitions, tolerance report of those measurements; filtering frequency for acceleration;

k) initial resistance of daisy chain nets;

l) failure detection equipment and failure criteria;

m) test results including the number of drops to failure for each location on each test board, failure mechanisms and representative pictures;

n) data analysis showing mean and standard deviation of failure data according to component groupings.

Annex A
(informative)

Preferred board construction, material, design and layout

A.1 Preferred board construction, material and design

The preferred test board should use built-up multilayer technology incorporating microvias using 1+6+1 stack-up. This is recommended because typical PCB assemblies used in handheld electronic systems are constructed using high density, build-up technology. The test board should have a nominal thickness of 1,0 mm. A thinner board (0,8 mm) can also be used but correlation between the drop test performance and the different board thicknesses needs to be established. Table A.1 provides the thickness, copper coverage and material for each layer. The dielectric materials should meet the mechanical properties given in Table A.2. The PCB should have organic solderability preservatives (OSP) as surface finish to avoid any copper oxidation before component mounting. The glass transition temperature, T_g, of each dielectric material, as well as of the composite board, should be 130 °C or greater. The modulus and T_g of the dielectric materials should be specified. The composite values (modulus and T_g) should be measured on at least one representative test board at the component mounting location. The boards should be symmetrical in construction about the mid-plane of the board, except for the minor differences in the top and bottom two layers.

Table A.1 – Test board stack-up and material

Board layer	Thickness µm	Copper coverage %	Material
Solder mask	20		LPI [a]
Layer 1	25	Pads + traces (via in pad)	Copper
Dielectric 1-2	60		FR4 [b,c]
Layer 2	25	40 % 70 % including daisy chain links	Copper
Dielectric 2-3	60		FR4 [c]
Layer 3	18	70 %	Copper
Dielectric 3-4	100		FR4 [c]
Layer 4	18	70 %	Copper
Dielectric 4-5	100		FR4 [c]
Layer 5	18	70 %	Copper
Dielectric 5-6	130		FR4 [c]
Layer 6	18	70 %	Copper
Dielectric 6-7	100		FR4 [c]
Layer 7	18	70 %	Copper
Dielectric 7-8	100		FR4 [c]
Layer 8	18	70 %	Copper
Dielectric 8-9	60		FR4 [c]
Layer 9	25	70 %	Copper
Dielectric 9-10	60		FR4 [b,c]
Layer 10	25	Pads + traces + daisy chain links (no via in pad)	Copper
Solder mask	20		LPI [a]

[a] Liquid photo-imageable.

[b] Resin-coated copper; usage as an alternative to FR4 shall be documented.

[c] Details of the FR4 material shall be documented.

Table A.2 – Mechanical property requirements for dielectric materials

Property	Unit	FR4	RCC
Tensile strength	MPa	>100	>50
Tensile modulus	GPa	20 ± 2	2 ± 1
Tensile elongation	%	>3	>3
In-plane CTE (below T_g)	ppm/°C	14 ± 3	60 to 80
T_g	°C	>130	>130
Cu peel	N/mm	>1	>1

Since a typical product board may have a combination of microvias in pad and no vias in pad for area array packages for routing purposes, it is required that such components (BGAs, CSPs, etc.) be tested on boards with both microvia and non-microvia PCB pads. This should be accomplished by designing double-sided boards with mirror component footprints on each side (top and bottom) of the board. The board side A should have microvias in pads ("via in pad") on all component mounting pads while the board side B should have no microvias in pads ("no via in pads"). For board side A, the microvias in pads should be created with laser ablation with a via diameter of 110 µm. The vias should then be plated resulting in straight or near straight walls. The capture pad diameter should be at least 220 µm. Although two-sided boards should be designed, the component should only be mounted on one side at a time, resulting in two, single-sided assemblies ("side A assembly" and "side B assembly"), unless the component is anticipated for use in mirror-sided board assemblies. In that case, the components should be mounted on each side of the board.

As perimeter-leaded devices do not typically require microvia in pad, the test board for such devices (TSOP, quad flat pack, etc.) does not need to include microvias. The board should still be designed as double-sided with footprint of similar sized components on each side.

Although daisy-chain nets will typically not require plated-through holes (PTH) other than those required for manual probe pads and connectors, the test board should contain PTH in the component region (1,2 × the area covered by component) to approximate the mechanical effect of vias on actual application boards.

It is recommended that there should be 20 plated-through holes per square centimetre in the component region. The actual location and distribution of plated-through holes will depend on component size and I/O. The through holes should have a drill diameter of 300 µm and a finished plated hole diameter of 250 µm. The PTH pad diameters should measure 550 µm for the outer layer and 600 µm for the inner layers. It is recommended that the component mounting pads on the PCB be designed in accordance with the specification in Table A.3 for area array devices. The pad design for leaded and perimeter I/O devices should be in accordance with relevant national or international guidelines. All component attachment pads should be non-solder-mask-defined (NSMD) with solder mask clearance of 75 µm between the edge of the pad and the edge of solder mask. A smaller clearance can be used, as long as it does not cause any solder mask encroachment on pads due to mis-registrations.

Solder mask registration tolerance should not exceed 50 µm.

Table A.3 – Recommended test board pad sizes and solder mask openings

Component I/O pitch mm	PCB pad diameter mm	Solder mask opening mm
0,4	0,25	0,32
0,50	0,28	0,43
0,65	0,30	0,45
0,75 to 0,80	0,35	0,50
1,00	0,45	0,60

The track widths on the suggested test board should be 75 µm within the component area. This includes all tracks making contact with solder joint interconnect as well as with all internal layers. A track width of 100 µm should be used for all tracks outside of the component region. The board should have a matching daisy chain pattern such that one or multiple nets are formed through all interconnects after component mounting. Wherever necessary, additional test points within each net may be incorporated for failure location identification. Each additional test point should be clearly labelled using the row column format of the package. All routing and tracks within and just outside the component footprint should be done on layer 2 and layer 8 for area array packages and layer 1 and layer 8 for perimeter leaded packages.

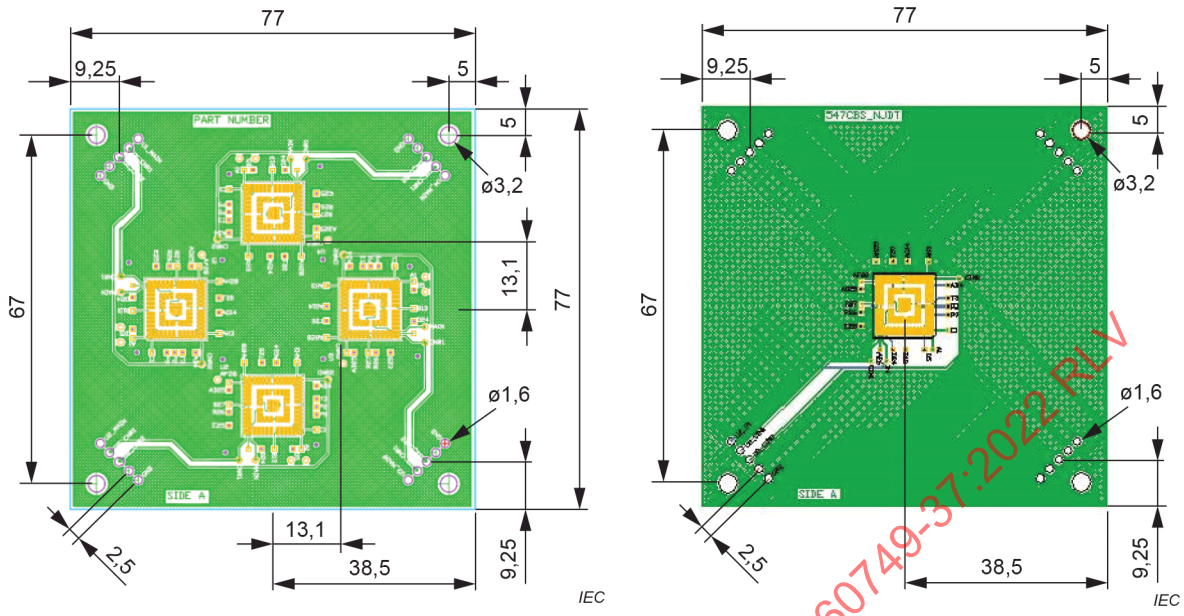
The suggested test board should have component mounting features such as Pin 1 identification and global/local fiducials.

A.2 Preferred test board size, layout, and component locations

The board footprint and layout is shown in Figure A.1. The overall board size is a 77 mm by 77 mm square board. The total number of components per board is 4 with an option of 1 component per board. In the case of four (4) components per board, these components are mounted orthogonally and totally symmetric with each other from the board center to the package edge with a distance of 13,10 mm. The maximum component size should be no more than 15 mm in length or width for the case of 4 components per board. All 4 sites on each side of the board (top and bottom) should have the same component footprint. A “common” footprint for multiple components can also be used if daisy chain requirements, as specified in 5.2, are met.

The daisy chain can be arranged as outer corner, inner corner and the main chain for each component. The outer corner chain contains the corner-most balls on the outer corners, i.e., these two corners are closer to the board edge. The inner corner chain contains the corner-most balls on two inner corners, i.e., these two corners are closer to the board centre. These corner balls should also be daisy-chained separately if the number of channel of monitoring is not limited. The remaining balls can be chained together and called main chain. All components should be the same and mix of different component sizes and styles should not be used on the same board, as this will affect the dynamic response of the board, making the results difficult to analyze.

Dimensions in millimetres



a) For 4 components

b) For one component

Figure A.1 – Board footprint and BGA layout

The mounting board used on the drop test fixture is designed with four holes. The locations of these holes are shown in Figure A.1. In the case of 4 components, all components shall be located with a distance of 13,10 mm from the inner edge of the component to the board center. The four components are numbered as U1, U2, U3, and U4, which are located at 12, 3, 6, and 9 o'clock, respectively. The area of the board in the length direction outside of components is restricted for labeling, through holes, edge fingers, and any other fixtures, if needed. As illustrated in Figure A.1, there is a space for a 5-pin plated through hole (PTH) connector on each corner, even though the connector is not to be mounted. The minimum gap of these holes to the screw hole as well as to any component edge should be 5 mm. These plated through holes provide the solder wiring for functional continuity test which can be done on each side (top and bottom) of the board.

For the option of 1 component per board, the component is mounted in the center of the board as shown in Figure A.1 b). In this case, screw holes and 5-pins PTH holes should remain in every corner (the same as those in the 4-component case). This is to ensure the total symmetric design for the board. This design may be used for a component with a larger body such as 17 mm. However, this should be clearly specified in the drop test report if one component per board is used. Figure A.2 provides an illustration that integrates both 4 component placement (primary board side) and option of single component (bottom site of board).

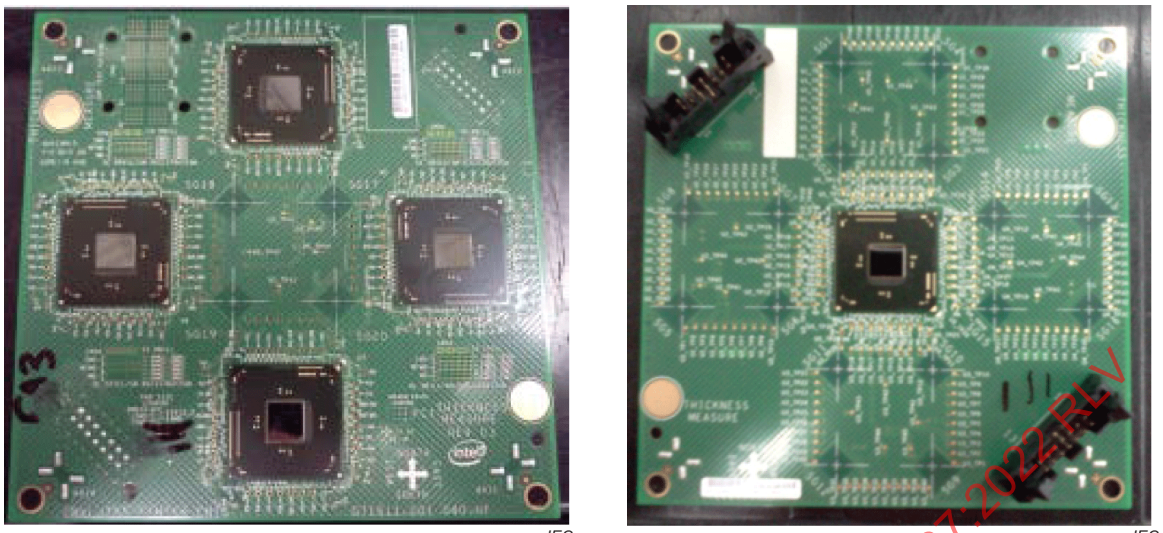


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Figure A.2 – Test vehicle with 4 component placement (top side – left) and 1 component at center location (bottom side – right).

Since the drop test performance is a function of the test board used for evaluation, this document defines a preferred test board construction, dimensions, and material that is representative of those used in handheld electronic products. If another board construction/material better represents a specific application, the test board construction, dimensions and material should be documented. The test data generated using such a board should be correlated at least once by generating the same data on same component using the preferred board defined in this document.

If materials or specifications are used other than those mentioned in this document, they should be clearly reported in the documentation.

Bibliography

IEC 60749-40, *Semiconductor devices – Mechanical and climatic test methods – Part 40: Board level drop test method using a strain gauge*

"Shock risk assessment of BGA components – Importance of physics based metrics"; Rahmani, H.; Vujosevic, M.; Pei, M, Proc. of ASME Int'l. Conf. on Nanochannels, Microchannels and Minichannels; San Francisco, CA; July 2015

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COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

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DISPOSITIFS À SEMICONDUCTEURS – MÉTHODES D'ESSAIS MÉCANIQUES ET CLIMATIQUES –

Partie 37: Méthode d'essai de chute au niveau de la carte avec utilisation d'un accéléromètre

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Cette deuxième édition, fondée sur le document JESD22-B111A du JEDEC, annule et remplace la première édition parue en 2008. Ce document est utilisé avec la permission du propriétaire des droits, JEDEC Solid State Technology Association. Cette édition constitue une révision technique.

Cette édition inclut les modifications techniques majeures suivantes par rapport à l'édition précédente:

a) correction d'une erreur technique précédente concernant les conditions d'essai;

b) mises à jour afin de refléter les progrès technologiques.

Le texte de cette Norme internationale est issu des documents suivants:

Projet	Rapport de vote
47/2651/CDV	47/2719/RVC

Le rapport de vote indiqué dans le tableau ci-dessus donne toute information sur le vote ayant abouti à son approbation.

La langue employée pour l'élaboration de cette Norme internationale est l'anglais.

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Une liste de toutes les parties de la série IEC 60749, publiées sous le titre général *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques*, se trouve sur le site web de l'IEC.

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INTRODUCTION

Les produits électroniques portatifs s'adaptent aux segments du marché de consommation et des portables. Les produits électroniques portatifs comprennent les appareils photo, les calculatrices, les téléphones cellulaires, les téléphones sans fil, les appareils de messagerie, les PC en format de poche, les cartes de l'association internationale pour la carte à mémoire pour ordinateur personnel (PCMCIA – *personal computer memory card international association*), les cartes à puce intelligentes, les assistants personnels numériques (PDA – *personal digital assistant*) et les autres produits électroniques que l'on peut ranger de manière pratique dans la poche et utiliser en les tenant dans la main.

Ces produits électroniques portatifs sont plus sujets à une chute au cours de leur durée de vie utile du fait de leur taille et de leur poids. Cet événement de chute peut non seulement provoquer des défaillances mécaniques dans le boîtier du dispositif, mais aussi créer des défaillances électriques aux cartes de circuit imprimé (PCB – *printed circuit board*) équipées montées à l'intérieur du boîtier, en raison du transfert d'énergie à travers les supports PCB. Les défaillances électriques résultent parfois de divers modes de défaillances tels que les craquelures de la carte de circuit imprimé, les craquelures de pistes sur la carte, les craquelures des interconnexions soudées entre les composants et la carte et les fissures de composants. Ce qui motive essentiellement ces défaillances est la flexion excessive de la carte de circuit imprimé en raison de l'accélération produite sur la carte par la chute du produit électronique portatif. Cette flexion de la carte provoque un mouvement relatif entre la carte et les composants montés sur celle-ci, donnant lieu à des défaillances de composants, d'interconnexion ou de carte. La défaillance dépend de la combinaison de la conception de la carte, de sa construction, de son matériau, de son épaisseur et de sa finition de surface, du matériau d'interconnexion et de la dimension des supports de la carte et de la taille des composants.

La corrélation entre les conditions d'essai et sur site n'est pas encore totalement établie. En conséquence, la procédure d'essai est actuellement plus appropriée pour une performance relative de composants que pour une utilisation en tant que critère d'acceptation/de refus. Plus exactement, les résultats peuvent être utilisés pour accroître les données existantes ou établir une ligne de base en vue d'efforts d'investigation potentiels dans les technologies de boîtiers/cartes.

La comparabilité entre les différents sites d'essai, méthodes d'acquisition de données et fabricants de cartes n'a pas encore été totalement démontrée par les données existantes. Par conséquent, si les données doivent être utilisées pour une comparaison directe de performance de composants, des études adaptées seront d'abord réalisées pour prouver que les données sont en fait comparables à travers les différents sites d'essai et conditions d'essai.

Cette méthode n'est pas destinée à remplacer les essais de caractérisation complète qui pourraient incorporer des tailles d'échantillons beaucoup plus grandes et un nombre accru de chutes. Dans le cas présent, en raison de la taille des échantillons et du nombre de chutes limités spécifiés, il est possible que des données de défaillances suffisantes ne soient pas produites dans chaque cas pour réaliser l'analyse statistique complète.

DISPOSITIFS À SEMICONDUCTEURS – MÉTHODES D'ESSAIS MÉCANIQUES ET CLIMATIQUES –

Partie 37: Méthode d'essai de chute au niveau de la carte avec utilisation d'un accéléromètre

1 Domaine d'application

La présente partie de l'IEC 60749 fournit une méthode d'essai destinée à évaluer et comparer la performance de chute des composants électroniques à montage en surface dans des applications de produits électroniques portatifs dans un environnement d'essai accéléré, où une flexion excessive d'une carte de circuit imprimé provoque une défaillance de produit. Le but est de normaliser la carte d'essai et la méthodologie d'essai pour fournir une évaluation reproductible de la performance d'essai de chute des composants à montage en surface, en reproduisant les mêmes modes de défaillances que ceux observés normalement au cours d'un essai au niveau du produit.

Le présent document a pour objet de spécifier une méthode d'essai normalisée et une procédure de rapport. Il ne s'agit pas d'un essai d'homologation de composants et il n'est pas destiné à remplacer un essai de chute au niveau système qui est parfois utilisé pour homologuer un produit électronique portatif spécifique. La norme n'est pas prévue pour couvrir l'essai de chute exigé pour simuler les chocs liés au transport et à la manipulation de composants électroniques ou des cartes de circuit imprimé équipées. Ces exigences sont déjà abordées dans des méthodes d'essai telles que celles de l'IEC 60749-10. La méthode est applicable tant aux boîtiers à montage en surface en groupement bidimensionnel qu'aux sorties localisées en périphérie du composant.

Cette méthode d'essai utilise un accéléromètre pour mesurer la durée des chocs mécaniques et l'amplitude appliquée qui est proportionnelle à la contrainte sur un composant donné monté sur une carte normalisée. La méthode d'essai décrite dans l'IEC 60749-40 utilise une jauge de contrainte pour mesurer la contrainte et le taux de contrainte d'une carte au voisinage d'un composant. La spécification du client indique quelle méthode d'essai est à utiliser.

2 Références normatives

Les documents suivants sont cités dans le texte de sorte qu'ils constituent, pour tout ou partie de leur contenu, des exigences du présent document. Pour les références datées, seule l'édition citée s'applique. Pour les références non datées, la dernière édition du document de référence s'applique (y compris les éventuels amendements).

IEC 60749-10:2022, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 10: Chocs mécaniques – Dispositif et sous-ensemble*

IEC 60749-20, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 20: Résistance des CMS à boîtier plastique à l'effet combiné de l'humidité et de la chaleur de brasage*

IEC 60749-20-1, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 20-1: Manipulation, emballage, étiquetage et transport des composants pour montage en surface sensibles à l'effet combiné de l'humidité et de la chaleur de brasage*

3 Termes et définitions

Pour les besoins du présent document, les termes et définitions suivants s'appliquent.

L'ISO et l'IEC tiennent à jour des bases de données terminologiques destinées à être utilisées en normalisation, consultables aux adresses suivantes:

IEC Electropedia: disponible à l'adresse https://www.electropedia.org/

ISO Online browsing platform: disponible à l'adresse https://www.iso.org/obp

3.1
composant
dispositif à semiconducteurs encapsulé (sous boîtier)

3.2
ensemble simple face
carte de circuit imprimé équipée dont les composants sont montés sur un seul côté de la carte

3.3
ensemble double face
carte de circuit imprimé équipée dont les composants sont montés sur les faces supérieure et inférieure de la carte

3.4
produit électronique portatif
produit que l'on peut ranger de manière pratique dans une poche (de taille suffisante) et utiliser en le tenant dans la main

Note 1 à l'article: Les produits électroniques portatifs comprennent les appareils photo, les calculatrices, les téléphones cellulaires, les appareils de messagerie, les PC tenant dans la paume de la main (précédemment appelés "organiseurs de poche", les cartes de l'association internationale pour la carte à mémoire pour ordinateur personnel (PCMCIA), les cartes à puce intelligentes, les téléphones mobiles, les assistants personnels numériques (PDA) et autres dispositifs de communication.

3.5
accélération de crête
accélération maximale au cours du mouvement dynamique de l'appareillage d'essai

3.6
durée d'impulsion
intervalle d'accélération
iintervalle de temps entre l'instant où l'accélération atteint pour la première fois 10 % de son niveau de crête spécifié et l'instant où l'accélération revient pour la première fois à 10 % du niveau de crête spécifié après avoir atteint ce niveau de crête

3.7
hauteur de chute d'une table de chute
hauteur de chute libre de la table de chute nécessaire pour atteindre l'accélération de crête et la durée d'impulsion spécifiées

3.8
événement
discontinuité électrique de résistance supérieure à 1 000 Ω d'une durée de 1 µs ou supérieure

3.9
détecteur d'événement
appareil de contrôle de la continuité capable de détecter la discontinuité électrique de résistance supérieure à 1 000 Ω d'une durée de 1 µs ou supérieure

4 Appareillage d'essai et composants d'essai

4.1 Appareillage d'essai

L'appareillage d'essai de chocs doit être capable de procurer des impulsions de choc jusqu'à une accélération de crête de 2 900 $m \cdot s^{-2}$ avec une durée d'impulsion comprise entre 0,3 ms et 8,0 ms au corps du dispositif et une variation de la vitesse de 1 250 $mm \cdot s^{-1}$ à 5 430 $mm \cdot s^{-1}$. Pour les essais à l'état libre, une variation de la vitesse de 1 250 $mm \cdot s^{-1}$ à 5 430 $mm \cdot s^{-1}$ et une durée d'impulsion comprise entre 0,3 ms et 2,0 ms sont suffisantes. A l'inverse, pour les essais à l'état monté, un appareillage capable d'appliquer au corps du composant une variation de la vitesse de 1 000 $mm \cdot s^{-1}$ à 5 430 $mm \cdot s^{-1}$ et une durée d'impulsion comprise entre 5,0 ms et 8,0 ms est suffisant.

L'impulsion d'accélération doit avoir une forme semi-sinusoïdale avec un écart admissible par rapport à l'accélération de crête spécifiée inférieur ou égal à ±10 %. La variation de la vitesse d'essai doit être de ±10 % du niveau spécifié. La durée de l'impulsion doit être mesurée entre les points à 10 % de l'accélération de crête pendant le temps de montée et à 10 % de l'accélération de crête pendant le temps de descente. Les tolérances absolues de la durée d'impulsion doivent être égales à ±15 % de la durée spécifiée. Le transducteur du matériel d'essai doit avoir une fréquence naturelle supérieure à 5 fois la fréquence de l'impulsion de choc établie et mesurée par l'intermédiaire d'un filtre passe-bas dont la largeur de bande est supérieure à 5 fois la fréquence de l'impulsion de choc établie. Le filtrage ne doit pas remplacer un bon montage de mesures et de bonnes pratiques de procédure.

Un étalonnage approprié du matériel doit être effectué avant tout essai.

4.2 Composants d'essai

Le présent document couvre tous les dispositifs à semiconducteurs sous boîtier à montage en surface en groupement bidimensionnel et à sorties localisées en périphérie de boîtier, tels que les boîtiers à billes (BGA – *ball grid arrays*), les boîtiers à aires de brasure (LGA – *land grid arrays*), les boîtiers de taille proche de celle des puces (CSP – *chip scale packages*), les boîtiers minces de faible encombrement (TSOP – *thin small outline packages*), et les boîtiers minces carrés sans pattes (QFN – *quad flat no-lead packages*) généralement utilisés dans les produits électroniques portatifs. La dimension maximale du corps du composant couverte par le présent document est généralement de 15 mm x 15 mm. Une dimension de corps plus importante peut être utilisée pour une disposition de carte particulière, comme cela est décrit en détail en 4.3. Tous les composants utilisés pour cet essai doivent être de type à connexion en chaîne. Cette connexion en chaîne est établie au niveau de la puce ou en établissant des liaisons de connexion en chaîne au niveau de la grille de connexion ou au niveau du matériau de base. Dans le cas de puce sans chaîne de connexion, une puce mécanique fictive doit être utilisée à l'intérieur du boîtier pour simuler la structure réelle du boîtier. La taille et l'épaisseur de la puce doivent être analogues à la taille fonctionnelle de la puce à utiliser dans l'application. Les matériaux, les dimensions et les processus d'assemblage du composant doivent être représentatifs du dispositif de production type.

4.3 Carte d'essai

Sachant que la performance d'essai de chute dépend de la carte d'essai utilisée pour l'évaluation, le présent document décrit une construction, des dimensions et un matériau de carte d'essai préférentiels qui sont représentatifs de ceux utilisés dans les produits électroniques portatifs. Dans le cas où une autre construction ou un autre matériau propose une meilleure représentation d'une application particulière, la construction, les dimensions et le matériau de la carte d'essai doivent être documentés. Les données d'essai produites lors de l'utilisation d'une telle carte doivent être corrélées au moins une fois en produisant des données identiques sur le même composant par l'utilisation de la carte préférentielle définie dans le présent document (voir les recommandations de l'Annex A).

4.4 Assemblage de cartes d'essai

Avant l'assemblage des cartes, tous les dispositifs doivent être examinés pour détecter des billes manquantes ou des connexions pliées. L'épaisseur de la carte, le gauchissement et les tailles des pastilles doivent également être mesurés en utilisant un plan d'échantillonnage. Un examen visuel doit être réalisé sur toutes les cartes pour l'application du vernis épargne, la contamination et la connexion en chaîne. Il est recommandé d'examiner et d'accepter les cartes conformément à une norme nationale ou internationale appropriée. Une carte doit également être utilisée pour mesurer les propriétés mécaniques (module et température de transition vitreuse, T_g) de la carte à l'emplacement du composant en utilisant des méthodes d'analyse mécanique dynamique (DMA – *dynamic mechanical analysis*) et d'analyse thermomécanique (TMA – *thermomechanical analysis*). Il est hautement recommandé de mesurer aussi le coefficient de dilatation thermique (CTE – *coefficient of thermal expansion*) de la carte dans les sens X, Y, et Z. Les mesurages des propriétés mécaniques ne sont pas exigés pour chaque lot de cartes, à moins qu'un changement de processus de fabrication, de matériau ou de fournisseur n'intervienne de lot en lot.

Les composants doivent être étuvés selon l'IEC 60749-20 et l'IEC 60749-20-1 avant l'assemblage de cartes. Les cartes d'essai doivent être assemblées en utilisant les meilleures méthodes connues du processus d'assemblage des circuits imprimés, représentatives des méthodes de production. Au moins une carte doit être utilisée pour régler le procédé de montage de carte tel que le dépôt de pâte à braser par impression, le positionnement de la pâte et le profil de refusion. Tous les ensembles doivent être à simple face uniquement, sauf si une utilisation du composant dans les ensembles de cartes à face en miroir est prévue. Dans ce cas, les composants doivent être montés sur chaque face de la carte.

Un examen au rayonnement X 100 % est recommandé sur les unités assemblées pour vérifier les vides, les courts-circuits et autres anomalies. L'essai de continuité électrique doit également être réalisé sur toutes les unités montées pour détecter tout circuit ouvert ou court-circuit.

4.5 Nombre de composants et taille d'échantillons

La conception de la carte recommandée dans l'Annex A permet 4 emplacements pour le montage des composants et le montage des 4 composants est recommandé. Sachant que la carte est conçue avec une symétrie complète, il est attendu que les 4 composants soient soumis à une performance de chute identique et de ce fait, les résultats des essais sont traités comme un seul groupe. Une analyse statistique de l'équivalence des données est suggérée pour garantir que la variabilité dans la performance des composants est insignifiante avant tout suivi par des données exhaustives ou une homologation complète. Afin d'obtenir des résultats significatifs sur le plan statistique, une quantité totale minimale de 6 cartes ou 24 composants est recommandée pour chaque conception.

Sachant que le nombre et la taille des composants montés sur la carte peuvent influencer la réponse dynamique de la carte d'essai équipée au cours de la chute, il est exigé que des données supplémentaires soient fournies à chaque fois que la configuration à 1 composant est employée. Les données supplémentaires doivent comparer directement l'effet du montage de composants facultatifs (cas à 1 composant) à la configuration de montage à 4 composants privilégiée. Cette comparaison doit être fournie pour un composant similaire du point de vue de la taille (de l'ordre de 20 % tant en longueur qu'en largeur) au composant qui a été soumis à l'essai en utilisant uniquement la configuration à 1 composant par carte.

Dans le cas d'un montage à 1 composant sur la carte, le Tableau 1 doit être utilisé pour déterminer la quantité minimale de cartes assemblées exigée pour les essais et le nombre total de composants à soumettre à l'essai. Des tailles d'échantillons supérieures à celles spécifiées ci-dessous peuvent également être utilisées pour produire des données statistiquement suffisantes.

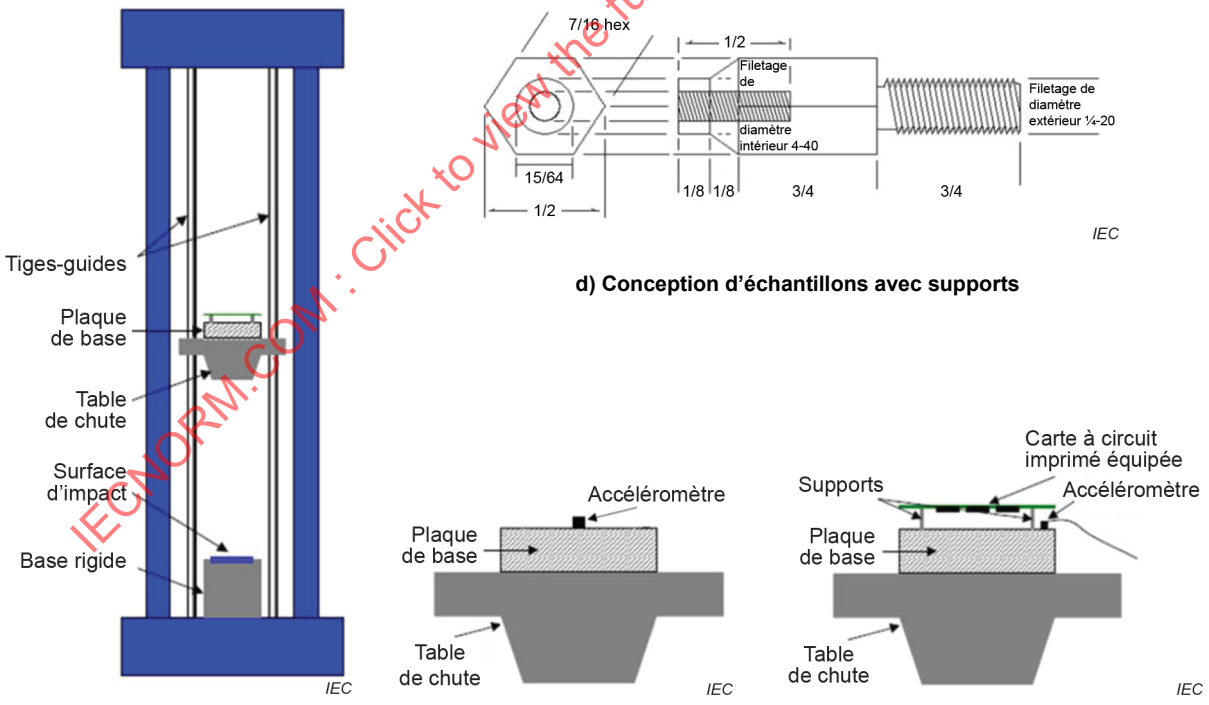
Tableau 1 – Quantité de cartes d'essai et de composants exigés pour les essais

Nombre de composants par carte	Emplacement	Nombre de cartes		Nombre total de composants
		Assemblage face A (trou de liaison dans la pastille)	Assemblage face B (sans trou de liaison dans la pastille)	
4	U1, U2, U3 et U4	6	6	48
1	Centre de la carte	16	16	32

5 Procédure d'essai

5.1 Matériels et paramètres d'essai

L'appareillage d'essai aux chocs doit être monté sur une table de laboratoire robuste, ou sur un support équivalent, et avec une mise à niveau avant utilisation. Des dispositifs doivent être fournis dans l'appareillage (tels qu'un mécanisme de freinage automatique) pour éliminer les rebonds et pour prévenir les chocs multiples sur la carte. La Figure 1 représente l'appareillage d'essai de chute type dans lequel la table de chute effectue une course descendante sur des tiges-guides et vient heurter l'installation rigide. L'installation rigide est généralement couverte d'un certain type de matériau pour obtenir les niveaux d'impulsion et d'accélération souhaités. La partie inférieure de la table de chute est habituellement légèrement arrondie pour garantir une très petite zone de contact avec la surface d'impact.



a) Appareillage d'essai de chute type

b) Installation de précaractérisation sans carte d'essai

c) Installation d'assemblage avec carte

d) Conception d'échantillons avec supports

Figure 1 – Détail de l'appareillage d'essai de chute

Une plaque de base avec des supports adaptés doit être montée de manière rigide sur la table de chute. L'épaisseur et les emplacements de montage de la plaque de base doivent être sélectionnés de sorte qu'il n'y ait aucun mouvement relatif entre la table de chute et n'importe quelle partie de la plaque de base au cours de l'essai de chute. Cette plaque sert de structure

de montage pour les cartes de circuit imprimé équipées. Cela est représenté à la Figure 1. La carte de circuit imprimé équipée doit être montée sur des supports de la plaque de base au moyen de quatre vis, une à chaque coin de la carte. La carte doit être montée au moyen de quatre vis à épaulement de précision adaptées (telles que M3 × 0,5). Les données d'essai suggèrent que les variations de l'accélération de la réponse et de la contrainte sont réduites de manière significative en fonction du choix des vis. Étant donné que la longueur d'épaulement est nominale, un certain nombre de rondelles doit être placé entre la tête de vis et la surface supérieure de la carte (épaisseur de 1,0 mm nominale) pour éviter tout espace entre la partie supérieure des supports et la surface inférieure de la carte. Du fait de l'empilage de tolérance, un petit espace est toutefois possible mais celui-ci ne doit pas dépasser 50 µm. L'utilisation de vis à épaulement élimine la nécessité de resserrer les vis entre les chutes. Les vis doivent être serrées selon un schéma diagonal dans l'ordre des coins SO, NE, SE et NO de la carte. La vis doit être serrée jusqu'à ce que l'épaulement de la vis atteigne son plus bas niveau en se plaçant contre le support. Le nombre de rondelles utilisées doit être le même pour l'ensemble des quatre vis. Un gabarit adapté pour la carte peut être utilisé à la place du montage de la carte directement sur la plaque.

L'expérience avec différentes orientations de carte suggère que l'orientation horizontale de la carte dont les composants sont orientés vers le bas donne lieu à une flexion maximale de la carte (PCB) et, de ce fait, à l'orientation la plus défavorable pour les défaillances. Par conséquent, le présent document exige que la carte adopte une orientation horizontale et que les composants soient orientés vers le bas au cours de l'essai. L'essai de chute selon une autre orientation de carte n'est pas exigé mais peut être réalisé si cela est jugé nécessaire. Cependant, il s'agit d'une option d'essai additionnelle qui ne remplace pas l'essai dans l'orientation exigée.

Le présent document exige la condition d'essai B (15 000 $m \cdot s^{-2}$, 0,5 ms de durée, impulsion semi-sinusoïdale), comme cela est répertorié dans le Tableau 1 de l'IEC 60749-10:2022, comme l'impulsion de choc en entrée sur l'assemblage de circuits imprimés. Il s'agit de l'impulsion de choc appliquée à la plaque de base et elle doit être mesurée par l'accéléromètre monté au centre de la plaque de base ou à proximité des montants supports de la carte. La variation de la vitesse de l'impulsion de chute doit également être contrôlée et maintenue à 4,67 m/s. Le calcul de la variation de la vitesse est défini par l'impulsion effective pour laquelle l'accélération doit être égale ou supérieure à 1 500 $m \cdot s^{-2}$, comme représenté à la Figure 2. Aucun rebond n'est admis dans ce calcul.