IEC 60749-5

Edition 3.0 2023-12
REDLINE VERSION

INTERNATIONAL STANDARD

colour inside

Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test

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INTERNATIONAL
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IEC 60749-5 has been prepared by IEC technical committee 47: Semiconductor devices. It is an International Standard.

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This edition includes the following significant technical changes with respect to the previous edition:

a) the specification of the test equipment is changed to require the need to minimize relative humidity gradients and maximize air flow between semiconductor devices under test;
b) the specification of the test equipment fixtures is changed to require the avoidance of condensation on devices under test and on electrical fixtures connecting the devices to the test equipment;
c) replacement of references to “virtual junction” with “die”.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2820/FDIS	47/2827/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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- reconfirmed,
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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 5: Steady-state temperature humidity bias life test

1 Scope

This part of IEC 60749 provides a steady-state temperature and humidity bias life test to evaluate the reliability of non-hermetic packaged ~~solid-state~~ semiconductor devices in humid environments.

This test method is considered destructive.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-4, *Semiconductor devices – Mechanical and climatic test methods – Part 4: Damp heat, steady-state, highly accelerated stress test (HAST)*

3 Terms and definitions

No terms and definitions are listed in this document.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

4 General

~~This test employs conditions of~~ Temperature, humidity and bias ~~which~~ conditions are applied to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

Where both this steady-state, humidity bias test and the damp heat, highly accelerated stress test (HAST) of IEC 60749-4 are performed, the results of this 85 °C/85 % RH steady-state test will take priority over the results of the HAST test, which is an accelerated test designed to activate the same failure mechanisms.

5 Equipment

5.1 Equipment summary

The test requires a temperature-humidity test chamber capable of maintaining a specified temperature and relative humidity continuously, while providing electrical connections to the devices under test in a specified biasing configuration.

5.2 Temperature and relative humidity

The chamber shall be capable of providing controlled conditions of temperature and relative humidity during ramp-up to, and ramp-down from the specified test conditions.

~~Care should be taken to ensure that~~ The test chamber dry bulb temperature ~~exceeds~~ shall exceed the wet bulb temperature at all times.

5.3 Devices under stress

Devices under stress shall be physically located to minimize temperature gradients. Devices under test shall be physically located in order to minimize relative humidity gradients and maximize air flow between devices.

5.4 Minimizing release of contamination

~~Care shall be exercised in the choice of~~ Board and socket materials shall be chosen in order to minimize release of contamination, and to minimize degradation due to corrosion and other mechanisms.

5.5 Ionic contamination

~~The test apparatus (card cage, test boards, sockets, wiring, storage containers, etc.) shall be controlled to avoid ionic contamination of the test devices.~~

The test devices shall be placed in the test apparatus to minimise ionic contamination from items such as the card cage, test boards, sockets, wiring and storage containers.

5.6 Deionized water

Deionized water with a minimum resistivity of 1 × 104 Ωm at room temperature shall be used.

6 Test conditions

6.1 Test conditions summary

Test conditions consist of a temperature, relative humidity, and duration used in conjunction with an electrical bias configuration specific to the device.

6.2 Temperature, relative humidity and duration

Unless otherwise required by the detail specification, the temperature, relative humidity and test duration as shown in Table 1 shall be applied.

Table 1 – Temperature, relative humidity and duration

Temperature (dry bulb) °C	Relative humidity [a] %	Temperature [b] (wet bulb) °C	Vapour pressure [b] kPa	Duration [c] h
85 ± 2	85 ± 5	81,0	49,1	1 000 $^{-24}_{+168}$

[a] Tolerances apply to the entire useable test area.

[b] For information only.

[c] The test conditions are to be applied continuously, except during any interim readouts, when the devices should be returned to stress within the time specified in 7.6.

6.3 Biasing guidelines

Apply bias according to the following guidelines:

a) minimize power dissipation;

a) alternate pin bias as much as possible;

b) distribute potential differences across chip metallization as much as possible;

c) maximize voltage within operating range;

NOTE The priority of the above guidelines depends on the mechanism and specific device characteristics.

d) either of two kinds of bias can be used to satisfy these guidelines, whichever is more severe:

1) Continuous bias

The DC bias shall be applied continuously. ~~Continuous bias is more severe than cycled bias when the virtual junction temperature is <10 °C higher than the chamber ambient temperature or, if the virtual junction temperature is not known when the heat dissipation of the device under test (DUT) is less than 200 mW. If the heat dissipation of the DUT exceeds 200 mW, then the virtual junction temperature should be calculated. If the virtual junction temperature[1] exceeds the chamber ambient temperature by more than 5 °C then the virtual junction temperature rise above the chamber ambient should be included in reports of test results since acceleration of failure mechanisms will be affected.~~

Continuous bias is more severe if the die temperature (T_j) is <10 °C higher than the chamber ambient temperature.

If the die temperature is not known, and the heat dissipation of the device under test (DUT) is less than 200 mW, the die temperature is assumed to be less than 10 °C above ambient temperature.

If the heat dissipation of the DUT exceeds 200 mW, the die temperature should be calculated or measured.

If the die temperature exceeds the chamber ambient temperature by more than 5 °C, the rise of the die temperature above the chamber ambient should be included in reports of test results since acceleration of failure mechanisms will be affected.

~~NOTE 2 Based on the power dissipation and the thermal resistance or impedance that corresponds to the mode of operation, the virtual junction temperature can be calculated from the formula $T_j = T_{case} + (P \times R_{th})$ or $T_j = T_{amb} + (P \times R_{th})$~~

~~where~~

~~T_j is the virtual junction temperature;~~

~~P is the power dissipation;~~

~~[1] The virtual junction temperature is the theoretical temperature which is based on a simplified representation of the thermal and electrical behaviour of the semiconductor device.~~

~~R_{th} is the thermal resistance.~~

2) Cycled bias

The DC voltage applied to the devices under test shall be periodically interrupted with an appropriate frequency and duty cycle. If the biasing configuration results in a temperature rise above the chamber ambient, ΔT_{ja}, exceeding 10 °C, then cycled bias, when optimized for a specific device type, will be more severe than continuous bias. Heating as a result of power dissipation tends to drive moisture away from the die and thereby hinders moisture-related failure mechanisms. Cycled bias permits moisture collection on the die during the off periods when device power dissipation does not occur. Cycling the DUT bias with 1 h on and 1 h off is optimal for most plastic-encapsulated microcircuits. The ~~virtual junction~~ die temperature, as calculated on the basis of the known thermal impedance and dissipation should be quoted with the results whenever it exceeds the chamber ambient by 5 °C or more.

6.4 Biasing choice and reporting

Criteria for choosing continuous or cyclical bias, and whether or not to report the amount by which the ~~virtual junction~~ die temperature exceeds the chamber ambient temperature, are summarized in Table 2.

Table 2 – Criteria for choosing continuous or cyclical bias

ΔT_{ja}	Continuous or cyclical bias	Include value of ΔT_{ja} in test report?
ΔT_{ja} < 5 °C or power per DUT < 200 mW	Continuous	No
(ΔT_{ja} ≥ 5 °C or power per DUT ≥ 200 mW), and ΔT_{ja} < 10 °C	Continuous	Yes
ΔT_{ja} ≥ 10 °C	Cyclical [a]	Yes
[a] Cycling the DUT bias with one hour on and one hour off is optimal for most plastic-encapsulated microcircuits.		

7 Procedures

7.1 Mounting

The test devices shall be mounted in such a way as to expose them to a specified condition of temperature and humidity as given in Table 1 with a specified electrical biasing condition. Exposure of devices to excessively hot conditions, dry ambient conditions or conditions that result in condensation on devices and electrical fixtures shall be avoided, particularly during ramp-up and ramp-down. Appropriate attention should also be made to avoid any water dripping on the devices under stress.

7.2 Ramp-up

The time to reach stable temperature and relative humidity conditions ~~should~~ shall be less than 3 h. Condensation on the devices under stress and/or fixtures/hardware shall be avoided at all times by ensuring that ~~the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times~~ their temperature is always higher than the dew point temperature.

7.3 Ramp-down

Ramp-down ~~should~~ shall not exceed 3 h. Condensation shall be avoided by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times during ramp down.

NOTE For a DUT with a cavity in the package, condensation can occur due to the length of the ramp down time.

7.4 Test clock

The test clock starts when the temperature and relative humidity reach the set points, and stops at the beginning of ramp-down.

7.5 Bias

Bias application during ramp-up and ramp-down is optional. Bias should be verified after devices are loaded, prior to the start of the test clock. Bias should also be verified after the test clock stops, but before devices are removed from the chamber.

7.6 Read-out

An electrical test shall be performed not later than 48 h after the end of ramp-down.

For intermediate read-outs, devices ~~should~~ shall be returned to stress within 96 h of the end of ramp-down. Moisture loss can be reduced by placing the device in sealed moisture barrier ~~bag sealed in ambient air~~ bags (without ~~vacuum or~~ desiccant). When devices are placed in sealed bags, the “test window clock” runs at one-third of the rate of devices exposed to laboratory ambient conditions. Thus, the test window can be extended to as much as 144 h, and the time to return to stress to as much as 288 h by enclosing the devices in moisture-proof bags.

The electrical test parameters should be chosen to preserve any defect (i.e. by limiting the applied test current).

Additional time-to-test delay or the return-to-stress delay time is allowed if justified by technical data.

7.7 Handling

Suitable hand-covering shall be used to manage devices, boards and fixtures. Contamination control is important in any accelerated moisture stress test.

8 Failure criteria

A device ~~has~~ shall be considered to have failed if it does not pass the specified end point tests or if its functionality cannot be demonstrated under nominal and worst-case conditions as specified in the applicable procurement document or data sheet.

9 Safety

The equipment manufacturer’s recommendations and local safety regulations shall be followed.

10 Summary

The following details shall be specified in the applicable procurement document:

a) test duration, if other than that specified in Table 1;
b) measurements after test (see 7.6);
c) biasing configuration (see 6.3);
d) temperature of die during test if more than 5 °C above the chamber ambient (see 6.3 e) 1));
e) frequency and duty cycle of bias if cycled bias is to be used (see 6.3 e) 2)).

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Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 5: Essai continu de durée de vie sous température et humidité avec polarisation

IEC 60749-5:2023-12(en-fr)

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4 General

Temperature, humidity and bias conditions are applied to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

Where both this steady-state, humidity bias test and the damp heat, highly accelerated stress test (HAST) of IEC 60749-4 are performed, the results of this 85 °C/85 % RH steady-state test will take priority over the results of the HAST test, which is an accelerated test designed to activate the same failure mechanisms.

5 Equipment

5.1 Equipment summary

The test requires a temperature-humidity test chamber capable of maintaining a specified temperature and relative humidity continuously, while providing electrical connections to the devices under test in a specified biasing configuration.

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The chamber shall be capable of providing controlled conditions of temperature and relative humidity during ramp-up to, and ramp-down from the specified test conditions.

The test chamber dry bulb temperature shall exceed the wet bulb temperature at all times.

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Devices under stress shall be physically located to minimize temperature gradients. Devices under test shall be physically located in order to minimize relative humidity gradients and maximize air flow between devices.

5.4 Minimizing release of contamination

Board and socket materials shall be chosen in order to minimize release of contamination, and to minimize degradation due to corrosion and other mechanisms.

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The test devices shall be placed in the test apparatus to minimise ionic contamination from items such as the card cage, test boards, sockets, wiring and storage containers.

5.6 Deionized water

Deionized water with a minimum resistivity of 1 × 104 Ωm at room temperature shall be used.

6 Test conditions

6.1 Test conditions summary

Test conditions consist of a temperature, relative humidity, and duration used in conjunction with an electrical bias configuration specific to the device.

6.2 Temperature, relative humidity and duration

Unless otherwise required by the detail specification, the temperature, relative humidity and test duration as shown in Table 1 shall be applied.

Table 1 – Temperature, relative humidity and duration

Temperature (dry bulb) °C	Relative humidity [a] %	Temperature [b] (wet bulb) °C	Vapour pressure [b] kPa	Duration [c] h
85 ± 2	85 ± 5	81,0	49,1	1 000 $^{-24}_{+168}$

[a] Tolerances apply to the entire useable test area.

[b] For information only.

[c] The test conditions are to be applied continuously, except during any interim readouts, when the devices should be returned to stress within the time specified in 7.6.

6.3 Biasing guidelines

Apply bias according to the following guidelines:

a) minimize power dissipation;

b) alternate pin bias as much as possible;

c) distribute potential differences across chip metallization as much as possible;

d) maximize voltage within operating range;

NOTE The priority of the above guidelines depends on the mechanism and specific device characteristics.

e) either of two kinds of bias can be used to satisfy these guidelines, whichever is more severe:

1) Continuous bias

The DC bias shall be applied continuously.

Continuous bias is more severe if the die temperature (T_j) is <10 °C higher than the chamber ambient temperature.

If the die temperature is not known, and the heat dissipation of the device under test (DUT) is less than 200 mW, the die temperature is assumed to be less than 10 °C above ambient temperature.

If the heat dissipation of the DUT exceeds 200 mW, the die temperature should be calculated or measured.

If the die temperature exceeds the chamber ambient temperature by more than 5 °C, the rise of the die temperature above the chamber ambient should be included in reports of test results since acceleration of failure mechanisms will be affected.

2) Cycled bias

The DC voltage applied to the devices under test shall be periodically interrupted with an appropriate frequency and duty cycle. If the biasing configuration results in a temperature rise above the chamber ambient, ΔT_{ja}, exceeding 10 °C, then cycled bias, when optimized for a specific device type, will be more severe than continuous bias. Heating as a result of power dissipation tends to drive moisture away from the die and thereby hinders moisture-related failure mechanisms. Cycled bias permits moisture collection on the die during the off periods when device power dissipation does not occur. Cycling the DUT bias with 1 h on and 1 h off is optimal for most plastic-encapsulated microcircuits. The die temperature, as calculated on the basis of the known thermal impedance and dissipation should be quoted with the results whenever it exceeds the chamber ambient by 5 °C or more.

6.4 Biasing choice and reporting

Criteria for choosing continuous or cyclical bias, and whether or not to report the amount by which the die temperature exceeds the chamber ambient temperature, are summarized in Table 2.

Table 2 – Criteria for choosing continuous or cyclical bias

ΔT_{ja}	Continuous or cyclical bias	Include value of ΔT_{ja} in test report?
ΔT_{ja} < 5 °C or power per DUT < 200 mW	Continuous	No
(ΔT_{ja} ≥ 5 °C or power per DUT ≥ 200 mW), and ΔT_{ja} < 10 °C	Continuous	Yes
ΔT_{ja} ≥ 10 °C	Cyclical [a]	Yes

[a] Cycling the DUT bias with one hour on and one hour off is optimal for most plastic-encapsulated microcircuits.

7 Procedures

7.1 Mounting

The test devices shall be mounted in such a way as to expose them to a specified condition of temperature and humidity as given in Table 1 with a specified electrical biasing condition. Exposure of devices to excessively hot conditions, dry ambient conditions or conditions that result in condensation on devices and electrical fixtures shall be avoided, particularly during ramp-up and ramp-down. Appropriate attention should also be made to avoid any water dripping on the devices under stress.

7.2 Ramp-up

The time to reach stable temperature and relative humidity conditions shall be less than 3 h. Condensation on the devices under stress and/or fixtures/hardware shall be avoided at all times by ensuring that their temperature is always higher than the dew point temperature.

7.3 Ramp-down

Ramp-down shall not exceed 3 h. Condensation shall be avoided by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times during ramp down.

NOTE For a DUT with a cavity in the package, condensation can occur due to the length of the ramp down time.

7.4 Test clock

The test clock starts when the temperature and relative humidity reach the set points, and stops at the beginning of ramp-down.

7.5 Bias

Bias application during ramp-up and ramp-down is optional. Bias should be verified after devices are loaded, prior to the start of the test clock. Bias should also be verified after the test clock stops, but before devices are removed from the chamber.

7.6 Read-out

An electrical test shall be performed not later than 48 h after the end of ramp-down.

For intermediate read-outs, devices shall be returned to stress within 96 h of the end of ramp-down. Moisture loss can be reduced by placing the device in sealed moisture barrier bags (without desiccant). When devices are placed in sealed bags, the “test window clock” runs at one-third of the rate of devices exposed to laboratory ambient conditions. Thus, the test window can be extended to as much as 144 h, and the time to return to stress to as much as 288 h by enclosing the devices in moisture-proof bags.

The electrical test parameters should be chosen to preserve any defect (i.e. by limiting the applied test current).

Additional time-to-test delay or the return-to-stress delay time is allowed if justified by technical data.

7.7 Handling

Suitable hand-covering shall be used to manage devices, boards and fixtures. Contamination control is important in any accelerated moisture stress test.

8 Failure criteria

A device shall be considered to have failed if it does not pass the specified end point tests or if its functionality cannot be demonstrated under nominal and worst-case conditions as specified in the applicable procurement document or data sheet.

9 Safety

The equipment manufacturer's recommendations and local safety regulations shall be followed.

10 Summary

The following details shall be specified in the applicable procurement document:

a) test duration, if other than that specified in Table 1;
b) measurements after test (see 7.6);
c) biasing configuration (see 6.3);
d) temperature of die during test if more than 5 °C above the chamber ambient (see 6.3 e) 1));
e) frequency and duty cycle of bias if cycled bias is to be used (see 6.3 e) 2)).

SOMMAIRE

COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

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DISPOSITIFS À SEMICONDUCTEURS – MÉTHODES D'ESSAIS MÉCANIQUES ET CLIMATIQUES –

Partie 5: Essai continu de durée de vie sous température et humidité avec polarisation

AVANT-PROPOS

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L'IEC 60749-5 a été établie par le comité d'études 47 de l'IEC: Dispositifs à semiconducteurs. Il s'agit d'une Norme internationale.

Fondée sur le document JEDEC JESD22-A101D.01, cette troisième édition annule et remplace la deuxième édition parue en 2017. Ce document a été utilisé avec l'autorisation du détenteur du droit d'auteur, JEDEC Solid State Technology Association. Cette édition constitue une révision technique.

Cette édition inclut les modifications techniques majeures suivantes par rapport à l'édition précédente:

a) la spécification de l'équipement d'essai est modifiée pour exiger la nécessité de réduire le plus possible les gradients d'humidité relative et d'augmenter le plus possible la circulation d'air entre les dispositifs à semiconducteurs en essai;

b) la spécification des fixations de l'équipement d'essai est modifiée pour exiger la prévention de la condensation sur les dispositifs en essai et sur les fixations électriques reliant les dispositifs à l'équipement d'essai;

c) le remplacement des références au terme "jonction virtuelle" par "pastille".

Le texte de cette Norme internationale est issu des documents suivants:

Projet	Rapport de vote
47/2820/FDIS	47/2827/RVD

Le rapport de vote indiqué dans le tableau ci-dessus donne toute information sur le vote ayant abouti à son approbation.

La langue employée pour l'élaboration de cette Norme internationale est l'anglais.

Ce document a été rédigé selon les Directives ISO/IEC, Partie 2, il a été développé selon les Directives ISO/IEC, Partie 1 et les Directives ISO/IEC, Supplément IEC, disponibles sous www.iec.ch/members_experts/refdocs. Les principaux types de documents développés par l'IEC sont décrits plus en détail sous www.iec.ch/publications.

Une liste de toutes les parties de la série IEC 60749, publiées sous le titre général *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques*, se trouve sur le site web de l'IEC.

Le comité a décidé que le contenu de ce document ne sera pas modifié avant la date de stabilité indiquée sur le site web de l'IEC sous webstore.iec.ch dans les données relatives au document recherché. À cette date, le document sera

- reconduit,
- supprimé, ou
- révisé.

DISPOSITIFS À SEMICONDUCTEURS – MÉTHODES D'ESSAIS MÉCANIQUES ET CLIMATIQUES –

Partie 5: Essai continu de durée de vie sous température et humidité avec polarisation

1 Domaine d'application

La présente partie de l'IEC 60749 décrit un essai continu de durée de vie utilisant la température et l'humidité avec polarisation pour évaluer la fiabilité des dispositifs à semiconducteurs sous boîtier non hermétique dans les environnements humides.

Cette méthode d'essai est considérée comme destructive.

2 Références normatives

Les documents suivants sont cités dans le texte de sorte qu'ils constituent, pour tout ou partie de leur contenu, des exigences du présent document. Pour les références datées, seule l'édition citée s'applique. Pour les références non datées, la dernière édition du document de référence s'applique (y compris les éventuels amendements).

IEC 60749-4, *Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 4: Essai continu fortement accéléré de contrainte de chaleur humide (HAST)*

3 Termes et définitions

Aucun terme n'est défini dans le présent document.

L'ISO et l'IEC tiennent à jour des bases de données terminologiques destinées à être utilisées en normalisation, consultables aux adresses suivantes:

- IEC Electropedia: disponible à l'adresse https://www.electropedia.org/
- ISO Online browsing platform: disponible à l'adressehttps://www.iso.org/obp

4 Généralités

Des conditions de température, d'humidité et de polarisation sont appliquées pour accélérer la pénétration de l'humidité à travers le matériau de protection externe (enrobage ou scellement) ou par l'interface entre le matériau de protection externe et les conducteurs métalliques qui le traversent.

Lorsque cet essai continu de durée de vie sous température et humidité avec polarisation ainsi que l'essai fortement accéléré de contrainte de chaleur humide (HAST, *Highly Accelerated Stress Test*) de l'IEC 60749-4 sont utilisés tous les deux, les résultats de l'essai continu à 85 °C/85 % d'humidité relative (HR) sont privilégiés par rapport à ceux de l'essai HAST, qui est un essai accéléré conçu pour déclencher les mêmes mécanismes de défaillance.