IEC 62386-101

Edition 3.0 2022-11
COMMENTED VERSION

INTERNATIONAL STANDARD

colour inside

Digital addressable lighting interface – Part 101: General requirements – System components

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DIGITAL ADDRESSABLE LIGHTING INTERFACE –

Part 101: General requirements – System components

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This commented version (CMV) of the official standard IEC 62386-101:2022 edition 3.0 allows the user to identify the changes made to the previous IEC 62386-101:2014+ AMD1:2018 CSV edition 2.1. Furthermore, comments from IEC TC 34 experts are provided to explain the reasons of the most relevant changes, or to clarify any part of the content.

A vertical bar appears in the margin wherever a change has been made. Additions are in green text, deletions are in strikethrough red text. Experts' comments are identified by a blue-background number. Mouse over a number to display a pop-up note with the comment.

This publication contains the CMV and the official standard. The full list of comments is available at the end of the CMV.

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IEC 62386-101 has been prepared by IEC technical committee 34: Lighting. It is an International Standard.

This third edition cancels and replaces the second edition published in 2014 and Amendment 1:2018. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) the scope has been updated;

b) safety and earthing have been updated and extended;

c) references have been updated;

d) the use of bus-power and external-power has been clarified;

e) polarity sensitivity for bus units including a bus power supply has been updated;

f) frame sizes of 32 bits are no longer reserved.

The text of this International Standard is based on the following documents:

Draft	Report on voting
34/947/FDIS	34/988/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

This Part 101 of IEC 62386 is intended to be used in conjunction with:

- Part 102, which contains general requirements for the relevant product type (control gear), and with the appropriate Part 2xx (particular requirements for control gear);
- Part 103, which contains general requirements for the relevant product type (control devices), and the appropriate Part 3xx (particular requirements for control devices);
- Part 104, which contains general requirements for wireless and alternative wired system components;
- Part 105, which contains particular requirements for firmware transfer for control gear and control devices.

A list of all parts in the IEC 62386 series, published under the general title *Digital addressable lighting interface*, can be found on the IEC website.

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The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

IEC 62386 contains several parts, referred to as series. The IEC 62386 series specifies a bus system for control by digital signals of electronic lighting equipment. The IEC 62386-1xx series includes the basic specifications. Part 101 contains general requirements for system components, Part 102 extends this information with general requirements for control gear and Part 103 extends it further with general requirements for control devices. Parts 104 and 105 can be applied to control gear or control devices. Part 104 gives requirements for wireless and alternative wired system components. Part 105 describes firmware transfer. Part 150 gives requirements for an auxiliary power supply which can be stand-alone, or built into control gear or control devices.

The IEC 62386-2xx series extends the general requirements for control gear with lamp specific extensions (mainly for backward compatibility with Edition 1 of IEC 62386) and with control gear specific features.

The IEC 62386-3xx series extends the general requirements for control devices with input device specific extensions describing the instance types as well as some common features that can be combined with multiple instance types.

This ~~second~~ third edition of IEC 62386-101 is intended to be used in conjunction with IEC 62386-102~~:2014 and IEC 62386-102:2014/AMD1:—~~ and with the various parts that make up the IEC 62386-2xx series for control gear, together with IEC 62386-103~~:2014 and IEC 62386-103:2014/AMD1 —~~ and the various parts that make up the IEC 62386-3xx series of particular requirements for control devices. The division into separately published parts provides for ease of future amendments and revisions. Additional requirements will be added as and when a need for them is recognized.

The setup of the standards is graphically represented in Figure 1 below.

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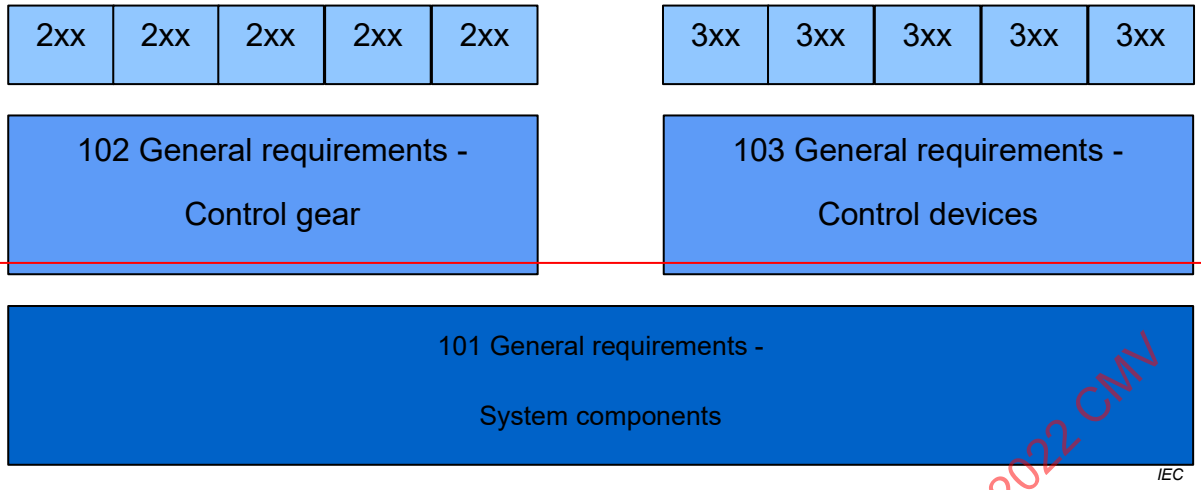

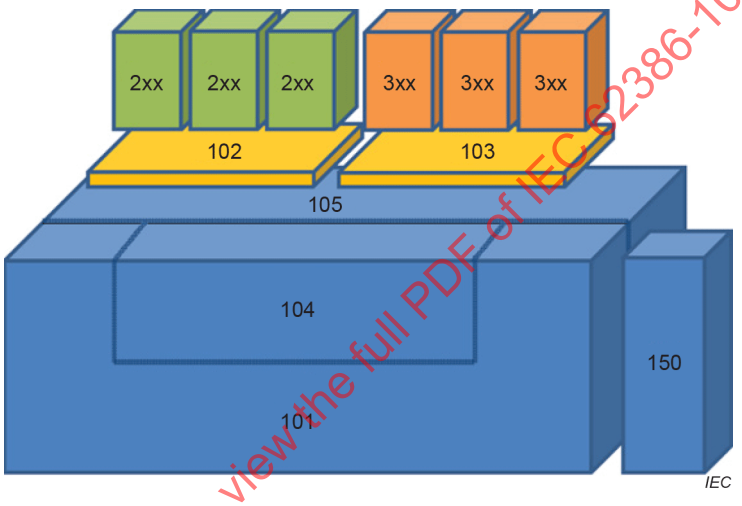

Figure 1 – IEC 62386 graphical overview 1

When this part of IEC 62386 refers to any of the clauses of the other ~~two~~ parts of the IEC 62386-1xx series, the extent to which such a clause is applicable ~~and the order in which the tests are to be performed are~~ is specified. The other parts also include additional requirements, as necessary.

All numbers used in this document are decimal numbers unless otherwise noted. Hexadecimal numbers are given in the format 0xVV, where VV is the value. Binary numbers are given in the format XXXXXXXXb or in the format XXXX XXXX, where X is 0 or 1, "x" in binary numbers means "don't care".

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DIGITAL ADDRESSABLE LIGHTING INTERFACE –

Part 101: General requirements – System components

1 Scope

This part of IEC 62386 is applicable to system components in a bus system for control by digital signals of electronic lighting equipment~~ which is in line with the requirements of IEC 61347 (all parts), with the addition of DC supplies~~.

~~NOTE Tests in this standard are type tests. Requirements for testing individual bus units during production are not included.~~

The control methods, algorithms and data exchange methods of application controllers used for lighting control are not within the scope of the IEC 62386 series. EMC requirements are not within the scope of the IEC 62386 series. **2**

2 Normative references **3**

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61347-1:2015, *Lamp controlgear – Part 1: General and safety requirements*
IEC 61347-1:2015/AMD1:2017

IEC 62386-102:~~2014~~2022, *Digital addressable lighting interface – Part 102: General requirements – Control gear*
~~IEC 62386-102:2014/AMD1:– [1]~~

IEC 62386-103:~~2014~~2022, *Digital addressable lighting interface – Part 103: General requirements – Control devices*
~~IEC 62386-103:2014/AMD1:– [2]~~

IEC 62386-104, *Digital addressable lighting interface – Part 104: General requirements – Wireless and alternative wired system components*

IEC 62386-105, *Digital addressable lighting interface – Part 105: Particular requirements for control gear and control devices – Firmware Transfer*

IEC 62386-2xx (all parts), *Digital addressable lighting interface – Part 2xx: Particular requirements for control gear*

IEC 62386-3xx (all parts), *Digital addressable lighting interface – Part 3xx: Particular requirements for control devices*

~~[1] Under preparation. Stage at the time of publication: IEC DECFDIS 62386-102/AMD1:2018.~~

~~[2] Under preparation. Stage at the time of publication: IEC RFDIS 62386-103/AMD1:2018.~~

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IEC 61000-4-11, *Electromagnetic compatibility (EMC) – Part 4-11:Testing and measurement techniques – Voltage dips, short interruptions and voltage variations immunity tests for equipment with input current up to 16 A per phase*

IEC 60664-1, *Insulation coordination for equipment within low-voltage supply systems – Part 1: Principles, requirements and tests*

IEC 60990:2016, *Methods of measurement of touch current and protective conductor current*

IEC 61643-11, *Low-voltage surge protective devices – Part 11: Surge protective devices connected to low-voltage power systems – Requirements and test methods*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
active state
phase of low level voltage during a transmission

Note 1 to entry: Noise and short pulses may be ignored and therefore do not change the state.

3.2
advanced bus power supply
bus power supply capable of checking the bus for fault conditions before switching on its output continuously

Note 1 to entry: Examples of fault conditions are mains voltage connected to the bus or short circuit of the bus.

3.3
application controller
control device that is connected to the bus and sends commands in order to control input devices and/or control gear connected to the same bus

3.4
backward frame
frame used for backward transmission

3.5
backward transmission
transmission of data as a reply to and triggered by a forward transmission

3.6
bus
two-wire connection line carrying power and frames

3.7
bus powered
drawing the power for operation from the bus

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3.8
bus power down
bus power interruption longer than 45 ms

3.9
bus power interruption
abnormal condition where the bus voltage is in the receiver low level voltage range, but not because of a transmitter being active

3.10
bus power supply
unit feeding defined energy to the bus

3.11
bus unit
logical unit or combination of logical units, containing one transmitter and optionally one receiver

Note 1 to entry: See 4.6.6.

3.12
charge overshoot
product of current overshoot time and current overshoot amplitude

~~Note 1 to entry: Within this standard the charge overshoot is a simple multiplication of the current overshoot time and the current overshoot amplitude.~~

3.13
collision
situation in which two or more transmitters are transmitting simultaneously

Note 1 to entry: Collisions can go unnoticed if the transmission timing is sufficiently similar and the transmitted frame content is identical.

3.14
command
forward transmission with appropriate information content, intended to cause a reaction in the receiver

Note 1 to entry: A receiver, having decoded a command can, when appropriate, decide to ignore the command.

Note 2 to entry: Refer to IEC 62386-102, IEC 62386-103, IEC 62386-104, IEC 62386-105, the IEC 62386-2xx series and IEC 62386-3xx series for command definitions.

3.15
control device
device that is connected to the bus and sends commands to other devices ~~(for example control gear)~~ connected to the same bus

Note 1 to entry: Control devices can also receive commands and backward transmissions. Control devices can contain application controllers and/or input devices.

3.16
control gear
device that is connected to the bus and receives commands in order to control at least one output in a direct or indirect way

Note 1 to entry: The lamp controlgear described in IEC 61347-1 can cover control gear.

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3.17
current overshoot time
time per bit during which the current supplied by the bus power supply is above the allowed maximum of 250 mA after a transition from idle state to active state

Note 1 to entry: See 6.5.4.

3.18
destroy area
time slot where a valid frame cannot be ~~guaranteed and therefore the frame has to be invalidated~~ ensured

3.19
edge
change from active state to idle state or vice versa

3.20
event message
command sent by a control device in order to distribute information on the bus

3.21
externally powered
drawing the power for operation from a separate power supply

Note 1 to entry: The separate power supply can be mains power, DC power, etc.

3.22
forward frame
frame used for forward transmission

3.23
forward frame priority
property of a forward frame used to prioritize access to the bus

3.24
forward transmission
transmission of data initiated by a control device

Note 1 to entry: See also 3.5.

3.25
frame
set of consecutive bits followed by a stop condition

Note 1 to entry: See Clause 8 for the timing definition of a stop condition.

3.26
grey area
time slot containing the decision point separating adjacent time slots

Note 1 to entry: A grey area indicates that the decision is arbitrary. Typically the previous or next entry in a table should be used as an action. See Clause 8 for further information.

3.27
idle state
phase of high level voltage between and during transmissions

Note 1 to entry: Noise and short pulses may be ignored and therefore do not change the state.

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3.28
input device
control device that is connected to the bus and sends commands using a multi-master transmitter in order to distribute information about user actions and/or sensor values

Note 1 to entry: Input devices do not transmit commands to the control gear.

3.29
instance
signal processing unit of an input device

3.30
instruction
command transmitted to change one or more variables in a bus unit 4

3.31
integrated bus power supply
bus power supply integrated into a physical device also containing a bus unit

3.32
interface
terminals or wires for connection to the bus

3.33
logical unit
control gear or control device that conforms to IEC 62386-102 or IEC 62386-103

Note 1 to entry: See 4.6.6.

3.34
multi-master application controller
application controller that is ~~intended to share~~ capable of sharing 5 the bus with other control devices and uses a multi-master transmitter

3.35
multi-master transmitter
transmitter that follows the multi-master timing and supports collision detection, collision avoidance, and collision recovery methods

Note 1 to entry: Multi-master transmitters are used in control devices intended for multi-master control systems.

3.36
proprietary forward frame
~~frame other than a standard forward frame, reserved forward frame or backward frame~~

~~Note 1 to entry: Proprietary frames are intended for manufacturer-specific purposes~~

forward frame for manufacturer-specific purposes

3.37
query
command transmitted to observe a variable in a bus unit

Note 1 to entry: A query can be followed by a backward frame.

3.38
receiver
part of a bus unit detecting and decoding frames on the bus

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3.39
reserved
intended for future use ~~by this standard~~

3.40
send-twice command
command transmitted by send-twice forward frames

Note 1 to entry: Refer to 9.4, IEC 62386-102, IEC 62386-103, the IEC 62386-2xx series and IEC 62386-3xx series for further details on send-twice commands.

3.41
send-twice forward frame
forward frame that needs to be transmitted twice with a limited settling time in order to be processed by the receiver

3.42
settling time
time during which the bus is in idle state after the last rising edge of one frame and before the first falling edge of the next frame

3.43
single-master application controller
application controller that is ~~intended not to share the bus with other control devices~~ not required to use a multi-master transmitter **6**

Note 1 to entry: The implication is that no other application controllers, and no other input devices with event messages enabled, may be connected to the bus.

3.44
standard forward frame
forward frame as defined and described in the IEC 62386 series

3.45
system failure
bus power interruption longer than 550 ms

3.46
transaction
uninterruptible set of one or more consecutive forward frames transmitted from a single control device, with zero or more backward frames

3.47
transmitter
part of a bus unit placing frames on the bus

3.48
voltage overshoot time
time per bit during which the voltage supplied by the bus power supply is above 20,5 V after a transition from active state to idle state

Note 1 to entry: See 6.5.4.

3.49
voltage undershoot time
time per bit during which the voltage supplied by the bus power supply is below 12,0 V after a transition from active state to idle state

Note 1 to entry: See 6.5.4.

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3.50
frame accepted
frame that has been received and uses the correct frame type and data bit content

3.51
frame ignored
frame received but not accepted

3.52
frame received
frame with a valid start bit, valid data bits, and a stop condition

3.53
frame rejected
frame not received

3.54
FELV
functional extra-low voltage
ELV in a circuit provided for functional purposes and not fulfilling the requirements for SELV (or PELV)

Note 1 to entry: FELV has basic insulation from LV.

Note 2 to entry: An FELV circuit is not safe to touch.

[SOURCE: IEC 60598-1:2020, 1.2.42.1, modified – The notes have been added.]

4 General

4.1 Purpose

The standardization of the digital addressable lighting interface is intended to achieve interoperable multi-vendor operation below the level of building management systems.

~~EN 50491 and ISO 14672 are not applicable for the purposes of this standard.~~

Annex A gives further information for systems.

NOTE The IEC 63044 series and ISO/IEC 14762 are not applicable for the purposes of this IEC 62386 series. The IEC 63044 series can be applicable to application controllers if intended to be used as HBES/BACS.

4.2 Version number

The version shall be in the format "x.y", where the major version number x is in the range of 0 to 62 and the minor version number y is in the range of 0 to 2. When the version number is encoded into a byte, the major version number x shall be placed in bits 7 to 2 and the minor version number y shall be placed in bits 1 to 0.

At each amendment to an edition of IEC 62386-101 the minor version number shall be incremented by one.

At a new edition of IEC 62386-101 the major version number shall be incremented by one and the minor version number shall be set to 0.

The current version number is ~~"2.01"~~ "3.0".

NOTE ~~Normally 2 amendments on IEC documents are made before a new edition is created.~~ IEC documents are generally subject to two amendments before a new edition is prepared.

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4.3 System structure and architecture

A system ~~conformant to this standard~~ shall consist of the components listed in Table 1.

Table 1 – System components

Component	Quantity	For detailed information see
Bus power supply	≥ 1	Clause 6
Control gear	≥ 0	IEC 62386-102~~:2014 and IEC 62386-102:2014/AMD1:~~
Application controller	≥ 1	IEC 62386-103~~:2014 and IEC 62386-103:2014/AMD1:~~
Input devices	≥ 0	IEC 62386-103~~:2014 and IEC 62386-103:2014/AMD1:~~
Bus	1	Subclause 4.8 and Clause A.2

In a system all bus units as well as the bus power supplies are connected in parallel to the bus.

NOTE As a consequence of this, every frame is visible to all power supplies, control gear, and control devices on the bus.

Figure 2 shows a system structure example.

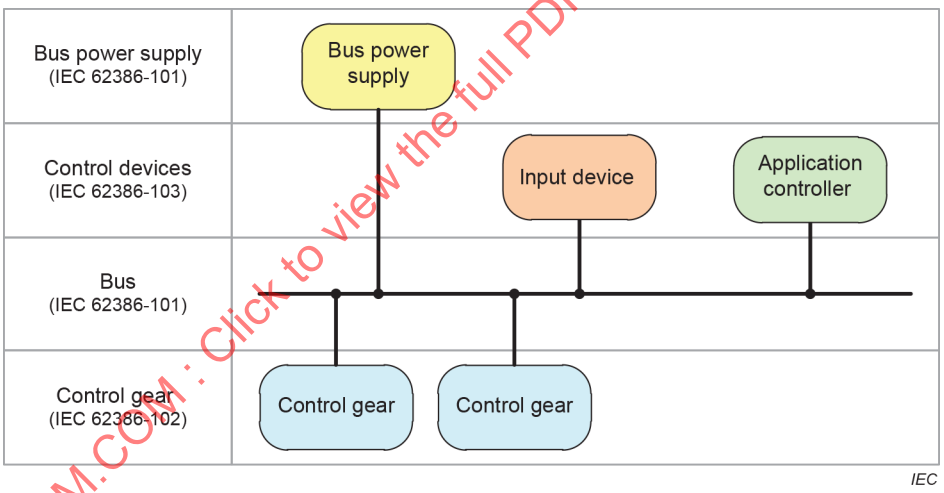

Figure 2 – System structure example

See 4.8 for detailed information on the wiring and Clause A.2 for information on possible system architectures.

4.4 System information flow

Figure 3 shows the different frame types that are used for communication between the bus units in a system. A backward frame is only ever transmitted in response to a forward frame.

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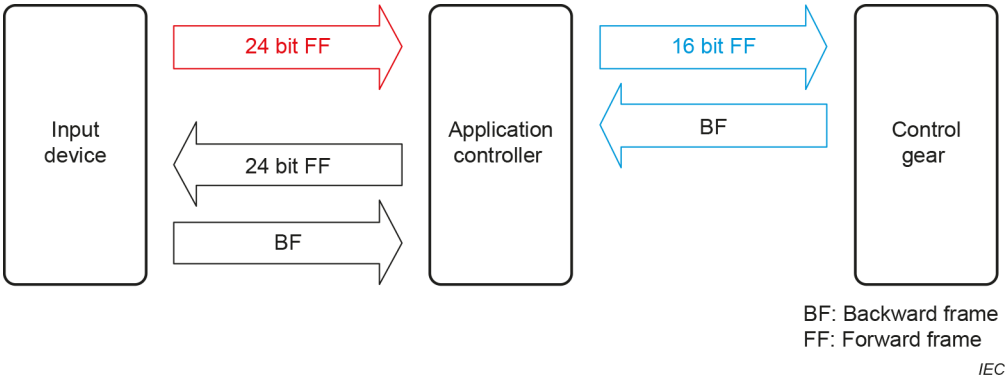

Figure 3 – Communication between bus units (example)

A direct information flow from an input device to control gear is not allowed. In addition to communications shown in Figure 3, for firmware transfer (IEC 62386-105), application controllers can transmit 32-bit forward frames and all three of the bus units shown can receive 32-bit forward frames. Multi-master application controllers can also be transmitters of 8-bit backward frames. 7

NOTE An example of a system conforming to this document can consist of an application controller and control gear only, see A.2.4. In such a system, user input does not result in 24-bit forward frames on the bus.

4.5 Command types

Bus units conforming to this document shall use the following different types of commands for communication:

- event messages,
- instructions, and
- queries.

NOTE Refer to the other parts of the IEC 62386 series for further details on event messages, instructions and queries.

4.6 Bus units

4.6.1 Transmitters and receivers in bus units

Table 2 gives a short summary of the different receivers and transmitters allowed for each bus unit. It is not allowed for a bus unit to transmit or receive other frames than the ones indicated in Table 2, except proprietary forward frames. See 7.4 for details of the different frame types.

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Table 2 – Transmitters and receivers in bus units

Bus unit	Receiver of	Transmitter of	
Control gear	32-bit forward frames 8	Backward frames, following the single-master timing requirements[a]	
	16-bit forward frames		
Input device	32-bit forward frames	24-bit forward frames	Following the multi-master timing requirements
	24-bit forward frames	Backward frames[a]	
Multi-master application controller	32-bit forward frames	32-bit forward frames	
	24-bit forward frames	24-bit forward frames	
	16-bit forward frames[b]	16-bit forward frames	
	Backward frames	Backward frames[a]	
Single-master application controller	Backward frames[c]	16-bit forward frames, following the single-master timing requirements[d]	

[a] No collision detection or collision avoidance methods shall be applied to backward frame transmissions.

[B] Only applicable when the multi-master application controller is able to process 16-bit forward frames transmitted by other application controllers.

[C] Only required if the single-master application controller uses addressing or queries.

[D] A single-master application controller can also send 24-bit frames if polling input devices, and 32-bit forward frames.

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4.6.2 Control gear

A control gear shall be conformant to this document and to IEC 62386-102 and the applicable parts of the IEC 62386-2xx series.

It shall contain a receiver for 16-bit forward frames and a transmitter for transmitting backward frames. The backward frame transmitter shall conform to the timing requirements for a single-master transmitter defined in 8.1 and shall not implement collision detection or recovery. It can contain a receiver for 32-bit forward frames.

4.6.3 Input device

An input device shall be conformant to this document and to IEC 62386-103 and the applicable parts of the IEC 62386-3xx series.

It shall contain a multi-master transmitter following the multi-master transmitter timing requirements defined in 8.3 to transmit 24-bit forward frames. It shall also contain a transmitter to transmit backward frames. The backward frame transmitter shall conform to the timing requirements for a ~~single-~~multi-master transmitter and shall not implement collision detection or recovery.

NOTE Although they are logically distinct objects, the multi-master transmitter and the backward frame transmitter can share the same hardware.

An input device shall contain a receiver to receive 24-bit forward frames transmitted by other control devices. It can contain a receiver for 32-bit forward frames.

4.6.4 Single-master application controller

A single-master application controller shall be conformant to this document and to IEC 62386-103.

It shall contain a transmitter following the transmitter timing requirements defined in 8.1 to transmit forward frames.

NOTE ~~1~~ Typically, however, a single-master application controller also contains a receiver to receive backward frames transmitted by control gear.

A single-master application controller shall use the commands defined in IEC 62386-102 and, if applicable, the relevant parts of the IEC 62386-2xx series to communicate with the control gear.

~~NOTE 2 The control methods and algorithms of an application controller used for lighting control are not in the scope of IEC 62386.~~

4.6.5 Multi-master application controller

A multi-master application controller shall be conformant to this document and to IEC 62386-103.

It shall contain a multi-master transmitter following the multi-master transmitter timing requirements defined in 8.3 to transmit forward frames. It shall also contain a transmitter to transmit backward frames. The backward frame transmitter shall conform to the timing requirements for a multi-master transmitter and shall not implement collision detection or recovery **9**. It shall contain a receiver to receive backward frames as well as forward frames transmitted by other control devices. It can contain a receiver for 32-bit forward frames. It shall not transmit backward frames in response to 16-bit forward frames.

A multi-master application controller shall use the commands defined in IEC 62386-102 and, if applicable, the relevant parts of the IEC 62386-2xx series to communicate with the control gear. It shall use the commands defined in IEC 62386-103 and, if applicable, the relevant parts of the IEC 62386-3xx series to communicate with control devices. If applicable, a multi-master application controller shall use the commands defined in IEC 62386-105 to achieve firmware transfer to control gear and control devices.

NOTE ~~1~~ A multi-master application controller can also receive and process 16-bit forward frames transmitted by other application controllers and/or react to queries.

~~NOTE 2 The control methods and algorithms of an application controller used for lighting control are not in the scope of IEC 62386.~~

~~NOTE 3 The standardisation of data exchange between different application controllers sharing the same bus is not in the scope of IEC 62386.~~

4.6.6 Sharing an interface

More than one logical unit may share one physical interface. Figure 4 shows an example where n logical units and a bus power supply share the physical interface.

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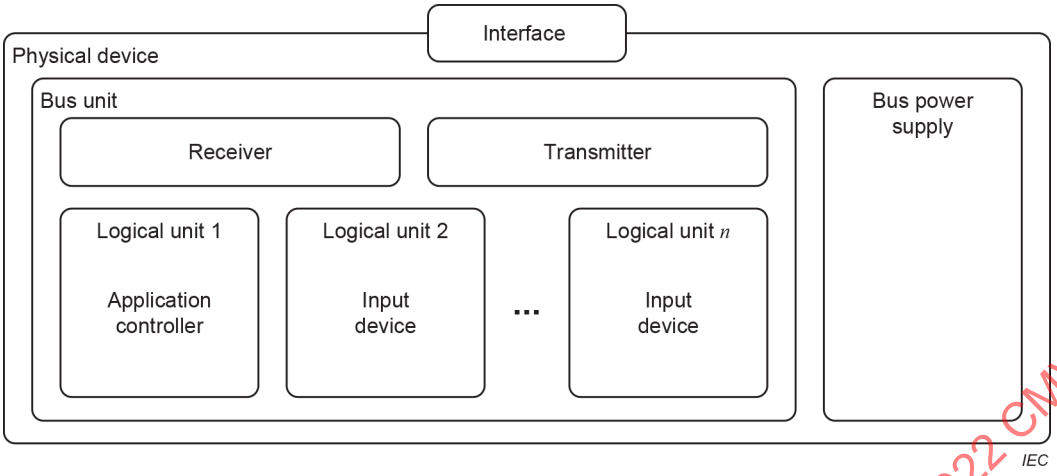

Figure 4 – Example of a shared interface

An application controller may be built into a bus unit which also contains an input device, with both the application controller and the input device sharing the same physical interface. A bus unit of that kind shall support a command to deactivate the application controller, thus enabling the bus unit to be used in the same way as if it contained only the input device.

4.6.7 Power for operation 10

Bus units shall be solely bus powered or solely externally powered, or meet one of the following two cases:

- The bus unit is configurable between bus powered and externally powered, where the configuration shall not be automatic based upon the presence or absence of the supply, and the bus unit meets the following conditions:
  - connection or removal of the external supply or bus power supply shall not cause operation to change between bus powered and externally powered, and
  - it meets the requirements for bus powered bus units when configured as bus powered, and meets the requirements for externally powered bus units when configured as externally powered, and
  - changing the configured power source does not change any functionality that is described in any part of the IEC 62386 series, except due to requirements that differ between bus powered and externally powered bus units.
- The bus unit is bus powered, uses an external supply only for behaviour not specified in any part of the IEC 62386 series, and meets the requirements in the implemented parts of the IEC 62386 series with the external supply disconnected.

NOTE 1 An example of a bus unit that is configurable between bus powered and externally powered is a sensor which can draw a relatively high current when bus powered, limiting the number of such devices that can be connected to the bus, or can be configured to be externally powered and so allow more devices on the bus.

NOTE 2 An example of a bus unit that is bus powered, but uses an external supply only for behaviour not specified in any part of the IEC 62386 series, is a bus powered push-button panel with a backlight, where the backlight operates only when an external supply is connected.

NOTE 3 An example of a bus unit that does not meet these requirements is bus powered LED control gear, requiring a second device to provide power for the LEDs, where the second device is externally powered. Another example is a bus powered pulse width modulation (PWM) dimmer which requires an external 24 V DC supply to drive its output – the dimmer can instead be externally powered from the 24 V DC supply.

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4.7 Bus power supply and load calculations

4.7.1 Current demand coverage

In one system the sum of all bus units' current consumption when not transmitting (see 5.5, Table 10) shall not exceed the sum of all bus supplies' guaranteed supply current (see 6.5.1, Table 13). See also Clause A.5.

Additional current is needed during transmission to drive dynamic processes such as charging capacitances within the system.

$$\sum I_{\text{Bus Unit}} + I_{\text{Dynamic Processes}} \leq \sum I_{\text{Power Supply Guaranteed}}$$

There is no universally valid equation for calculating the current needed for dynamic processes since this current depends on the system wiring and system structure.

4.7.2 Maximum signal current compliance

The sum of all bus power supplies' maximum supply current connected to the bus shall never exceed 250 mA.

$$\sum I_{\text{Power Supply Guaranteed}} \leq \sum I_{\text{Power Supply Maximum}} \leq 250\ \text{mA}$$

4.7.3 Simplified system calculation

For a system consisting of just one bus power supply, bus powered bus units, and n externally powered bus units, for example control gear, the following simplification is recommended:

$$2\ \text{mA} \times n_{\text{Externally Powered Bus Units}} + \sum I_{\text{Bus Powered Bus Units}} \leq \frac{I_{\text{Power Supply Guaranteed}}}{1{,}2}$$

The factor 1,2 is ~~a ballpark figure and~~ an approximation that takes an additional current of 20 % needed for dynamic processes into account.

4.8 Wiring

4.8.1 Wiring structure

The bus wiring should be connected in a star topology, a linear topology or a mixture of both. The wiring shall not be done in a ring structure. The two leads which serve as the bus shall be located in the same cable or cable conduit. In the cable or cable conduit the two leads shall be next to each other in order to prevent unintended coupling to other signals.

NOTE Depending on local installation directives and insulation requirements the two wires can be located in the same cable as the mains power supply leads.

4.8.2 Wiring specification

Apart from transient effects during transmission, at all times during the operation of the system, the voltage across the interface of any device shall not differ by more than 2,0 V from the voltage across the interface of each and every other device connected to the bus. See also Clause A.1 for further details.

NOTE 1 The voltage drop depends on the sum of the supply currents of all power supplies, the specific resistance of the leads and the wiring length.

NOTE 2 This requirement can limit the total wiring length in the system.

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4.9 Electrical safety requirements 11

4.9.1 General

This Subclause 4.9 describes the additional safety requirements for the implementation of digital addressable lighting interface, in addition to the product safety requirements given in the relevant product safety standard.

4.9.2 Insulation

~~The minimum requirement for system components conformant to this standard shall be basic insulation as defined in IEC 61347-1.~~

The bus wiring and the interface shall be considered a FELV circuit or network.

NOTE 1 This means that systems other than FELV are not covered by this document.

The interface shall have at least basic insulation as required for at least 230 V AC mains, or the product working voltage, whichever is higher, according to IEC 60664-1.

NOTE 2 This voltage level is applicable to e.g. the basic insulation between the interface circuit and mains or the supplementary insulation between the bus wiring and touchable conductive parts of the user interface.

If the working voltage exceeds 230 V AC (RMS), and this working voltage can be applied on the interface in the case of a single fault condition, then there shall be a warning included in the manual, also recommended to be marked on the product, indicating that the working voltage is higher than 230 V AC (RMS).

NOTE 3 Working voltage is defined in IEV 581-21-19. This is not usually the mains voltage.

The insulation between the mains and the interface shall be designed for the applicable overvoltage category (OVC), as defined in IEC 60664-1, and shall not be less than OVC II.

NOTE 4 If bus wiring is likely, when installed, to be subjected to impulse voltages that exceed OVC II, then additional measures to be provided to the bus can be considered, for example impulse voltage protection or use of products designed for higher OVC. This can be related to bus wiring being partly outdoors.

4.9.3 Electric strength

The requirements of IEC 61347-1:2015, Clause 12 apply, replacing the term "lamp controlgear" with the term "bus unit".

The value used for working voltage shall be at least 230 V AC, or the product working voltage, whichever is higher.

The over voltage protective device (SPD) shall be disconnected if it complies with IEC 61643-11, when conducting the insulation and electric strength test.

4.9.4 Limitation of the touch current from the device to the bus

The touch current shall be limited to 0,5 mA RMS.

The touch current shall be measured with the measuring network described in IEC 60990:2016, Figure 4.

The value of the touch current shall be made available in the product documentation by the manufacturer of the product.

Annex B gives further information on touch current.

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NOTE The use of the term "touch current" does not indicate that the interface is accessible to touch.

4.10 Earthing of the bus

~~The requirement for system components conformant to this standard shall be as defined in IEC 61347-1.~~

The interface terminals shall not be connected to earth, except in the following situations:

- a device containing a bus power supply having a maximum supply current of 250 mA, where the negative interface terminal is permitted to be connected to earth;
- through a capacitor connected to earth as described in 5.3 or 6.3. **12**

NOTE Unexpected currents, caused by multiple connections of the circuit to protective earth, could cause fire in the bus wiring. Earthing could also break the safety requirements for certain luminaires.

4.11 Power interruptions at bus units

4.11.1 Different levels of power interruptions

Table 3 and Table 4 show the different levels of power interruptions at bus units.

Table 3 – Power-interruption timing of external power

Minimum	Typical	Maximum	Description
		200 ms	Short interruptions of external power supply[a]
> 200 ms		< 5 s	Grey area
5 s			External power cycle[b]
[a] See 4.11.2. [b] See 4.11.3.			

Table 4 – Power-interruption timing of bus power

Minimum	Typical	Maximum	Description
		40 ms	Short interruptions of bus power supply[a]
> 40 ms		< 45 ms	Grey area
45 ms			Bus power down[b]
> 450 ms		< 550 ms	Grey area for system failure
550 ms			System failure[b]
[a] See 4.11.4. [b] See 4.11.5.			

4.11.2 Short power interruptions of external power supply

The requirements of 4.11 are applicable for bus units in steady state without communication on the bus.

NOTE 1 Steady state implies for example that the device has finished its power-up and is ready for the intended operation without any changes of the output in progress.

Functional tests for short power interruptions shall be done with test methods and test equipment according to IEC 61000-4-11 at the minimum specified power supply voltage, with test voltage levels given in Table 5. For AC supply the voltage shift shall occur at zero crossing.

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Table 5 – Short power interruptions

	Test levels
Test voltage level 1	70 %
Test voltage level 2	0 %
Number of periods with AC supply	10
Interruption time with DC supply	200 ms

During the power supply interruption, a change of the state may occur. After the power supply interruption, the bus unit shall be in, or shall re-establish within 30 min, the same state as before the interruption.

NOTE 2 The 30 min time limit is chosen to allow for the long re-ignition time of certain lamp types.

4.11.3 External power cycle

After an external power cycle (see Table 3), an externally powered bus unit shall apply power-on behaviour to all logical units simultaneously. During an external power cycle, a bus unit ~~might~~ can possibly still respond to commands.

NOTE The power-on behaviour is defined in IEC 62386-102 and IEC 62386-103.

4.11.4 Short interruptions of bus power supply

Bus units shall not interpret short bus power interruptions of up to 40 ms as power down.

NOTE This implies that short bus power interruptions will not trigger power-on behaviour.

Tests for the short interruption of the bus power supply shall be done at the minimum bus power supply voltage.

4.11.5 Bus power down

A bus powered bus unit may interpret bus power down as an external power cycle (see 4.11.1). It shall interpret system failure as an external power cycle. The external power cycle and corresponding power-on 13 behaviour shall apply to all logical units simultaneously. See Table 4.

NOTE The power-on behaviour is defined in IEC 62386-102 and IEC 62386-103.

4.11.6 System start-up timing

After external power-on, a bus power supply shall be able to supply the guaranteed supply current given in Table 13 after the bus power supply start-up time specified in Table 6 at the latest.

A receiver shall be ready to receive frames within the maximum receiver start-up time specified in Table 6.

A transmitter or a multi-master transmitter shall not start transmissions earlier than the transmitter start-up time specified in Table 6.

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Table 6 – Start-up timing

	Minimum	Typical	Maximum	Condition
Bus power supply start-up time			250 ms	Guaranteed supply current reached
Advanced bus power supply start-up time			400 ms	
Integrated bus power supply start-up time			400 ms [a]	
			5 s [b]	
Receiver start-up time for externally powered bus units, after external power cycle			450 ms [e]	
Receiver start-up time for externally powered bus units, after bus power down			100 ms	U = 10 V [d]
Receiver start-up time after bus power down for bus powered bus units			1 200 ms	
Transmitter start-up time	110 ms [c]			
Multi-master transmitter start-up time	110 ms			

[a] Applicable if other bus power supplies are allowed in the system.

[b] Applicable if no other bus power supplies are allowed in the system.

[c] Not applicable for transmitters of bus units which cannot determine the bus state.

[d] Idle state, bus voltage measured at the interface of the bus unit.

[e] If an external power cycle occurred and the bus power is not available within 350 ms, the 100 ms timing is applicable.

Figure 5 shows an example of the system start-up timing.

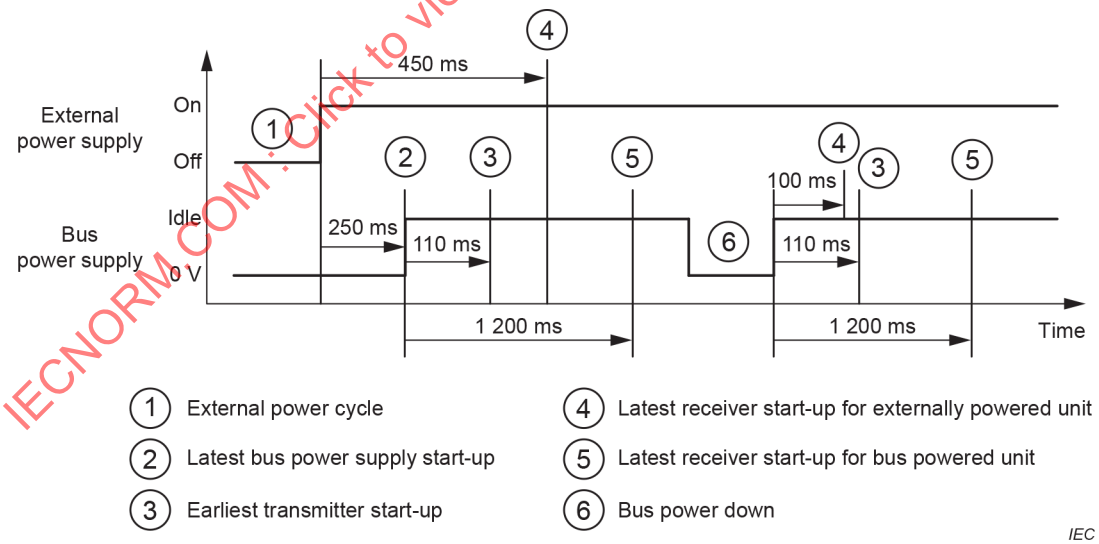

Figure 5 – Start-up timing example

NOTE It follows from the provisions of 4.11.6 that a transmitter could be transmitting before all receivers are ready to receive.

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5 Electrical specification

5.1 General

All voltages and currents refer to the interface of the bus unit.

The control interface shall be polarity insensitive, except when a bus power supply is integrated. If the integrated bus power supply is switchable 14, polarity sensitivity is permitted for both states of the bus power supply (enabled and disabled).

Overvoltage protection is optional, but recommended for the highest rated voltage of the system. If overvoltage protection is not included, it is recommended that the design ensures safe operation in case mains voltage is applied to the interface.

5.2 Marking of the interface

The interface shall be marked with "da" or "DA" (for data) on the bus unit. If colour coding is used, the colours representing the "da" or "DA" shall be given on the bus unit.

If there is more than one interface, additional marking shall be used to enable the interfaces to be distinguished from one another.

5.3 Capacitors between the interface and earth

If capacitors are connected between the interface circuit and any other part of the device, such as earth, these shall be connected from the negative side of the rectified interface signal. Such capacitors shall fulfil the insulation requirements given in 4.9.

NOTE The capacitance seen on the bus is affected by the capacitance to earth where a capacitor connected between the negative side of the interface and earth on one bus unit is used with another bus unit containing a capacitor connected between the positive side of the interface and earth.

5.4 Signal voltage rating

The voltage levels in the system during normal operation shall always be in the range of the nominal system voltage given in Table 7. All bus units as well as the bus power supplies shall withstand the absolute maximum system voltage given in Table 7. Testing shall be done with a current of ~~maximum~~ 260 mA for a duration of 1 s.

NOTE 1 Voltages outside the nominal system voltage range ~~might~~ could occur, as a result of ringing on the bus, for example.

Devices need to be polarity insensitive (see 5.1) or power supplies need to be able to withstand reverse voltages (see 9.7).

Table 7 – System voltage levels

	Minimum	Typical	Maximum
Nominal system voltage U	0 V		20,5 V
Absolute maximum system voltage	0 V		22,5 V

The voltage levels at the receiver interface shall be interpreted according to Table 8.

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Table 8 – Receiver voltage levels

	Minimum	Typical	Maximum
High level voltage	9,5 V		22,5 V
Threshold voltage	> 6,5 V	8,0 V	< 9,5 V
Low level voltage	0 V		6,5 V

The voltage levels of a transmitter shall be as shown in Table 9.

Table 9 – Transmitter voltage levels

	Minimum	Typical	Maximum
Low level voltage	0 V		4,5 V
High level voltage[a]	10,0 V [b]		22,5 V

[a] The high level voltage is not under control of a transmitter, but is determined by the power supply and its location on the bus.

[b] 10 V is derived from the minimum power supply voltage of 12 V minus the maximum voltage drop of 2 V on the bus.

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5.5 Signal current rating

The relation between the current I_{BUS} and the voltage U at the interface of the bus unit shall be as shown in Table 10.

Table 10 – Current rating

	Minimum	Typical	Maximum	Condition
Externally powered bus unit current consumption I_{BUS} when not transmitting			2,0 mA	0 V ≤ U ≤ 22,5 V
Bus powered bus unit current consumption I_{BUS} when not transmitting			250 mA [a]	
Current consumption I_{BUS} when not transmitting	10 µA [b]			U_{TH} ≤ U ≤ 22,5 V [c]
Transmitter sink current	250 mA			U ≤ 4,5 V [d]

[a] This is the theoretical maximum current. In reality a device should consume less current. See 4.7, 5.6 and the last paragraph of this subclause 5.5.

[b] The minimum current consumption is necessary for discharging the wiring capacitances and input capacitances of the bus units connected.

[c] U_{TH} is the threshold voltage of the receiver.

[d] This is the required resulting voltage when sinking the maximum current.

Bus units shall not draw more than their specified maximum current, not even during power up or power down. For bus powered units the actual value to use for testing is the documented maximum current consumption.

5.6 Marking of bus powered bus unit

If a bus unit is bus powered, the maximum current consumption in mA shall be shown in the literature. It is also recommended that this should be shown on the label.

The start-up time of a bus powered bus unit shall be shown in the literature and optionally on the label.

The maximum current shall take tolerances and temperature drift into account.

5.7 Signal rise time and fall time

The rise time t_{RISE} and fall time t_{FALL} of the signal shall fulfil the requirements given in Table 11. Figure 6 and Figure 7 illustrate the levels used for measuring t_{RISE} and t_{FALL}.

Table 11 – Signal rise and fall times

	Minimum	Typical	Maximum	Condition
t_{RISE}, t_{FALL} for transmitter and multi-master transmitter	3 µs [a]			Measured between 10 % and 90 % of the signal voltage swing. Test shall be done at a bus voltage U_{BUS} of 20,5 V at 250 mA unless there is an integrated bus power supply with I_{max} = 250 mA, in which case no additional bus power supply shall be used **15**.
t_{RISE}, t_{FALL} for transmitter			25 µs	Measured between: 4,5 V and 11,5 V at U_{BUS} ≥ 12 V bus voltage 4,5 V and (U_{BUS} – 0,5 V) at 10 V ≤ U_{BUS} < 12 V
t_{RISE}, t_{FALL} for multi-master transmitter			15 µs	
[a] The system resonance frequency depends on the system components including the wiring. Therefore there is no minimum value that ensures the absence of ringing in all cases. The minimum t_{RISE} and t_{FALL} should be considered to avoid EMI problems.				

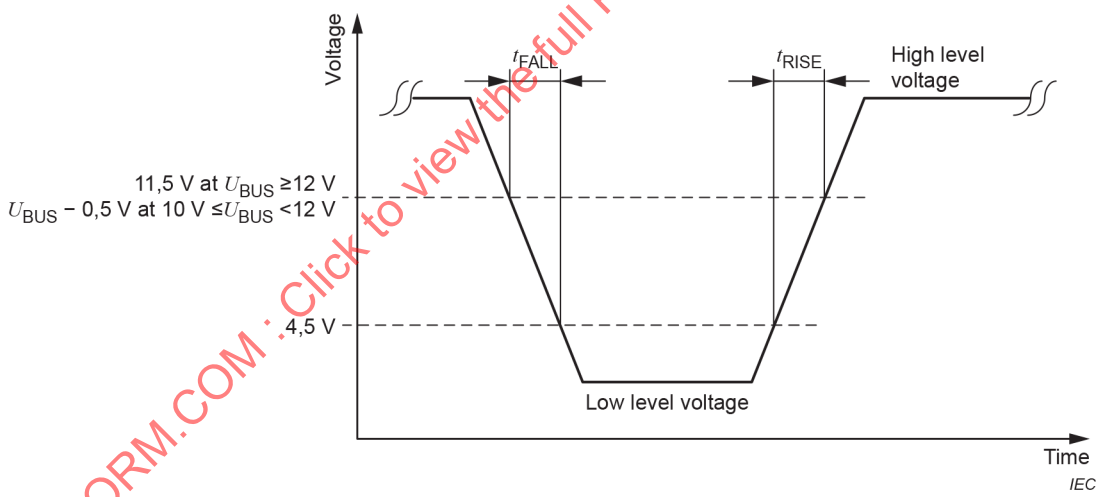

Figure 6 – Maximum signal rise and fall time measurements

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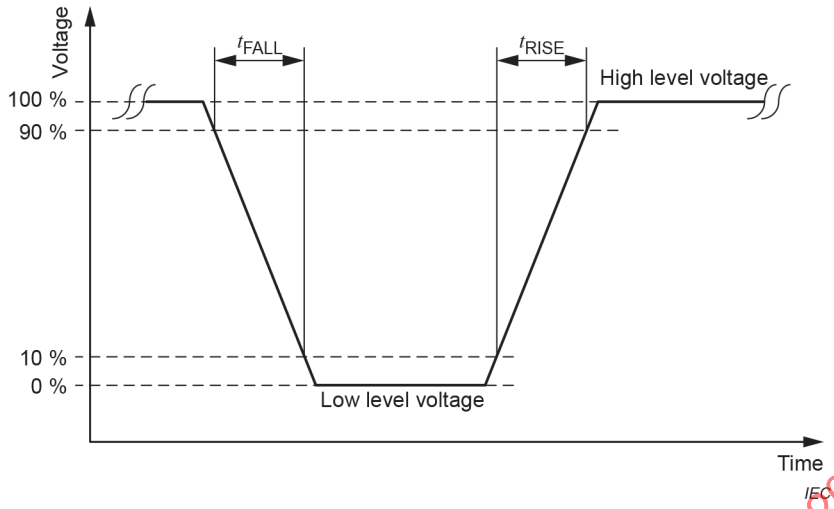

Figure 7 – Minimum signal rise and fall time measurements

NOTE It follows that any control gear~~/~~ or control device causing a change of logic level on the bus by means of changing its own impedance, ~~should~~ will change its impedance at a rate such that the timing requirements of Table 11 are met.

6 Bus power supply

6.1 General

A bus power supply can be a stand-alone bus power supply unit or it can be integrated with any bus unit into one physical device.

All voltages and currents refer to the interface of the bus power supply unit, whether integrated or not.

Apart from transient instances of discharging the capacitance of the bus and of any electrically passive components connected to the bus, a bus power supply shall, for bus voltages in the range of 0 V to 22,5 V, never draw a current of more than 1 mA from the bus, even if its own external power supply has failed. This requirement is inapplicable to power supplies with a maximum current rating of 250 mA.

6.2 Marking of the bus power supply terminals

In addition to the marking requirements defined in 5.2, the bus power supply terminals shall be marked with "+" and "–" to indicate the polarity. If colour coding is used, the colours representing the "+" and "–" shall be given on the bus power supply.

6.3 Capacitors between the interface and earth

If capacitors are connected from the interface circuit to any other part of the device, such as earth, these shall be connected from the negative side of the interface signal. Such capacitors shall fulfil the insulation requirements given in 4.9.

NOTE The capacitance seen on the bus is affected by the capacitance to earth where a capacitor connected between the negative side of the interface and earth on one bus unit is used with another bus unit containing a capacitor connected between the positive side of the interface and earth.

6.4 Voltage rating

The bus power supply shall withstand the voltages shown in Table 7. The bus power supply output voltage shall be as shown in Table 12.

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Table 12 – Bus power supply output voltage

	Minimum	Typical	Maximum	Condition
Output voltage	12,0 V	16,0 V	20,5 V	Full supply voltage range, full load range, full temperature range, idle state

6.5 Current rating

6.5.1 General current rating

The current that the bus power supply is capable of providing to the bus shall be as shown in Table 13.

Both the maximum supply current and the guaranteed supply current shall be stated in the literature. It is also recommended that these should be shown on the label. The guaranteed supply current shall be an absolute minimum and the maximum supply current shall be an absolute maximum.

NOTE 1 Owing to internal power consumption the guaranteed supply current can be less than the maximum supply current when the bus power supply unit is integrated into a bus unit.

NOTE 2 Typically the maximum supply current is maximum at the minimum allowed temperature for the bus power supply, while the guaranteed supply current is minimum at the maximum allowed temperature of the bus power supply.

NOTE 3 The bus power supply current and the transmitter sink current influence signal timing due to the wiring capacitance.

Table 13 – Bus power supply current rating

	Minimum	Typical	Maximum	Condition
Maximum supply current	Guaranteed supply current		250 mA	Full voltage range, full temperature range
Guaranteed supply current[a]	8,0 mA		Maximum supply current	U = 12,0 V, full temperature range
[a] See also 4.6.7.				

6.5.2 Single bus power supply current rating

A bus power supply that is designed to be the only one in the system shall be marked with a maximum supply current of 250 mA. Such a power supply should be able to withstand any ringing on the bus; no test is provided.

NOTE The guaranteed supply current can be substantially lower than the maximum supply current.

6.5.3 Integrated bus power supply current rating

If a power supply is integrated into a bus unit and this bus power supply is the only allowed bus power supply in the system, the minimum transmitter sink current of this bus unit may be reduced to the maximum supply current of the bus power supply.

6.5.4 Dynamic behaviour of the bus power supply

The bus power supply behaviour in case of transitions from open to short circuit shall be as shown in Table 14 and Figure 8.

The bus power supply behaviour in case of transitions from short to open circuit shall be as shown in Table 14 and Figure 9.

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Table 14 – Bus power supply dynamic behaviour

	Minimum	Typical	Maximum	Condition
Voltage undershoot amplitude			0,5 V	Transition from short to open circuit
Voltage undershoot time			100 µs	
Voltage overshoot amplitude			2,0 V	
Voltage overshoot time			100 µs	
Voltage rise time			10 µs	Measured from 0 V to 12 V
Current overshoot amplitude			200 mA	2,5 V/µs transition from open to short circuit
Current overshoot time			10 µs	
Charge overshoot			1 µAs	

If there is more than one overshoot/undershoot, the highest amplitude shall be taken as overshoot/undershoot amplitude. The sum of all overshoot/undershoot times shall be used as overshoot/undershoot time.

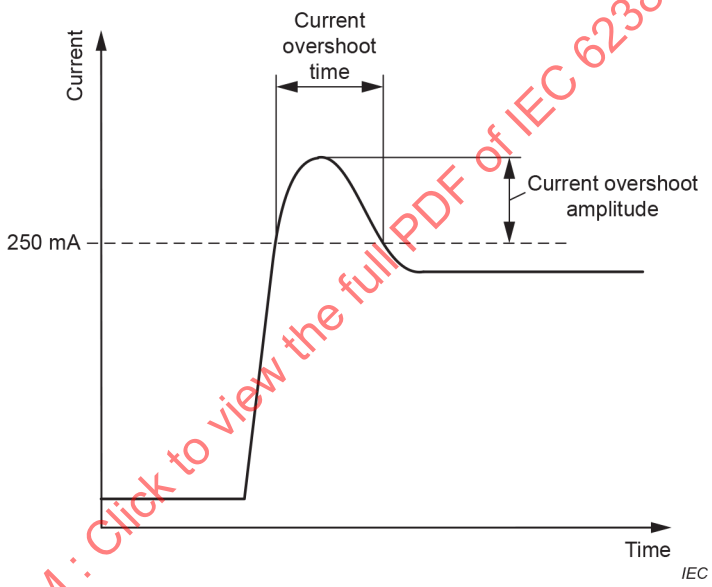

Figure 8 – Bus power supply current behaviour

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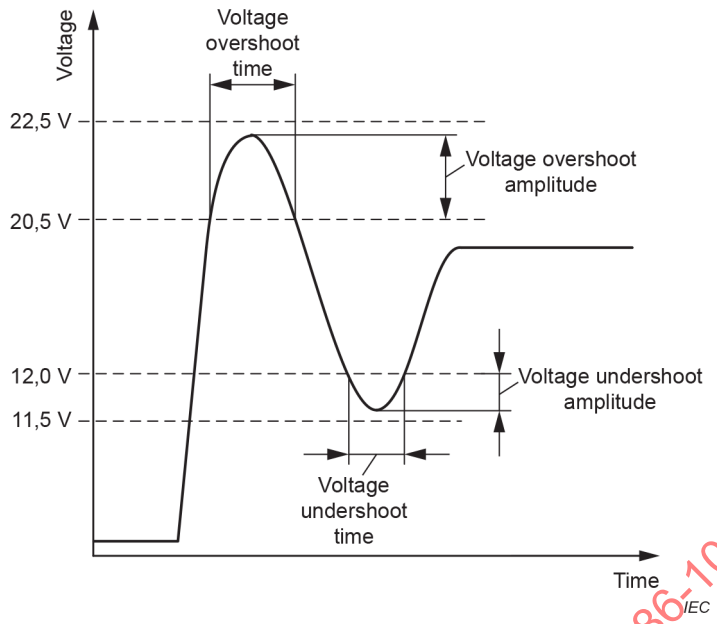

Figure 9 – Bus power supply voltage behaviour

6.6 Bus power supply timing requirements

6.6.1 Short power supply interruptions

The requirements of 4.11.1 and 4.11.2 apply with the following addition:

The bus power supply shall not interrupt the bus power for ~~less than~~ 450 ms or longer.

This requirement means that short power supply interruptions do not cause system failure. However any interruption of the bus power longer than 40 ms ~~may~~ can have an effect on bus powered devices. Therefore it is recommended that the bus power interruption should not exceed 40 ms.

6.6.2 Short circuit behaviour

On detection of a short circuit which exists for longer than the minimum shutdown delay time given in Table 15, the bus power supply may shut down for a period up to the maximum restart period given in Table 15. On each restart the power supply shall turn on the output for at least the minimum retry time given in Table 15.

NOTE A system failure condition cannot be caused solely by the behaviour of a power supply conforming to these requirements.

Table 15 – Short circuit timing behaviour

	Minimum	Typical	Maximum
Shutdown delay time	600 ms		
Retry time	150 ms [a]		
Restart period			15 s
[a] A minimum retry time of 600 ms is recommended.			

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In a system, there ~~shall be~~ should not be more than one power supply with the shutdown mechanism. This is to prevent the possibility of two or more power supplies entering shutdown, followed by them retrying at different times, with neither able to return to normal operation due to insufficient supply current to restore a loaded bus, and so remaining in the shutdown state **16**.

If a bus power supply uses the shutdown mechanism, this shall be stated in the literature. It is also recommended that the information about this shutdown mechanism be shown on the label.

Bus power supplies without the shutdown mechanism shall be short circuit proof, such that after removal of the short circuit, the bus voltage shall recover with the voltage rise time given in Table 14.

7 Transmission protocol structure

7.1 General

This Clause 7 describes the encoding of forward frames and of backward frames ~~shall be as described in the following subclauses~~. Figure 10 shows an example of a frame. The most significant bit shall always be transmitted first, immediately after the start bit. The least significant bit shall always be transmitted last, immediately before the stop condition. The bit numbering shall always be zero-based. Thus the most significant bit of an n-bit frame shall be bit n-1.

Figure 10 – Frame example

7.2 Bit encoding

7.2.1 Start bit and data bit encoding

The start bit as well as the data bits shall be bi-phase encoded. A logical 1 shall contain a rising edge inside the encoded bit; a logical 0 shall contain a falling edge inside the encoded bit, as shown in Figure 11.

Figure 11 – Bi-phase encoded bits

A start bit shall be encoded as logical 1.

7.2.2 Stop condition encoding

The stop condition shall be encoded as idle state. The stop condition shall start at the last rising edge.

NOTE If the last bit of the frame is logical 1, the stop condition begins inside this bit. If the last bit of the frame is logical 0, the stop condition begins at the end of this bit.

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7.3 Frame description

A frame shall consist of:

- 1 start bit;
- n data bits;
- 1 stop condition.

NOTE 1 The number of data bits n depends on the type of frame.

NOTE 2 A frame with n data bits is called an n-bit frame.

7.4 Frame types

7.4.1 16-bit forward frame

A 16-bit forward frame shall contain n = 16 data bits.

NOTE This type of forward frame can be used to communicate with control gear conformant to IEC 62386-102.

7.4.2 24-bit forward frame

A 24-bit forward frame shall contain n = 24 data bits.

NOTE This type of forward frame can be used by and to communicate with control devices conformant to IEC 62386-103.

7.4.3 32-bit forward frame 17

A 32-bit forward frame shall contain n = 32 data bits.

NOTE This type of forward frame is used for firmware transfers to control gear and control devices conformant to IEC 62386-105.

7.4.4 Reserved forward frame

Frames with n = 20 ~~or n = 32~~ data bits are reserved forward frames. They shall not be used.

7.4.5 Backward frame

A backward frame shall contain n = 8 data bits.

Backward frames shall be used only as answers to forward frames.

7.4.6 Proprietary forward frames

There are two kinds of proprietary forward frames.

- Proprietary forward frames which differ from the ~~forward~~ frames defined or reserved in this document in the number of data bits. Such proprietary forward frames shall trigger a frame size violation in bus units which are not designed to interpret them.
- Proprietary forward frames which differ from the ~~forward~~ frames defined or reserved in this document in the start bit, data bit or stop condition encoding. Such proprietary forward frames shall trigger a bit timing violation in bus units which are not designed to interpret them.

A transmitter sending proprietary forward frames shall comply with the frame sequence timing requirements given in Table 17.

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A multi-master transmitter sending proprietary forward frames shall comply with the frame sequence timing requirements given in Table 22 and shall use by default priority 5 only, until configured otherwise.

NOTE Proprietary forward frames can trigger backward frames.

A receiver designed for proprietary frames with n = 8 to n = 15 bits can distinguish such frames from overlapping backward frames by a variety of methods. Nevertheless it is recommended that such designs be avoided.

8 Timing

8.1 Single-master 18 transmitter timing

8.1.1 Single-master transmitter bit timing

The transmitter bit timing shall conform to the limits shown in Table 16. Figure 12 illustrates a portion of a typical frame.

NOTE 1 This timing definition is used for control gear and single-master control devices. Multi-master control devices are subject to tighter timing constraints. See 8.3.1.

NOTE 2 See Clause A.4 for further details on the change in timing definitions with the change from the first edition to the second edition of this standard.

Regardless of the low level voltage and the high level voltage, the timing is measured at a level of 8,0 V.

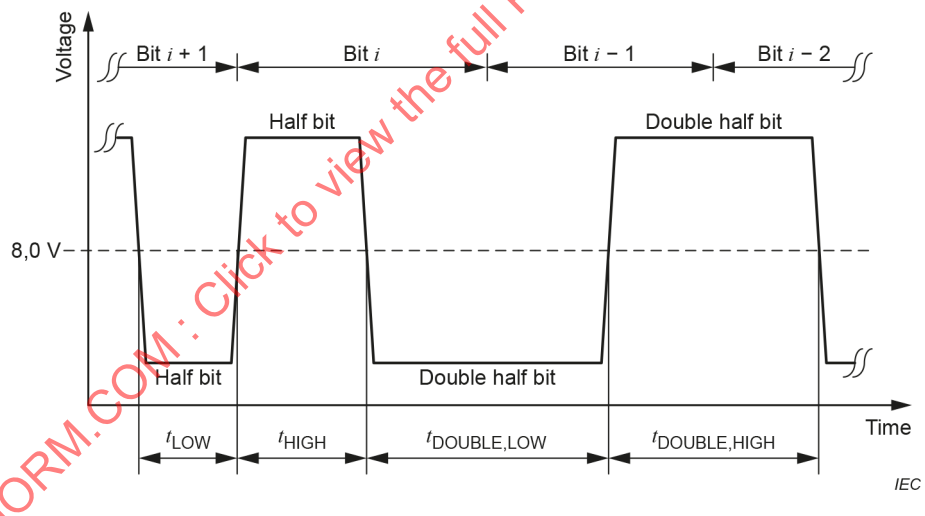

Figure 12 – Bit timing example

Table 16 – Transmitter bit timing

	Minimum	Typical	Maximum
Half bit time t_{HIGH}, t_{LOW}	366,7 µs	416,7 µs	466,7 µs
Double half bit time $t_{DOUBLE,LOW}$, $t_{DOUBLE,HIGH}$	733,3 µs	833,3 µs	933,3 µs
Stop condition time T_{STOP}	2 450 µs		

8.1.2 Single-master transmitter frame sequence timing

Figure 13 shows the settling time between two consecutive frames.

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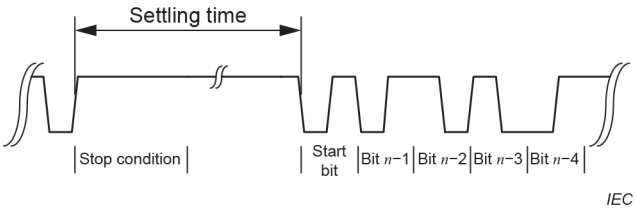

Figure 13 – Settling time illustration

For the settling time the values given in Table 17 shall apply.

NOTE When designing a bus powered bus unit, the minimum transmitter settling time can be regarded as a period during which power can reliably be drawn from the bus.

Table 17 – Transmitter settling time values

	Minimum	Typical	Maximum
Settling time between a forward frame and a backward frame[a]	5,5 ms		10,5 ms
Settling time between any other frame and a forward frame	13,5 ms [b]		75,0 ms [c]

[a] A transmitter shall start the transmission of its backward frame (if any) within the time slot defined in this Table 17, regardless of whether any other transmitter has already started to transmit a backward frame of its own. The settling time apparent on the bus will naturally depend upon the timing of the first backward frame transmitted; the notional settling time for later backward frames can be regarded as a delay time.

[b] Also applicable after overlapping backward frames causing a receiver bit timing violation or a receiver frame size violation.

[c] Only applicable for send-twice forward frames, see 9.4.

8.2 Receiver timing

8.2.1 Receiver bit timing

A receiver shall receive or reject frames according to the bit timing requirements as follows.

It is recommended that short pulses and spikes ~~should be~~ are ignored.

For logical bits starting with an edge, the timing given in Table 18 shall apply to the duration from this starting edge, to the next edge. This period can be the first half bit of a start bit, or a stop condition, or the first half bit of another logical bit where the previous logical bit is of the same value.

The timing in Table 19 shall apply from the edge inside a logical bit, to the next edge. This period can be a half bit, a double half bit or a stop condition.

Figure 14 shows which table is applicable at which time period in an example.

After the minimum stop condition given in Table 18 and Table 19, a frame is regarded as having been received.

NOTE 1 For the significance of ~~this~~ regarding the frame as received, see 9.1.1.

NOTE 2 Receiving a valid backward frame does not necessarily imply that it was sent by a single transmitter as backward frames can overlap synchronously, or nearly so.

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Table 18 – Receiver timing starting at the beginning of a logical bit

Minimum	Typical	Maximum	Description
		< 333,3 µs	Grey area
333,3 µs	416,7 µs	500 µs	Half bit
> 500 µs		< 750 µs	Grey area
750 µs		1 400 µs [a] 45 ms [b]	Bit timing violation
> 1 400 µs [a]		< 2 400 µs [a]	Grey area
2 400 µs [a]			Stop condition

[a] Only applicable for idle state.

[b] Only applicable for active state. Active state longer than 45 ms shall be interpreted as bus power down.

Table 19 – Receiver timing starting at an edge inside of a logical bit

Minimum	Typical	Maximum	Description
		< 333,3 µs	Grey area
333,3 µs	416,7 µs	500 µs	Half bit
> 500 µs		< 666,7 µs	Grey area[c]
666,7 µs	833,3 µs	1 000 µs	2 half bits
> 1 000 µs		< 1 200 µs	Grey area
1 200 µs		1 400 µs [a] 45 ms [b]	Bit timing violation
> 1 400 µs [a]		< 2 400 µs [a]	Grey area
2 400 µs [a]			Stop condition

[a] Only applicable for idle state.

[b] Only applicable for active state. Active state longer than 45 ms shall be interpreted as bus power down.

[c] If an edge occurs after a time within the grey area, the receiver can conclude that it is a timing violation. This can be caused for example, by overlapping backward frames.

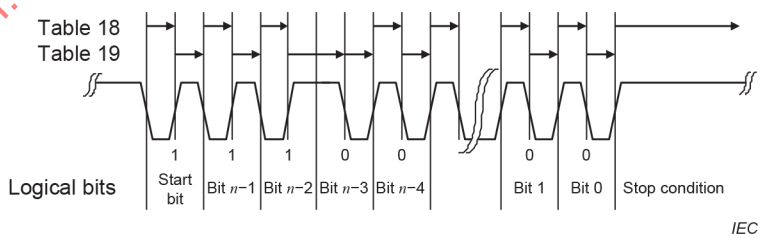

Figure 14 – Receiver timing decision example

8.2.2 Receiver bit timing violation

If a receiver detects a bit timing violation it shall reject the frame, except in case of a backward frame. See 8.2.5.

After the detection of a bit timing violation, the receiver shall be ready for decoding the next frame immediately after detection of a stop condition.

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NOTE A receiver bit timing violation could be the result of more than one transmitter being active, e. g. in case of overlapping backward frames.

8.2.3 Receiver frame size violation

If a receiver detects a frame with a number of data bits not supported by that receiver, this shall trigger a frame size violation and shall be ignored, except in case of a backward frame, see 8.2.5.

After a frame size violation the receiver shall be ready to decode the next frame immediately after the detection of a stop condition.

NOTE A receiver frame size violation could be the result of more than one transmitter being active, or the result of a proprietary forward frame, see 7.4.6.

8.2.4 Receiver frame sequence timing

Decoding of a new frame shall only start after detection of a stop condition.

NOTE This requirement ensures that for example, a 24-bit forward frame is not interpreted as a 16-bit forward frame when the receiver starts up during the transmission of the 24-bit forward frame.

A receiver shall accept frame sequences with the settling times given in Table 20.

Table 20 – Receiver settling time values

	Minimum	Typical	Maximum	Description
Settling time between forward frame and backward frame	> 1,4 ms [a]		< 2,4 ms	Grey area[b]
	2,4 ms		12,4 ms	Frame shall be interpreted as backward frame.
	> 12,4 ms		< 13,4 ms	Grey area[b]
	13,4 ms			Frame shall not be interpreted as backward frame.
Settling time between forward frame and forward frame	> 1,4 ms [a]		< 2,4 ms	Grey area[b]
	2,4 ms			Frame shall be interpreted as forward frame.
Settling time between first and second forward frame of send-twice forward frames[c]	> 1,4 ms [a]		< 2,4 ms	Grey area[b]
	2,4 ms		94 ms	Frames shall be interpreted as send-twice forward frames.
	> 94 ms		< 105 ms	Grey area[c d]
	105 ms			Frames shall be interpreted as two separate forward frames.
Settling time between backward frame and forward frame	> 1,4 ms [a]		< 2,4 ms	Grey area[b]
	2,4 ms			Frame shall be interpreted as forward frame.

[a] Because of the definition of the stop condition this is the minimum time to distinguish frames.

[b] Frames within this area can be interpreted in multiple ways.

[c] See 9.4.

[d] Frames within this area can be interpreted as send-twice forward frames or as two separate forward frames.

8.2.5 Reception of backward frames

The reception of a backward frame shall start with the first active state after the forward frame which triggered the backward frame if this first active state is detected within a maximum of 13,4 ms settling time.

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If this frame triggers a frame size violation or bit timing violation, it shall be interpreted as a backward frame. It is possible that such a frame ~~might~~ will contain information that is worth processing in certain cases. See also 7.4.5 and 9.6.2.

8.3 Multi-master transmitter timing

8.3.1 Multi-master transmitter bit timing

The multi-master transmitter bit timing shall be according to the values given in Table 21.

Figure 12 illustrates a portion of a typical frame.

Regardless of the low level voltage and the high level voltage, the timing is measured at a level of 8,0 V.

Table 21 – Multi-master transmitter bit timing

	Minimum	Typical	Maximum
Half bit time t_{HIGH}, t_{LOW}	400,0 µs	416,7 µs	433,3 µs
Double half bit time $t_{DOUBLE,LOW}$, $t_{DOUBLE,HIGH}$	800,0 µs	833,3 µs	866,7 µs
Stop condition time T_{STOP}	2 450 µs		

A multi-master transmitter shall follow the rules of collision avoidance (see 9.2.2), collision detection (see 9.2.3), and collision recovery (see 9.2.4).

8.3.2 Multi-master transmitter frame sequence timing

In order to minimize the probability of collisions, different frame priorities shall be realized using different settling times.

NOTE 1 The usage of the forward frame priorities is described in IEC 62386-103.

Figure 13 shows the settling time between two consecutive frames.

For the settling time of frames with different priorities, the values given in Table 22 shall apply.

NOTE 2 When designing a bus powered bus unit, the minimum transmitter settling time can be regarded as a period during which power can reliably be drawn from the bus.

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Table 22 – Multi-master transmitter settling time values

Settling time between	Minimum	Typical	Maximum
Forward frame and backward frame[a]	5,5 ms		10,5 ms
Any frame and forward frame (priority 1)[b]	13,5 ms	[c]	14,7 ms [d]
Any frame and forward frame (priority 2)[b]	14,9 ms	[c]	16,1 ms [d]
Any frame and forward frame (priority 3)[b]	16,3 ms	[c]	17,7 ms [d]
Any frame and forward frame (priority 4)[b]	17,9 ms	[c]	19,3 ms [d]
Any frame and forward frame (priority 5)[b]	19,5 ms	[c]	21,1 ms [d]

[a] This is a delay time where the backward frame can start regardless of transitions in between.

[b] Also applicable after overlapping backward frames causing a receiver bit timing violation or a receiver frame size violation.

[c] It is strongly recommended that a multi-master transmitter starts its transmission at a random point of time within the minimum and maximum settling time corresponding to the intended priority, as this helps in avoiding collisions. Clock tolerances need to be considered.

[d] When a multi-master transmitter intends to send a frame with a certain priority but the maximum settling time for this priority has already passed, the transmitter can start its transmission immediately considering collision avoidance.

9 Method of operation

9.1 Dealing with frames and commands

9.1.1 General

The flow from the moment a number of bits are received on the bus interface until a command is executed is illustrated in Figure 15. The conditions to enter the next state are described in 9.1.2, 9.1.3, 9.1.4 and 9.1.5. This Subclause 9.1 does not necessarily apply when using proprietary forward frames.

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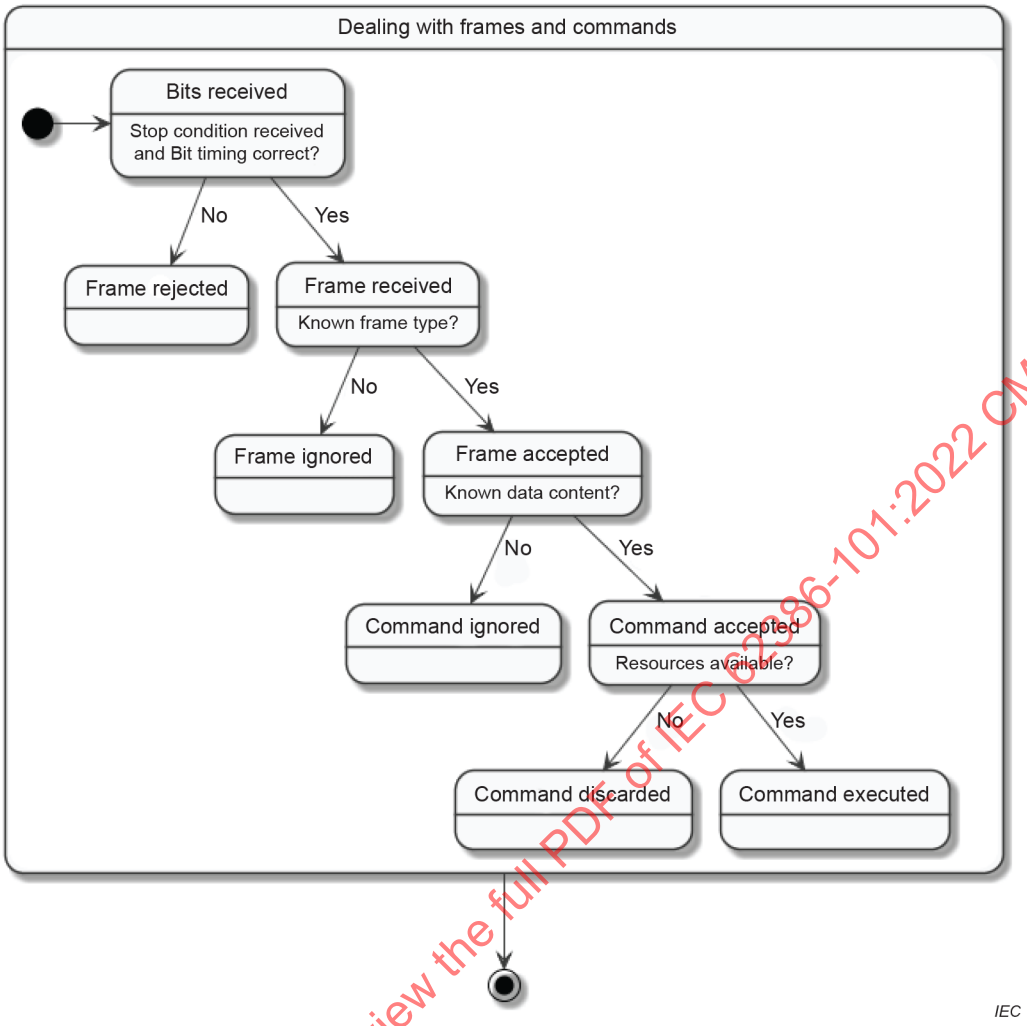

Figure 15 – Dealing with frames and commands

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9.1.2 Frame received or rejected

Any frame consisting of valid bits and a stop condition shall be considered received, otherwise it shall be considered rejected.

9.1.3 Frame accepted or ignored

Any received frame that uses the correct frame type and correct number of data bits for a particular receiver shall be considered accepted, otherwise it shall be considered ignored.

9.1.4 Command accepted or ignored

Any accepted frame shall be analysed for content. If the content forms a command, this command shall be accepted, otherwise it shall be considered as an ignored command.

NOTE Further details on commands are given in IEC 62386-102, IEC 62386-103, the IEC 62386-2xx series and the IEC 62386-3xx series.

9.1.5 Command executed or discarded

Any accepted command shall be executed in the settling time between the frame in which it was received and the next possible frame on the bus, except when explicitly stated otherwise in the description of the command. Execution of the command could depend on resources to handle the command.

Accepted commands that are not executed are considered discarded.

NOTE 1 The next frame on the bus could be a new command or the answer to the received command.

NOTE 2 This timing requirement refers to the change of and the reaction to internal signals of a bus unit. The delay time between external signals and internal signals of a bus unit is not within the scope of this document, but could be a performance issue of a system.

The refresh rate of internal variables (for example a status) should be such that a correct new value can be observed immediately following a command that changes this value (for example a configuration command), except when explicitly stated otherwise in the description of the command.

The execution of a command ~~may~~ can involve the triggering of a process which itself takes longer than the settling time between frames.

NOTE 3 An example for such a process is a running fade.

9.2 Collision avoidance, collision detection and collision recovery

9.2.1 General

Collision avoidance (9.2.2), collision detection (9.2.3), and collision recovery (9.2.4) apply to multi-master transmitters only. They do not apply to backward transmissions.

A multi-master transmitter shall always attempt to avoid collisions before sending a forward frame.

As collisions cannot be avoided in all situations, a collision detection mechanism is necessary. A transmitter detecting a collision shall always cancel its own transmission immediately.

If, after collision detection, the resulting signal on the bus violates the timing requirements of 9.2.3, a collision recovery mechanism shall be applied.

9.2.2 Collision avoidance

Collision avoidance shall be achieved by checking the settling time before transmitting a forward frame. This implies that a multi-master transmitter shall not start a transmission when the bus is not in idle state.

NOTE The settling time depends on the frame priority used.

9.2.3 Collision detection

Collision detection shall be applied during the transmission of any forward frame.

When the resulting signal on the bus shown in Table 24 is not identical to the signal the multi-master transmitter intended to transmit, the multi-master transmitter shall immediately stop its transmission.

When the transmitter that stopped its transmission can guarantee that the timing of the signal created before stopping the transmission does not meet one of the destroy areas given in Table 23 and Table 24, it shall return to collision avoidance as described in 9.2.2. The transmitter ~~might~~ may restart its transmission if it is still required. See also Clause A.3.

Otherwise the transmitter that stopped its transmission shall check the timing of the signal on the bus:

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- When the timing of the resulting signal does not meet one of the destroy areas given in Table 23 and Table 24, the transmitter shall return to collision avoidance as described in 9.2.2. The transmitter ~~might~~ may restart its transmission if it is still required.

NOTE 1 In this case the resulting frame on the bus is still a valid forward frame and can be received by any bus unit on the bus.

- When the timing of the resulting signal on the bus meets one of the destroy areas given in Table 23 and Table 24, the transmitter shall follow the collision recovery method described in 9.2.4. After collision recovery the transmitter ~~might~~ may restart its transmission.

NOTE 2 In this case there would be a risk that one or more devices connected to the bus could interpret the frame as containing relevant data, whilst others could reject it. This risk is averted by destroying the frame and thereby ensuring that all receivers will regard it as invalid.

Table 23 – Checking a logical bit, starting at an edge at the beginning of the bit

Minimum	Typical	Maximum	Description
		< 100 µs	Grey area[c]
100 µs		356,7 µs	Destroy area[a]
> 356,7 µs		< 400,0 µs	Grey area
400,0 µs		433,3 µs	Valid half bit
> 433,3 µs		< 476,7 µs	Grey area
476,7 µs			Destroy area[a b]

[a] Signals within the destroy area shall lead to collision recovery described in 9.2.4.

[b] Only applicable for active state.

[c] Pulses in this grey area may be ignored and not considered in decisions on timing as they ~~may~~ can result from noise.

Table 24 – Checking a logical bit, starting at an edge inside the bit

Minimum	Typical	Maximum	Description
		< 100 µs	Grey area[c]
100 µs		356,7 µs	Destroy area[a]
> 356,7 µs		< 400,0 µs	Grey area
400,0 µs		433,3 µs	Valid half bit
> 433,3 µs		< 476,7 µs	Grey area
476,7 µs		723,3 µs	Destroy area[a]
> 723,3 µs		< 800,0 µs	Grey area
800,0 µs	833,3 µs	866,7 µs	2 valid half bits
> 866,7 µs		< 943,3 µs	Grey area
943,3 µs			Destroy area[a b]

[a] Signals within the destroy area shall lead to collision recovery described in 9.2.4.

[b] Only applicable for active state.

[c] Pulses in this grey area may be ignored and not considered in decisions on timing as they ~~may~~ can result from noise.

The signal delay times of the transmitter and the receiver necessary for the check need to be taken into account when at multi-master transmitters. See Clause A.3.

Figure 16 shows which table is applicable at which time period in an example.

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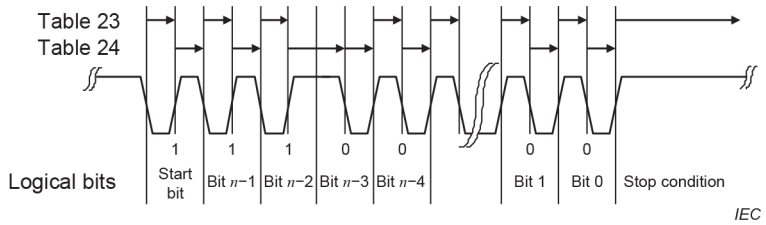

Figure 16 – Collision detection timing decision example

9.2.4 Collision recovery

When starting the collision recovery the multi-master transmitter shall force the bus to active state for the break time t_{BREAK} given in Table 25 within 450 µs at the latest.

NOTE 1 This results in all bus units detecting a bit timing violation. All multi-master transmitters will enter the collision recovery process.

After the break time the multi-master transmitter shall check the bus. If the bus is in active state, the multi-master transmitter shall return to collision avoidance as described in 9.2.2. Otherwise the multi-master transmitter shall return to collision avoidance as described in 9.2.2 also, but it shall restart its original transmission with a reduced settling time $t_{RECOVER}$.

NOTE 2 By this method the last transmitter releasing the bus will be the first restarting to transmit its forward frame.

Table 25 – Collision recovery timing

	Minimum	Typical	Maximum
Break time t_{BREAK}	1,2 ms		1,4 ms
Recovery time $t_{RECOVER}$	4,0 ms	[a]	4,6 ms
[a] It is strongly recommended that a multi-master transmitter start its transmission at a random point of time in the interval between the minimum and maximum recovery time, as this helps in avoiding collisions.			

It is possible that when using proprietary frames this break time ~~may~~ is not ~~be~~ long enough to guarantee detection. Care should be taken that the proprietary frame is still valid, or a proprietary solution should be in place for these frames.

Figure 17 shows an example of the collision recovery mechanism:

Multi-master transmitter 1 detects a collision at point A of the frame it is intending to transmit and immediately forces the bus to active state for the break time t_{BREAK}. Multi-master transmitter 2 now detects the collision at point B of the frame it is intending to transmit. It also forces the bus to active state for the break time t_{BREAK}.

At the end of the break time t_{BREAK} of multi-master transmitter 1 the bus is still in active state (point C). Therefore multi-master transmitter 1 enters collision avoidance with the normal settling time depending on the priority of the forward frame to be transmitted. The settling time of multi-master transmitter 1 begins when the bus returns to idle state.

At the end of the break time of multi-master transmitter 2 the bus returns to idle state (point D). Therefore multi-master transmitter 2 enters collision avoidance with the reduced settling time $t_{RECOVER}$. As a consequence transmitter 2 will restart its transmission whilst transmitter 1 is still waiting for the end of its settling time.

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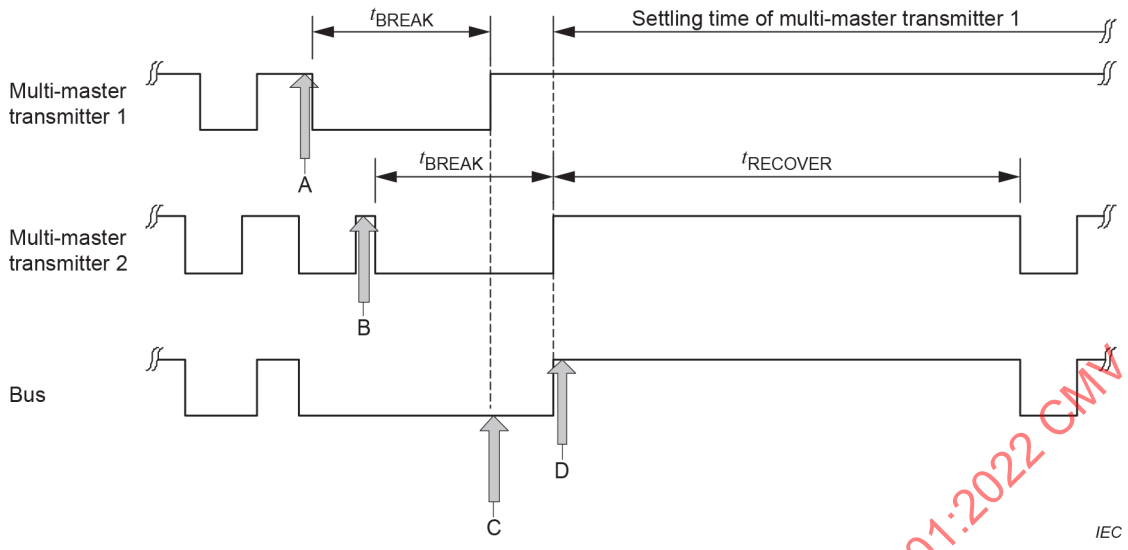

NOTE The traces of multi-master transmitter 1 and multi-master transmitter 2 are shown only for explanation and cannot be measured in a real system, where only the signal labelled "Bus" occurs.

Figure 17 – Collision recovery example

9.3 Transactions

This Subclause 9.3 shall apply for multi-master transmitters only.

The purpose of transactions is to ensure that a sequence of commands sent by one control device cannot be interrupted by another control device.

The first frame of the transaction shall be sent with priority 2, 3, 4 or 5. All remaining forward frames of the transaction shall be sent with priority 1. The priority of the first frame of a transaction shall depend on the primary purpose of the transaction. See IEC 62386-103 for details on priorities.

NOTE By definition a transaction can consist of a single forward frame.

Except during commissioning, a single transaction should not exceed a total duration of 400 ms so that more than one control device can get access to the bus in a reasonable time. The total duration of successively transmitted transactions from a single control device should not exceed 400 ms without at least one multi-master transmitter settling time exceeding the maximum settling time for priority 5.

9.4 Send-twice forward frames and send-twice commands

Some of the commands defined in IEC 62386-102, IEC 62386-103, the IEC 62386-2xx series and the IEC 62386-3xx series need to be accepted twice within a defined period of time before being executed. Control devices shall use send-twice forward frames for transmission of such commands.

A transmitter shall transmit two identical forward frames which make up a send-twice forward frame:

- with a settling time as shown in Table 17; see footnote c in the table, and
- without any other forward frame in-between.

A multi-master transmitter shall transmit two identical forward frames which make up a send-twice forward frame as a transaction.

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A receiver shall accept two consecutive forward frames as a send-twice forward frame, if all of the following conditions hold:

- the settling time between the two identical forward frames is less than or equal to the maximum receiver settling time given in Table 20;
- no active state occurs in between the two forward frames;
- the two forward frames are identical.

If any one of the above conditions is not met, the receiver shall interpret all frames as separate forward frames. Consequently the last forward frame received in this context may be interpreted as the first forward frame of a new pair of send-twice forward frames.

9.5 Command iteration

Some of the commands defined in IEC 62386-102, IEC 62386-103, the IEC 62386-2xx series, and the IEC 62386-3xx series, trigger and extend appropriate functions when repeated periodically.

In addition to the requirements given in 8.1 and 8.3, a transmitter shall transmit the commands of a command iteration following the requirements given in Table 26.

NOTE There could be other frames sent in-between the frames of a command iteration.

Table 26 – Transmitter command iteration timing

	Minimum	Typical	Maximum	Description
Transmitter command iteration interval			175 ms	Measured between the last rising edge of one frame and the last rising edge of the next following frame of a command iteration.

A receiver shall trigger the appropriate function when the frame of the first command of command iteration is accepted.

A receiver shall extend the appropriate function after each acceptance of the command if the frame is received before the maximum receiver command iteration timeout given in Table 27, even if other frames are received within the command iteration.

Table 27 – Receiver command iteration timing

	Minimum	Typical	Maximum	Description
Receiver command iteration timeout[a]	12,6 ms		180 ms	Accept as command of a command iteration.
	> 180 ms		< 220 ms	Grey area
	220 ms			Reject as command of a command iteration.
[a] Measured between the point of time one frame of the command iteration was received and the next following frame was received; see 8.2.1.				

9.6 Usage of a shared interface

9.6.1 General

This Subclause 9.6 applies only to ~~products~~ bus units where more than one logical unit or instance share the same physical interface.

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9.6.2 Backward frames

The transmitter shall transmit a valid backward frame if the content of the backward frame of all logical units is identical. The answer NO to a query shall not be considered a backward frame with content.

If the content is not identical, the transmitter shall transmit a corrupted backward frame that contains an active state of at least 1 300 µs and maximum 2 000 µs.

NOTE This is to simulate overlapping backward frames.

9.6.3 Forward frames

The transmitter shall transmit the forward frames generated within the bus unit sequencially considering the priorities.

NOTE This is to ensure that a bus unit does not cause internally generated collisions.

9.7 Use of multiple bus power supplies

The sum of the maximum supply current of all bus power supply units connected to the bus shall not exceed 250 mA.

Bus power supplies shall not be connected to the bus with reversed polarity, however all power supplies shall be protected for such cases, which includes the capability to handle the power dissipation caused by reverse polarity.

NOTE 1 ~~In particular, the power dissipation has to be taken into account in such case of faulty wiring, as the voltage can be −22,5 V worst case. A Zener diode could be used.~~ In determining the power dissipation, faulty wiring can result in a worst-case voltage of −22,5 V due to reverse polarity. A Zener-diode could be used for reverse polarity protection.

NOTE 2 Whenever multiple power supplies are used, there is a possibility that the system ~~might~~ will not have enough power to continue normal operation when one of the power supplies fails.

NOTE 3 See also Clause A.5.

~~9.7 Command execution~~ 19

~~A command, having been received as described in 8.2, shall then be executed in the settling time between the frame in which it was received and the next possible frame on the bus, except when explicitly stated otherwise in the description of the command.~~

~~NOTE 1 The next frame on the bus could be a new command or the answer to the received command.~~

~~NOTE 2 This timing requirement refers to the change of and the reaction to internal signals of a bus unit. The delay time between external signals and internal signals of a bus unit is not in the scope of this standard, but could be a performance issue of a system.~~

~~The refresh rate of internal variables (for example a status) should be such that a correct new value can be observed immediately following a command that changes this value (for example a configuration command), except when explicitly stated otherwise in the description of the command.~~

~~The execution of a command may involve the triggering of a process which itself takes longer than the settling time between frames.~~

~~NOTE 3 An example for such a process is a running fade.~~

10 Declaration of variables

There are no variables for control gear or control devices defined in this document.

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11 Definition of commands

There are no commands for control gear or control devices defined in this document.

~~12 Test procedures~~

~~Void~~

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Annex A
(informative)

Background information for systems

A.1 Wiring information

The sum of the resistive voltage drop is one of the factors limiting the system size. The maximum allowed voltage drop ΔU on the bus ~~shall be less or equal~~ of 2,0 V~~. It depends on~~, is determined from the bus supply current I_B and the total resistance R_T of the wiring:

$$\Delta U = R_T \times I_B$$

The total resistance R_T of the wiring depends on the specific resistance ρ of the wires used, the cross-section A of the wires and the wiring length L:

$$R_T = 2 \times \rho \times \frac{L}{A}$$

NOTE 1 For the total resistance the length ~~has to be~~ is doubled, since two wires are necessary for the bus, hence the factor two in the formula.

NOTE 2 The specific resistance is temperature dependent.

For the maximum allowed voltage drop of ΔU = 2,0 V and the maximum allowed bus supply current of I_B = 250 mA the following relation between cross-section A and wiring length L can be derived from the above formulae:

$$L = 4\,\Omega \times \frac{A}{\rho}$$

$$L = 4 \times \frac{A}{\rho}$$

Table A.1 shows the maximum cable length L between any two bus units or bus power supplies for different wiring cross-sections A and wiring materials at different temperatures.

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Table A.1 – Maximum cable length

Material	*A* mm^2	Maximum cable length *L* m		
		25 °C	50 °C	75 °C
Copper	0,14	31	28	26
	0,50	112	102	93
	0,75	168	153	140
	1,00	224	204	187
	1,50	300[a]	300[a]	281
	2,00	300[a]	300[a]	300[a]
	2,50	300[a]	300[a]	300[a]
Aluminium	0,14	19	17	16
	0,50	68	62	57
	0,75	102	93	86
	1,00	136	125	115
	1,50	205	187	172
	2,00	273	250	230
	2,50	300[a]	300[a]	288

[a] Cable lengths of more than 300 m are not recommended.

A.2 System architectures

A.2.1 General

Architectures mentioned in this Annex A are examples. Other architectures are also possible.

A.2.2 Single-master architecture

A lighting control system in a single-master architecture ~~may~~ can consist of:

- a bus power supply,
- a single-master application controller,
- at least one control gear.

Figure A.1 shows an example where the single-master application controller shares the physical interface with the bus power supply.

The single-master application controller ~~may~~ can be equipped with:

- buttons and sensors,
- terminals for connection to buttons and sensors, or
- communication interfaces to other bus systems.

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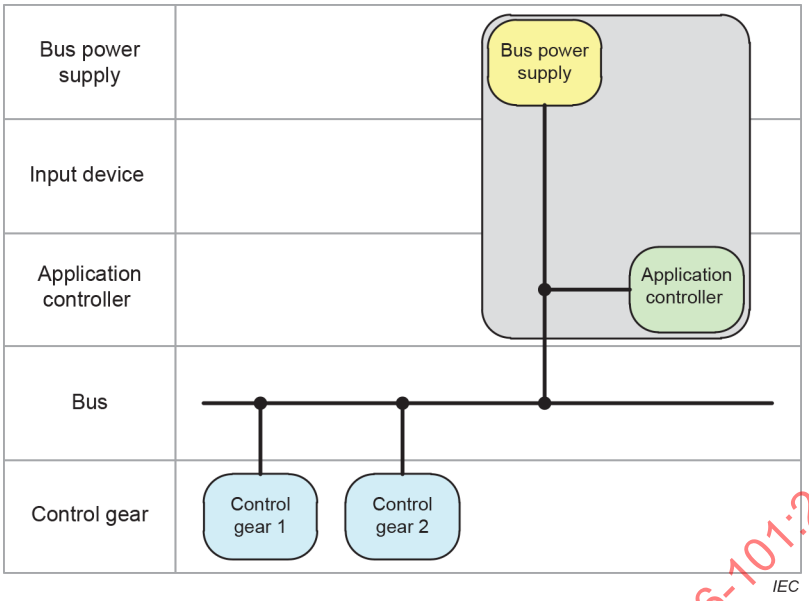

Figure A.1 – Single-master architecture example

In such a system architecture the single-master application controller uses 16-bit forward frames to transmit commands to the control gear.

NOTE Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series.

A.2.3 Multi-master architecture with one application controller

A lighting control system in a multi-master architecture with one application controller ~~may~~ can consist of:

- a bus power supply,
- a multi-master application controller,
- at least one input device, and
- at least one control gear.

Figure A.2 shows an example of a system with one multi-master application controller and two input devices.

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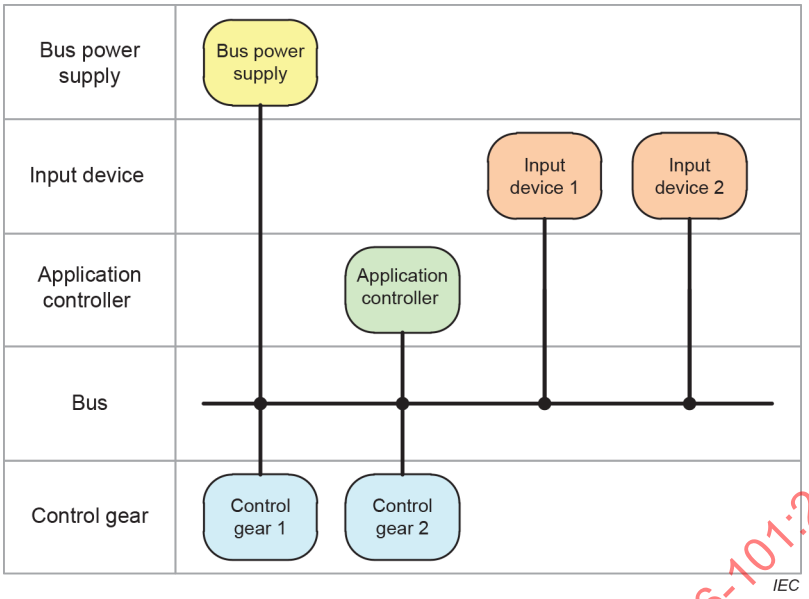

Figure A.2 – Multi-master architecture example with one application controller

In such a system architecture the multi-master application controller uses 16-bit forward frames to transmit commands to the control gear. ~~It may use~~ 24-bit forward frames are used to configure and control the input devices. The input devices use 24-bit forward frames to transmit information to the application controller.

NOTE Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series. Commands for communication between multi-master application controllers and input devices are defined in IEC 62386-103 and the IEC 62386-3xx series.

A.2.4 Multi-master architecture with more than one application controller

A lighting control system in a multi-master architecture with more than one application controller ~~may~~ can consist of:

- a bus power supply,
- at least two multi-master application controllers, and
- at least one control gear.

Figure A.3 shows an example of a system with two application controllers.

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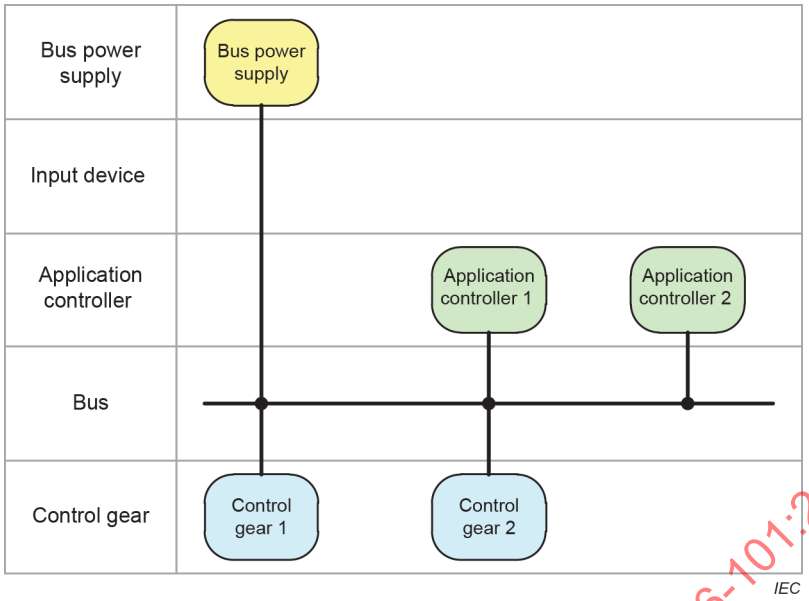

Figure A.3 – Multi-master architecture example with two application controllers

In such a system architecture the two multi-master application controllers use 16-bit forward frames to transmit commands to the control gear. Since more than one multi-master application controller has control over the system, it is clear that these multi-master application controllers ~~shall~~ should be able to cooperate in order to ensure some level of system integrity.

NOTE 1 Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series.

NOTE 2 The two multi-master application controllers can communicate with each other using 24-bit forward frames.

A.2.5 Multi-master architecture with integrated input device

A lighting control system with a multi-master architecture with an integrated input device ~~may~~ can consist of:

- a bus power supply,
- at least one multi-master application controller,
- at least one input device integrated into a multi-master application controller, and
- at least one control gear.

Figure A.4 shows an example of a system with an integrated input device.

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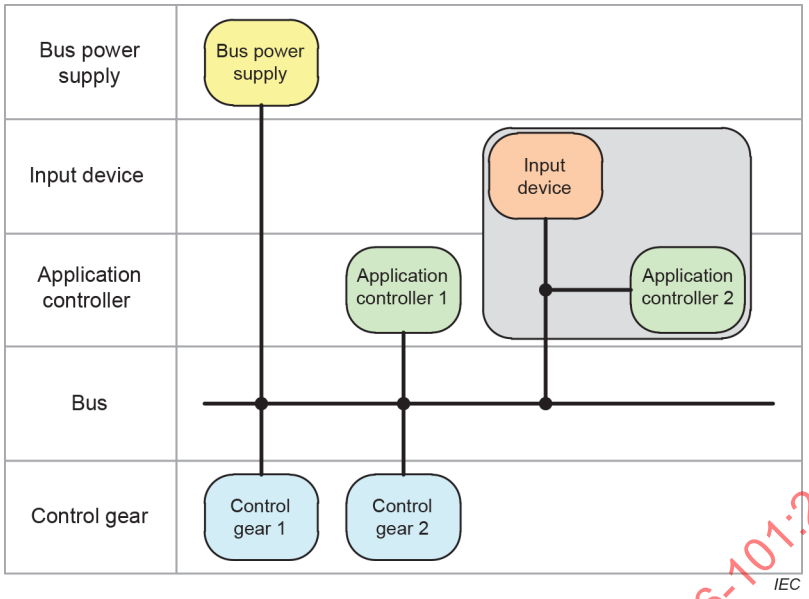

Figure A.4 – Multi-master architecture example with integrated input device

There are two possible modes of operation.

- Multi-master application controller 1 is the only control device which transmits 16-bit forward frames to the control gear. It receives and processes 24-bit forward frames from the input device. The multi-master application controller 2 is disabled in this case.
- Both multi-master application controllers transmit 16-bit forward frames to the control gear and both multi-master application controllers receive and process 24-bit forward frames from the input device. Since more than one multi-master application controller has control over the system, it is clear that these two multi-master application controllers ~~shall~~ should be able to cooperate in order to ensure some level of system integrity. The multi-master application controller 2 and the input device can act as one or as two logical units on the bus.

NOTE 1 Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series.

NOTE 2 The two multi-master application controllers can communicate with each other using 24-bit forward frames.

A.2.6 Multi-master architecture with integrated input device and power supply

A lighting control system in a multi-master architecture with an integrated input device and integrated bus power supply ~~may~~ can consist of:

- zero or more input devices,
- at least one input device and bus power supply integrated into a multi-master application controller, and
- at least one control gear.

Figure A.5 shows an example of a system with an integrated input device and integrated bus power supply.

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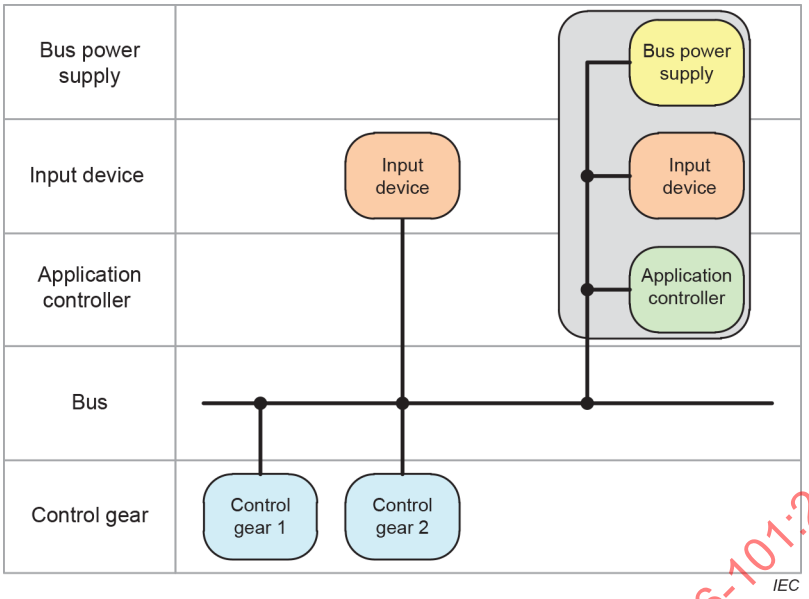

Figure A.5 – Multi-master architecture example with integrated input device and bus power supply

In such a system architecture the multi-master application controller uses 16-bit forward frames to transmit commands to the control gear. ~~It may use~~ 24-bit forward frames are used to configure and control the input devices. The input devices use 24-bit forward frames to transmit information to the application controller.

NOTE Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series. Commands for communication between multi-master application controllers and input devices are defined in IEC 62386-103 and the IEC 62386-3xx series.

A.3 Collision detection

Figure A.6 shows all the timing related issues when transmitting. To read it, start with the TX micro line (which is the microcontroller output to the transmitter circuit), see what happens on the bus and finally see what happens on the RX micro lines (which are the microcontroller input for receiving and checking the timing). All possible delays are accounted for.

The dotted horizontal lines show the thresholds of the local receiver used to check the transmission.

The dashed horizontal lines show the thresholds of a remote receiver, which are valid due to the bus influence. The maximum/minimum remote thresholds are 2,0 V above/below the local thresholds, since a 2,0 V voltage drop is possible on the bus.

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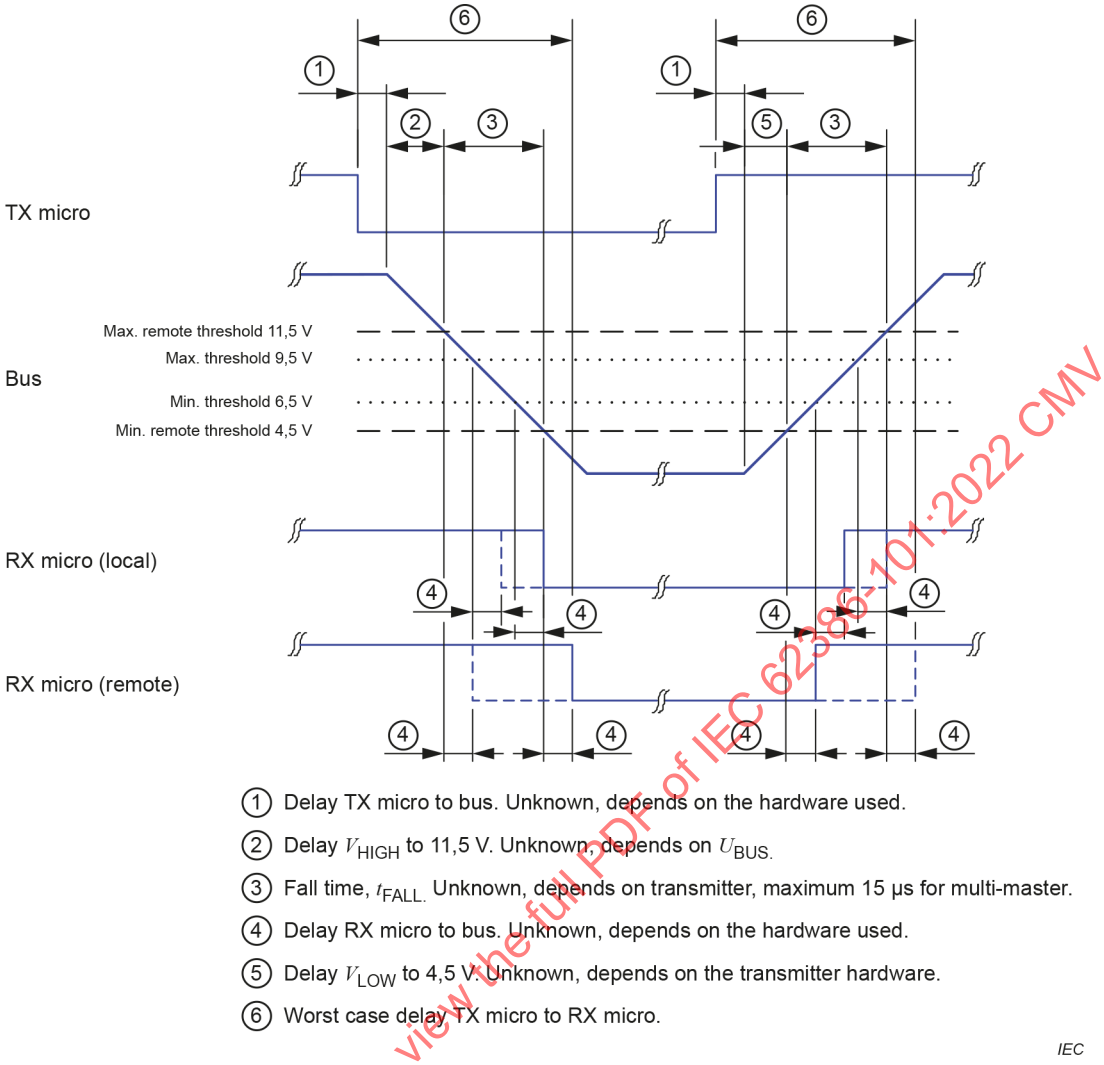

Figure A.6 – Collision detection timing diagram

A.4 Timing definition explanations

A.4.1 General

The aim of this Annex A is to explain the change of timing definitions from Edition 1 of IEC 62386-101:2009 to Edition 2 of IEC 62386-101:2014.

A.4.2 Receiver timing

The receiver timing is in the main points unchanged from Edition 1. The timing tolerances of 10 % have been replaced by absolute minimum and maximum time values.

All timing requirements are given and tested at a fixed threshold voltage of 8,0 V.

A.4.3 Transmitter timing

Edition 1 of IEC 62386-101 did not explicitly define any transmitter timing. Transmitter timing was only given implicitly by the receiver timing and its tolerances. Timing definitions suitable for a proper working multi-master system were not defined.

Also the influence of the wiring and the receiver threshold voltage on signal timing was not fully considered in Edition 1.

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Edition 2 of IEC 62386-101 defines the timings both for single-master and for multi-master transmitters, taking into account all influences upon those timings.

Except where otherwise stated, all timing requirements are given for a fixed threshold voltage of 8,0 V. This threshold voltage is applicable to the test procedures both for transmitters and for receivers. This was not the case in Edition 1.

A.4.4 Grey areas

The definitions in Edition 1 of IEC 62386-101 and IEC 62386-102 did not explicitly define tolerances for the decision points of the receiver timings.

For this reason Edition 2 of IEC 62386-101 introduced so called "grey areas". The design engineer can put the decision point inside this grey area.

Grey areas guarantee that any receiver can interoperate with any transmitter, since the grey areas provide a suitable safety margin. As a consequence the grey areas decrease the possible tolerances for transmitters.

Figure A.7 illustrates the influences that are taken into consideration at the steps from the receiver timing requirements to the multi-master timing requirements.

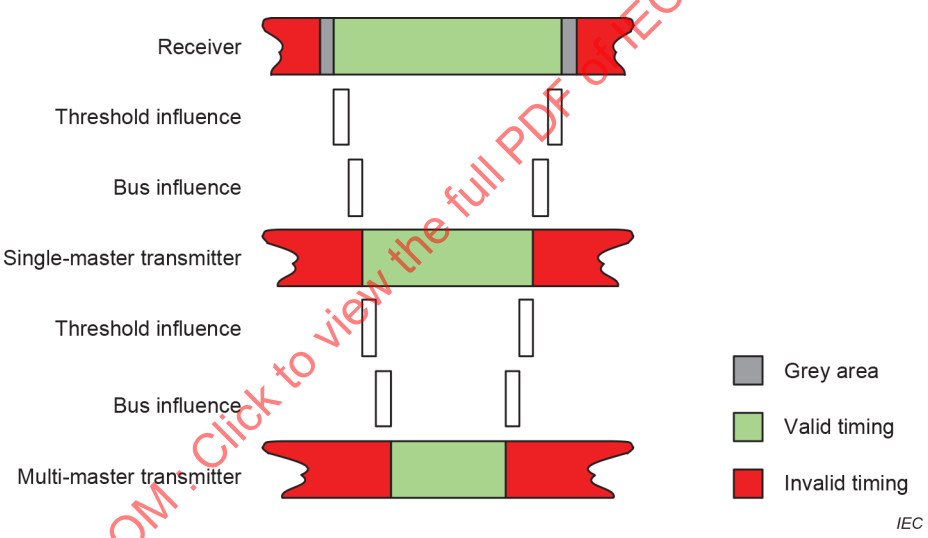

Figure A.7 – Transmitter and receiver timing illustration

A.5 Maximum current consumption calculation explanation

A.5.1 Single bus power supply

A bus power supply is characterized by two current values, its maximum supply current and its guaranteed supply current, as illustrated in Figure A.8.

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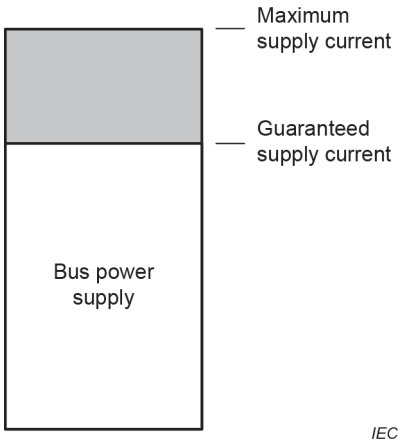

Figure A.8 – Bus power supply current values

The minimum guaranteed supply current is the parameter which ensures that the power supply is sufficient for the combined current demand of all bus units connected. Figure A.9 illustrates that the sum of current demand of all bus units connected ~~shall~~ should be less than or equal to the minimum guaranteed supply current.

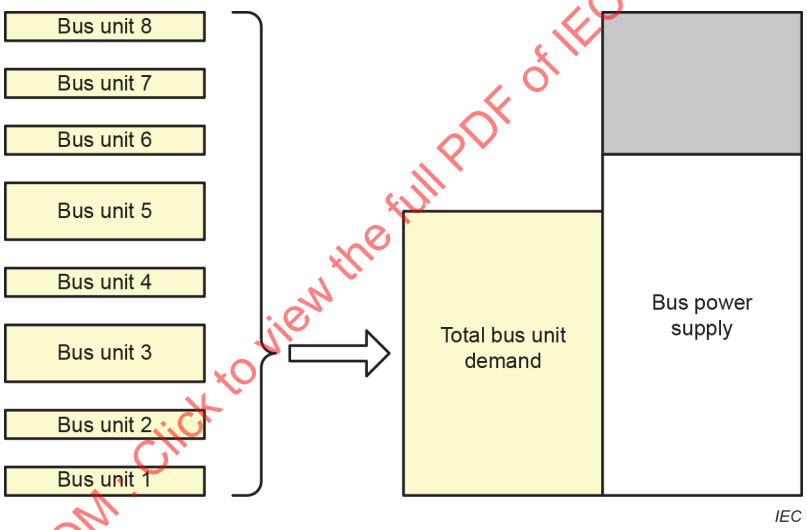

Figure A.9 – Current demand coverage

The maximum supply current is limited to 250 mA as ~~described~~ specified in 6.5.

A.5.2 Multiple bus power supplies

When the current demand of the bus units connected is greater than the guaranteed supply current of a single bus power supply, more than one bus power supply ~~may~~ can be used. In this case the sum of their guaranteed supply currents covers the current demand of the system.

~~Care shall be taken that~~ When selecting bus power supplies for a system, the sum of the maximum supply currents ~~does not exceed~~ can be up to the system limit of 250 mA. Figure A.10 illustrates the situation with four bus power supplies.

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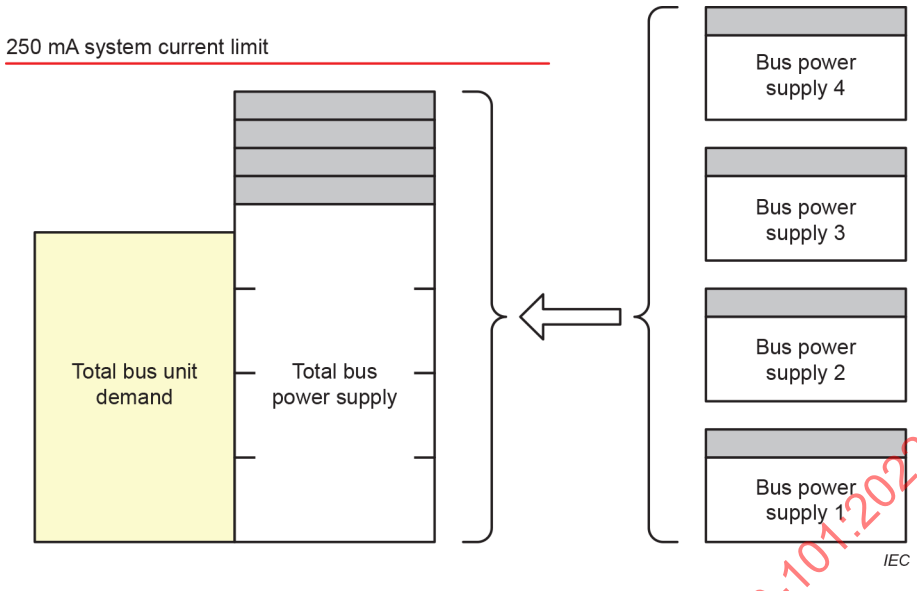

Figure A.10 – Combination of four bus power supplies

A.5.3 Redundant bus power supplies

In some cases a second bus power supply ~~may~~ can be connected to the bus for ~~safety~~ reliability reasons. Thus each of them is capable of covering the complete current demand on its own. If one power supply fails, the current demand can still be covered by the remaining bus power supply.

In such a configuration it is especially important to check that the sum of all maximum currents does not exceed the normative general limit of 250 mA.

Figure A.11 illustrates the situation when using redundant bus power supplies.

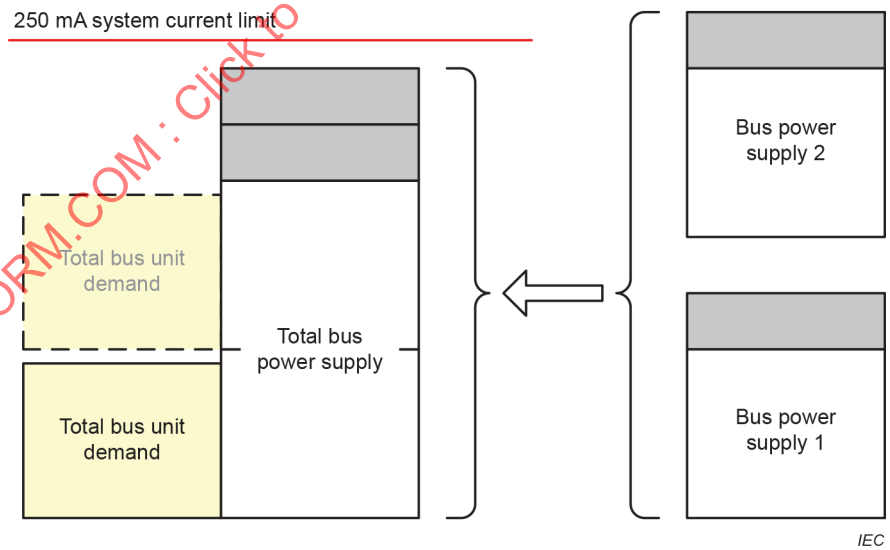

Figure A.11 – Redundant bus power supplies

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A.6 Communication layer overview

A.6.1 General

Table A.2 shows where the specific layers of the open systems interconnection (OSI) communication layer model are handled in different parts of the IEC 62386 series. The ISO/OSI layers are defined in ISO/IEC 7498-1.

Table A.2 – OSI layer model of the IEC 62386 series

OSI layer	Meaning	Description
7 Application	Application specific	Part 102: Instructions and queries for control gear Parts 2xx: Application extended instructions and queries for control gear Part 103: Instructions, queries and event messages ~~at/for~~ to/from control devices Part 104: Instructions and queries for wireless and alternative wired system components Part 105: Instructions and queries for bus units supporting firmware transfer Parts 3xx: ~~Input~~ Control device specific instructions, queries and event messages
6 Presentation	Meaning of codes	Part 102: Address encoding, instruction and query encoding, backward frame encoding ~~at~~ in control gear Part 103: Address encoding, instruction and query encoding, backward frame encoding ~~at~~ in control devices Part 104: Address encoding, instruction and query encoding, backward frame encoding for wireless and alternative wired system components Part 105: Address encoding, instruction and query encoding, backward frame encoding in bus units supporting firmware transfer
5 Session	Request /response	Part 102 and Part 103: Query (16-bit/24-bit forward frame)/Response (8-bit backward frame)
4 Transport	Control transaction	Partially supported through transactions
3 Network	Resolve addresses	First 8 bits of each forward frame: Part 102: 64 short addresses, 16 group addresses, broadcast Part 103: 64 short addresses, 32 control groups, 32 instance groups, 32 instance types, broadcast Part 103: System addresses
2 Data link	Secure telegram	Partially supported through start-stop-framing and fixed length of frames
1 Physical	Bit level	Part 101: • voltage levels, rise/fall time, frame sequence timing, timing tolerances, timing violations • frame types: 16-bit forward frames, 24-bit forward frames, 20-bit ~~/ 32 bit~~ reserved forward frames, 32-bit forward frames, 8-bit backward frames • Manchester encoding, start bit, stop condition, frame size violations • media access rules: collision detection, avoidance and recovery Part 104: • Supported physical layers for wireless and alternative wired system components

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A.6.2 Physical layer

The physical layer is based on a definition of allowed expected bit numbers and Manchester Code checking inside the specified tolerances (IEC 62386-101).

A.6.3 Data link layer

The data link layer checks the quality of data received at the logical layer. The IEC 62386 series ensures data link quality through Manchester Code violation detection, fixed telegram length, start-stop-framing, and bit number checking only. The absence of cyclic redundancy check (CRC) checking is a compromise necessary for simplicity and efficient use of the available bandwidth.

A.6.4 Network layer

The network layer defines logical addressing of devices. ~~Part 101~~ IEC 62386-102 defines 16-bit forward frame addressing and IEC 62386-103 defines 24-bit forward frame addressing formats. A bus unit needs to determine which of the two address spaces is applicable by checking the length of the frames received.

A.6.5 Transport layer

The transport layer ensures data transmission. Within the IEC 62386 series, ~~checks~~ data transmission is checked through session layer commands, the principle of operation for this master-~~slave~~responder communication system.

A.6.6 Session layer

The session layer defines the request/response mechanism (IEC 62386-102 and IEC 62386-103).

A.6.7 Presentation layer

The presentation layer defines format classes for data, commands and special commands (IEC 62386-102, IEC 62386-103 and IEC 62386-105).

A.6.8 Application layer

The application layer defines application specific codes and data formats (IEC 62386-102, IEC 62386-103, IEC 62386-104, IEC 62386-105, IEC 62386-2xx series, IEC 62386-3xx series).

A.7 Effects ~~on~~ of combining version number 1 and version number 2.y devices

Table A.3 shows the effects of replacing~~/~~ or adding a certain edition device (given vertically) in a system formed by devices of the same edition (given horizontally), where minor version number y is currently in the range of 0 to 1.

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Table A.3 – Effects ~~on~~ of combining version number 1 and version number 2.y devices

	Version 1 system	Version 2.y single-master system	Version 2.y multi-master system
Version 1 control gear	Usually it works but there ~~might~~ can be trouble due to incorrect specified timing	Usually it works but there ~~might~~ can be trouble due to new specified timing, commands or behaviour	Usually it works but there ~~might~~ can be trouble due to new specified timing, commands or behaviour
Version 1 control device	Usually it works but there ~~might~~ can be trouble due to incorrect specified timing	The entire system will behave as a version 1 single-master system	Combination is not possible (multi-master controllers are not defined in version 1)
Version 2.y control gear	Usually it works but there ~~might~~ can be trouble due to incorrect specified timing and minor issues ~~may~~ can occur when memory banks are used	Combination is possible	Combination is possible
Version 2.y single-master controller	The entire system will behave as a version 2.y single-master system, as long as only 102 version 1 commands are used	Combination is possible	Combination is not possible (single-master controllers are not meant to be used in a multi-master system)
Version 2.y multi-master controller	The entire system will behave as a version 2.y multi-master system, as long as only 102 version 1 commands are used	Combination is possible	Combination is possible
Version 1 bus power supply	Combination is possible	Combination is possible	The combination is not guaranteed due to new specified timing or behaviour
Version 2.y bus power supply	Combination is possible	Combination is possible	Combination is possible

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Annex B 20
(informative)

Touch current

The touch current of the interface, as specified in 4.9.4, is current I_1 in Figure B.1 and Figure B.2.

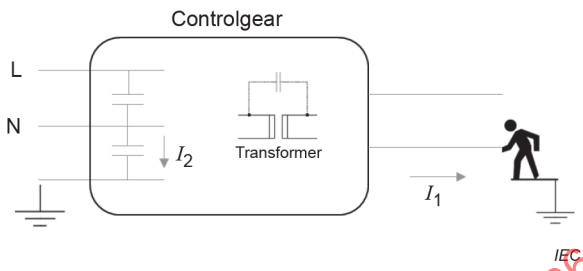

Figure B.1 – Touch current from a bus unit

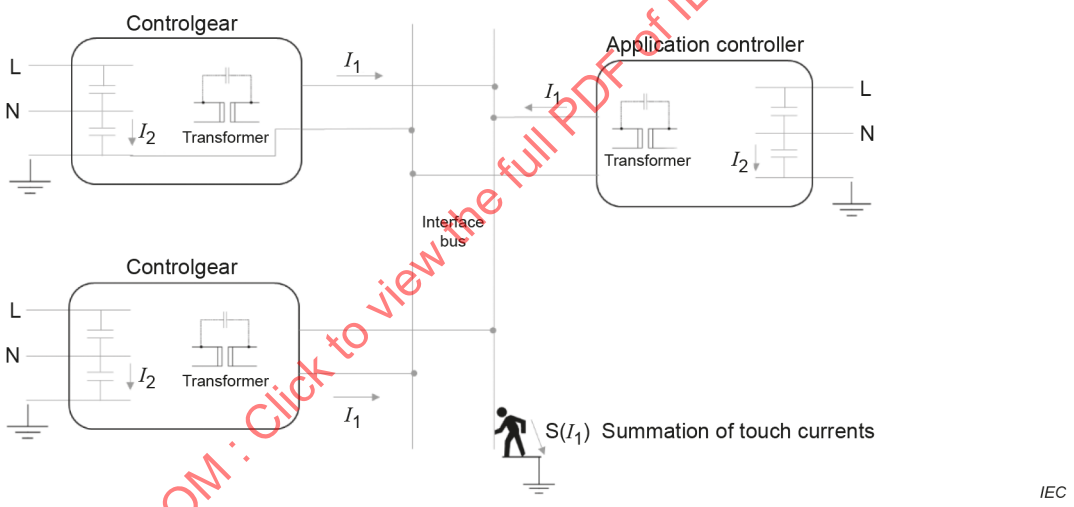

Figure B.2 – Summation of touch currents from several bus units

The summation of touch current is specified in IEC TS 63117.

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IEC 63044 (all parts), *Home and Building Electronic Systems (HBES) and Building Automation and Control Systems (BACS)*

IEC TS 63117, *General requirements for lighting systems – Safety*

ISO/IEC 7498-1, *Information technology – Open Systems Interconnection – Basic Reference Model: The Basic Model*

ISO/IEC 14762, *Information technology – Functional safety requirements for home and building electronic systems (HBES)*

GS1 General Specifications, available at: www.gs1.org

~~EN 50491 (all parts), *General requirements for home and building electronic systems (HBES) and Building Automation and Control Systems (BACS)*~~

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List of comments

1 Figure 1 is updated since the IEC 62386 series was extended by new parts.

2 Other standards give EMC requirements. This standard includes requirements for bus signals and EMC component connections within the bus units, primarily to ensure correct communications between bus units.

3 New references are added to cover further parts of the IEC 62386 series, and to cover extended safety requirements defined in Subclauses 4.9 and 4.10.

4 This definition is often overlooked, but is important, for example, for correct understanding of the IDENTIFY DEVICE command in IEC 62386-102. Query commands not meeting this definition are therefore not instructions.

5 Multi-master application controllers can make use of event message from input devices, which are always multi-masters. Without multi-mastering, application controllers can only rely upon polling (querying) the input devices due to the possibility of event messages causing collisions.

6 This is a clarification.

7 The possibility to transmit or receive 32-bit frames is new with this edition, but the transmission by application controllers of 8-bit backward frames is simply a clarification.

8 32-bit frames are used in IEC 62386-105 (firmware transfer).

9 The requirements given in previous edition 2.0 are unchanged, but extra detail is given for clarity.

10 This clause is added to clarify the possible use of bus-power and external-power to avoid misuse, as some requirements in this document are more relaxed for bus-powered devices. It also allows a case where bus-power and external-power can be used together – a case that was not explicitly allowed or disallowed in previous edition 2.0.

11 Additional requirements are added in Subclauses 4.9 and 4.10 to make a system conformant to the IEC 62386 series safer. These have been retrieved from applicable existing safety standards, but do not remove or change any requirements in the applicable safety standards.

12 Such a capacitor might be used to help with EMC compliance. The requirement here helps to prevent excessive capacitance being effectively connected in parallel across the bus (through earth) and so cause communications problems.

13 This is a clarification of “behaviour”.

14 Such switchable integrated bus power supply is defined in IEC 62386-250.

15 This is a clarification of the test condition.

16 This is a clarification of the shutdown mechanism.

17 32-bit frames are no longer reserved as they are used in IEC 62386-105 (firmware transfer).

18 Renamed as the term “single-master transmitter” is used in several locations in this document.

19 This clause is removed because its content is already stated in Subclause 9.1.5.

20 This Annex is added to help understanding the requirements in Subclause 4.9.4.

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IEC 62386-101

Edition 3.0 2022-11

INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

Digital addressable lighting interface – Part 101: General requirements – System components

Interface d'éclairage adressable numérique – Partie 101: Exigences générales – Composants de système

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IEC 62386-101:2022-11(en-fr)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DIGITAL ADDRESSABLE LIGHTING INTERFACE –

Part 101: General requirements – System components

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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IEC 62386-101 has been prepared by IEC technical committee 34: Lighting. It is an International Standard.

This third edition cancels and replaces the second edition published in 2014 and Amendment 1:2018. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) the scope has been updated;
b) safety and earthing have been updated and extended;
c) references have been updated;
d) the use of bus-power and external-power has been clarified;
e) polarity sensitivity for bus units including a bus power supply has been updated;

f) frame sizes of 32 bits are no longer reserved.

The text of this International Standard is based on the following documents:

Draft	Report on voting
34/947/FDIS	34/988/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

This Part 101 of IEC 62386 is intended to be used in conjunction with:

- Part 102, which contains general requirements for the relevant product type (control gear), and with the appropriate Part 2xx (particular requirements for control gear);
- Part 103, which contains general requirements for the relevant product type (control devices), and the appropriate Part 3xx (particular requirements for control devices);
- Part 104, which contains general requirements for wireless and alternative wired system components;
- Part 105, which contains particular requirements for firmware transfer for control gear and control devices.

A list of all parts in the IEC 62386 series, published under the general title *Digital addressable lighting interface*, can be found on the IEC website

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The "colour inside" logo on the cover page of this document indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

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INTRODUCTION

IEC 62386 contains several parts, referred to as series. The IEC 62386 series specifies a bus system for control by digital signals of electronic lighting equipment. The IEC 62386-1xx series includes the basic specifications. Part 101 contains general requirements for system components, Part 102 extends this information with general requirements for control gear and Part 103 extends it further with general requirements for control devices. Parts 104 and 105 can be applied to control gear or control devices. Part 104 gives requirements for wireless and alternative wired system components. Part 105 describes firmware transfer. Part 150 gives requirements for an auxiliary power supply which can be stand-alone, or built into control gear or control devices.

The IEC 62386-2xx series extends the general requirements for control gear with lamp specific extensions (mainly for backward compatibility with Edition 1 of IEC 62386) and with control gear specific features.

The IEC 62386-3xx series extends the general requirements for control devices with input device specific extensions describing the instance types as well as some common features that can be combined with multiple instance types.

This third edition of IEC 62386-101 is intended to be used in conjunction with IEC 62386-102 and with the various parts that make up the IEC 62386-2xx series for control gear, together with IEC 62386-103 and the various parts that make up the IEC 62386-3xx series of particular requirements for control devices. The division into separately published parts provides for ease of future amendments and revisions. Additional requirements will be added as and when a need for them is recognized.

The setup of the standards is graphically represented in Figure 1 below.

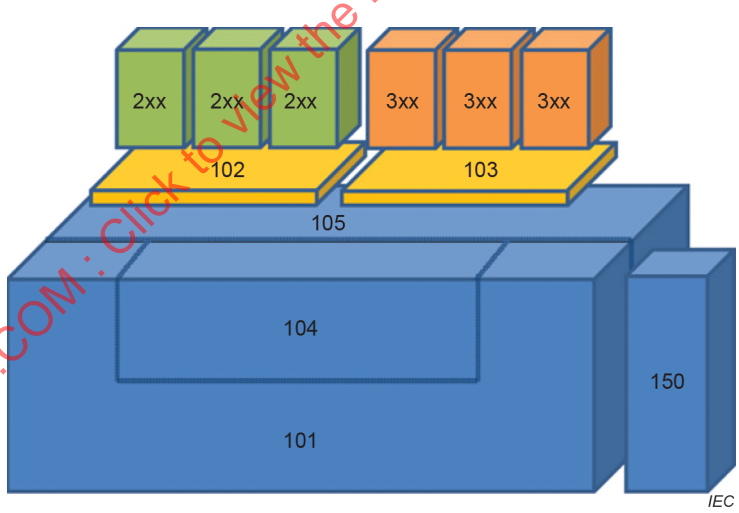

Figure 1 – IEC 62386 graphical overview

When this part of IEC 62386 refers to any of the clauses of the other parts of the IEC 62386-1xx series, the extent to which such a clause is applicable is specified. The other parts also include additional requirements, as necessary.

All numbers used in this document are decimal numbers unless otherwise noted. Hexadecimal numbers are given in the format 0xVV, where VV is the value. Binary numbers are given in the format XXXXXXXXb or in the format XXXX XXXX, where X is 0 or 1, "x" in binary numbers means "don't care".

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DIGITAL ADDRESSABLE LIGHTING INTERFACE –

Part 101: General requirements – System components

1 Scope

This part of IEC 62386 is applicable to system components in a bus system for control by digital signals of electronic lighting equipment.

The control methods, algorithms and data exchange methods of application controllers used for lighting control are not within the scope of the IEC 62386 series. EMC requirements are not within the scope of the IEC 62386 series.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61347-1:2015, *Lamp controlgear – Part 1: General and safety requirements*
IEC 61347-1:2015/AMD1:2017

IEC 62386-102:2022, *Digital addressable lighting interface – Part 102: General requirements – Control gear*

IEC 62386-103:2022, *Digital addressable lighting interface – Part 103: General requirements – Control devices*

IEC 62386-104, *Digital addressable lighting interface – Part 104: General requirements – Wireless and alternative wired system components*

IEC 62386-105, *Digital addressable lighting interface – Part 105: Particular requirements for control gear and control devices – Firmware Transfer*

IEC 62386-2xx (all parts), *Digital addressable lighting interface – Part 2xx: Particular requirements for control gear*

IEC 62386-3xx (all parts), *Digital addressable lighting interface – Part 3xx: Particular requirements for control devices*

IEC 61000-4-11, *Electromagnetic compatibility (EMC) – Part 4-11:Testing and measurement techniques – Voltage dips, short interruptions and voltage variations immunity tests for equipment with input current up to 16 A per phase*

IEC 60664-1, *Insulation coordination for equipment within low-voltage supply systems – Part 1: Principles, requirements and tests*

IEC 60990:2016, *Methods of measurement of touch current and protective conductor current*

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IEC 61643-11, *Low-voltage surge protective devices – Part 11: Surge protective devices connected to low-voltage power systems – Requirements and test methods*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
active state
phase of low level voltage during a transmission

Note 1 to entry: Noise and short pulses may be ignored and therefore do not change the state.

3.2
advanced bus power supply
bus power supply capable of checking the bus for fault conditions before switching on its output continuously

Note 1 to entry: Examples of fault conditions are mains voltage connected to the bus or short circuit of the bus.

3.3
application controller
control device that is connected to the bus and sends commands in order to control input devices and/or control gear connected to the same bus

3.4
backward frame
frame used for backward transmission

3.5
backward transmission
transmission of data as a reply to and triggered by a forward transmission

3.6
bus
two-wire connection line carrying power and frames

3.7
bus powered
drawing the power for operation from the bus

3.8
bus power down
bus power interruption longer than 45 ms

3.9
bus power interruption
abnormal condition where the bus voltage is in the receiver low level voltage range, but not because of a transmitter being active

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3.10
bus power supply
unit feeding defined energy to the bus

3.11
bus unit
logical unit or combination of logical units, containing one transmitter and optionally one receiver

Note 1 to entry: See 4.6.6.

3.12
charge overshoot
product of current overshoot time and current overshoot amplitude

3.13
collision
situation in which two or more transmitters are transmitting simultaneously

Note 1 to entry: Collisions can go unnoticed if the transmission timing is sufficiently similar and the transmitted frame content is identical.

3.14
command
forward transmission with appropriate information content, intended to cause a reaction in the receiver

Note 1 to entry: A receiver, having decoded a command can, when appropriate, decide to ignore the command.

Note 2 to entry: Refer to IEC 62386-102, IEC 62386-103, IEC 62386-104, IEC 62386-105, the IEC 62386-2xx series and IEC 62386-3xx series for command definitions.

3.15
control device
device that is connected to the bus and sends commands to other devices connected to the same bus

Note 1 to entry: Control devices can also receive commands and backward transmissions. Control devices can contain application controllers and/or input devices.

3.16
control gear
device that is connected to the bus and receives commands in order to control at least one output in a direct or indirect way

Note 1 to entry: The lamp controlgear described in IEC 61347-1 can cover control gear.

3.17
current overshoot time
time per bit during which the current supplied by the bus power supply is above the allowed maximum of 250 mA after a transition from idle state to active state

Note 1 to entry: See 6.5.4.

3.18
destroy area
time slot where a valid frame cannot be ensured

3.19
edge
change from active state to idle state or vice versa

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3.20
event message
command sent by a control device in order to distribute information on the bus

3.21
externally powered
drawing the power for operation from a separate power supply

Note 1 to entry: The separate power supply can be mains power, DC power, etc.

3.22
forward frame
frame used for forward transmission

3.23
forward frame priority
property of a forward frame used to prioritize access to the bus

3.24
forward transmission
transmission of data initiated by a control device

Note 1 to entry: See also 3.5.

3.25
frame
set of consecutive bits followed by a stop condition

Note 1 to entry: See Clause 8 for the timing definition of a stop condition.

3.26
grey area
time slot containing the decision point separating adjacent time slots

Note 1 to entry: A grey area indicates that the decision is arbitrary. Typically the previous or next entry in a table should be used as an action. See Clause 8 for further information.

3.27
idle state
phase of high level voltage between and during transmissions

Note 1 to entry: Noise and short pulses may be ignored and therefore do not change the state.

3.28
input device
control device that is connected to the bus and sends commands using a multi-master transmitter in order to distribute information about user actions and/or sensor values

Note 1 to entry: Input devices do not transmit commands to the control gear.

3.29
instance
signal processing unit of an input device

3.30
instruction
command transmitted to change one or more variables in a bus unit

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3.31
integrated bus power supply
bus power supply integrated into a physical device also containing a bus unit

3.32
interface
terminals or wires for connection to the bus

3.33
logical unit
control gear or control device that conforms to IEC 62386-102 or IEC 62386-103

Note 1 to entry: See 4.6.6.

3.34
multi-master application controller
application controller that is capable of sharing the bus with other control devices and uses a multi-master transmitter

3.35
multi-master transmitter
transmitter that follows the multi-master timing and supports collision detection, collision avoidance, and collision recovery methods

Note 1 to entry: Multi-master transmitters are used in control devices intended for multi-master control systems.

3.36
proprietary forward frame
forward frame for manufacturer-specific purposes

3.37
query
command transmitted to observe a variable in a bus unit

Note 1 to entry: A query can be followed by a backward frame.

3.38
receiver
part of a bus unit detecting and decoding frames on the bus

3.39
reserved
intended for future use

3.40
send-twice command
command transmitted by send-twice forward frames

Note 1 to entry: Refer to 9.4, IEC 62386-102, IEC 62386-103, the IEC 62386-2xx series and IEC 62386-3xx series for further details on send-twice commands.

3.41
send-twice forward frame
forward frame that needs to be transmitted twice with a limited settling time in order to be processed by the receiver

3.42
settling time
time during which the bus is in idle state after the last rising edge of one frame and before the first falling edge of the next frame

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3.43
single-master application controller
application controller that is not required to use a multi-master transmitter

Note 1 to entry: The implication is that no other application controllers, and no other input devices with event messages enabled, may be connected to the bus.

3.44
standard forward frame
forward frame as defined and described in the IEC 62386 series

3.45
system failure
bus power interruption longer than 550 ms

3.46
transaction
uninterruptible set of one or more consecutive forward frames transmitted from a single control device, with zero or more backward frames

3.47
transmitter
part of a bus unit placing frames on the bus

3.48
voltage overshoot time
time per bit during which the voltage supplied by the bus power supply is above 20,5 V after a transition from active state to idle state

Note 1 to entry: See 6.5.4.

3.49
voltage undershoot time
time per bit during which the voltage supplied by the bus power supply is below 12,0 V after a transition from active state to idle state

Note 1 to entry: See 6.5.4.

3.50
frame accepted
frame that has been received and uses the correct frame type and data bit content

3.51
frame ignored
frame received but not accepted

3.52
frame received
frame with a valid start bit, valid data bits, and a stop condition

3.53
frame rejected
frame not received

3.54
FELV
functional extra-low voltage
ELV in a circuit provided for functional purposes and not fulfilling the requirements for SELV (or PELV)

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Note 1 to entry: FELV has basic insulation from LV.

Note 2 to entry: An FELV circuit is not safe to touch.

[SOURCE: IEC 60598-1:2020, 1.2.42.1, modified – The notes have been added.]

4 General

4.1 Purpose

The standardization of the digital addressable lighting interface is intended to achieve interoperable multi-vendor operation below the level of building management systems.

Annex A gives further information for systems.

NOTE The IEC 63044 series and ISO/IEC 14762 are not applicable for the purposes of this IEC 62386 series. The IEC 63044 series can be applicable to application controllers if intended to be used as HBES/BACS.

4.2 Version number

The version shall be in the format "x.y", where the major version number x is in the range of 0 to 62 and the minor version number y is in the range of 0 to 2. When the version number is encoded into a byte, the major version number x shall be placed in bits 7 to 2 and the minor version number y shall be placed in bits 1 to 0.

At each amendment to an edition of IEC 62386-101 the minor version number shall be incremented by one.

At a new edition of IEC 62386-101 the major version number shall be incremented by one and the minor version number shall be set to 0.

The current version number is "3.0".

NOTE IEC documents are generally subject to two amendments before a new edition is prepared.

4.3 System structure and architecture

A system shall consist of the components listed in Table 1.

Table 1 – System components

Component	Quantity	For detailed information see
Bus power supply	≥ 1	Clause 6
Control gear	≥ 0	IEC 62386-102
Application controller	≥ 1	IEC 62386-103
Input devices	≥ 0	IEC 62386-103
Bus	1	Subclause 4.8 and Clause A.2

In a system all bus units as well as the bus power supplies are connected in parallel to the bus.

NOTE As a consequence of this, every frame is visible to all power supplies, control gear, and control devices on the bus.

Figure 2 shows a system structure example.

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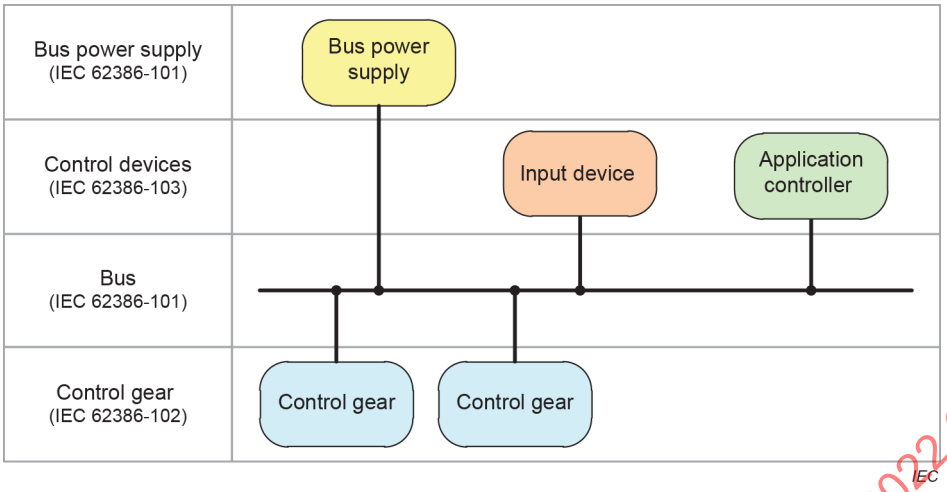

Figure 2 – System structure example

See 4.8 for detailed information on the wiring and Clause A.2 for information on possible system architectures.

4.4 System information flow

Figure 3 shows the different frame types that are used for communication between the bus units in a system. A backward frame is only ever transmitted in response to a forward frame.

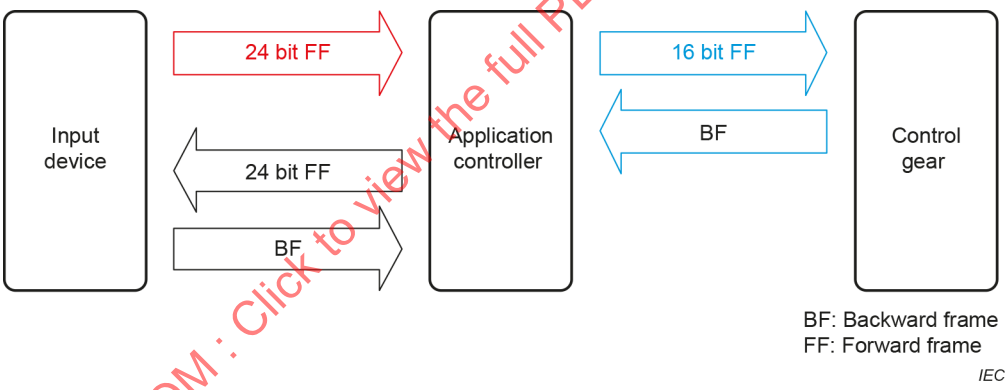

Figure 3 – Communication between bus units (example)

A direct information flow from an input device to control gear is not allowed. In addition to communications shown in Figure 3, for firmware transfer (IEC 62386-105), application controllers can transmit 32-bit forward frames and all three of the bus units shown can receive 32-bit forward frames. Multi-master application controllers can also be transmitters of 8-bit backward frames.

NOTE An example of a system conforming to this document can consist of an application controller and control gear only, see A.2.4. In such a system, user input does not result in 24-bit forward frames on the bus.

4.5 Command types

Bus units conforming to this document shall use the following different types of commands for communication:

- event messages,
- instructions, and
- queries.

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NOTE Refer to the other parts of the IEC 62386 series for further details on event messages, instructions and queries.

4.6 Bus units

4.6.1 Transmitters and receivers in bus units

Table 2 gives a short summary of the different receivers and transmitters allowed for each bus unit. It is not allowed for a bus unit to transmit or receive other frames than the ones indicated in Table 2, except proprietary forward frames. See 7.4 for details of the different frame types.

Table 2 – Transmitters and receivers in bus units

Bus unit	Receiver of	Transmitter of	
Control gear	32-bit forward frames	Backward frames, following the single-master timing requirements[a]	
	16-bit forward frames		
Input device	32-bit forward frames	24-bit forward frames	Following the multi-master timing requirements
	24-bit forward frames	Backward frames[a]	
Multi-master application controller	32-bit forward frames	32-bit forward frames	
	24-bit forward frames	24-bit forward frames	
	16-bit forward frames[b]	16-bit forward frames	
	Backward frames	Backward frames[a]	
Single-master application controller	Backward frames[c]	16-bit forward frames, following the single-master timing requirements[d]	

[a] No collision detection or collision avoidance methods shall be applied to backward frame transmissions.

[b] Only applicable when the multi-master application controller is able to process 16-bit forward frames transmitted by other application controllers.

[c] Only required if the single-master application controller uses addressing or queries.

[d] A single-master application controller can also send 24-bit frames if polling input devices, and 32-bit forward frames.

4.6.2 Control gear

A control gear shall be conformant to this document and to IEC 62386-102 and the applicable parts of the IEC 62386-2xx series.

It shall contain a receiver for 16-bit forward frames and a transmitter for transmitting backward frames. The backward frame transmitter shall conform to the timing requirements for a single-master transmitter defined in 8.1 and shall not implement collision detection or recovery. It can contain a receiver for 32-bit forward frames.

4.6.3 Input device

An input device shall be conformant to this document and to IEC 62386-103 and the applicable parts of the IEC 62386-3xx series.

It shall contain a multi-master transmitter following the multi-master transmitter timing requirements defined in 8.3 to transmit 24-bit forward frames. It shall also contain a transmitter to transmit backward frames. The backward frame transmitter shall conform to the timing requirements for a multi-master transmitter and shall not implement collision detection or recovery.

NOTE Although they are logically distinct objects, the multi-master transmitter and the backward frame transmitter can share the same hardware.

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An input device shall contain a receiver to receive 24-bit forward frames transmitted by other control devices. It can contain a receiver for 32-bit forward frames.

4.6.4 Single-master application controller

A single-master application controller shall be conformant to this document and to IEC 62386-103.

It shall contain a transmitter following the transmitter timing requirements defined in 8.1 to transmit forward frames.

NOTE Typically, however, a single-master application controller also contains a receiver to receive backward frames transmitted by control gear.

A single-master application controller shall use the commands defined in IEC 62386-102 and, if applicable, the relevant parts of the IEC 62386-2xx series to communicate with the control gear.

4.6.5 Multi-master application controller

A multi-master application controller shall be conformant to this document and to IEC 62386-103.

It shall contain a multi-master transmitter following the multi-master transmitter timing requirements defined in 8.3 to transmit forward frames. It shall also contain a transmitter to transmit backward frames. The backward frame transmitter shall conform to the timing requirements for a multi-master transmitter and shall not implement collision detection or recovery. It shall contain a receiver to receive backward frames as well as forward frames transmitted by other control devices. It can contain a receiver for 32-bit forward frames. It shall not transmit backward frames in response to 16-bit forward frames.

A multi-master application controller shall use the commands defined in IEC 62386-102 and, if applicable, the relevant parts of the IEC 62386-2xx series to communicate with the control gear. It shall use the commands defined in IEC 62386-103 and, if applicable, the relevant parts of the IEC 62386-3xx series to communicate with control devices. If applicable, a multi-master application controller shall use the commands defined in IEC 62386-105 to achieve firmware transfer to control gear and control devices.

NOTE A multi-master application controller can also receive and process 16-bit forward frames transmitted by other application controllers and/or react to queries.

4.6.6 Sharing an interface

More than one logical unit may share one physical interface. Figure 4 shows an example where *n* logical units and a bus power supply share the physical interface.

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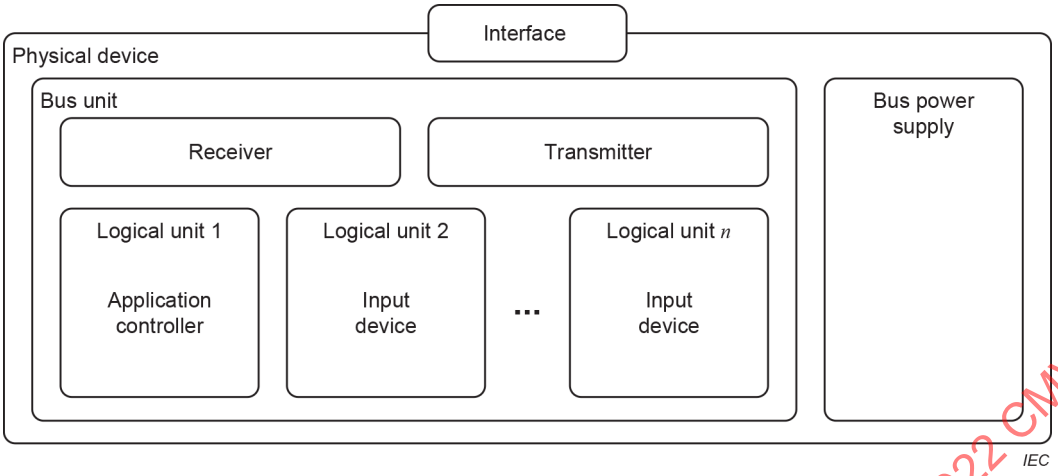

Figure 4 – Example of a shared interface

An application controller may be built into a bus unit which also contains an input device, with both the application controller and the input device sharing the same physical interface. A bus unit of that kind shall support a command to deactivate the application controller, thus enabling the bus unit to be used in the same way as if it contained only the input device.

4.6.7 Power for operation

Bus units shall be solely bus powered or solely externally powered, or meet one of the following two cases:

- The bus unit is configurable between bus powered and externally powered, where the configuration shall not be automatic based upon the presence or absence of the supply, and the bus unit meets the following conditions:
  - connection or removal of the external supply or bus power supply shall not cause operation to change between bus powered and externally powered, and
  - it meets the requirements for bus powered bus units when configured as bus powered, and meets the requirements for externally powered bus units when configured as externally powered, and
  - changing the configured power source does not change any functionality that is described in any part of the IEC 62386 series, except due to requirements that differ between bus powered and externally powered bus units.
- The bus unit is bus powered, uses an external supply only for behaviour not specified in any part of the IEC 62386 series, and meets the requirements in the implemented parts of the IEC 62386 series with the external supply disconnected.

NOTE 1 An example of a bus unit that is configurable between bus powered and externally powered is a sensor which can draw a relatively high current when bus powered, limiting the number of such devices that can be connected to the bus, or can be configured to be externally powered and so allow more devices on the bus.

NOTE 2 An example of a bus unit that is bus powered, but uses an external supply only for behaviour not specified in any part of the IEC 62386 series, is a bus powered push-button panel with a backlight, where the backlight operates only when an external supply is connected.

NOTE 3 An example of a bus unit that does not meet these requirements is bus powered LED control gear, requiring a second device to provide power for the LEDs, where the second device is externally powered. Another example is a bus powered pulse width modulation (PWM) dimmer which requires an external 24 V DC supply to drive its output – the dimmer can instead be externally powered from the 24 V DC supply.

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4.7 Bus power supply and load calculations

4.7.1 Current demand coverage

In one system the sum of all bus units' current consumption when not transmitting (see 5.5, Table 10) shall not exceed the sum of all bus supplies' guaranteed supply current (see 6.5.1, Table 13). See also Clause A.5.

Additional current is needed during transmission to drive dynamic processes such as charging capacitances within the system.

$$\sum I_{\text{Bus Unit}} + I_{\text{Dynamic Processes}} \leq \sum I_{\text{Power Supply Guaranteed}}$$

There is no universally valid equation for calculating the current needed for dynamic processes since this current depends on the system wiring and system structure.

4.7.2 Maximum signal current compliance

The sum of all bus power supplies' maximum supply current connected to the bus shall never exceed 250 mA.

$$\sum I_{\text{Power Supply Guaranteed}} \leq \sum I_{\text{Power Supply Maximum}} \leq 250\ \text{mA}$$

4.7.3 Simplified system calculation

For a system consisting of just one bus power supply, bus powered bus units, and n externally powered bus units, for example control gear, the following simplification is recommended:

$$2\ \text{mA} \times n_{\text{Externally Powered Bus Units}} + \sum I_{\text{Bus Powered Bus Units}} \leq \frac{I_{\text{Power Supply Guaranteed}}}{1{,}2}$$

The factor 1,2 is an approximation that takes an additional current of 20 % needed for dynamic processes into account.

4.8 Wiring

4.8.1 Wiring structure

The bus wiring should be connected in a star topology, a linear topology or a mixture of both. The wiring shall not be done in a ring structure. The two leads which serve as the bus shall be located in the same cable or cable conduit. In the cable or cable conduit the two leads shall be next to each other in order to prevent unintended coupling to other signals.

NOTE Depending on local installation directives and insulation requirements the two wires can be located in the same cable as the mains power supply leads.

4.8.2 Wiring specification

Apart from transient effects during transmission, at all times during the operation of the system, the voltage across the interface of any device shall not differ by more than 2,0 V from the voltage across the interface of each and every other device connected to the bus. See also Clause A.1 for further details.

NOTE 1 The voltage drop depends on the sum of the supply currents of all power supplies, the specific resistance of the leads and the wiring length.

NOTE 2 This requirement can limit the total wiring length in the system.

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4.9 Electrical safety requirements

4.9.1 General

This Subclause 4.9 describes the additional safety requirements for the implementation of digital addressable lighting interface, in addition to the product safety requirements given in the relevant product safety standard.

4.9.2 Insulation

The bus wiring and the interface shall be considered a FELV circuit or network.

NOTE 1 This means that systems other than FELV are not covered by this document.

The interface shall have at least basic insulation as required for at least 230 V AC mains, or the product working voltage, whichever is higher, according to IEC 60664-1.

NOTE 2 This voltage level is applicable to e.g. the basic insulation between the interface circuit and mains or the supplementary insulation between the bus wiring and touchable conductive parts of the user interface.

If the working voltage exceeds 230 V AC (RMS), and this working voltage can be applied on the interface in the case of a single fault condition, then there shall be a warning included in the manual, also recommended to be marked on the product, indicating that the working voltage is higher than 230 V AC (RMS).

NOTE 3 Working voltage is defined in IEV 581-21-19. This is not usually the mains voltage.

The insulation between the mains and the interface shall be designed for the applicable overvoltage category (OVC), as defined in IEC 60664-1, and shall not be less than OVC II.

NOTE 4 If bus wiring is likely, when installed, to be subjected to impulse voltages that exceed OVC II, then additional measures to be provided to the bus can be considered, for example impulse voltage protection or use of products designed for higher OVC. This can be related to bus wiring being partly outdoors.

4.9.3 Electric strength

The requirements of IEC 61347-1:2015, Clause 12 apply, replacing the term "lamp controlgear" with the term "bus unit".

The value used for working voltage shall be at least 230 V AC, or the product working voltage, whichever is higher.

The over voltage protective device (SPD) shall be disconnected if it complies with IEC 61643-11, when conducting the insulation and electric strength test.

4.9.4 Limitation of the touch current from the device to the bus

The touch current shall be limited to 0,5 mA RMS.

The touch current shall be measured with the measuring network described in IEC 60990:2016, Figure 4.

The value of the touch current shall be made available in the product documentation by the manufacturer of the product.

Annex B gives further information on touch current.

NOTE The use of the term "touch current" does not indicate that the interface is accessible to touch.

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4.10 Earthing of the bus

The interface terminals shall not be connected to earth, except in the following situations:

- a device containing a bus power supply having a maximum supply current of 250 mA, where the negative interface terminal is permitted to be connected to earth;
- through a capacitor connected to earth as described in 5.3 or 6.3.

NOTE Unexpected currents, caused by multiple connections of the circuit to protective earth, could cause fire in the bus wiring. Earthing could also break the safety requirements for certain luminaires.

4.11 Power interruptions at bus units

4.11.1 Different levels of power interruptions

Table 3 and Table 4 show the different levels of power interruptions at bus units.

Table 3 – Power-interruption timing of external power

Minimum	Typical	Maximum	Description
		200 ms	Short interruptions of external power supply[a]
> 200 ms		< 5 s	Grey area
5 s			External power cycle[b]
[a] See 4.11.2. [b] See 4.11.3.			

Table 4 – Power-interruption timing of bus power

Minimum	Typical	Maximum	Description
		40 ms	Short interruptions of bus power supply[a]
> 40 ms		< 45 ms	Grey area
45 ms			Bus power down[b]
> 450 ms		< 550 ms	Grey area for system failure
550 ms			System failure[b]
[a] See 4.11.4. [b] See 4.11.5.			

4.11.2 Short power interruptions of external power supply

The requirements of 4.11 are applicable for bus units in steady state without communication on the bus.

NOTE 1 Steady state implies for example that the device has finished its power-up and is ready for the intended operation without any changes of the output in progress.

Functional tests for short power interruptions shall be done with test methods and test equipment according to IEC 61000-4-11 at the minimum specified power supply voltage, with test voltage levels given in Table 5. For AC supply the voltage shift shall occur at zero crossing.

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Table 5 – Short power interruptions

	Test levels
Test voltage level 1	70 %
Test voltage level 2	0 %
Number of periods with AC supply	10
Interruption time with DC supply	200 ms

During the power supply interruption, a change of the state may occur. After the power supply interruption, the bus unit shall be in, or shall re-establish within 30 min, the same state as before the interruption.

NOTE 2 The 30 min time limit is chosen to allow for the long re-ignition time of certain lamp types.

4.11.3 External power cycle

After an external power cycle (see Table 3), an externally powered bus unit shall apply power-on behaviour to all logical units simultaneously. During an external power cycle, a bus unit can possibly still respond to commands.

NOTE The power-on behaviour is defined in IEC 62386-102 and IEC 62386-103.

4.11.4 Short interruptions of bus power supply

Bus units shall not interpret short bus power interruptions of up to 40 ms as power down.

NOTE This implies that short bus power interruptions will not trigger power-on behaviour.

Tests for the short interruption of the bus power supply shall be done at the minimum bus power supply voltage.

4.11.5 Bus power down

A bus powered bus unit may interpret bus power down as an external power cycle (see 4.11.1). It shall interpret system failure as an external power cycle. The external power cycle and corresponding power-on behaviour shall apply to all logical units simultaneously. See Table 4.

NOTE The power-on behaviour is defined in IEC 62386-102 and IEC 62386-103.

4.11.6 System start-up timing

After external power-on, a bus power supply shall be able to supply the guaranteed supply current given in Table 13 after the bus power supply start-up time specified in Table 6 at the latest.

A receiver shall be ready to receive frames within the maximum receiver start-up time specified in Table 6.

A transmitter or a multi-master transmitter shall not start transmissions earlier than the transmitter start-up time specified in Table 6.

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Table 6 – Start-up timing

	Minimum	Typical	Maximum	Condition
Bus power supply start-up time			250 ms	Guaranteed supply current reached
Advanced bus power supply start-up time			400 ms	
Integrated bus power supply start-up time			400 ms [a]	
			5 s [b]	
Receiver start-up time for externally powered bus units, after external power cycle			450 ms [e]	
Receiver start-up time for externally powered bus units, after bus power down			100 ms	U = 10 V [d]
Receiver start-up time after bus power down for bus powered bus units			1 200 ms	
Transmitter start-up time	110 ms [c]			
Multi-master transmitter start-up time	110 ms			

[a] Applicable if other bus power supplies are allowed in the system.

[b] Applicable if no other bus power supplies are allowed in the system.

[c] Not applicable for transmitters of bus units which cannot determine the bus state.

[d] Idle state, bus voltage measured at the interface of the bus unit.

[e] If an external power cycle occurred and the bus power is not available within 350 ms, the 100 ms timing is applicable.

Figure 5 shows an example of the system start-up timing.

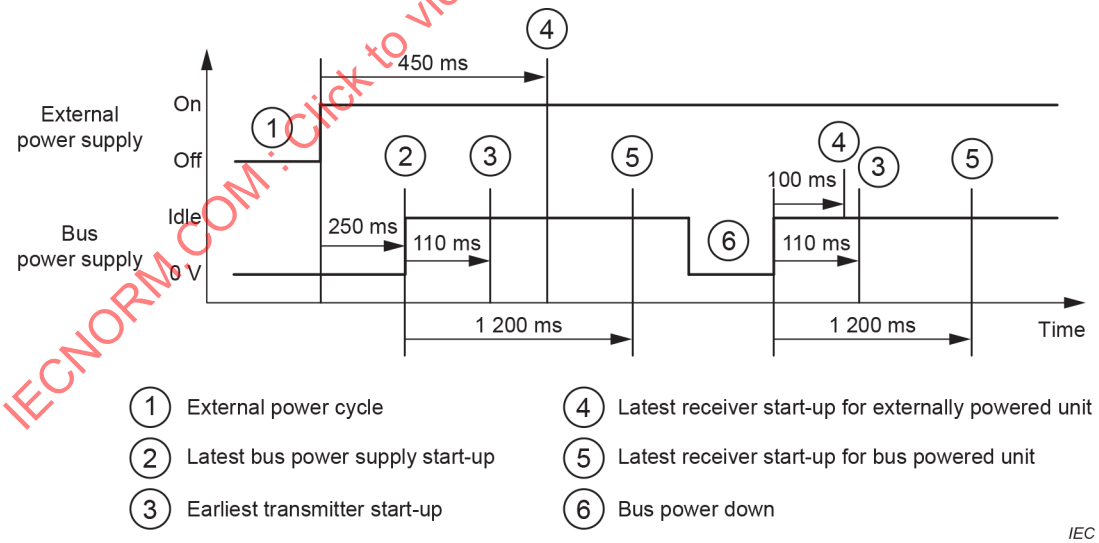

Figure 5 – Start-up timing example

NOTE It follows from the provisions of 4.11.6 that a transmitter could be transmitting before all receivers are ready to receive.

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5 Electrical specification

5.1 General

All voltages and currents refer to the interface of the bus unit.

The control interface shall be polarity insensitive, except when a bus power supply is integrated. If the integrated bus power supply is switchable, polarity sensitivity is permitted for both states of the bus power supply (enabled and disabled).

Overvoltage protection is optional, but recommended for the highest rated voltage of the system. If overvoltage protection is not included, it is recommended that the design ensures safe operation in case mains voltage is applied to the interface.

5.2 Marking of the interface

The interface shall be marked with "da" or "DA" (for data) on the bus unit. If colour coding is used, the colours representing the "da" or "DA" shall be given on the bus unit.

If there is more than one interface, additional marking shall be used to enable the interfaces to be distinguished from one another.

5.3 Capacitors between the interface and earth

If capacitors are connected between the interface circuit and any other part of the device, such as earth, these shall be connected from the negative side of the rectified interface signal. Such capacitors shall fulfil the insulation requirements given in 4.9.

NOTE The capacitance seen on the bus is affected by the capacitance to earth where a capacitor connected between the negative side of the interface and earth on one bus unit is used with another bus unit containing a capacitor connected between the positive side of the interface and earth.

5.4 Signal voltage rating

The voltage levels in the system during normal operation shall always be in the range of the nominal system voltage given in Table 7. All bus units as well as the bus power supplies shall withstand the absolute maximum system voltage given in Table 7. Testing shall be done with a current of 260 mA for a duration of 1 s.

NOTE 1 Voltages outside the nominal system voltage range could occur, as a result of ringing on the bus, for example.

Devices need to be polarity insensitive (see 5.1) or power supplies need to be able to withstand reverse voltages (see 9.7).

Table 7 – System voltage levels

	Minimum	Typical	Maximum
Nominal system voltage U	0 V		20,5 V
Absolute maximum system voltage	0 V		22,5 V

The voltage levels at the receiver interface shall be interpreted according to Table 8.

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Table 8 – Receiver voltage levels

	Minimum	Typical	Maximum
High level voltage	9,5 V		22,5 V
Threshold voltage	> 6,5 V	8,0 V	< 9,5 V
Low level voltage	0 V		6,5 V

The voltage levels of a transmitter shall be as shown in Table 9.

Table 9 – Transmitter voltage levels

	Minimum	Typical	Maximum
Low level voltage	0 V		4,5 V
High level voltage[a]	10,0 V [b]		22,5 V

[a] The high level voltage is not under control of a transmitter, but is determined by the power supply and its location on the bus.

[b] 10 V is derived from the minimum power supply voltage of 12 V minus the maximum voltage drop of 2 V on the bus.

5.5 Signal current rating

The relation between the current I_{BUS} and the voltage U at the interface of the bus unit shall be as shown in Table 10.

Table 10 – Current rating

	Minimum	Typical	Maximum	Condition
Externally powered bus unit current consumption I_{BUS} when not transmitting			2,0 mA	0 V ≤ U ≤ 22,5 V
Bus powered bus unit current consumption I_{BUS} when not transmitting			250 mA [a]	
Current consumption I_{BUS} when not transmitting	10 µA [b]			U_{TH} ≤ U ≤ 22,5 V [c]
Transmitter sink current	250 mA			U ≤ 4,5 V [d]

[a] This is the theoretical maximum current. In reality a device should consume less current. See 4.7, 5.6 and the last paragraph of this subclause 5.5.

[b] The minimum current consumption is necessary for discharging the wiring capacitances and input capacitances of the bus units connected.

[c] U_{TH} is the threshold voltage of the receiver.

[d] This is the required resulting voltage when sinking the maximum current.

Bus units shall not draw more than their specified maximum current, not even during power up or power down. For bus powered units the actual value to use for testing is the documented maximum current consumption.

5.6 Marking of bus powered bus unit

If a bus unit is bus powered, the maximum current consumption in mA shall be shown in the literature. It is also recommended that this should be shown on the label.

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The start-up time of a bus powered bus unit shall be shown in the literature and optionally on the label.

The maximum current shall take tolerances and temperature drift into account.

5.7 Signal rise time and fall time

The rise time t_{RISE} and fall time t_{FALL} of the signal shall fulfil the requirements given in Table 11. Figure 6 and Figure 7 illustrate the levels used for measuring t_{RISE} and t_{FALL}.

Table 11 – Signal rise and fall times

	Minimum	Typical	Maximum	Condition
t_{RISE}, t_{FALL} for transmitter and multi-master transmitter	3 µs [a]			Measured between 10 % and 90 % of the signal voltage swing. Test shall be done at a bus voltage U_{BUS} of 20,5 V at 250 mA unless there is an integrated bus power supply with I_{max} = 250 mA, in which case no additional bus power supply shall be used.
t_{RISE}, t_{FALL} for transmitter			25 µs	Measured between: 4,5 V and 11,5 V at U_{BUS} ≥ 12 V bus voltage 4,5 V and (U_{BUS} – 0,5 V) at 10 V ≤ U_{BUS} < 12 V
t_{RISE}, t_{FALL} for multi-master transmitter			15 µs	
[a] The system resonance frequency depends on the system components including the wiring. Therefore there is no minimum value that ensures the absence of ringing in all cases. The minimum t_{RISE} and t_{FALL} should be considered to avoid EMI problems.				

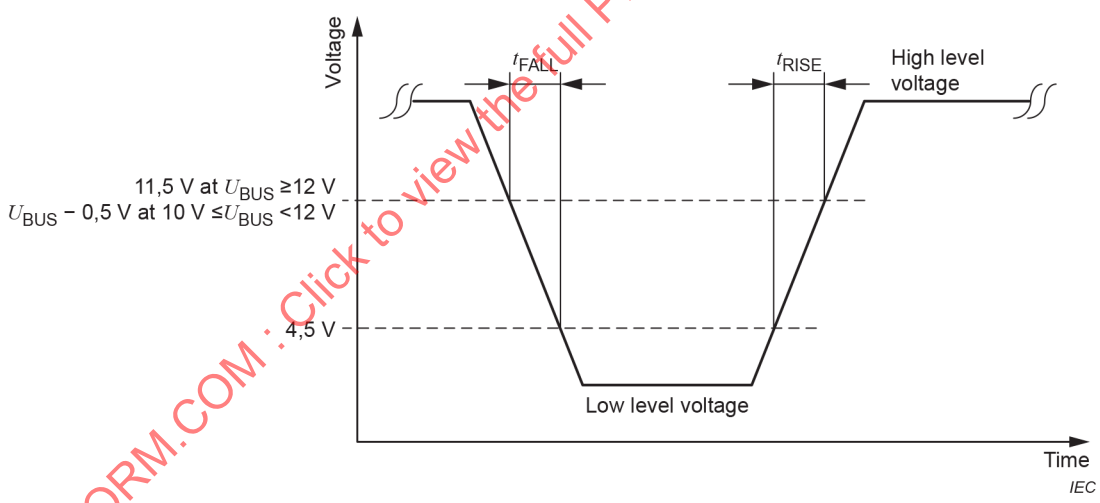

Figure 6 – Maximum signal rise and fall time measurements

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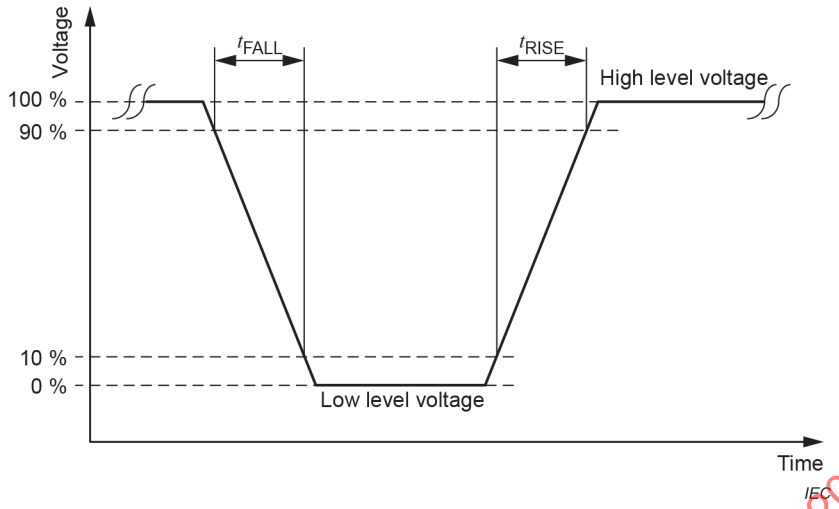

Figure 7 – Minimum signal rise and fall time measurements

NOTE It follows that any control gear or control device causing a change of logic level on the bus by means of changing its own impedance, will change its impedance at a rate such that the timing requirements of Table 11 are met.

6 Bus power supply

6.1 General

A bus power supply can be a stand-alone bus power supply unit or it can be integrated with any bus unit into one physical device.

All voltages and currents refer to the interface of the bus power supply unit, whether integrated or not.

Apart from transient instances of discharging the capacitance of the bus and of any electrically passive components connected to the bus, a bus power supply shall, for bus voltages in the range of 0 V to 22,5 V, never draw a current of more than 1 mA from the bus, even if its own external power supply has failed. This requirement is inapplicable to power supplies with a maximum current rating of 250 mA.

6.2 Marking of the bus power supply terminals

In addition to the marking requirements defined in 5.2, the bus power supply terminals shall be marked with "+" and "–" to indicate the polarity. If colour coding is used, the colours representing the "+" and "–" shall be given on the bus power supply.

6.3 Capacitors between the interface and earth

If capacitors are connected from the interface circuit to any other part of the device, such as earth, these shall be connected from the negative side of the interface signal. Such capacitors shall fulfil the insulation requirements given in 4.9.

NOTE The capacitance seen on the bus is affected by the capacitance to earth where a capacitor connected between the negative side of the interface and earth on one bus unit is used with another bus unit containing a capacitor connected between the positive side of the interface and earth.

6.4 Voltage rating

The bus power supply shall withstand the voltages shown in Table 7. The bus power supply output voltage shall be as shown in Table 12.

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Table 12 – Bus power supply output voltage

	Minimum	Typical	Maximum	Condition
Output voltage	12,0 V	16,0 V	20,5 V	Full supply voltage range, full load range, full temperature range, idle state

6.5 Current rating

6.5.1 General current rating

The current that the bus power supply is capable of providing to the bus shall be as shown in Table 13.

Both the maximum supply current and the guaranteed supply current shall be stated in the literature. It is also recommended that these should be shown on the label. The guaranteed supply current shall be an absolute minimum and the maximum supply current shall be an absolute maximum.

NOTE 1 Owing to internal power consumption the guaranteed supply current can be less than the maximum supply current when the bus power supply unit is integrated into a bus unit.

NOTE 2 Typically the maximum supply current is maximum at the minimum allowed temperature for the bus power supply, while the guaranteed supply current is minimum at the maximum allowed temperature of the bus power supply.

NOTE 3 The bus power supply current and the transmitter sink current influence signal timing due to the wiring capacitance.

Table 13 – Bus power supply current rating

	Minimum	Typical	Maximum	Condition
Maximum supply current	Guaranteed supply current		250 mA	Full voltage range, full temperature range
Guaranteed supply current[a]	8,0 mA		Maximum supply current	U = 12,0 V, full temperature range
[a] See also 4.6.7.				

6.5.2 Single bus power supply current rating

A bus power supply that is designed to be the only one in the system shall be marked with a maximum supply current of 250 mA. Such a power supply should be able to withstand any ringing on the bus; no test is provided.

NOTE The guaranteed supply current can be substantially lower than the maximum supply current.

6.5.3 Integrated bus power supply current rating

If a power supply is integrated into a bus unit and this bus power supply is the only allowed bus power supply in the system, the minimum transmitter sink current of this bus unit may be reduced to the maximum supply current of the bus power supply.

6.5.4 Dynamic behaviour of the bus power supply

The bus power supply behaviour in case of transitions from open to short circuit shall be as shown in Table 14 and Figure 8.

The bus power supply behaviour in case of transitions from short to open circuit shall be as shown in Table 14 and Figure 9.

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Table 14 – Bus power supply dynamic behaviour

	Minimum	Typical	Maximum	Condition
Voltage undershoot amplitude			0,5 V	Transition from short to open circuit
Voltage undershoot time			100 µs	
Voltage overshoot amplitude			2,0 V	
Voltage overshoot time			100 µs	
Voltage rise time			10 µs	Measured from 0 V to 12 V
Current overshoot amplitude			200 mA	2,5 V/µs transition from open to short circuit
Current overshoot time			10 µs	
Charge overshoot			1 µAs	

If there is more than one overshoot/undershoot, the highest amplitude shall be taken as overshoot/undershoot amplitude. The sum of all overshoot/undershoot times shall be used as overshoot/undershoot time.

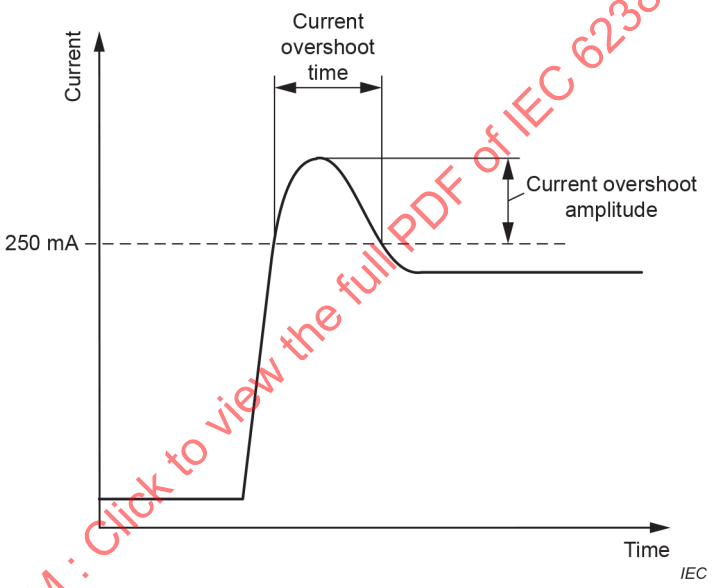

Figure 8 – Bus power supply current behaviour

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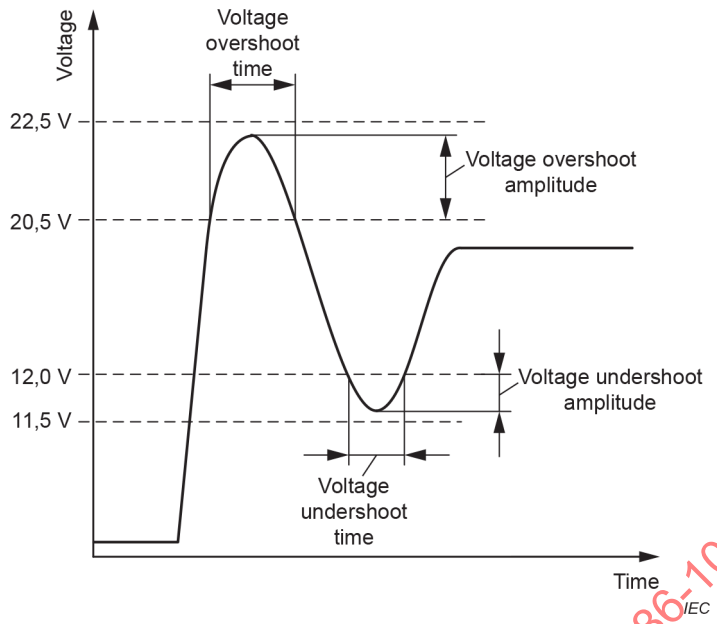

Figure 9 – Bus power supply voltage behaviour

6.6 Bus power supply timing requirements

6.6.1 Short power supply interruptions

The requirements of 4.11.1 and 4.11.2 apply with the following addition:

The bus power supply shall not interrupt the bus power for 450 ms or longer.

This requirement means that short power supply interruptions do not cause system failure. However any interruption of the bus power longer than 40 ms can have an effect on bus powered devices. Therefore it is recommended that the bus power interruption should not exceed 40 ms.

6.6.2 Short circuit behaviour

On detection of a short circuit which exists for longer than the minimum shutdown delay time given in Table 15, the bus power supply may shut down for a period up to the maximum restart period given in Table 15. On each restart the power supply shall turn on the output for at least the minimum retry time given in Table 15.

NOTE A system failure condition cannot be caused solely by the behaviour of a power supply conforming to these requirements.

Table 15 – Short circuit timing behaviour

	Minimum	Typical	Maximum
Shutdown delay time	600 ms		
Retry time	150 ms [a]		
Restart period			15 s
[a] A minimum retry time of 600 ms is recommended.			

In a system, there should not be more than one power supply with the shutdown mechanism. This is to prevent the possibility of two or more power supplies entering shutdown, followed by them retrying at different times, with neither able to return to normal operation due to insufficient supply current to restore a loaded bus, and so remaining in the shutdown state.

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If a bus power supply uses the shutdown mechanism, this shall be stated in the literature. It is also recommended that the information about this shutdown mechanism be shown on the label.

Bus power supplies without the shutdown mechanism shall be short circuit proof, such that after removal of the short circuit, the bus voltage shall recover with the voltage rise time given in Table 14.

7 Transmission protocol structure

7.1 General

This Clause 7 describes the encoding of forward frames and of backward frames. Figure 10 shows an example of a frame. The most significant bit shall always be transmitted first, immediately after the start bit. The least significant bit shall always be transmitted last, immediately before the stop condition. The bit numbering shall always be zero-based. Thus the most significant bit of an n-bit frame shall be bit n-1.

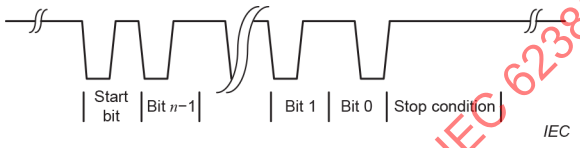

Figure 10 – Frame example

7.2 Bit encoding

7.2.1 Start bit and data bit encoding

The start bit as well as the data bits shall be bi-phase encoded. A logical 1 shall contain a rising edge inside the encoded bit; a logical 0 shall contain a falling edge inside the encoded bit, as shown in Figure 11.

Figure 11 – Bi-phase encoded bits

A start bit shall be encoded as logical 1.

7.2.2 Stop condition encoding

The stop condition shall be encoded as idle state. The stop condition shall start at the last rising edge.

NOTE If the last bit of the frame is logical 1, the stop condition begins inside this bit. If the last bit of the frame is logical 0, the stop condition begins at the end of this bit.

7.3 Frame description

A frame shall consist of:

- 1 start bit;
- n data bits;
- 1 stop condition.

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NOTE 1 The number of data bits n depends on the type of frame.

NOTE 2 A frame with n data bits is called an n-bit frame.

7.4 Frame types

7.4.1 16-bit forward frame

A 16-bit forward frame shall contain n = 16 data bits.

NOTE This type of forward frame can be used to communicate with control gear conformant to IEC 62386-102.

7.4.2 24-bit forward frame

A 24-bit forward frame shall contain n = 24 data bits.

NOTE This type of forward frame can be used by and to communicate with control devices conformant to IEC 62386-103.

7.4.3 32-bit forward frame

A 32-bit forward frame shall contain n = 32 data bits.

NOTE This type of forward frame is used for firmware transfers to control gear and control devices conformant to IEC 62386-105.

7.4.4 Reserved forward frame

Frames with n = 20 data bits are reserved forward frames. They shall not be used.

7.4.5 Backward frame

A backward frame shall contain n = 8 data bits.

Backward frames shall be used only as answers to forward frames.

7.4.6 Proprietary forward frames

There are two kinds of proprietary forward frames.

- Proprietary forward frames which differ from the frames defined or reserved in this document in the number of data bits. Such proprietary forward frames shall trigger a frame size violation in bus units which are not designed to interpret them.
- Proprietary forward frames which differ from the frames defined or reserved in this document in the start bit, data bit or stop condition encoding. Such proprietary forward frames shall trigger a bit timing violation in bus units which are not designed to interpret them.

A transmitter sending proprietary forward frames shall comply with the frame sequence timing requirements given in Table 17.

A multi-master transmitter sending proprietary forward frames shall comply with the frame sequence timing requirements given in Table 22 and shall use by default priority 5 only, until configured otherwise.

NOTE Proprietary forward frames can trigger backward frames.

A receiver designed for proprietary frames with n = 8 to n = 15 bits can distinguish such frames from overlapping backward frames by a variety of methods. Nevertheless it is recommended that such designs be avoided.

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8 Timing

8.1 Single-master transmitter timing

8.1.1 Single-master transmitter bit timing

The transmitter bit timing shall conform to the limits shown in Table 16. Figure 12 illustrates a portion of a typical frame.

NOTE 1 This timing definition is used for control gear and single-master control devices. Multi-master control devices are subject to tighter timing constraints. See 8.3.1.

NOTE 2 See Clause A.4 for further details on the change in timing definitions with the change from the first edition to the second edition of this standard.

Regardless of the low level voltage and the high level voltage, the timing is measured at a level of 8,0 V.

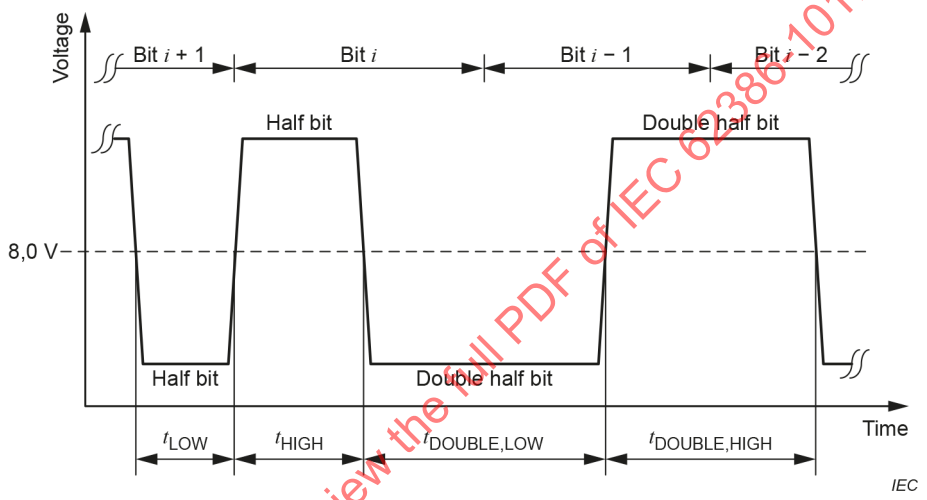

Figure 12 – Bit timing example

Table 16 – Transmitter bit timing

	Minimum	Typical	Maximum
Half bit time t_{HIGH}, t_{LOW}	366,7 µs	416,7 µs	466,7 µs
Double half bit time $t_{DOUBLE,LOW}$, $t_{DOUBLE,HIGH}$	733,3 µs	833,3 µs	933,3 µs
Stop condition time T_{STOP}	2 450 µs		

8.1.2 Single-master transmitter frame sequence timing

Figure 13 shows the settling time between two consecutive frames.

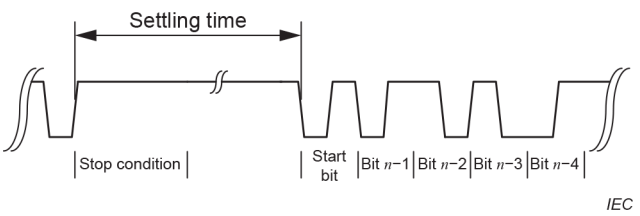

Figure 13 – Settling time illustration

For the settling time the values given in Table 17 shall apply.

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NOTE When designing a bus powered bus unit, the minimum transmitter settling time can be regarded as a period during which power can reliably be drawn from the bus.

Table 17 – Transmitter settling time values

	Minimum	Typical	Maximum
Settling time between a forward frame and a backward frame[a]	5,5 ms		10,5 ms
Settling time between any other frame and a forward frame	13,5 ms [b]		75,0 ms [c]

[a] A transmitter shall start the transmission of its backward frame (if any) within the time slot defined in this Table 17, regardless of whether any other transmitter has already started to transmit a backward frame of its own. The settling time apparent on the bus will naturally depend upon the timing of the first backward frame transmitted; the notional settling time for later backward frames can be regarded as a delay time.

[b] Also applicable after overlapping backward frames causing a receiver bit timing violation or a receiver frame size violation.

[c] Only applicable for send-twice forward frames, see 9.4.

8.2 Receiver timing

8.2.1 Receiver bit timing

A receiver shall receive or reject frames according to the bit timing requirements as follows.

It is recommended that short pulses and spikes are ignored.

For logical bits starting with an edge, the timing given in Table 18 shall apply to the duration from this starting edge, to the next edge. This period can be the first half bit of a start bit, or a stop condition, or the first half bit of another logical bit where the previous logical bit is of the same value.

The timing in Table 19 shall apply from the edge inside a logical bit, to the next edge. This period can be a half bit, a double half bit or a stop condition.

Figure 14 shows which table is applicable at which time period in an example.

After the minimum stop condition given in Table 18 and Table 19, a frame is regarded as having been received.

NOTE 1 For the significance of regarding the frame as received, see 9.1.1.

NOTE 2 Receiving a valid backward frame does not necessarily imply that it was sent by a single transmitter as backward frames can overlap synchronously, or nearly so.

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Table 18 – Receiver timing starting at the beginning of a logical bit

Minimum	Typical	Maximum	Description
		< 333,3 µs	Grey area
333,3 µs	416,7 µs	500 µs	Half bit
> 500 µs		< 750 µs	Grey area
750 µs		1 400 µs [a] 45 ms [b]	Bit timing violation
> 1 400 µs [a]		< 2 400 µs [a]	Grey area
2 400 µs [a]			Stop condition

[a] Only applicable for idle state.

[b] Only applicable for active state. Active state longer than 45 ms shall be interpreted as bus power down.

Table 19 – Receiver timing starting at an edge inside of a logical bit

Minimum	Typical	Maximum	Description
		< 333,3 µs	Grey area
333,3 µs	416,7 µs	500 µs	Half bit
> 500 µs		< 666,7 µs	Grey area[c]
666,7 µs	833,3 µs	1 000 µs	2 half bits
> 1 000 µs		< 1 200 µs	Grey area
1 200 µs		1 400 µs [a] 45 ms [b]	Bit timing violation
> 1 400 µs [a]		< 2 400 µs [a]	Grey area
2 400 µs [a]			Stop condition

[a] Only applicable for idle state.

[b] Only applicable for active state. Active state longer than 45 ms shall be interpreted as bus power down.

[c] If an edge occurs after a time within the grey area, the receiver can conclude that it is a timing violation. This can be caused for example, by overlapping backward frames.

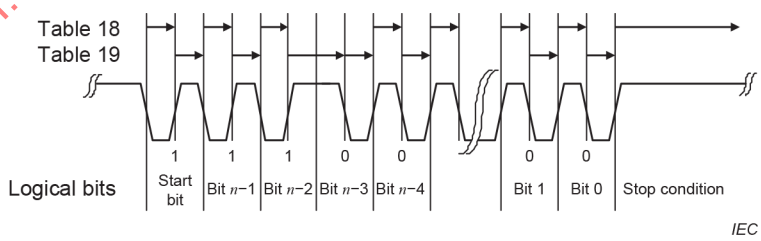

Figure 14 – Receiver timing decision example

8.2.2 Receiver bit timing violation

If a receiver detects a bit timing violation it shall reject the frame, except in case of a backward frame. See 8.2.5.

After the detection of a bit timing violation, the receiver shall be ready for decoding the next frame immediately after detection of a stop condition.

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NOTE A receiver bit timing violation could be the result of more than one transmitter being active, e. g. in case of overlapping backward frames.

8.2.3 Receiver frame size violation

If a receiver detects a frame with a number of data bits not supported by that receiver, this shall trigger a frame size violation and shall be ignored, except in case of a backward frame, see 8.2.5.

After a frame size violation the receiver shall be ready to decode the next frame immediately after the detection of a stop condition.

NOTE A receiver frame size violation could be the result of more than one transmitter being active, or the result of a proprietary forward frame, see 7.4.6.

8.2.4 Receiver frame sequence timing

Decoding of a new frame shall only start after detection of a stop condition.

NOTE This requirement ensures that for example, a 24-bit forward frame is not interpreted as a 16-bit forward frame when the receiver starts up during the transmission of the 24-bit forward frame.

A receiver shall accept frame sequences with the settling times given in Table 20.

Table 20 – Receiver settling time values

	Minimum	Typical	Maximum	Description
Settling time between forward frame and backward frame	> 1,4 ms [a]		< 2,4 ms	Grey area[b]
	2,4 ms		12,4 ms	Frame shall be interpreted as backward frame.
	> 12,4 ms		< 13,4 ms	Grey area[b]
	13,4 ms			Frame shall not be interpreted as backward frame.
Settling time between forward frame and forward frame	> 1,4 ms [a]		< 2,4 ms	Grey area[b]
	2,4 ms			Frame shall be interpreted as forward frame.
Settling time between first and second forward frame of send-twice forward frames[c]	> 1,4 ms [a]		< 2,4 ms	Grey area[b]
	2,4 ms		94 ms	Frames shall be interpreted as send-twice forward frames.
	> 94 ms		< 105 ms	Grey area[c d]
	105 ms			Frames shall be interpreted as two separate forward frames.
Settling time between backward frame and forward frame	> 1,4 ms [a]		< 2,4 ms	Grey area[b]
	2,4 ms			Frame shall be interpreted as forward frame.

[a] Because of the definition of the stop condition this is the minimum time to distinguish frames.

[b] Frames within this area can be interpreted in multiple ways.

[c] See 9.4.

[d] Frames within this area can be interpreted as send-twice forward frames or as two separate forward frames.

8.2.5 Reception of backward frames

The reception of a backward frame shall start with the first active state after the forward frame which triggered the backward frame if this first active state is detected within a maximum of 13,4 ms settling time.

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If this frame triggers a frame size violation or bit timing violation, it shall be interpreted as a backward frame. It is possible that such a frame will contain information that is worth processing in certain cases. See also 7.4.5 and 9.6.2.

8.3 Multi-master transmitter timing

8.3.1 Multi-master transmitter bit timing

The multi-master transmitter bit timing shall be according to the values given in Table 21.

Figure 12 illustrates a portion of a typical frame.

Regardless of the low level voltage and the high level voltage, the timing is measured at a level of 8,0 V.

Table 21 – Multi-master transmitter bit timing

	Minimum	Typical	Maximum
Half bit time t_{HIGH}, t_{LOW}	400,0 µs	416,7 µs	433,3 µs
Double half bit time $t_{DOUBLE,LOW}$, $t_{DOUBLE,HIGH}$	800,0 µs	833,3 µs	866,7 µs
Stop condition time T_{STOP}	2 450 µs		

A multi-master transmitter shall follow the rules of collision avoidance (see 9.2.2), collision detection (see 9.2.3), and collision recovery (see 9.2.4).

8.3.2 Multi-master transmitter frame sequence timing

In order to minimize the probability of collisions, different frame priorities shall be realized using different settling times.

NOTE 1 The usage of the forward frame priorities is described in IEC 62386-103.

Figure 13 shows the settling time between two consecutive frames.

For the settling time of frames with different priorities, the values given in Table 22 shall apply.

NOTE 2 When designing a bus powered bus unit, the minimum transmitter settling time can be regarded as a period during which power can reliably be drawn from the bus.

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Table 22 – Multi-master transmitter settling time values

Settling time between	Minimum	Typical	Maximum
Forward frame and backward frame[a]	5,5 ms		10,5 ms
Any frame and forward frame (priority 1)[b]	13,5 ms	[c]	14,7 ms [d]
Any frame and forward frame (priority 2)[b]	14,9 ms	[c]	16,1 ms [d]
Any frame and forward frame (priority 3)[b]	16,3 ms	[c]	17,7 ms [d]
Any frame and forward frame (priority 4)[b]	17,9 ms	[c]	19,3 ms [d]
Any frame and forward frame (priority 5)[b]	19,5 ms	[c]	21,1 ms [d]

[a] This is a delay time where the backward frame can start regardless of transitions in between.

[b] Also applicable after overlapping backward frames causing a receiver bit timing violation or a receiver frame size violation.

[c] It is strongly recommended that a multi-master transmitter starts its transmission at a random point of time within the minimum and maximum settling time corresponding to the intended priority, as this helps in avoiding collisions. Clock tolerances need to be considered.

[d] When a multi-master transmitter intends to send a frame with a certain priority but the maximum settling time for this priority has already passed, the transmitter can start its transmission immediately considering collision avoidance.

9 Method of operation

9.1 Dealing with frames and commands

9.1.1 General

The flow from the moment a number of bits are received on the bus interface until a command is executed is illustrated in Figure 15. The conditions to enter the next state are described in 9.1.2, 9.1.3, 9.1.4 and 9.1.5. This Subclause 9.1 does not necessarily apply when using proprietary forward frames.

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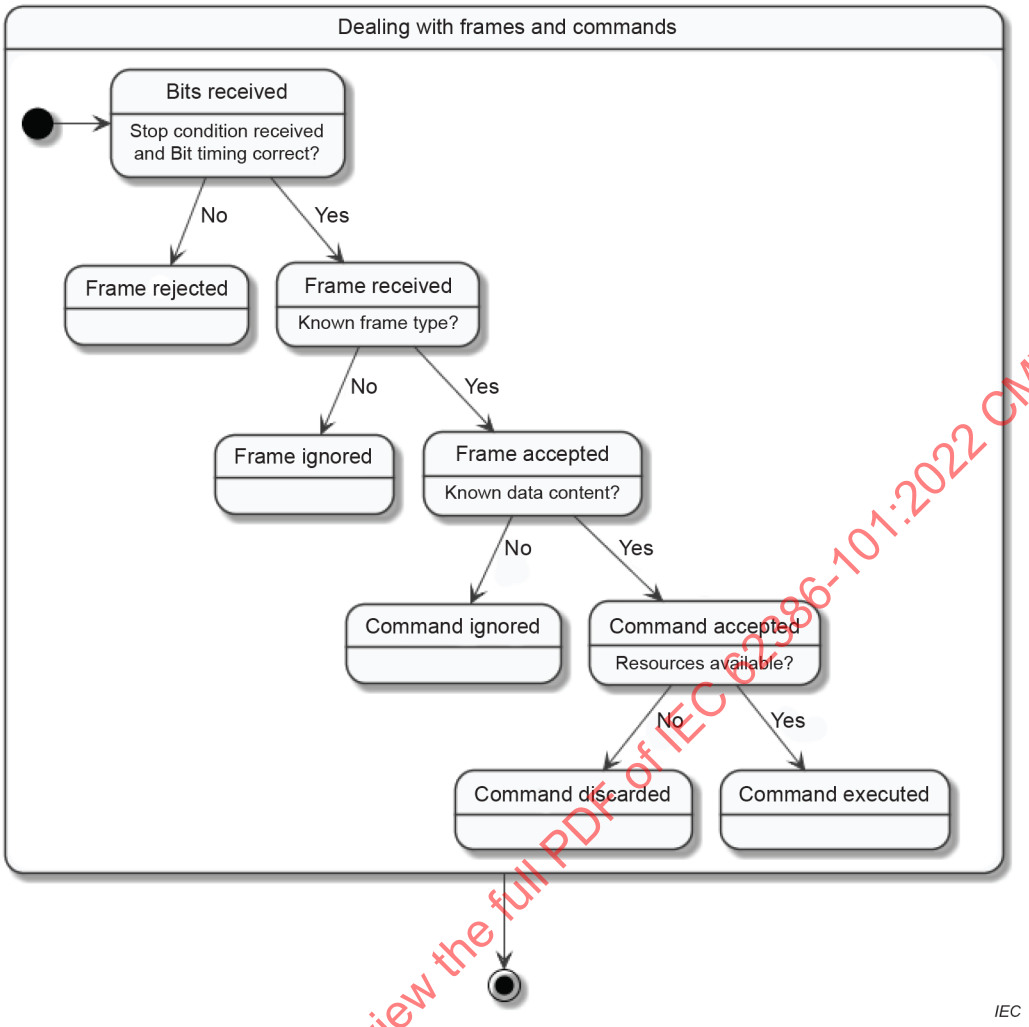

Figure 15 – Dealing with frames and commands

9.1.2 Frame received or rejected

Any frame consisting of valid bits and a stop condition shall be considered received, otherwise it shall be considered rejected.

9.1.3 Frame accepted or ignored

Any received frame that uses the correct frame type and correct number of data bits for a particular receiver shall be considered accepted, otherwise it shall be considered ignored.

9.1.4 Command accepted or ignored

Any accepted frame shall be analysed for content. If the content forms a command, this command shall be accepted, otherwise it shall be considered as an ignored command.

NOTE Further details on commands are given in IEC 62386-102, IEC 62386-103, the IEC 62386-2xx series and the IEC 62386-3xx series.

9.1.5 Command executed or discarded

Any accepted command shall be executed in the settling time between the frame in which it was received and the next possible frame on the bus, except when explicitly stated otherwise in the description of the command. Execution of the command could depend on resources to handle the command.

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Accepted commands that are not executed are considered discarded.

NOTE 1 The next frame on the bus could be a new command or the answer to the received command.

NOTE 2 This timing requirement refers to the change of and the reaction to internal signals of a bus unit. The delay time between external signals and internal signals of a bus unit is not within the scope of this document, but could be a performance issue of a system.

The refresh rate of internal variables (for example a status) should be such that a correct new value can be observed immediately following a command that changes this value (for example a configuration command), except when explicitly stated otherwise in the description of the command.

The execution of a command can involve the triggering of a process which itself takes longer than the settling time between frames.

NOTE 3 An example for such a process is a running fade.

9.2 Collision avoidance, collision detection and collision recovery

9.2.1 General

Collision avoidance (9.2.2), collision detection (9.2.3), and collision recovery (9.2.4) apply to multi-master transmitters only. They do not apply to backward transmissions.

A multi-master transmitter shall always attempt to avoid collisions before sending a forward frame.

As collisions cannot be avoided in all situations, a collision detection mechanism is necessary. A transmitter detecting a collision shall always cancel its own transmission immediately.

If, after collision detection, the resulting signal on the bus violates the timing requirements of 9.2.3, a collision recovery mechanism shall be applied.

9.2.2 Collision avoidance

Collision avoidance shall be achieved by checking the settling time before transmitting a forward frame. This implies that a multi-master transmitter shall not start a transmission when the bus is not in idle state.

NOTE The settling time depends on the frame priority used.

9.2.3 Collision detection

Collision detection shall be applied during the transmission of any forward frame.

When the resulting signal on the bus shown in Table 24 is not identical to the signal the multi-master transmitter intended to transmit, the multi-master transmitter shall immediately stop its transmission.

When the transmitter that stopped its transmission can guarantee that the timing of the signal created before stopping the transmission does not meet one of the destroy areas given in Table 23 and Table 24, it shall return to collision avoidance as described in 9.2.2. The transmitter may restart its transmission if it is still required. See also Clause A.3.

Otherwise the transmitter that stopped its transmission shall check the timing of the signal on the bus:

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- When the timing of the resulting signal does not meet one of the destroy areas given in Table 23 and Table 24, the transmitter shall return to collision avoidance as described in 9.2.2. The transmitter may restart its transmission if it is still required.

NOTE 1 In this case the resulting frame on the bus is still a valid forward frame and can be received by any bus unit on the bus.

- When the timing of the resulting signal on the bus meets one of the destroy areas given in Table 23 and Table 24, the transmitter shall follow the collision recovery method described in 9.2.4. After collision recovery the transmitter may restart its transmission.

NOTE 2 In this case there would be a risk that one or more devices connected to the bus could interpret the frame as containing relevant data, whilst others could reject it. This risk is averted by destroying the frame and thereby ensuring that all receivers will regard it as invalid.

Table 23 – Checking a logical bit, starting at an edge at the beginning of the bit

Minimum	Typical	Maximum	Description
		< 100 µs	Grey area[c]
100 µs		356,7 µs	Destroy area[a]
> 356,7 µs		< 400,0 µs	Grey area
400,0 µs		433,3 µs	Valid half bit
> 433,3 µs		< 476,7 µs	Grey area
476,7 µs			Destroy area[a b]

[a] Signals within the destroy area shall lead to collision recovery described in 9.2.4.

[b] Only applicable for active state.

[c] Pulses in this grey area may be ignored and not considered in decisions on timing as they can result from noise.

Table 24 – Checking a logical bit, starting at an edge inside the bit

Minimum	Typical	Maximum	Description
		< 100 µs	Grey area[c]
100 µs		356,7 µs	Destroy area[a]
> 356,7 µs		< 400,0 µs	Grey area
400,0 µs		433,3 µs	Valid half bit
> 433,3 µs		< 476,7 µs	Grey area
476,7 µs		723,3 µs	Destroy area[a]
> 723,3 µs		< 800,0 µs	Grey area
800,0 µs	833,3 µs	866,7 µs	2 valid half bits
> 866,7 µs		< 943,3 µs	Grey area
943,3 µs			Destroy area[a b]

[a] Signals within the destroy area shall lead to collision recovery described in 9.2.4.

[b] Only applicable for active state.

[c] Pulses in this grey area may be ignored and not considered in decisions on timing as they can result from noise.

The signal delay times of the transmitter and the receiver necessary for the check need to be taken into account when at multi-master transmitters. See Clause A.3.

Figure 16 shows which table is applicable at which time period in an example.

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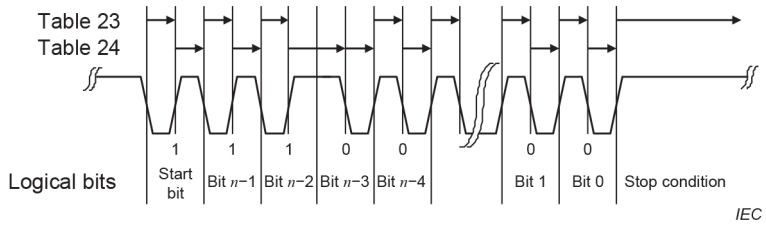

Figure 16 – Collision detection timing decision example

9.2.4 Collision recovery

When starting the collision recovery the multi-master transmitter shall force the bus to active state for the break time t_{BREAK} given in Table 25 within 450 µs at the latest.

NOTE 1 This results in all bus units detecting a bit timing violation. All multi-master transmitters will enter the collision recovery process.

After the break time the multi-master transmitter shall check the bus. If the bus is in active state, the multi-master transmitter shall return to collision avoidance as described in 9.2.2. Otherwise the multi-master transmitter shall return to collision avoidance as described in 9.2.2 also, but it shall restart its original transmission with a reduced settling time $t_{RECOVER}$.

NOTE 2 By this method the last transmitter releasing the bus will be the first restarting to transmit its forward frame.

Table 25 – Collision recovery timing

	Minimum	Typical	Maximum
Break time t_{BREAK}	1,2 ms		1,4 ms
Recovery time $t_{RECOVER}$	4,0 ms	[a]	4,6 ms
[a] It is strongly recommended that a multi-master transmitter start its transmission at a random point of time in the interval between the minimum and maximum recovery time, as this helps in avoiding collisions.			

It is possible that when using proprietary frames this break time is not long enough to guarantee detection. Care should be taken that the proprietary frame is still valid, or a proprietary solution should be in place for these frames.

Figure 17 shows an example of the collision recovery mechanism:

Multi-master transmitter 1 detects a collision at point A of the frame it is intending to transmit and immediately forces the bus to active state for the break time t_{BREAK}. Multi-master transmitter 2 now detects the collision at point B of the frame it is intending to transmit. It also forces the bus to active state for the break time t_{BREAK}.

At the end of the break time t_{BREAK} of multi-master transmitter 1 the bus is still in active state (point C). Therefore multi-master transmitter 1 enters collision avoidance with the normal settling time depending on the priority of the forward frame to be transmitted. The settling time of multi-master transmitter 1 begins when the bus returns to idle state.

At the end of the break time of multi-master transmitter 2 the bus returns to idle state (point D). Therefore multi-master transmitter 2 enters collision avoidance with the reduced settling time $t_{RECOVER}$. As a consequence transmitter 2 will restart its transmission whilst transmitter 1 is still waiting for the end of its settling time.

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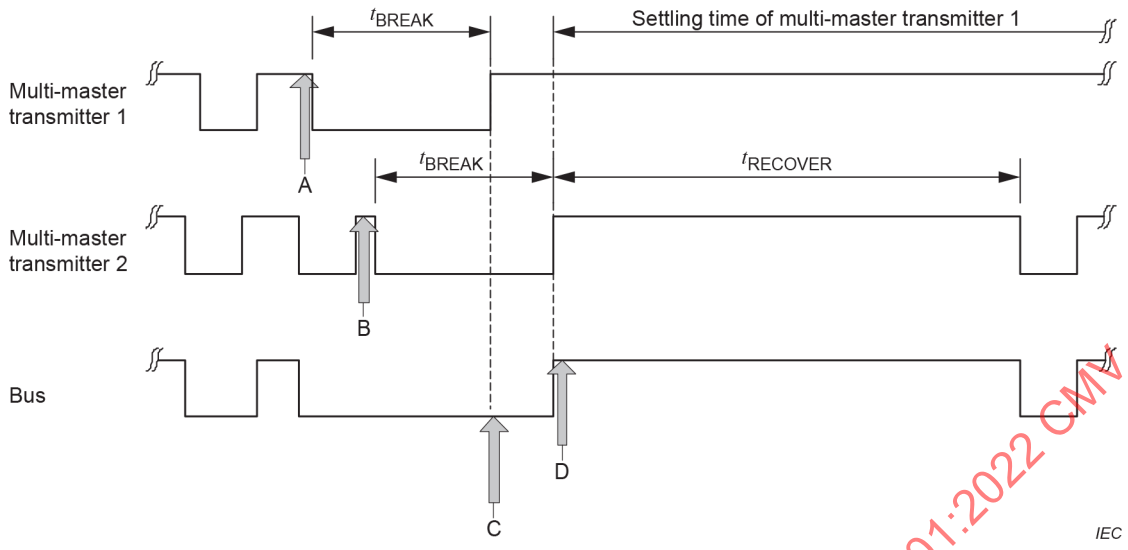

NOTE The traces of multi-master transmitter 1 and multi-master transmitter 2 are shown only for explanation and cannot be measured in a real system, where only the signal labelled "Bus" occurs.

Figure 17 – Collision recovery example

9.3 Transactions

This Subclause 9.3 shall apply for multi-master transmitters only.

The purpose of transactions is to ensure that a sequence of commands sent by one control device cannot be interrupted by another control device.

The first frame of the transaction shall be sent with priority 2, 3, 4 or 5. All remaining forward frames of the transaction shall be sent with priority 1. The priority of the first frame of a transaction shall depend on the primary purpose of the transaction. See IEC 62386-103 for details on priorities.

NOTE By definition a transaction can consist of a single forward frame.

Except during commissioning, a single transaction should not exceed a total duration of 400 ms so that more than one control device can get access to the bus in a reasonable time. The total duration of successively transmitted transactions from a single control device should not exceed 400 ms without at least one multi-master transmitter settling time exceeding the maximum settling time for priority 5.

9.4 Send-twice forward frames and send-twice commands

Some of the commands defined in IEC 62386-102, IEC 62386-103, the IEC 62386-2xx series and the IEC 62386-3xx series need to be accepted twice within a defined period of time before being executed. Control devices shall use send-twice forward frames for transmission of such commands.

A transmitter shall transmit two identical forward frames which make up a send-twice forward frame:

- with a settling time as shown in Table 17; see footnote c in the table, and
- without any other forward frame in-between.

A multi-master transmitter shall transmit two identical forward frames which make up a send-twice forward frame as a transaction.

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A receiver shall accept two consecutive forward frames as a send-twice forward frame, if all of the following conditions hold:

- the settling time between the two identical forward frames is less than or equal to the maximum receiver settling time given in Table 20;
- no active state occurs in between the two forward frames;
- the two forward frames are identical.

If any one of the above conditions is not met, the receiver shall interpret all frames as separate forward frames. Consequently the last forward frame received in this context may be interpreted as the first forward frame of a new pair of send-twice forward frames.

9.5 Command iteration

Some of the commands defined in IEC 62386-102, IEC 62386-103, the IEC 62386-2xx series, and the IEC 62386-3xx series, trigger and extend appropriate functions when repeated periodically.

In addition to the requirements given in 8.1 and 8.3, a transmitter shall transmit the commands of a command iteration following the requirements given in Table 26.

NOTE There could be other frames sent in-between the frames of a command iteration.

Table 26 – Transmitter command iteration timing

	Minimum	Typical	Maximum	Description
Transmitter command iteration interval			175 ms	Measured between the last rising edge of one frame and the last rising edge of the next following frame of a command iteration.

A receiver shall trigger the appropriate function when the frame of the first command of command iteration is accepted.

A receiver shall extend the appropriate function after each acceptance of the command if the frame is received before the maximum receiver command iteration timeout given in Table 27, even if other frames are received within the command iteration.

Table 27 – Receiver command iteration timing

	Minimum	Typical	Maximum	Description
Receiver command iteration timeout[a]	12,6 ms		180 ms	Accept as command of a command iteration.
	> 180 ms		< 220 ms	Grey area
	220 ms			Reject as command of a command iteration.
[a] Measured between the point of time one frame of the command iteration was received and the next following frame was received; see 8.2.1.				

9.6 Usage of a shared interface

9.6.1 General

This Subclause 9.6 applies only to bus units where more than one logical unit or instance share the same physical interface.

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9.6.2 Backward frames

The transmitter shall transmit a valid backward frame if the content of the backward frame of all logical units is identical. The answer NO to a query shall not be considered a backward frame with content.

If the content is not identical, the transmitter shall transmit a corrupted backward frame that contains an active state of at least 1 300 µs and maximum 2 000 µs.

NOTE This is to simulate overlapping backward frames.

9.6.3 Forward frames

The transmitter shall transmit the forward frames generated within the bus unit sequencially considering the priorities.

NOTE This is to ensure that a bus unit does not cause internally generated collisions.

9.7 Use of multiple bus power supplies

The sum of the maximum supply current of all bus power supply units connected to the bus shall not exceed 250 mA.

Bus power supplies shall not be connected to the bus with reversed polarity, however all power supplies shall be protected for such cases, which includes the capability to handle the power dissipation caused by reverse polarity.

NOTE 1 In determining the power dissipation, faulty wiring can result in a worst-case voltage of −22,5 V due to reverse polarity. A Zener-diode could be used for reverse polarity protection.

NOTE 2 Whenever multiple power supplies are used there is a possibility that the system will not have enough power to continue normal operation when one of the power supplies fails.

NOTE 3 See also Clause A.5.

10 Declaration of variables

There are no variables for control gear or control devices defined in this document.

11 Definition of commands

There are no commands for control gear or control devices defined in this document.

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Annex A
(informative)

Background information for systems

A.1 Wiring information

The sum of the resistive voltage drop is one of the factors limiting the system size. The maximum allowed voltage drop ΔU on the bus of 2,0 V, is determined from the bus supply current I_B and the total resistance R_T of the wiring:

$$\Delta U = R_T \times I_B$$

The total resistance R_T of the wiring depends on the specific resistance ρ of the wires used, the cross-section A of the wires and the wiring length L:

$$R_T = 2 \times \rho \times \frac{L}{A}$$

NOTE 1 For the total resistance the length is doubled, since two wires are necessary for the bus, hence the factor two in the formula.

NOTE 2 The specific resistance is temperature dependent.

For the maximum allowed voltage drop of ΔU = 2,0 V and the maximum allowed bus supply current of I_B = 250 mA the following relation between cross-section A and wiring length L can be derived from the above formulae:

$$L = 4 \times \frac{A}{\rho}$$

Table A.1 shows the maximum cable length L between any two bus units or bus power supplies for different wiring cross-sections A and wiring materials at different temperatures.

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Table A.1 – Maximum cable length

Material	*A* mm^2	Maximum cable length *L* m		
		25 °C	50 °C	75 °C
Copper	0,14	31	28	26
	0,50	112	102	93
	0,75	168	153	140
	1,00	224	204	187
	1,50	300[a]	300[a]	281
	2,00	300[a]	300[a]	300[a]
	2,50	300[a]	300[a]	300[a]
Aluminium	0,14	19	17	16
	0,50	68	62	57
	0,75	102	93	86
	1,00	136	125	115
	1,50	205	187	172
	2,00	273	250	230
	2,50	300[a]	300[a]	288

[a] Cable lengths of more than 300 m are not recommended.

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A.2 System architectures

A.2.1 General

Architectures mentioned in this Annex A are examples. Other architectures are also possible.

A.2.2 Single-master architecture

A lighting control system in a single-master architecture can consist of:

- a bus power supply,
- a single-master application controller,
- at least one control gear.

Figure A.1 shows an example where the single-master application controller shares the physical interface with the bus power supply.

The single-master application controller can be equipped with:

- buttons and sensors,
- terminals for connection to buttons and sensors, or
- communication interfaces to other bus systems.

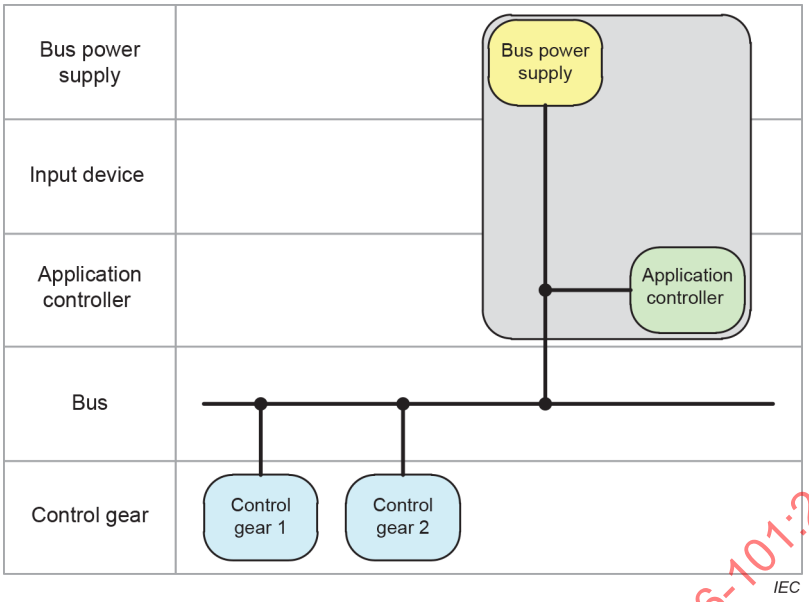

Figure A.1 – Single-master architecture example

In such a system architecture the single-master application controller uses 16-bit forward frames to transmit commands to the control gear.

NOTE Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series.

A.2.3 Multi-master architecture with one application controller

A lighting control system in a multi-master architecture with one application controller can consist of:

- a bus power supply,
- a multi-master application controller,
- at least one input device, and
- at least one control gear.

Figure A.2 shows an example of a system with one multi-master application controller and two input devices.

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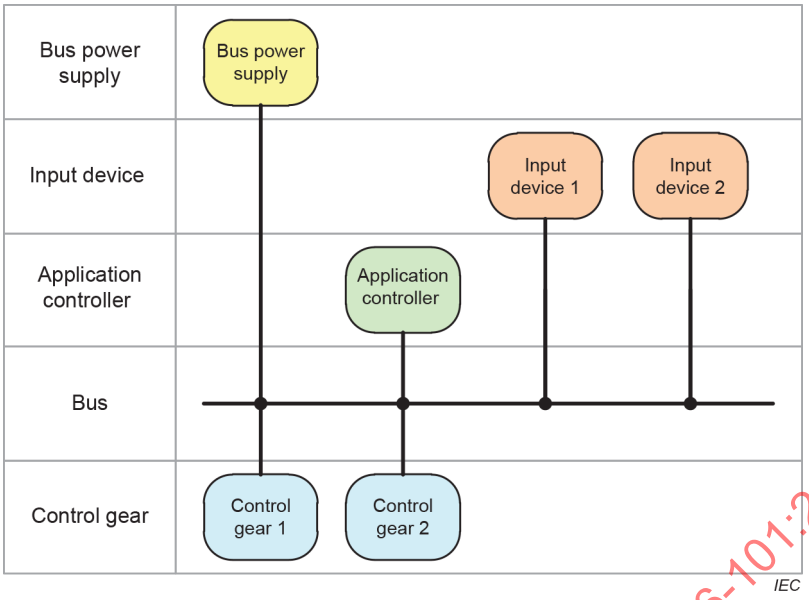

Figure A.2 – Multi-master architecture example with one application controller

In such a system architecture the multi-master application controller uses 16-bit forward frames to transmit commands to the control gear. 24-bit forward frames are used to configure and control the input devices. The input devices use 24-bit forward frames to transmit information to the application controller.

NOTE Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series. Commands for communication between multi-master application controllers and input devices are defined in IEC 62386-103 and the IEC 62386-3xx series.

A.2.4 Multi-master architecture with more than one application controller

A lighting control system in a multi-master architecture with more than one application controller can consist of:

- a bus power supply,
- at least two multi-master application controllers, and
- at least one control gear.

Figure A.3 shows an example of a system with two application controllers.

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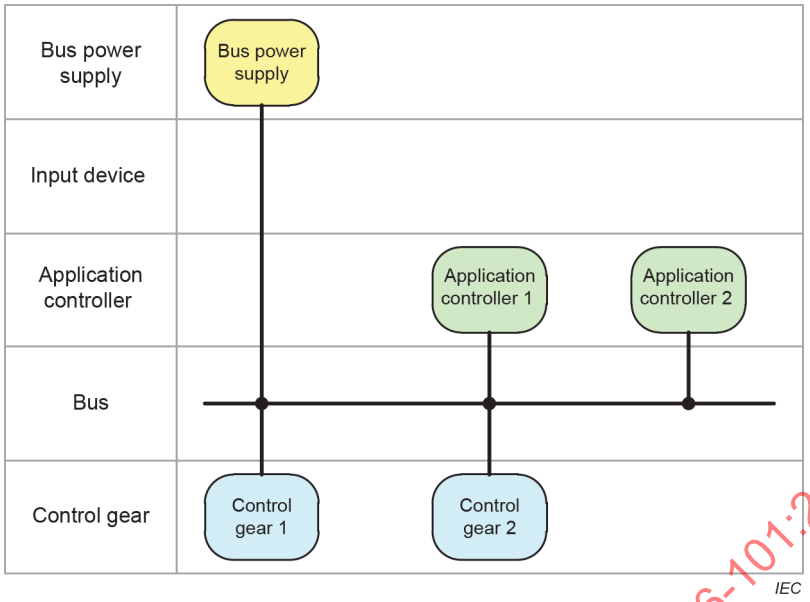

Figure A.3 – Multi-master architecture example with two application controllers

In such a system architecture the two multi-master application controllers use 16-bit forward frames to transmit commands to the control gear. Since more than one multi-master application controller has control over the system, it is clear that these multi-master application controllers should be able to cooperate in order to ensure some level of system integrity.

NOTE 1 Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series.

NOTE 2 The two multi-master application controllers can communicate with each other using 24-bit forward frames.

A.2.5 Multi-master architecture with integrated input device

A lighting control system with a multi-master architecture with an integrated input device can consist of:

- a bus power supply,
- at least one multi-master application controller,
- at least one input device integrated into a multi-master application controller, and
- at least one control gear.

Figure A.4 shows an example of a system with an integrated input device.

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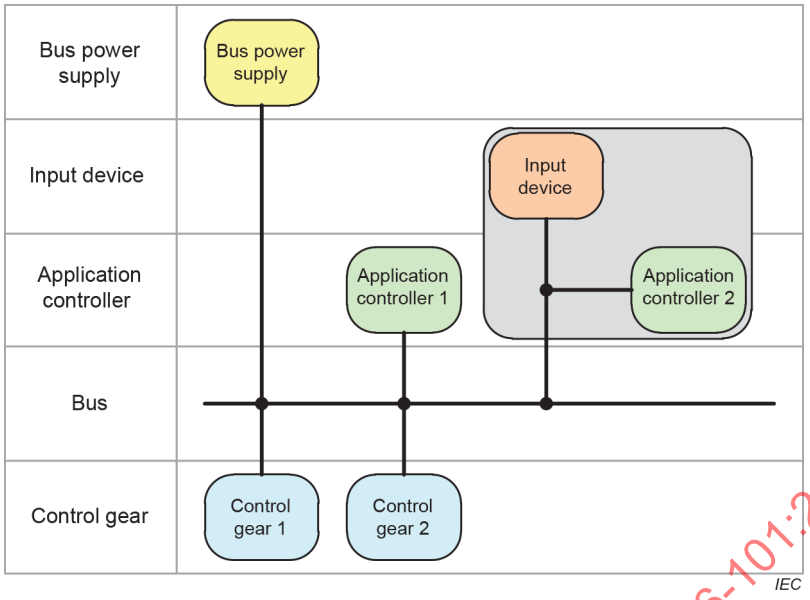

Figure A.4 – Multi-master architecture example with integrated input device

There are two possible modes of operation.

- Multi-master application controller 1 is the only control device which transmits 16-bit forward frames to the control gear. It receives and processes 24-bit forward frames from the input device. The multi-master application controller 2 is disabled in this case.
- Both multi-master application controllers transmit 16-bit forward frames to the control gear and both multi-master application controllers receive and process 24-bit forward frames from the input device. Since more than one multi-master application controller has control over the system, it is clear that these two multi-master application controllers should be able to cooperate in order to ensure some level of system integrity. The multi-master application controller 2 and the input device can act as one or as two logical units on the bus.

NOTE 1 Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series.

NOTE 2 The two multi-master application controllers can communicate with each other using 24-bit forward frames.

A.2.6 Multi-master architecture with integrated input device and power supply

A lighting control system in a multi-master architecture with an integrated input device and integrated bus power supply can consist of:

- zero or more input devices,
- at least one input device and bus power supply integrated into a multi-master application controller, and
- at least one control gear.

Figure A.5 shows an example of a system with an integrated input device and integrated bus power supply.

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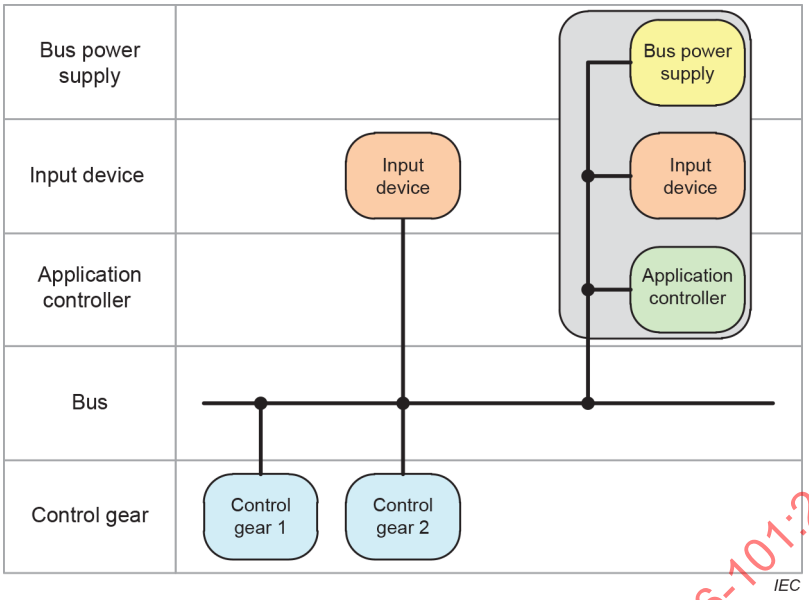

Figure A.5 – Multi-master architecture example with integrated input device and bus power supply

In such a system architecture the multi-master application controller uses 16-bit forward frames to transmit commands to the control gear. 24-bit forward frames are used to configure and control the input devices. The input devices use 24-bit forward frames to transmit information to the application controller.

NOTE Control gear commands are defined in IEC 62386-102 and the IEC 62386-2xx series. Commands for communication between multi-master application controllers and input devices are defined in IEC 62386-103 and the IEC 62386-3xx series.

A.3 Collision detection

Figure A.6 shows all the timing related issues when transmitting. To read it, start with the TX micro line (which is the microcontroller output to the transmitter circuit), see what happens on the bus and finally see what happens on the RX micro lines (which are the microcontroller input for receiving and checking the timing). All possible delays are accounted for.

The dotted horizontal lines show the thresholds of the local receiver used to check the transmission.

The dashed horizontal lines show the thresholds of a remote receiver, which are valid due to the bus influence. The maximum/minimum remote thresholds are 2,0 V above/below the local thresholds, since a 2,0 V voltage drop is possible on the bus.

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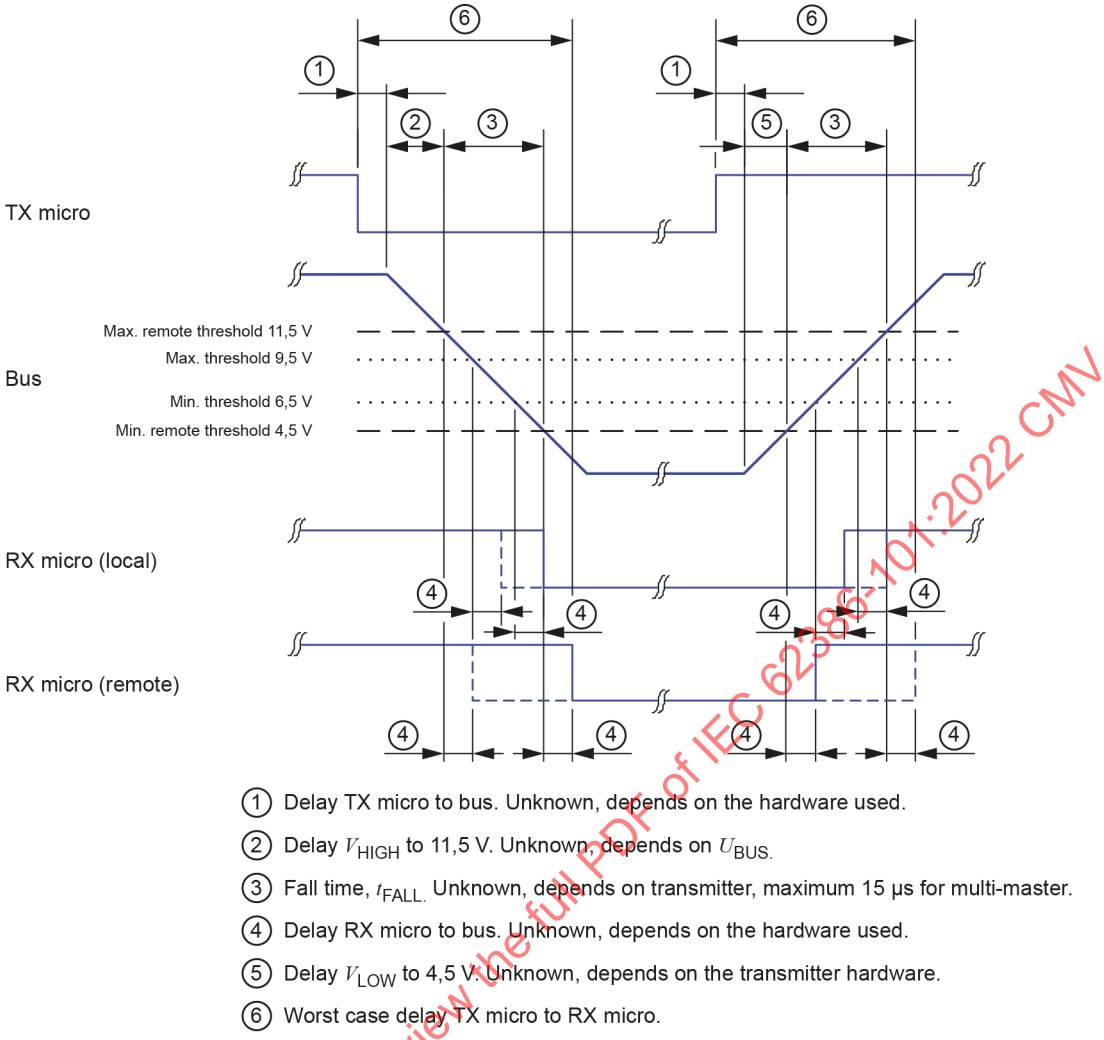

Figure A.6 – Collision detection timing diagram

A.4 Timing definition explanations

A.4.1 General

The aim of this Annex A is to explain the change of timing definitions from Edition 1 of IEC 62386-101:2009 to Edition 2 of IEC 62386-101:2014.

A.4.2 Receiver timing

The receiver timing is in the main points unchanged from Edition 1. The timing tolerances of 10 % have been replaced by absolute minimum and maximum time values.

All timing requirements are given and tested at a fixed threshold voltage of 8,0 V.

A.4.3 Transmitter timing

Edition 1 of IEC 62386-101 did not explicitly define any transmitter timing. Transmitter timing was only given implicitly by the receiver timing and its tolerances. Timing definitions suitable for a proper working multi-master system were not defined.

Also the influence of the wiring and the receiver threshold voltage on signal timing was not fully considered in Edition 1.

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Edition 2 of IEC 62386-101 defines the timings both for single-master and for multi-master transmitters, taking into account all influences upon those timings.

Except where otherwise stated, all timing requirements are given for a fixed threshold voltage of 8,0 V. This threshold voltage is applicable to the test procedures both for transmitters and for receivers. This was not the case in Edition 1.

A.4.4 Grey areas

The definitions in Edition 1 of IEC 62386-101 and IEC 62386-102 did not explicitly define tolerances for the decision points of the receiver timings.

For this reason Edition 2 of IEC 62386-101 introduced so called "grey areas". The design engineer can put the decision point inside this grey area.

Grey areas guarantee that any receiver can interoperate with any transmitter, since the grey areas provide a suitable safety margin. As a consequence the grey areas decrease the possible tolerances for transmitters.

Figure A.7 illustrates the influences that are taken into consideration at the steps from the receiver timing requirements to the multi-master timing requirements.

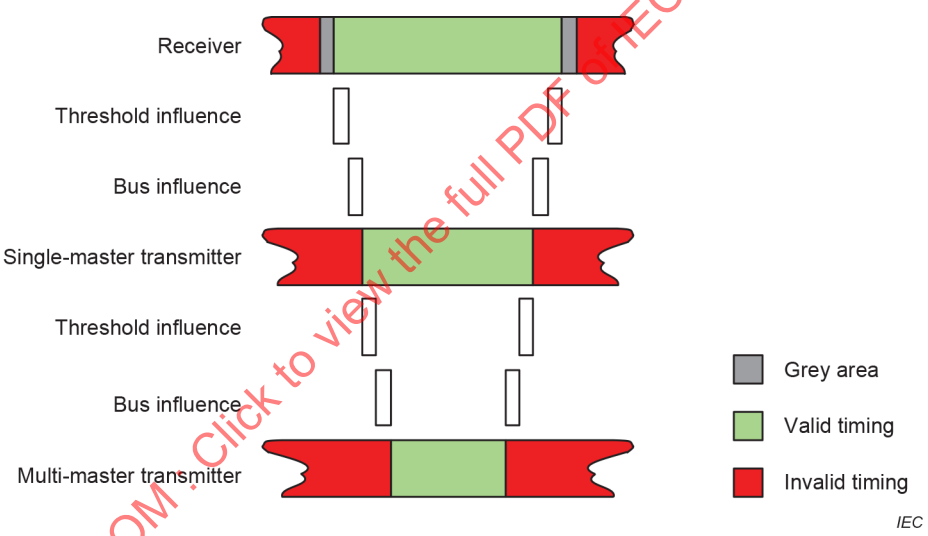

Figure A.7 – Transmitter and receiver timing illustration

A.5 Maximum current consumption calculation explanation

A.5.1 Single bus power supply

A bus power supply is characterized by two current values, its maximum supply current and its guaranteed supply current, as illustrated in Figure A.8.

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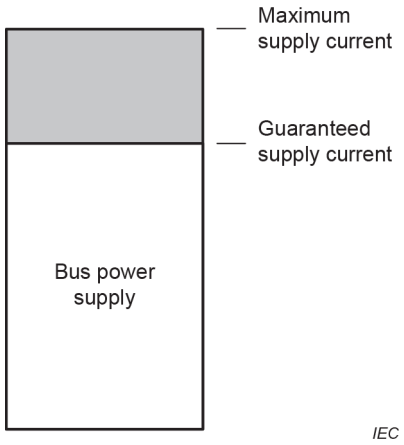

Figure A.8 – Bus power supply current values

The minimum guaranteed supply current is the parameter which ensures that the power supply is sufficient for the combined current demand of all bus units connected. Figure A.9 illustrates that the sum of current demand of all bus units connected should be less than or equal to the minimum guaranteed supply current.

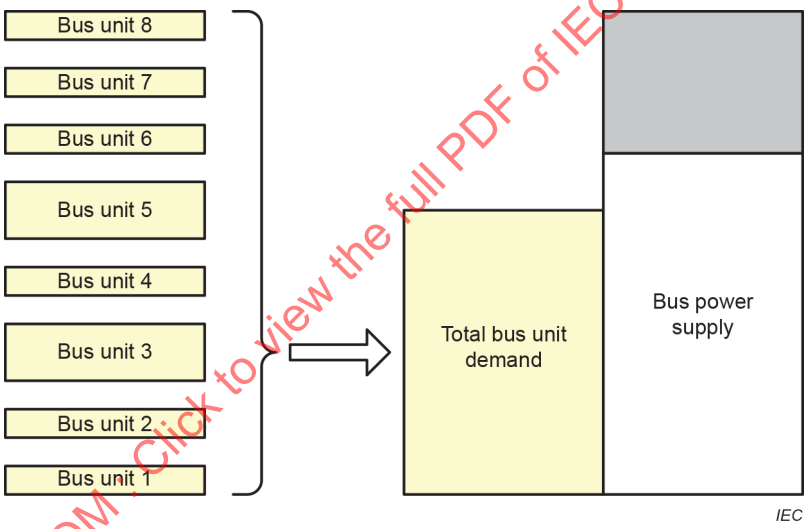

Figure A.9 – Current demand coverage

The maximum supply current is limited to 250 mA as specified in 6.5.

A.5.2 Multiple bus power supplies

When the current demand of the bus units connected is greater than the guaranteed supply current of a single bus power supply, more than one bus power supply can be used. In this case the sum of their guaranteed supply currents covers the current demand of the system.

When selecting bus power supplies for a system, the sum of the maximum supply currents can be up to the system limit of 250 mA. Figure A.10 illustrates the situation with four bus power supplies.

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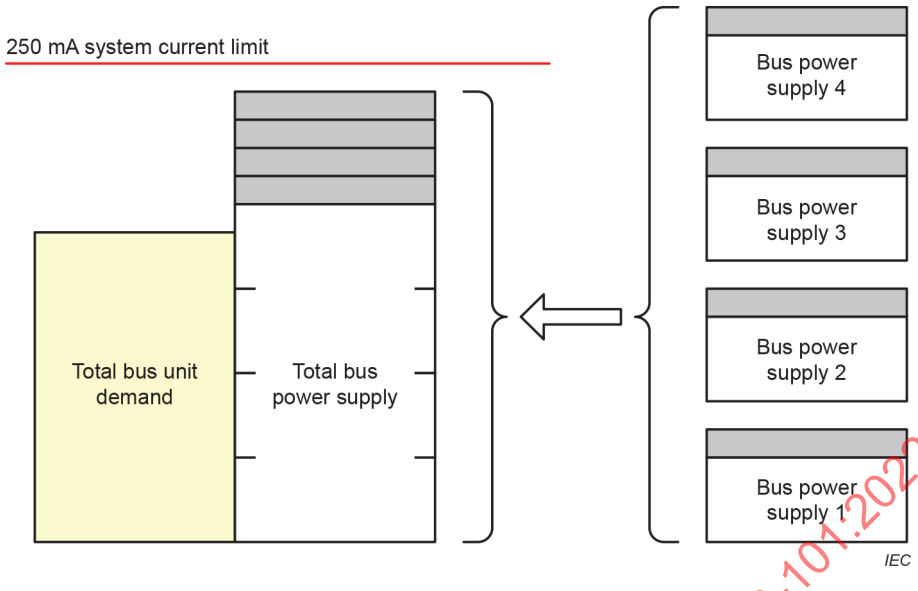

Figure A.10 – Combination of four bus power supplies

A.5.3 Redundant bus power supplies

In some cases a second bus power supply can be connected to the bus for reliability reasons. Thus each of them is capable of covering the complete current demand on its own. If one power supply fails, the current demand can still be covered by the remaining bus power supply.

In such a configuration it is especially important to check that the sum of all maximum currents does not exceed the normative general limit of 250 mA.

Figure A.11 illustrates the situation when using redundant bus power supplies.

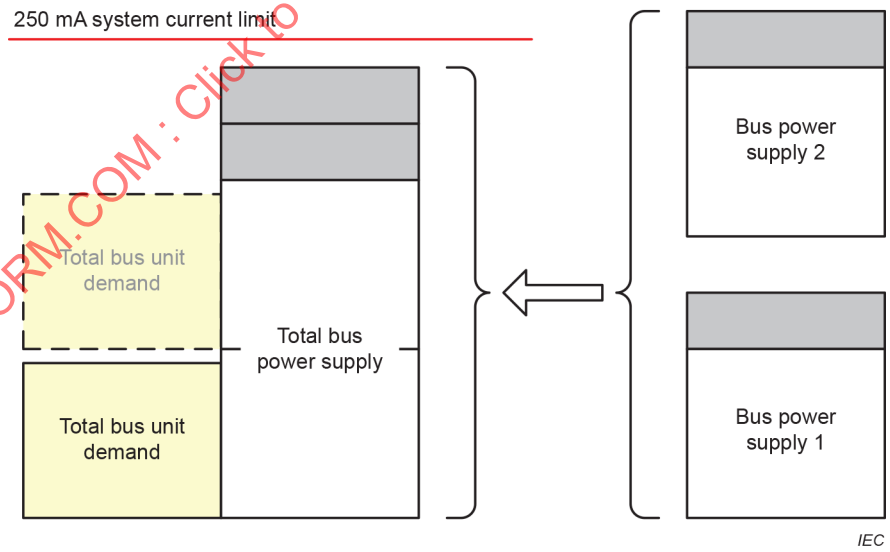

Figure A.11 – Redundant bus power supplies

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A.6 Communication layer overview

A.6.1 General

Table A.2 shows where the specific layers of the open systems interconnection (OSI) communication layer model are handled in different parts of the IEC 62386 series. The ISO/OSI layers are defined in ISO/IEC 7498-1.

Table A.2 – OSI layer model of the IEC 62386 series

OSI layer	Meaning	Description
7 Application	Application specific	Part 102: Instructions and queries for control gear Parts 2xx: Application extended instructions and queries for control gear Part 103: Instructions, queries and event messages to/from control devices Part 104: Instructions and queries for wireless and alternative wired system components Part 105: Instructions and queries for bus units supporting firmware transfer Parts 3xx: Control device specific instructions, queries and event messages
6 Presentation	Meaning of codes	Part 102: Address encoding, instruction and query encoding, backward frame encoding in control gear Part 103: Address encoding, instruction and query encoding, backward frame encoding in control devices Part 104: Address encoding, instruction and query encoding, backward frame encoding for wireless and alternative wired system components Part 105: Address encoding, instruction and query encoding, backward frame encoding in bus units supporting firmware transfer
5 Session	Request /response	Part 102 and Part 103: Query (16-bit/24-bit forward frame)/Response (8-bit backward frame)
4 Transport	Control transaction	Partially supported through transactions
3 Network	Resolve addresses	First 8 bits of each forward frame: Part 102: 64 short addresses, 16 group addresses, broadcast Part 103: 64 short addresses, 32 control groups, 32 instance groups, 32 instance types, broadcast Part 103: System addresses
2 Data link	Secure telegram	Partially supported through start-stop-framing and fixed length of frames
1 Physical	Bit level	Part 101: • voltage levels, rise/fall time, frame sequence timing, timing tolerances, timing violations • frame types: 16-bit forward frames, 24-bit forward frames, 20-bit reserved forward frames, 32-bit forward frames, 8-bit backward frames • Manchester encoding, start bit, stop condition, frame size violations • media access rules: collision detection, avoidance and recovery Part 104: • Supported physical layers for wireless and alternative wired system components

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A.6.2 Physical layer

The physical layer is based on a definition of allowed expected bit numbers and Manchester Code checking inside the specified tolerances (IEC 62386-101).

A.6.3 Data link layer

The data link layer checks the quality of data received at the logical layer. The IEC 62386 series ensures data link quality through Manchester Code violation detection, fixed telegram length, start-stop-framing, and bit number checking only. The absence of cyclic redundancy check (CRC) checking is a compromise necessary for simplicity and efficient use of the available bandwidth.

A.6.4 Network layer

The network layer defines logical addressing of devices. IEC 62386-102 defines 16-bit forward frame addressing and IEC 62386-103 defines 24-bit forward frame addressing formats. A bus unit needs to determine which of the two address spaces is applicable by checking the length of the frames received.

A.6.5 Transport layer

The transport layer ensures data transmission. Within the IEC 62386 series, data transmission is checked through session layer commands, the principle of operation for this master-responder communication system.

A.6.6 Session layer

The session layer defines the request/response mechanism (IEC 62386-102 and IEC 62386-103).

A.6.7 Presentation layer

The presentation layer defines format classes for data, commands and special commands (IEC 62386-102, IEC 62386-103 and IEC 62386-105).

A.6.8 Application layer

The application layer defines application specific codes and data formats (IEC 62386-102, IEC 62386-103, IEC 62386-104, IEC 62386-105, IEC 62386-2xx series, IEC 62386-3xx series).

A.7 Effects of combining version number 1 and version number 2.y devices

Table A.3 shows the effects of replacing or adding a certain edition device (given vertically) in a system formed by devices of the same edition (given horizontally), where minor version number y is currently in the range of 0 to 1.

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Table A.3 – Effects of combining version number 1 and version number 2.y devices

	Version 1 system	**Version 2.y single-master system**	**Version 2.y multi-master system**
Version 1 control gear	Usually it works but there can be trouble due to incorrect specified timing	Usually it works but there can be trouble due to new specified timing, commands or behaviour	Usually it works but there can be trouble due to new specified timing, commands or behaviour
Version 1 control device	Usually it works but there can be trouble due to incorrect specified timing	The entire system will behave as a version 1 single-master system	Combination is not possible (multi-master controllers are not defined in version 1)
Version 2.y control gear	Usually it works but there can be trouble due to incorrect specified timing and minor issues can occur when memory banks are used	Combination is possible	Combination is possible
Version 2.y single-master controller	The entire system will behave as a version 2.y single-master system, as long as only 102 version 1 commands are used	Combination is possible	Combination is not possible (single-master controllers are not meant to be used in a multi-master system)
Version 2.y multi-master controller	The entire system will behave as a version 2.y multi-master system, as long as only 102 version 1 commands are used	Combination is possible	Combination is possible
Version 1 bus power supply	Combination is possible	Combination is possible	The combination is not guaranteed due to new specified timing or behaviour
Version 2.y bus power supply	Combination is possible	Combination is possible	Combination is possible

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Annex B
(informative)

Touch current

The touch current of the interface, as specified in 4.9.4, is current I_1 in Figure B.1 and Figure B.2.

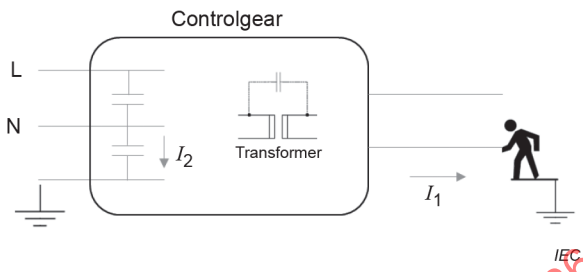

Figure B.1 – Touch current from a bus unit

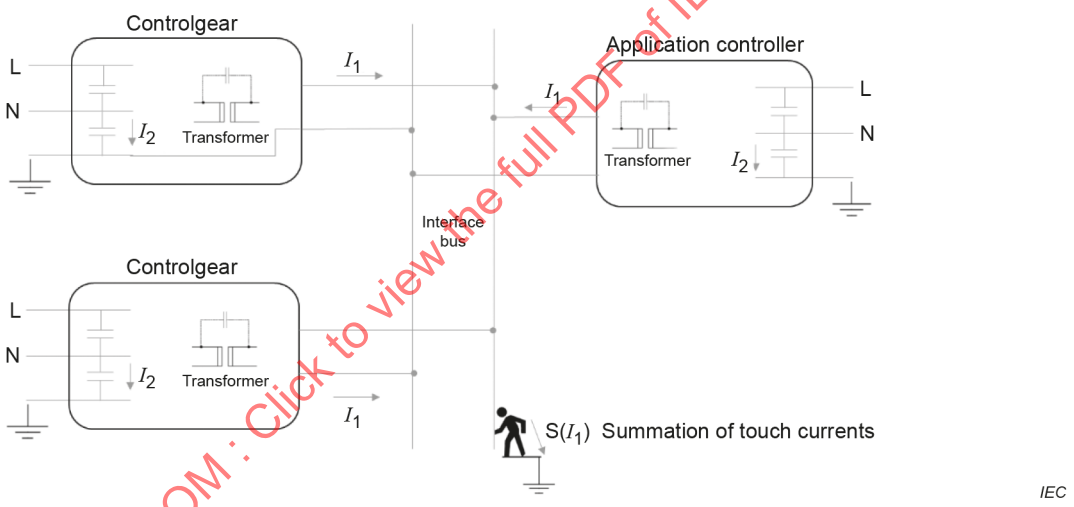

Figure B.2 – Summation of touch currents from several bus units

The summation of touch current is specified in IEC TS 63117.

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COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

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INTERFACE D'ÉCLAIRAGE ADRESSABLE NUMÉRIQUE –

Partie 101: Exigences générales – Composants de système

AVANT-PROPOS

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Cette troisième édition annule et remplace la seconde édition parue en 2014 et l'Amendement 1:2018. Cette édition constitue une révision technique.

Cette édition inclut les modifications techniques majeures suivantes par rapport à l'édition précédente:

a) le domaine d'application a été mis à jour;

b) les paragraphes relatifs à la sécurité et à la mise à la terre ont été mis à jour et élargis;

c) les références ont été mises à jour;

d) l'utilisation de l'alimentation du bus et de l'alimentation externe a été clarifiée;

e) la sensibilité à la polarité des bus, y compris l'alimentation électrique du bus, a été mise à jour;

f) les tailles de trames de 32 bits ne sont plus réservées.

Le texte de cette Norme internationale est issu des documents suivants:

Projet	Rapport de vote
34/947/FDIS	34/988/RVD

Le rapport de vote indiqué dans le tableau ci-dessus donne toute information sur le vote ayant abouti à son approbation.

La langue employée pour l'élaboration de cette Norme internationale est l'anglais.

Ce document a été rédigé selon les Directives ISO/IEC, Partie 2, il a été développé selon les Directives ISO/IEC, Partie 1 et les Directives ISO/IEC, Supplément IEC, disponibles sous www.iec.ch/members_experts/refdocs. Les principaux types de documents développés par l'IEC sont décrits plus en détail sous www.iec.ch/standardsdev/publications.

La présente Partie 101 de l'IEC 62386 est destinée à être utilisée conjointement avec:

- la Partie 102, qui contient les exigences générales pour le type de produit applicable (appareillage de commande), et avec la Partie 2xx (exigences particulières pour l'appareillage de commande) appropriée;
- la Partie 103, qui contient les exigences générales pour le type de produit applicable (dispositifs de commande), et avec la Partie 3xx (exigences particulières pour les dispositifs de commande) appropriée;
- la Partie 104, qui contient les exigences générales pour les composants de système à connexion alternative ou sans fil;
- la Partie 105, qui contient les exigences particulières relatives au transfert du microprogramme pour les appareillages et dispositifs de commande.

Une liste de toutes les parties de la série IEC 62386, publiées sous le titre général *Interface d'éclairage adressable numérique*, se trouve sur le site web de l'IEC.

Le comité a décidé que le contenu de ce document ne sera pas modifié avant la date de stabilité indiquée sur le site web de l'IEC sous webstore.iec.ch dans les données relatives au document recherché. À cette date, le document sera

- reconduit,
- supprimé,
- remplacé par une édition révisée, ou
- amendé.

IMPORTANT – Le logo "colour inside" qui se trouve sur la page de couverture de cette publication indique qu'elle contient des couleurs qui sont considérées comme utiles à une bonne compréhension de son contenu. Les utilisateurs devraient, par conséquent, imprimer cette publication en utilisant une imprimante couleur.

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INTRODUCTION

L'IEC 62386 est composée de plusieurs parties, appelées série. La série IEC 62386 spécifie un système à bus pour la commande par des signaux numériques des appareils d'éclairage électroniques. La série IEC 62386-1xx inclut les spécifications de base. La Partie 101 contient les exigences générales relatives aux composants de système, la Partie 102 étend ces informations avec les exigences générales relatives aux appareillages de commande et la Partie 103 étend ces informations avec les exigences générales relatives aux dispositifs de commande. Les Parties 104 et 105 peuvent s'appliquer à l'appareillage de commande ou aux dispositifs de commande. La Partie 104 fournit les exigences relatives aux composants de système à connexion alternative ou sans fil. La Partie 105 décrit le transfert du microprogramme. La Partie 150 fournit les exigences concernant une alimentation électrique auxiliaire qui peut être autonome ou intégrée aux appareillages de commande ou aux dispositifs de commande.

La série IEC 62386-2xx étend les exigences générales relatives aux appareillages de commande aux extensions spécifiques aux lampes (principalement pour la rétrocompatibilité avec l'Edition 1 de l'IEC 62386) et aux caractéristiques spécifiques aux appareillages de commande.

La série IEC 62386-3xx étend les exigences générales relatives aux dispositifs de commande aux extensions spécifiques aux dispositifs d'entrée décrivant les types d'instances, ainsi que certaines caractéristiques communes qui peuvent être combinées à plusieurs types d'instances.

Cette troisième édition de l'IEC 62386-101 est destinée à être utilisée conjointement avec l'IEC 62386-102 et avec les différentes parties qui composent la série IEC 62386-2xx relative aux appareillages de commande, ainsi qu'avec l'IEC 62386-103 et les différentes parties qui composent la série IEC 62386-3xx, qui spécifie des exigences particulières relatives aux dispositifs de commande. La présentation en parties publiées séparément facilitera les futurs amendements et révisions. Des exigences supplémentaires seront ajoutées en fonction des besoins identifiés.

La structure des normes est représentée sous forme de graphique à la Figure 1 ci-dessous.

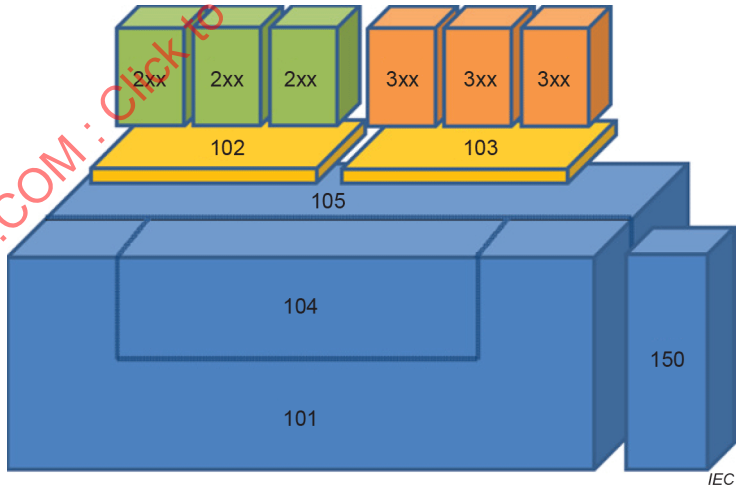

Figure 1 – Vue d'ensemble de l'IEC 62386

La présente partie de l'IEC 62386, tout en faisant référence à un article quelconque des autres parties de la série IEC 62386-1xx, spécifie la mesure dans laquelle un article s'applique. Les autres parties contiennent également des exigences supplémentaires, s'il y a lieu.

Tous les nombres utilisés dans le présent document sont des nombres décimaux, sauf indication contraire. Les nombres hexadécimaux sont donnés dans le format 0xVV, où VV est la valeur. Les nombres binaires sont donnés dans le format XXXXXXXb ou dans le format XXXX XXXX, où X est 0 ou 1; "x" dans les nombres binaires signifie que "la valeur n'a pas d'influence".

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INTERFACE D'ÉCLAIRAGE ADRESSABLE NUMÉRIQUE –

Partie 101: Exigences générales – Composants de système

1 Domaine d'application

La présente partie de l'IEC 62386 s'applique aux composants de système dans un système à bus pour la commande par des signaux numériques des appareils d'éclairage électroniques.

Les méthodes et algorithmes de commande et les méthodes d'échange de données des contrôleurs d'application utilisés pour la commande d'éclairage ne relèvent pas du domaine d'application de la série IEC 62386. Les exigences relatives à la compatibilité électromagnétique (CEM) ne relèvent pas du domaine d'application de la série IEC 62386.

2 Références normatives

Les documents suivants sont cités dans le texte de sorte qu'ils constituent, pour tout ou partie de leur contenu, des exigences du présent document. Pour les références datées, seule l'édition citée s'applique. Pour les références non datées, la dernière édition du document de référence s'applique (y compris les éventuels amendements).

IEC 61347-1:2015, *Appareillages de lampes – Partie 1: Exigences générales et exigences de sécurité*
IEC 61347-1:2015/AMD1:2017

IEC 62386-102:2022, *Interface d'éclairage adressable numérique – Partie 102: Exigences générales – Appareillages de commande*

IEC 62386-103:2022, *Interface d'éclairage adressable numérique – Partie 103: Exigences générales – Dispositifs de commande*

IEC 62386-104, *Interface d'éclairage adressable numérique – Partie 104: Exigences générales – Composants de système à connexion alternative ou sans fil*

IEC 62386-105, *Interface d'éclairage adressable numérique – Partie 105: Exigences particulières pour appareillages et dispositifs de commande – Transfert du microprogramme*

IEC 62386-2xx (toutes les parties), *Interface d'éclairage adressable numérique – Partie 2xx: Exigences particulières pour les appareillages de commande*

IEC 62386-3xx (toutes les parties), *Interface d'éclairage adressable numérique – Partie 3xx: Exigences particulières pour les dispositifs de commande*

IEC 61000-4-11, *Compatibilité électromagnétique (CEM) – Partie 4-11: Techniques d'essai et de mesure – Essais d'immunité aux creux de tension, coupures brèves et variations de tension pour les appareils à courant d'entrée inférieur ou égal à 16 A par phase*

IEC 60664-1, *Coordination de l'isolement des matériels dans les réseaux d'énergie électrique à basse tension – Partie 1: Principes, exigences et essais*

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IEC 60990:2016, *Méthodes de mesure du courant de contact et du courant dans le conducteur de protection*

IEC 61643-11, *Parafoudres basse tension – Partie 11: Parafoudres connectés aux systèmes basse tension – Exigences et méthodes d'essai*

3 Termes et définitions

Pour les besoins du présent document, les termes et définitions suivants s'appliquent.

L'ISO et l'IEC tiennent à jour des bases de données terminologiques destinées à être utilisées en normalisation, consultables aux adresses suivantes:

- IEC Electropedia: disponible à l'adresse http://www.electropedia.org/
- ISO Online browsing platform: disponible à l'adresse http://www.iso.org/obp

3.1
état actif
phase de la tension de niveau bas au cours d'une transmission

Note 1 à l'article: Le bruit et les impulsions brèves peuvent être ignorés et ne modifient donc pas l'état.

3.2
alimentation électrique avancée du bus
alimentation électrique du bus capable de vérifier les conditions de défaut sur le bus avant de mettre en marche sa sortie en continu

Note 1 à l'article: Le raccordement de la tension secteur au bus ou le court-circuit du bus sont des exemples de conditions de défaut.

3.3
contrôleur d'application
dispositif de commande raccordé au bus et qui envoie des commandes afin de commander les dispositifs d'entrée et/ou l'appareillage de commande raccordés au même bus

3.4
trame en arrière
trame utilisée pour la transmission en arrière

3.5
transmission en arrière
transmission de données en réponse à et déclenchée par une transmission en avant

3.6
bus
ligne de connexion à deux fils qui transporte de l'énergie électrique et des trames

3.7
alimenté par le bus
fourniture de l'énergie de fonctionnement par le bus

3.8
mise hors tension du bus
coupure de l'alimentation du bus de plus de 45 ms

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3.9
coupure de l'alimentation du bus
situation anormale où la tension du bus est dans la plage de tensions de niveau bas du récepteur, et non due à la présence d'un émetteur actif

3.10
alimentation électrique du bus
unité qui fournit au bus une énergie électrique définie

3.11
unité de bus
unité logique ou combinaison d'unités logiques, qui contient un émetteur et, en option, un récepteur

Note 1 à l'article: Voir 4.6.6.

3.12
dépassement de charge
produit du temps de dépassement du courant et de l'amplitude de dépassement du courant

3.13
collision
situation dans laquelle deux émetteurs ou plus émettent simultanément

Note 1 à l'article: Les collisions peuvent passer inaperçues si le cadencement de la transmission est suffisamment similaire et le contenu des trames transmises est identique.

3.14
commande
transmission en avant avec une quantité d'information appropriée, destinée à provoquer une réaction chez le récepteur

Note 1 à l'article: Un récepteur, après avoir décodé une commande, peut, le cas échéant, décider d'ignorer la commande.

Note 2 à l'article: Se reporter à l'IEC 62386-102, à l'IEC 62386-103, à l'IEC 62386-104, à l'IEC 62386-105, à la série IEC 62386-2xx et à la série IEC 62386-3xx pour les définitions des commandes.

3.15
dispositif de commande
dispositif raccordé au bus et qui envoie des commandes à d'autres dispositifs raccordés au même bus

Note 1 à l'article: Les dispositifs de commande peuvent aussi recevoir des commandes et des transmissions en arrière. Les dispositifs de commande peuvent contenir des contrôleurs d'application et/ou des dispositifs d'entrée.

3.16
appareillage de commande
dispositif raccordé au bus et qui reçoit des commandes afin de commander au moins une sortie de manière directe ou indirecte

Note 1 à l'article: L'appareillage de commande de lampe décrit dans l'IEC 61347-1 peut couvrir les appareillages de commande.

3.17
temps de dépassement du courant
temps par bit pendant lequel le courant fourni par l'alimentation électrique du bus est supérieur à la valeur maximale admise de 250 mA, après un passage de l'état de repos à l'état actif

Note 1 à l'article: Voir 6.5.4.

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3.18
zone de destruction
créneau temporel où une trame valide ne peut être assurée

3.19
front
passage de l'état actif à l'état de repos ou inversement

3.20
message d'événement
commande envoyée par un dispositif de commande en vue de diffuser des informations sur le bus

3.21
alimentation externe
fourniture de l'énergie de fonctionnement par une alimentation électrique distincte

Note 1 à l'article: L'alimentation électrique distincte peut être le secteur, un système d'alimentation en courant continu, etc.

3.22
trame en avant
trame utilisée pour la transmission en avant

3.23
priorité de trame en avant
propriété d'une trame en avant qui sert à prioriser l'accès au bus

3.24
transmission en avant
transmission de données initiée par un dispositif de commande

Note 1 à l'article: Voir aussi 3.5.

3.25
trame
ensemble de bits consécutifs suivis d'un état d'arrêt

Note 1 à l'article: Voir Article 8 pour la définition du cadencement d'un état d'arrêt.

3.26
zone grisée
créneau temporel qui contient le point de décision qui sépare les créneaux temporels adjacents

Note 1 à l'article: Une zone grisée indique que la décision est arbitraire. En général, il convient d'utiliser comme action l'entrée précédente ou suivante dans un tableau. Voir Article 8 pour de plus amples informations.

3.27
état de repos
phase de tension de niveau haut entre et pendant les transmissions

Note 1 à l'article: Le bruit et les impulsions brèves peuvent être ignorés et ne modifient donc pas l'état.

3.28
dispositif d'entrée
dispositif de commande raccordé au bus et qui envoie des commandes à l'aide d'un émetteur à plusieurs maîtres, afin de diffuser des informations sur les actions des utilisateurs et/ou les valeurs des capteurs

Note 1 à l'article: Les dispositifs d'entrée ne transmettent pas de commandes à l'appareillage de commande.

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3.29
instance
unité de traitement des signaux d'un dispositif d'entrée

3.30
instruction
commande transmise pour modifier une ou plusieurs variables dans une unité de bus

3.31
alimentation électrique intégrée du bus
alimentation électrique du bus intégrée dans un dispositif physique qui contient également une unité de bus

3.32
interface
bornes ou fils destinés à être raccordés au bus

3.33
unité logique
appareillage de commande ou dispositif de commande qui est conforme à l'IEC 62386-102 ou à l'IEC 62386-103

Note 1 à l'article: Voir 4.6.6.

3.34
contrôleur d'application à plusieurs maîtres
contrôleur d'application capable de partager le bus avec d'autres dispositifs de commande et qui utilise un émetteur à plusieurs maîtres

3.35
émetteur à plusieurs maîtres
émetteur qui suit le cadencement à plusieurs maîtres et prend en charge la détection de collisions, l'évitement de collisions et les méthodes de récupération en cas de collision

Note 1 à l'article: Les émetteurs à plusieurs maîtres sont utilisés dans les dispositifs de commande destinés aux systèmes de commande à plusieurs maîtres.

3.36
trame en avant propriétaire
trame en avant destinée à des usages propres au fabricant

3.37
requête
commande transmise pour observer une variable dans une unité de bus

Note 1 à l'article: Une requête peut être suivie d'une trame en arrière.

3.38
récepteur
partie d'une unité de bus qui détecte et décode des trames sur le bus

3.39
réservé
destiné à une utilisation ultérieure

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3.40
commande double envoi
commande transmise par les trames en avant double envoi

Note 1 à l'article: Se reporter au 9.4, à l'IEC 62386-102, à l'IEC 62386-103, à la série IEC 62386-2xx et à la série IEC 62386-3xx pour plus de détails sur les commandes double envoi.

3.41
trame en avant double envoi
trame en avant qui nécessite d'être transmise deux fois avec une durée d'établissement limitée, en vue d'être traitée par le récepteur

3.42
durée d'établissement
temps pendant lequel le bus est à l'état de repos après le dernier front montant d'une trame et avant le premier front descendant de la trame suivante

3.43
contrôleur d'application à un seul maître
contrôleur d'application qui n'est pas tenu d'utiliser un émetteur à plusieurs maîtres

Note 1 à l'article: Cela implique qu'aucun autre contrôleur d'application, ni aucun autre dispositif d'entrée avec messages d'événement activés, ne peut être connecté au bus.

3.44
trame en avant normalisée
trame en avant définie et décrite dans la série IEC 62386

3.45
défaillance système
coupure de l'alimentation du bus de plus de 550 ms

3.46
transaction
ensemble ininterruptible d'une ou de plusieurs trames en avant consécutives transmises par un seul dispositif de commande, sans aucune trame en arrière ou avec plusieurs trames en arrière

3.47
émetteur
partie d'une unité de bus qui place les trames sur le bus

3.48
temps de dépassement de la tension
temps par bit pendant lequel la tension fournie par l'alimentation électrique du bus est supérieure à 20,5 V après un passage de l'état actif à l'état de repos

Note 1 à l'article: Voir 6.5.4.

3.49
temps de sous-dépassement de la tension
temps par bit pendant lequel la tension fournie par l'alimentation électrique du bus est inférieure à 12,0 V après un passage de l'état actif à l'état de repos

Note 1 à l'article: Voir 6.5.4.

3.50
trame acceptée
trame reçue qui utilise le type de trames et le contenu de bit de données adéquats

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3.51
trame ignorée
trame reçue, mais non acceptée

3.52
trame reçue
trame avec un bit de départ et des bits de données valides, et un état d'arrêt

3.53
trame rejetée
trame non reçue

3.54
TBTF
très basse tension fonctionnelle
TBT dans un circuit prévu à des fins fonctionnelles et ne satisfaisant pas aux exigences de TBTS (ou de TBTP)

Note 1 à l'article: La TBTF présente une isolation principale par rapport à la BT.

Note 2 à l'article: Un circuit TBTF présente des risques en cas de contact.

[SOURCE: IEC 60598-1:2020, 1.2.42.1, modifié – Les Notes à l'article ont été ajoutées.]

4 Généralités

4.1 Objet

La normalisation de l'interface d'éclairage adressable numérique vise à assurer un fonctionnement multifournisseur interopérable sous le niveau de systèmes de gestion d'immeubles.

L'Annexe A donne des informations supplémentaires concernant les systèmes.

NOTE La série IEC 63044 et l'ISO/IEC 14762 ne s'appliquent pas pour les besoins de la présente série IEC 62386. La série IEC 63044 peut s'appliquer aux contrôleurs d'application s'ils sont destinés à être utilisés comme systèmes électroniques pour les foyers domestiques et les bâtiments (HBES) et comme systèmes de gestion technique du bâtiment (SGTB).

4.2 Numéro de version

La version doit se présenter sous le format "x.y", où le numéro de version principale x se situe dans la plage comprise entre 0 et 62 et le numéro de version secondaire y se situe dans la plage comprise entre 0 et 2. Lorsque le numéro de version est codé par octet, le numéro de version principale x doit se situer dans les bits 7 à 2 et le numéro de version secondaire y doit se situer dans les bits 1 à 0.

À chaque amendement d'une édition de l'IEC 62386-101, le numéro de version secondaire doit être augmenté de un.

Lors d'une nouvelle édition de l'IEC 62386-101, le numéro de version principale doit être augmenté de un et le numéro de version secondaire doit être égal à 0.

Le numéro de version actuel est "3.0".

NOTE Les documents IEC font généralement l'objet de deux amendements avant toute nouvelle édition.

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4.3 Structure et architecture de système

Un système doit être constitué des composants répertoriés dans le Tableau 1.

Tableau 1 – Composants de système

Composant	Grandeur	Pour plus d'informations, voir
Alimentation électrique du bus	≥ 1	Article 6
Appareillages de commande	≥ 0	IEC 62386-102
Contrôleur d'application	≥ 1	IEC 62386-103
Dispositifs d'entrée	≥ 0	IEC 62386-103
Bus	1	4.8 et Article A.2

Dans un système, toutes les unités de bus ainsi que les alimentations électriques du bus sont raccordées en parallèle au bus.

NOTE En conséquence, toutes les trames sont visibles pour toutes les alimentations électriques, tous les appareillages de commande et tous les dispositifs de commande sur le bus.

La Figure 2 représente un exemple de structure de système.

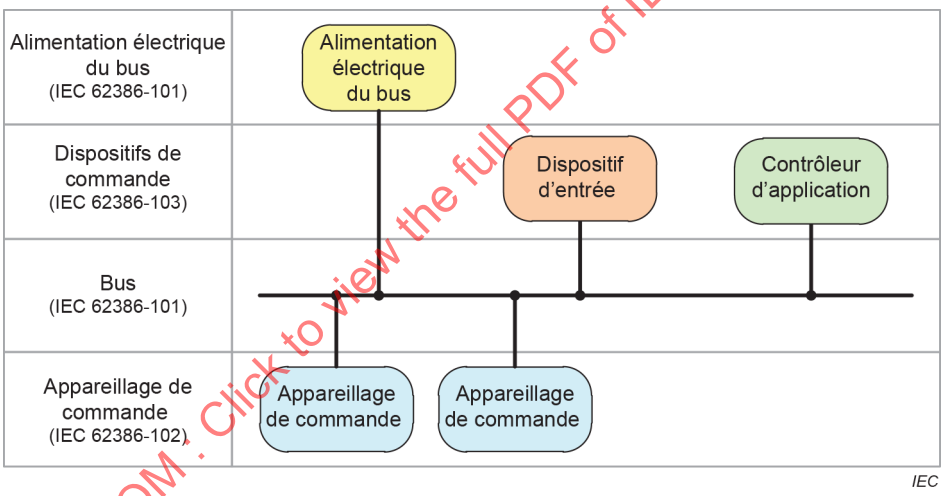

Figure 2 – Exemple de structure de système

Voir 4.8 pour des informations détaillées sur le câblage et l'Article A.2 pour des informations sur les architectures possibles de système.

4.4 Flux d'informations du système

La Figure 3 représente les différents types de trames qui sont utilisés pour la communication entre les unités de bus dans un système. Une trame en arrière n'est toujours transmise qu'en réponse à une trame en avant.

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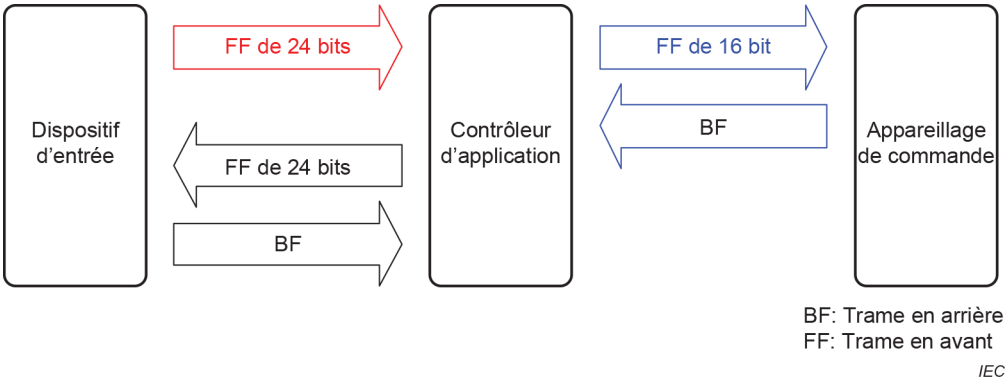

Figure 3 – Communication entre les unités de bus (exemple)

Un flux direct d'informations d'un dispositif d'entrée à un appareillage de commande n'est pas autorisé. Outre les communications représentées à la Figure 3, pour le transfert du microprogramme (IEC 62386-105), les contrôleurs d'application peuvent émettre des trames en avant de 32 bits et les trois unités de bus représentées peuvent recevoir des trames en avant de 32 bits. Les contrôleurs d'application à plusieurs maîtres peuvent également être des émetteurs de trames en arrière de 8 bits.

NOTE Un exemple de système conforme au présent document peut être constitué uniquement d'un contrôleur d'application et d'appareillages de commande; voir A.2.4. Dans un tel système, l'entrée de l'utilisateur ne donne pas lieu à des trames en avant de 24 bits sur le bus.

4.5 Types de commandes

Les unités de bus conformes au présent document doivent utiliser, pour la communication, les différents types de commandes suivants:

- messages d'événement;
- instructions; et
- requêtes.

NOTE Voir les autres parties de la série IEC 62386 pour plus de détails sur les messages d'événement, les instructions et les requêtes.

4.6 Unités de bus

4.6.1 Émetteurs et récepteurs dans les unités de bus

Le Tableau 2 fournit un récapitulatif des différents récepteurs et émetteurs autorisés pour chaque unité de bus. Il n'est pas admis qu'une unité de bus émette ou reçoive d'autres trames que celles indiquées dans le Tableau 2, à l'exception des trames en avant propriétaires. Voir 7.4 pour les détails des différents types de trames.

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Tableau 2 – Émetteurs et récepteurs dans les unités de bus

<table>
<tr><th>Unité de bus</th><th>Récepteur de</th><th colspan="2">Émetteur de</th></tr>
<tr><td rowspan="2">Appareillages de commande</td><td>Trames en avant de 32 bits</td><td colspan="2" rowspan="2">Trames en arrière, suivant les exigences de cadencement à un seul maître[a]</td></tr>
<tr><td>Trames en avant de 16 bits</td></tr>
<tr><td rowspan="2">Dispositif d'entrée</td><td>Trames en avant de 32 bits</td><td>Trames en avant de 24 bits</td><td rowspan="5">Suivant les exigences de cadencement à plusieurs maîtres</td></tr>
<tr><td>Trames en avant de 24 bits</td><td>Trames en arrière[a]</td></tr>
<tr><td rowspan="4">Contrôleur d'application à plusieurs maîtres</td><td>Trames en avant de 32 bits</td><td>Trames en avant de 32 bits</td></tr>
<tr><td>Trames en avant de 24 bits</td><td>Trames en avant de 24 bits</td></tr>
<tr><td>Trames en avant de 16 bits[b]</td><td>Trames en avant de 16 bits</td></tr>
<tr><td>Trames en arrière</td><td>Trames en arrière[a]</td></tr>
<tr><td>Contrôleur d'application à un seul maître</td><td>Trames en arrière[c]</td><td colspan="2">Trames en avant de 16 bits, suivant les exigences de cadencement à un seul maître[d]</td></tr>
</table>

[a] Aucune méthode de détection de collisions ou d'évitement de collisions ne doit être appliquée aux transmissions des trames en arrière.

[b] Applicable seulement lorsque le contrôleur d'application à plusieurs maîtres est capable de traiter les trames en avant de 16 bits transmises par d'autres contrôleurs d'application.

[c] Exigé seulement si le contrôleur d'application à un seul maître utilise des adressages ou des requêtes.

[d] Un contrôleur d'application à un seul maître peut également envoyer des trames de 24 bits en cas d'interrogation des dispositifs d'entrée, ainsi que des trames en avant de 32 bits.

4.6.2 Appareillages de commande

Un appareillage de commande doit être conforme au présent document ainsi qu'à l'IEC 62386-102 et aux parties applicables de la série IEC 62386-2xx.

Il doit comprendre un récepteur pour les trames en avant de 16 bits et un émetteur pour la transmission des trames en arrière. L'émetteur de trames en arrière doit satisfaire aux exigences de cadencement applicables à un émetteur à un seul maître défini en 8.1 et ne doit pas mettre en œuvre la détection de collisions ou la récupération en cas de collision. Il peut comprendre un récepteur pour les trames en avant de 32 bits.

4.6.3 Dispositif d'entrée

Un dispositif d'entrée doit être conforme au présent document ainsi qu'à l'IEC 62386-103 et aux parties applicables de la série IEC 62386-3xx.

Il doit contenir un émetteur à plusieurs maîtres suivant les exigences de cadencement de l'émetteur à plusieurs maîtres définies en 8.3 pour transmettre des trames en avant de 24 bits. Il doit également comprendre un émetteur pour la transmission des trames en arrière. L'émetteur de trames en arrière doit satisfaire aux exigences de cadencement applicables à un émetteur à plusieurs maîtres et ne doit pas mettre en œuvre la détection de collisions ou la récupération en cas de collision.

NOTE Même s'ils sont logiquement des objets distincts, l'émetteur à plusieurs maîtres et l'émetteur de trames en arrière peuvent partager le même matériel.

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Un dispositif d'entrée doit comporter un récepteur pour recevoir des trames en avant de 24 bits transmises par d'autres dispositifs de commande. Il peut comprendre un récepteur pour les trames en avant de 32 bits.

4.6.4 Contrôleur d'application à un seul maître

Un contrôleur d'application à un seul maître doit être conforme au présent document et à l'IEC 62386-103.

Il doit contenir un émetteur suivant les exigences de cadencement de l'émetteur définies en 8.1 pour transmettre des trames en avant.

NOTE En général, cependant, un contrôleur d'application à un seul maître contient également un récepteur pour recevoir des trames en arrière transmises par l'appareillage de commande.

Pour communiquer avec l'appareillage de commande, un contrôleur d'application à un seul maître doit utiliser les commandes définies dans l'IEC 62386-102 et, le cas échéant, dans les parties applicables de la série IEC 62386-2xx.

4.6.5 Contrôleur d'application à plusieurs maîtres

Un contrôleur d'application à plusieurs maîtres doit être conforme au présent document et à l'IEC 62386-103.

Il doit contenir un émetteur à plusieurs maîtres suivant les exigences de cadencement de l'émetteur à plusieurs maîtres définies en 8.3 pour transmettre des trames en avant. Il doit également comprendre un émetteur pour la transmission des trames en arrière. L'émetteur de trames en arrière doit satisfaire aux exigences de cadencement applicables à un émetteur à plusieurs maîtres et ne doit pas mettre en œuvre la détection de collisions ou la récupération en cas de collision. Il doit comprendre un récepteur pour recevoir des trames en arrière ainsi que des trames en avant transmises par d'autres dispositifs de commande. Il peut comprendre un récepteur pour les trames en avant de 32 bits. Il ne doit pas transmettre de trames en arrière en réponse à des trames en avant de 16 bits.

Pour communiquer avec l'appareillage de commande, un contrôleur d'application à plusieurs maîtres doit utiliser les commandes définies dans l'IEC 62386-102 et, le cas échéant, dans les parties applicables de la série IEC 62386-2xx. Pour communiquer avec les dispositifs de commande, il doit utiliser les commandes définies dans l'IEC 62386-103 et, le cas échéant, dans les parties applicables de la série IEC 62386-3xx. Le cas échéant, un contrôleur d'application à plusieurs maîtres doit utiliser les commandes définies dans l'IEC 62386-105 pour effectuer le transfert du microprogramme vers l'appareillage de commande et les dispositifs de commande.

NOTE Un contrôleur d'application à plusieurs maîtres peut également recevoir et traiter les trames en avant de 16 bits transmises par d'autres contrôleurs d'application et/ou réagir aux requêtes.

4.6.6 Partage d'une interface

Plusieurs unités logiques peuvent partager une même interface physique. La Figure 4 représente un exemple où n unités logiques et une alimentation électrique du bus partagent l'interface physique.

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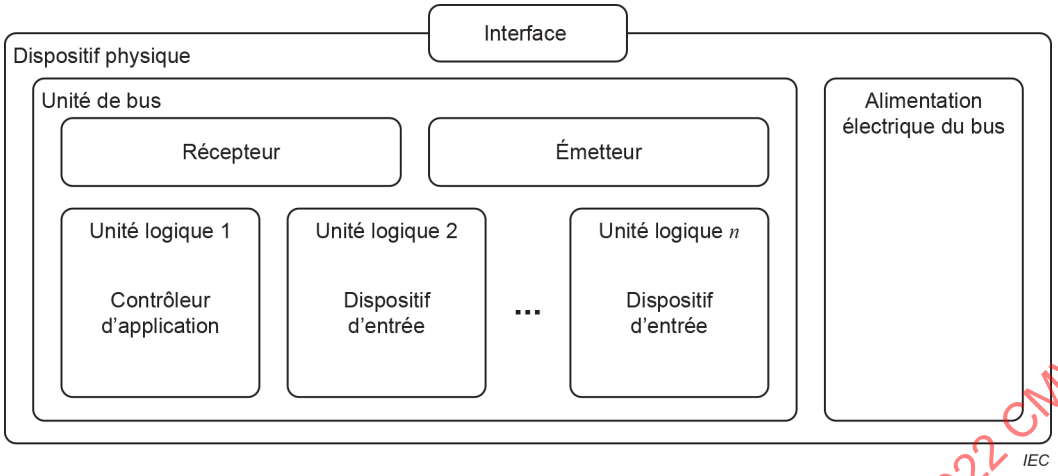

Figure 4 – Exemple d'une interface partagée

Un contrôleur d'application peut être intégré dans une unité de bus qui contient également un dispositif d'entrée, avec à la fois le contrôleur d'application et le dispositif d'entrée qui partagent la même interface physique. Une unité de bus de ce type doit prendre en charge une commande pour désactiver le contrôleur d'application, permettant ainsi d'utiliser l'unité de bus de la même façon que si elle ne contenait que le dispositif d'entrée.

4.6.7 Énergie de fonctionnement

Les unités de bus doivent être alimentées uniquement par le bus ou alimentées uniquement par une source externe, ou satisfaire à l'un des deux cas suivants:

- l'unité de bus est configurable entre une alimentation par le bus et une alimentation externe, la configuration ne devant pas être automatique selon la présence ou l'absence de l'alimentation, et que l'unité de bus satisfait aux conditions suivantes:
  - la connexion ou le retrait de l'alimentation externe ou de l'alimentation électrique du bus ne doit pas entraîner de changement de fonctionnement entre l'alimentation par le bus et l'alimentation externe; et
  - elle satisfait aux exigences des unités de bus alimentées par le bus lorsqu'elle est configurée comme étant alimentée par le bus et satisfait aux exigences des unités de bus avec alimentation externe lorsqu'elle est configurée comme étant alimentée par une source externe; et
  - la modification de la source d'alimentation configurée ne modifie aucune fonctionnalité décrite dans toute partie de la série IEC 62386, sauf en raison d'exigences différentes entre les unités de bus alimentées par le bus et les unités de bus avec alimentation externe;
- l'unité de bus est alimentée par le bus, utilise une alimentation externe uniquement en cas de comportement non spécifié dans toute partie de la série IEC 62386, et satisfait aux exigences des parties de la série IEC 62386 mises en œuvre avec l'alimentation externe déconnectée.

NOTE 1 Un exemple d'unité de bus configurable entre l'alimentation par le bus et l'alimentation externe est un capteur qui peut tirer un courant relativement élevé quand il est alimenté par le bus, ce qui limite le nombre de ces dispositifs qui peuvent être connectés au bus, ou qui peut être configuré pour être alimenté par une source externe et permettre ainsi plus de dispositifs sur le bus.

NOTE 2 Un exemple d'unité de bus alimentée par le bus, mais qui utilise une alimentation externe uniquement en cas de comportement non spécifié dans toute partie de la série IEC 62386, est un tableau à boutons-poussoirs alimenté par le bus avec un rétroéclairage qui fonctionne uniquement lorsqu'une alimentation externe est connectée.

NOTE 3 Un exemple d'unité de bus qui ne satisfait pas à ces exigences est un appareillage de commande à LED alimenté par le bus qui nécessite un deuxième dispositif pour alimenter les LED, le deuxième dispositif étant alimenté par une source externe. Un autre exemple est un gradateur à modulation de largeur d'impulsion alimenté par le bus qui nécessite une alimentation externe de 24 V en courant continu pour sa sortie (le gradateur peut être plutôt alimenté par l'alimentation externe de 24 V en courant continu).

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4.7 Alimentation électrique du bus et calculs de la charge

4.7.1 Couverture de la demande de courant

Dans un système, la somme de la consommation de courant de toutes les unités de bus, quand elles ne sont pas en transmission (voir 5.5, Tableau 10), ne doit pas dépasser la somme du courant d'alimentation garanti de toutes les alimentations du bus (voir 6.5.1, Tableau 13). Voir aussi Article A.5.

Le courant complémentaire est nécessaire lors de la transmission pour alimenter les processus dynamiques tels que les capacités de charge au sein du système.

$$\sum I_{\text{Unité de bus}} + I_{\text{Processus dynamiques}} \leq \sum I_{\text{Alimentation garantie}}$$

Il n'existe pas d'équation universellement valide pour calculer le courant nécessaire pour les processus dynamiques, puisque ce courant dépend du câblage du système et de la structure du système.

4.7.2 Conformité du courant de signal maximal

La somme du courant d'alimentation maximal de toutes les alimentations électriques du bus connectées au bus ne doit jamais dépasser 250 mA.

$$\sum I_{\text{Alimentation garantie}} \leq \sum I_{\text{Alimentation maximale}} \leq 250\ \text{mA}$$

4.7.3 Simplification des calculs dans le système

Pour un système constitué d'une seule alimentation électrique du bus, d'unités de bus alimentées par le bus et de n unités de bus avec alimentation externe, par exemple, un appareillage de commande, la simplification suivante est recommandée:

$$2\ \text{mA} \times n_{\text{Unités de bus avec alimentation externe}} + \sum I_{\text{Unités de bus alimentés par le bus}} \leq \frac{I_{\text{Alimentation garantie}}}{1{,}2}$$

Le facteur 1,2 est une approximation et prend en compte un courant complémentaire de 20 % nécessaire aux processus dynamiques.

4.8 Câblage

4.8.1 Structure du câblage

Il convient que le câblage du bus soit connecté dans une topologie en étoile, une topologie linéaire ou une combinaison des deux. Le câblage ne doit pas être réalisé dans une structure en anneau. Les deux conducteurs qui servent de bus doivent être placés dans le même câble ou conduit à câble. Les deux conducteurs doivent être côte à côte dans le câble ou conduit à câble, afin d'éviter tout couplage intempestif avec d'autres signaux.

NOTE En fonction des directives d'installation locales et des exigences d'isolation, les deux conducteurs peuvent être placés dans le même câble que les conducteurs de l'alimentation secteur.

4.8.2 Spécification du câblage

Outre les effets transitoires lors de la transmission, à tout moment pendant le fonctionnement du système, la tension aux bornes de l'interface de tout dispositif ne doit pas s'écarter de plus de 2,0 V de la tension aux bornes de l'interface de chacun, sans exception, des autres dispositifs connectés au bus. Voir aussi A.1 pour plus de détails.

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NOTE 1 La chute de tension dépend de la somme des courants d'alimentation de toutes les alimentations électriques, de la résistance spécifique des conducteurs et de la longueur du câblage.

NOTE 2 Cette exigence peut limiter la longueur totale du câblage au sein du système.

4.9 Exigences de sécurité électrique

4.9.1 Généralités

Le présent 4.9 décrit les exigences de sécurité supplémentaires pour la mise en œuvre de l'interface d'éclairage adressable numérique, en plus des exigences de sécurité du produit indiquées dans la norme de sécurité de produit pertinente.

4.9.2 Isolation

Le câblage du bus et l'interface doivent être considérés comme un réseau ou un circuit TBTF.

NOTE 1 Cela signifie que les systèmes autres que TBTF ne sont pas couverts par le présent document.

L'interface doit disposer d'au moins l'isolation principale exigée pour au moins une tension secteur en courant alternatif de 230 V, ou la tension de service du produit, si celle-ci est plus élevée, conformément à l'IEC 60664-1.

NOTE 2 Ce niveau de tension s'applique par exemple à l'isolation principale entre le circuit d'interface et le secteur ou à l'isolation supplémentaire entre le câblage du bus et les parties conductrices accessibles de l'interface utilisateur.

Si la tension de service dépasse 230 V en courant alternatif (valeur efficace), et si cette tension de service peut être appliquée sur l'interface en cas de condition de premier défaut, alors un avertissement qui indique que la tension de service est supérieure à 230 V en courant alternatif (valeur efficace) doit être inclus dans le manuel, et il est également recommandé de l'inscrire sur le produit.

NOTE 3 La tension de service est définie dans l'IEV 581-21-19. Généralement, il ne s'agit pas de la tension secteur.

L'isolation entre le secteur et l'interface doit être conçue pour la catégorie de surtension (OVC, *OverVoltage Category*) applicable, définie dans l'IEC 60664-1, et ne doit pas être inférieure à OVC II.

NOTE 4 Si le câblage du bus, lorsqu'il est installé, est susceptible d'être soumis à des tensions de choc supérieures à OVC II, l'application de mesures supplémentaires sur le bus peut être envisagée, par exemple une protection contre les tensions de choc ou l'utilisation de produits conçus pour une OVC plus élevée. Cela peut être lié au fait que le câblage du bus se trouve en partie à l'extérieur.

4.9.3 Rigidité diélectrique

Les exigences de l'Article 12 de l'IEC 61347-1:2015 s'appliquent, en remplaçant le terme "appareillage de lampe" par le terme "unité de bus".

La valeur utilisée pour la tension de service doit être au moins égale à 230 V en courant alternatif, ou la tension de service du produit, si celle-ci est plus élevée.

Le dispositif de protection contre les surtensions (SPD) doit être déconnecté s'il est conforme à l'IEC 61643-11, lors de la réalisation des essais d'isolation et de rigidité diélectrique.

4.9.4 Limitation du courant de contact entre le dispositif et le bus

Le courant de contact doit être limité à 0,5 mA en valeur efficace.

Le courant de contact doit être mesuré à l'aide du réseau de mesure décrit à la Figure 4 de l'IEC 60990:2016.

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La valeur du courant de contact doit être mise à disposition dans la documentation du produit par le fabricant du produit.

L'Annexe B donne des informations supplémentaires sur le courant de contact.

NOTE L'utilisation du terme "courant de contact" n'indique pas que l'interface peut être touchée.

4.10 Mise à la terre du bus

Les bornes de l'interface ne doivent pas être connectées à la terre, sauf dans les situations suivantes:

- un dispositif qui comporte une alimentation électrique du bus avec un courant d'alimentation maximal de 250 mA, lorsqu'il est admis de connecter la borne négative de l'interface à la terre;
- par l'intermédiaire d'un condensateur connecté à la terre, comme cela est décrit en 5.3 ou 6.3.

NOTE Des courants intempestifs provoqués par plusieurs connexions du circuit à la terre de protection peuvent causer des incendies dans le câblage du bus. La mise à la terre peut aussi enfreindre les exigences de sécurité relatives à certains luminaires.

4.11 Coupures d'alimentation dans les unités de bus

4.11.1 Différents niveaux de coupures d'alimentation

Le Tableau 3 et le Tableau 4 indiquent les différents niveaux de coupures d'alimentation dans les unités de bus.

Tableau 3 – Cadencement de coupure de l'alimentation électrique externe

Valeur minimale	Type	Valeur maximale	Description
		200 ms	Coupures de courte durée de l'alimentation électrique externe[a]
> 200 ms		< 5 s	Zone grisée
5 s			Cycle d'alimentation externe[b]
[a] Voir 4.11.2. [b] Voir 4.11.3.			

Tableau 4 – Cadencement de coupure de l'alimentation électrique du bus

Valeur minimale	Type	Valeur maximale	Description
		40 ms	Coupures de courte durée de l'alimentation électrique du bus[a]
> 40 ms		< 45 ms	Zone grisée
45 ms			Mise hors tension du bus[b]
> 450 ms		< 550 ms	Zone grisée pour la défaillance système
550 ms			Défaillance système[b]
[a] Voir 4.11.4. [b] Voir 4.11.5.			

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4.11.2 Coupures de courte durée de l'alimentation électrique externe

Les exigences données en 4.11 s'appliquent aux unités de bus en régime permanent sans communication sur le bus.

NOTE 1 Le régime permanent implique par exemple que le dispositif a terminé sa mise sous tension et qu'il est prêt pour le fonctionnement prévu, sans aucune modification de la sortie en cours.

Les essais fonctionnels relatifs aux coupures d'alimentation de courte durée doivent être effectués à l'aide de méthodes et d'équipements d'essai conformes à l'IEC 61000-4-11 à la tension d'alimentation électrique minimale spécifiée, avec les niveaux de tension d'essai indiqués dans le Tableau 5. Pour l'alimentation en courant alternatif, le décalage de la tension doit se produire au passage par zéro.

Tableau 5 – Coupures d'alimentation de courte durée

	Niveaux d'essai
Niveau de tension d'essai 1	70 %
Niveau de tension d'essai 2	0 %
Nombre de périodes sous alimentation en courant alternatif	10
Durée de coupure sous alimentation en courant continu	200 ms

Un changement d'état peut se produire lors de la coupure de l'alimentation électrique. Après la coupure de l'alimentation électrique, l'unité de bus doit être dans le même état qu'avant la coupure, ou doit être rétablie dans cet état dans les 30 min.

NOTE 2 Le délai de 30 min est choisi pour prendre en compte le long temps de réamorçage de certains types de lampes.

4.11.3 Cycle d'alimentation externe

Après un cycle d'alimentation externe (voir Tableau 3), une unité de bus avec alimentation externe doit appliquer un comportement sous tension à toutes les unités logiques de façon simultanée. Lors d'un cycle d'alimentation externe, une unité de bus peut toujours éventuellement répondre aux commandes.

NOTE Le comportement sous tension est défini dans l'IEC 62386-102 et l'IEC 62386-103.

4.11.4 Coupures de courte durée de l'alimentation électrique du bus

Les unités de bus ne doivent pas interpréter les brèves coupures de 40 ms au maximum de l'alimentation du bus comme une mise hors tension.

NOTE Cela implique que les coupures de courte durée de l'alimentation du bus ne déclenchent pas le comportement sous tension.

Les essais relatifs aux coupures de courte durée de l'alimentation électrique du bus doivent être effectués à la tension minimale de l'alimentation électrique du bus.

4.11.5 Mise hors tension du bus

Une unité de bus alimentée par le bus peut interpréter une mise hors tension du bus comme un cycle d'alimentation externe (voir 4.11.1). Elle doit interpréter une défaillance système comme un cycle d'alimentation externe. Le cycle d'alimentation externe et le comportement sous tension correspondant doivent s'appliquer à toutes les unités logiques simultanément. Voir Tableau 4.

NOTE Le comportement sous tension est défini dans l'IEC 62386-102 et l'IEC 62386-103.

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4.11.6 Cadencement du démarrage du système

Après la mise sous tension par une source externe, l'alimentation électrique du bus doit être capable de fournir le courant d'alimentation garanti donné dans le Tableau 13, après au plus tard le temps de démarrage de l'alimentation électrique du bus spécifié dans le Tableau 6.

Un récepteur doit être prêt à recevoir des trames dans le temps de démarrage maximal du récepteur spécifié dans le Tableau 6.

Un émetteur ou un émetteur à plusieurs maîtres ne doit pas démarrer les transmissions plus tôt que le temps de démarrage de l'émetteur spécifié dans le Tableau 6.

Tableau 6 – Cadencement du démarrage

	Valeur minimale	Type	Valeur maximale	Condition
Temps de démarrage de l'alimentation électrique du bus			250 ms	Courant d'alimentation garanti atteint
Temps de démarrage de l'alimentation électrique avancée du bus			400 ms	
Temps de démarrage de l'alimentation électrique intégrée du bus			400 ms [a]	
			5 s [b]	
Temps de démarrage du récepteur pour des unités de bus avec alimentation externe, après un cycle d'alimentation externe			450 ms [e]	
Temps de démarrage du récepteur pour des unités de bus avec alimentation externe, après mise hors tension du bus			100 ms	U = 10 V [d]
Temps de démarrage du récepteur pour des unités de bus alimentées par le bus, après mise hors tension du bus			1 200 ms	
Temps de démarrage de l'émetteur	110 ms [c]			
Temps de démarrage de l'émetteur à plusieurs maîtres	110 ms			

[a] Applicable si d'autres alimentations électriques du bus sont autorisées dans le système.

[b] Applicable si aucune autre alimentation électrique du bus n'est autorisée dans le système.

[c] Non applicable pour les émetteurs des unités de bus qui ne peuvent pas déterminer l'état du bus.

[d] État de repos, tension du bus mesurée au niveau de l'interface de l'unité de bus.

[e] Si un cycle d'alimentation externe s'est produit et l'alimentation du bus n'est pas disponible dans les 350 ms, le cadencement de 100 ms est applicable.

La Figure 5 représente un exemple de cadencement du démarrage du système.

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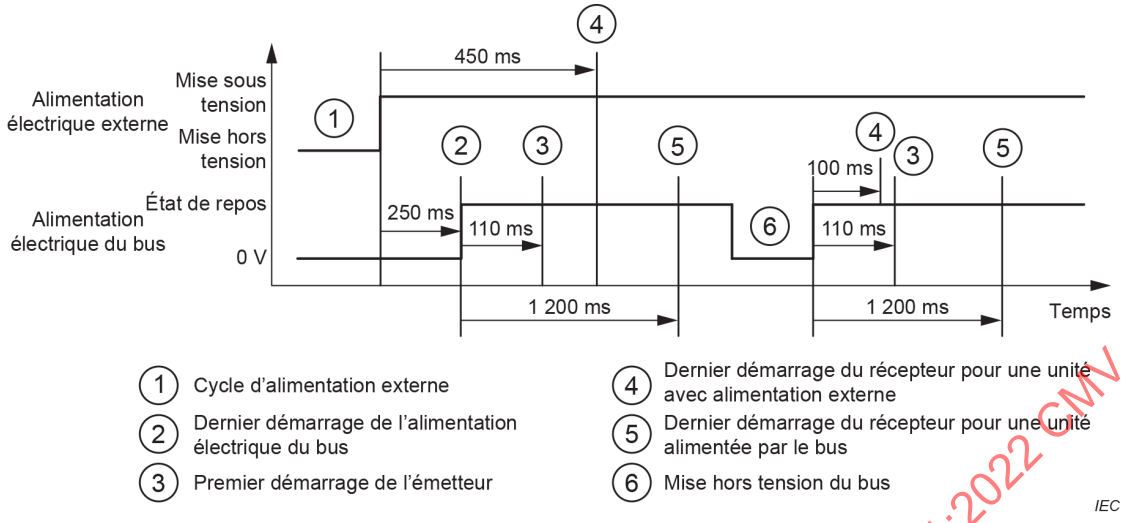

Figure 5 – Exemple de cadencement du démarrage

NOTE En se fondant sur les dispositions du 4.11.6, un émetteur peut alors émettre alors que tous les récepteurs ne sont pas encore prêts à recevoir.

5 Spécifications électriques

5.1 Généralités

Toutes les tensions et tous les courants se rapportent à l'interface de l'unité de bus.

L'interface de commande doit être insensible à la polarité, sauf si une alimentation électrique du bus est intégrée. Si l'alimentation électrique intégrée du bus est commutable, la sensibilité à la polarité est admise pour les deux états de l'alimentation électrique du bus (activée et désactivée).

La protection contre les surtensions est facultative, mais recommandée pour la tension assignée la plus élevée du système. En l'absence de protection contre les surtensions, il est recommandé que la conception assure un fonctionnement sûr en cas d'application de la tension secteur à l'interface.

5.2 Marquage de l'interface

L'interface doit porter le marquage "da" ou "DA" (pour *data*, données) sur l'unité de bus. Si le codage couleur est utilisé, les couleurs qui représentent le "da" ou "DA doivent figurer sur l'unité de bus.

S'il y a plus d'une interface, un marquage supplémentaire doit être utilisé pour permettre de distinguer les interfaces les unes des autres.

5.3 Condensateurs entre l'interface et la terre

Si des condensateurs sont connectés entre le circuit d'interface et toute autre partie du dispositif, telle que la terre, ils doivent être connectés par la partie négative du signal d'interface redressé. De tels condensateurs doivent satisfaire aux exigences d'isolation données en 4.9.

NOTE La capacité constatée sur le bus est influencée par la capacité à la terre lorsqu'un condensateur connecté entre la partie négative de l'interface et la terre sur une unité de bus est utilisé avec une autre unité de bus qui comprend un condensateur connecté entre la partie positive de l'interface et la terre.

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5.4 Caractéristiques assignées de tension de signal

Les niveaux de tension dans le système pendant le fonctionnement normal doivent toujours être dans la plage de tensions nominales du système donnée dans le Tableau 7. Toutes les unités de bus ainsi que les alimentations électriques du bus doivent résister à la tension maximale absolue du système donnée dans le Tableau 7. Les essais doivent être effectués avec un courant de 260 mA pendant une durée de 1 s.

NOTE 1 Des tensions en dehors de la plage de tensions nominales du système peuvent survenir, par exemple à la suite d'oscillations parasites sur le bus.

Il est nécessaire que les dispositifs soient insensibles à la polarité (voir 5.1), ou que les alimentations électriques soient capables de supporter les tensions inverses (voir 9.7).

Tableau 7 – Niveaux de tension du système

	Valeur minimale	Type	Valeur maximale
Tension nominale du système U	0 V		20,5 V
Tension maximale absolue du système	0 V		22,5 V

Les niveaux de tension à l'interface du récepteur doivent être interprétés selon le Tableau 8.

Tableau 8 – Niveaux de tension du récepteur

	Valeur minimale	Type	Valeur maximale
Tension niveau haut	9,5 V		22,5 V
Tension de seuil	> 6,5 V	8,0 V	< 9,5 V
Tension niveau bas	0 V		6,5 V

Les niveaux de tension d'un émetteur doivent être ceux indiqués dans le Tableau 9.

Tableau 9 – Niveaux de tension de l'émetteur

	Valeur minimale	Type	Valeur maximale
Tension niveau bas	0 V		4,5 V
Tension niveau haut[a]	10,0 V [b]		22,5 V

[a] La tension de niveau haut n'est pas sous la commande d'un émetteur, mais est déterminée par l'alimentation électrique et son positionnement sur le bus.

[b] La valeur 10 V est dérivée de la tension d'alimentation électrique minimale de 12 V moins la chute de tension maximale de 2 V sur le bus.

5.5 Caractéristiques assignées de courant de signal

La relation entre le courant I_{BUS} et la tension U à l'interface de l'unité de bus doit être celle indiquée dans le Tableau 10.

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