

INTERNATIONAL STANDARD



**Universal serial bus interfaces for data and power –
Part 1-3: Universal Serial Bus interfaces – Common components – USB Type-
CTM cable and connector specification**



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Part 1-3: Universal Serial Bus interfaces – Common components – USB Type-C™ cable and connector specification

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Universal Serial Bus Type-C Cable and Connector Specification

Revision 1.1
April 3, 2015

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	PalCONN/PalNova (Palpilot International Corp.)	Toshiba Corporation

Revision History

Revision	Date	Description
1.0	August 11, 2014	Initial Release
1.1	April 3, 2015	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.

1 Introduction

With the continued success of the USB interface, there exists a need to adapt USB technology to serve newer computing platforms and devices as they trend toward smaller, thinner and lighter form-factors. Many of these newer platforms and devices are reaching a point where existing USB receptacles and plugs are inhibiting innovation, especially given the relatively large size and internal volume constraints of the Standard-A and Standard-B versions of USB connectors. Additionally, as platform usage models have evolved, usability and robustness requirements have advanced and the existing set of USB connectors were not originally designed for some of these newer requirements. This specification is to establish a new USB connector ecosystem that addresses the evolving needs of platforms and devices while retaining all of the functional benefits of USB that form the basis for this most popular of computing device interconnects.

1.1 Purpose

This specification defines the USB Type-C™ receptacles, plug and cables.

The USB Type-C Cable and Connector Specification is guided by the following principles:

- Enable new and exciting host and device form-factors where size, industrial design and style are important parameters
- Work seamlessly with existing USB host and device silicon solutions
- Enhance ease of use for connecting USB devices with a focus on minimizing user confusion for plug and cable orientation

The USB Type-C Cable and Connector Specification defines a new receptacle, plug, cable and detection mechanisms that are compatible with existing USB interface electrical and functional specifications. This specification covers the following aspects that are needed to produce and use this new USB cable/connector solution in newer platforms and devices, and that interoperate with existing platforms and devices:

- USB Type-C receptacles, including electro-mechanical definition and performance requirements
- USB Type-C plugs and cable assemblies, including electro-mechanical definition and performance requirements
- USB Type-C to legacy cable assemblies and adapters
- USB Type-C-based device detection and interface configuration, including support for legacy connections
- USB Power Delivery optimized for the USB Type-C connector

The USB Type-C Cable and Connector Specification defines a standardized mechanism that supports Alternate Modes, such as repurposing the connector for docking-specific applications.

1.2 Scope

This specification is intended as a supplement to the existing [USB 2.0](#), [USB 3.1](#) and [USB Power Delivery](#) specifications. It addresses only the elements required to implement and support the USB Type-C receptacles, plugs and cables.

Normative information is provided to allow interoperability of components designed to this specification. Informative information, when provided, may illustrate possible design implementations.

1.3 Related Documents

USB 2.0 *Universal Serial Bus Revision 2.0 Specification*

This includes the entire document release package.

<http://www.usb.org/developers/docs>

USB 3.1 *Universal Serial Bus Revision 3.1 Specification*

This includes the entire document release package.

<http://www.usb.org/developers/docs>

USB PD *USB Power Delivery Specification, Revision 2.0, August 11, 2014*

<http://www.usb.org/developers/docs>

USB BB *USB Billboard Device Class Specification, Revision 1.0, August 11, 2014*

<http://www.usb.org/developers/docs>

USB BC *Battery Charging Specification, Revision 1.2 (including errata and ECNs through March 15, 2012), March 15, 2012*

<http://www.usb.org/developers/docs>

1.4 Conventions

1.4.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

1.4.2 Keywords

The following keywords differentiate between the levels of requirements and options.

1.4.2.1 Informative

Informative is a keyword that describes information with this specification that intends to discuss and clarify requirements and features as opposed to mandating them.

1.4.2.2 May

May is a keyword that indicates a choice with no implied preference.

1.4.2.3 N/A

N/A is a keyword that indicates that a field or value is not applicable and has no defined value and shall not be checked or used by the recipient.

1.4.2.4 Normative

Normative is a keyword that describes features that are mandated by this specification.

1.4.2.5 Optional

Optional is a keyword that describes features not mandated by this specification. However, if an optional feature is implemented, the feature shall be implemented as defined by this specification (optional normative).

1.4.2.6 Reserved

Reserved is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this specification and, unless otherwise stated, shall not be utilized or adapted by vendor implementation. A reserved bit, byte, word, or field shall be set to zero by the sender and shall be ignored by the receiver. Reserved field values shall not be sent by the sender and, if received, shall be ignored by the receiver.

1.4.2.7 Shall

Shall is a keyword indicating a mandatory (normative) requirement. Designers are mandated to implement all such requirements to ensure interoperability with other compliant Devices.

1.4.2.8 Should

Should is a keyword indicating flexibility of choice with a preferred alternative. Equivalent to the phrase “it is recommended that”.

1.4.3 Numbering

Numbers that are immediately followed by a lowercase “b” (e.g., 01b) are binary values. Numbers that are immediately followed by an uppercase “B” are byte values. Numbers that are immediately followed by a lowercase “h” (e.g., 3Ah) are hexadecimal values. Numbers not immediately followed by either a “b”, “B”, or “h” are decimal values.

1.5 Terms and Abbreviations

Term	Description
Accessory Mode	A reconfiguration of the connector based on the presence of Rd/Rd or Ra/Ra on CC1/CC2, respectively.
Active cable	An Electronically Marked Cable with additional electronics to condition the data path signals.
Alternate Mode	Operation defined by a vendor or standards organization that is associated with a SVID assigned by the USB-IF. Entry and exit into and from an Alternate Mode is controlled by the USB PD Structured VDM Enter Mode and Exit Mode commands.
Audio Adapter Accessory Mode	The Accessory Mode defined by the presence of Ra/Ra on CC1/CC2, respectively. See A.
BFSK	Binary Frequency Shift Keying used for USB PD communication over VBUS.
BMC	Biphase Mark Coding used for USB PD communication over the CC wire.
Captive cable	A cable that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end.
CC	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
Debug Accessory Mode	The Accessory Mode defined by the presence of Rd/Rd on CC1/CC2, respectively. See B.
Default VBUS	VBUS voltage as defined by the USB 2.0 and USB 3.1 specifications. Note: where used, 5 V connotes the same meaning.
DFP	Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources VBUS and VCONN, and supports data. A charge-only DFP port only sources VBUS.
Direct connect	The host's DFP is connected directly with no USB hub in between, either via a cable or without (e.g., thumb drive), to the device's UFP.
DRP	The acronym used in this specification to refer to a USB port that can operate as either a Source or a Sink. The role that the port offers may be fixed to either a Source or Sink or may alternate between the two port states. Initially when operating as a Source, the port will also take on the role of a DFP and when operating as a Sink, the port will also take on the role of a UFP. The port's role may be changed dynamically either to reverse power or data roles.
DR_Swap	USB PD Data Role Swap.
Electronically Marked Cable	A USB Type-C cable that uses USB PD to provide the cable's characteristics.
Initiator	The port initiating a Vendor Defined Message. It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Initiator will be a host.
Passive cable	A cable that does not incorporate any electronics to condition the data path signals. A passive cable may or may not be electronically marked.
Port Partner	Refers to the port (device or host) a port is attached to.
Powered cable	A cable with electronics in the plug that requires VCONN indicated by the presence of Ra between the VCONN pin and ground.
PR_Swap	USB PD Power Role Swap.
Responder	The port responding to the Initiator of a Vendor Defined Message (VDM). It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Responder will be a device.
SBU	Sideband Use.
SID	A Standard ID (SID) is a unique 16-bit value assigned by the USB-IF to identify an industry standard.
Sink	Port asserting Rd on CC and consuming power from VBUS; most commonly a Device.
Source	Port asserting Rp on CC and providing power over VBUS; most commonly a Host or Hub DFP.

Term	Description
SVID	General reference to either a SID or a VID. Used by USB PD Structured VDMs when requesting SIDs and VIDs from a device.
Type-A	A general reference to all versions of USB “A” plugs and receptacles.
Type-B	A general reference to all versions of USB “B” plugs and receptacles.
Type-C Plug	A USB plug conforming to the mechanical and electrical requirements in this specification.
Type-C Port	The USB port associated to a USB Type-C receptacle. This includes the USB signaling, CC logic, multiplexers and other associated logic.
Type-C Receptacle	A USB receptacle conforming to the mechanical and electrical requirements of this specification.
UFP	Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks VBUS and supports data.
USB 2.0 Type-C Cable	A USB Type-C to Type-C cable that only supports USB 2.0 data operation. This cable does not include USB 3.1 or SBU wires.
USB 2.0 Type-C Plug	A USB Type-C plug specifically designed to implement the USB 2.0 Type-C cable.
USB Full-Featured Type-C Cable	A USB Type-C to Type-C cable that supports USB 2.0 and USB 3.1 data operation. This cable includes SBU wires.
USB Full-Featured Type-C Plug	A USB Type-C plug specifically designed to implement the USB Full-Featured Type-C cable.
VCONN-powered accessory	An accessory that is powered from VCONN to operate in an Alternate Mode.
VCONN_Swap	USB PD VCONN Swap.
VDM	Vendor Defined Message as defined by the USB PD specification.
VID	A Vendor ID (VID) is a unique 16-bit value assigned by the USB-IF to identify a vendor.
vSafe0V	VBUS “0 volts” as defined by the USB PD specification.
vSafe5V	VBUS “5 volts” as defined by the USB PD specification.

2 Overview

2.1 Introduction

The USB Type-C™ receptacle, plug and cable provide a smaller, thinner and more robust alternative to existing [USB 3.1](#) interconnect (Standard and Micro USB cables and connectors). This new solution targets use in very thin platforms, ranging from ultra-thin notebook PCs down to smart phones where existing Standard-A and Micro-AB receptacles are deemed too large, difficult to use, or inadequately robust. Some key specific enhancements include:

- The USB Type-C receptacle may be used in very thin platforms as its total system height for the mounted receptacle is under 3 mm
- The USB Type-C plug enhances ease of use by being plug-able in either upside-up or upside-down directions
- The USB Type-C cable enhances ease of use by being plug-able in either direction between host and devices

While the USB Type-C interconnect no longer physically differentiates plugs on a cable by being an A-type or B-type, the USB interface still maintains such a host-to-device logical relationship. Determination of this host-to-device relationship is accomplished through a [Configuration Channel](#) (CC) that is connected through the cable. In addition, the [Configuration Channel](#) is used to set up and manage power and Alternate/Accessory Modes.

Using the [Configuration Channel](#), the USB Type-C interconnect defines a simplified 5 volt VBUS-based power delivery and charging solution that supplements what is already defined in the [USB 3.1 Specification](#). More advanced power delivery and battery charging features over the USB Type-C interconnect are based on the [USB Power Delivery Specification](#). As a product implementation improvement, the USB Type-C interconnect shifts the [USB PD](#) communication protocol from being communicated over VBUS to being delivered across the USB Type-C [Configuration Channel](#).

The USB Type-C receptacle, plug and cable designs are intended to support future USB functional extensions. As such, consideration was given to frequency scaling performance, pin-out arrangement and the configuration mechanisms when developing this solution. The definition of future USB functional extensions is not in the scope of this specification but rather will be provided in future releases of the base USB Specification, i.e., beyond the existing [USB 3.1 Specification](#).

Figure 2-1 illustrates the comprehensive functional signal plan for the USB Type-C receptacle, not all signals shown are required in all platforms or devices. As shown, the receptacle signal list functionally delivers both [USB 2.0](#) (D+ and D-) and [USB 3.1](#) (TX and RX pairs) data buses, USB power (VBUS) and ground (GND), [Configuration Channel](#) signals (CC1 and CC2), and two Sideband Use (SBU) signal pins. Multiple sets of USB data bus signal locations in this layout facilitate being able to functionally map the USB signals independent of plug orientation in the receptacle. For reference, the signal pins are labeled.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 2-1 – USB Type-C Receptacle Interface (Front View)

Figure 2-2 illustrates the comprehensive functional signal plan for the USB Type-C plug. Only one CC pin is connected through the cable to establish signal orientation and the other CC pin is repurposed as VCONN for powering electronics in the USB Type-C plug. Also, only one set of [USB 2.0](#) D+/D- wires are implemented in a USB Type-C cable. For USB Type-C cables that only intend to support [USB 2.0](#) functionality, the [USB 3.1](#) and SBU signals are not implemented.

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	VCONN			SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Figure 2-2 – USB Full-Featured Type-C Plug Interface (Front View)

2.2 USB Type-C Receptacles, Plugs and Cables

Cables and connectors, including USB Type-C to USB legacy cables and adapters, are explicitly defined within this specification. These are the only connectors and cables that are authorized by the licensing terms of this specification. All licensed cables and connectors are required to comply with the compliance and certification requirements that are developed and maintained by the [USB-IF](#).

The following USB Type-C receptacles and plugs are defined.

- USB Type-C receptacle for [USB 2.0](#), [USB 3.1](#) and full-featured platforms and devices
- USB Full-Featured Type-C plug
- [USB 2.0](#) Type-C plug

The following USB Type-C cables are defined.

- USB Full-Featured Type-C cable with a USB Full-Featured Type-C plug at both ends for [USB 3.1](#) and full-featured applications
- [USB 2.0](#) Type-C cable with a [USB 2.0](#) Type-C plug at both ends for [USB 2.0](#) applications
- Captive cable with either a USB Full-Featured Type-C plug or [USB 2.0](#) Type-C plug at one end

All of the defined USB Type-C receptacles, plugs and cables support USB charging applications, including support for the optional USB Type-C-specific implementation of the [USB Power Delivery Specification](#) (See Section 4.6.2.4).

All USB Full-Featured Type-C cables are electronically marked. [USB 2.0](#) Type-C cables may be electronically marked. See Section 4.9 for the requirements of Electronically Marked Cables.

The following USB Type-C to USB legacy cables and adapters are defined.

- [USB 3.1](#) Type-C to Legacy Host cable with a USB Full-Featured Type-C plug at one end and a [USB 3.1](#) Standard-A plug at the other end – *this cable supports use of a USB Type-C-based device with a legacy USB host*
- [USB 2.0](#) Type-C to Legacy Host cable with a [USB 2.0](#) Type-C plug at one end and a [USB 2.0](#) Standard-A plug at the other end – *this cable supports use of a USB Type-C-based device with a legacy [USB 2.0](#) host (primarily for mobile charging and sync applications)*
- [USB 3.1](#) Type-C to Legacy Device cable with a USB Full-Featured Type-C plug at one end and a [USB 3.1](#) Standard-B plug at the other end – *this cable supports use of legacy [USB 3.1](#) hubs and devices with a USB Type-C-based host*
- [USB 2.0](#) Type-C to Legacy Device cable with a [USB 2.0](#) Type-C plug at one end and a [USB 2.0](#) Standard-B plug at the other end – *this cable supports use of legacy [USB 2.0](#) hubs and devices with a USB Type-C-based host*
- [USB 2.0](#) Type-C to Legacy Mini Device cable with a [USB 2.0](#) Type-C plug at one end and a [USB 2.0](#) Mini-B plug at the other end – *this cable supports use of legacy devices with a [USB 2.0](#) Type-C-based host*
- [USB 3.1](#) Type-C to Legacy Micro Device cable with a USB Full-Featured Type-C plug at one end and a [USB 3.1](#) Micro-B plug at the other end – *this cable supports use of legacy [USB 3.1](#) hubs and devices with a USB Type-C-based host*
- [USB 2.0](#) Type-C to Legacy Micro Device cable with a [USB 2.0](#) Type-C plug at one end and a [USB 2.0](#) Micro-B plug at the other end – *this cable supports use of legacy [USB 2.0](#) hubs and devices with a USB Type-C-based host*
- [USB 3.1](#) Type-C to Legacy Standard-A adapter with a USB Full-Featured Type-C plug at one end and a [USB 3.1](#) Standard-A receptacle at the other end – *this adapter supports use of a legacy USB “thumb drive” style device or a legacy USB ThinCard device with a [USB 3.1](#) Type-C-based host*
- [USB 2.0](#) Type-C to Legacy Micro-B adapter with a [USB 2.0](#) Type-C plug at one end and a [USB 2.0](#) Micro-B receptacle at the other end – *this adapter supports charging a USB Type-C-based mobile device using a legacy USB Micro-B-based chargers, either captive cable-based or used in conjunction with a legacy [USB 2.0](#) Standard-A to Micro-B cable*

Where implementations of USB Type-C to USB legacy cables are required to support [USB PD](#) BFSK-based communications, they shall do so by incorporating the required [USB PD](#) plug, incorporating the appropriate VBUS to ground decoupling capacitance, ensuring the VBUS wire is impedance controlled as specified in [USB PD](#), and complying with the cable requirements for the legacy connector end of the cable. USB Type-C to USB legacy adapters do not support [USB PD](#) BFSK-based communications.

USB Type-C receptacle to USB legacy adapters are explicitly not defined or allowed. Such adapters would allow many invalid and potentially unsafe cable connections to be constructed by users.

2.3 Configuration Process

The USB Type-C receptacle, plug and cable solution incorporates a configuration process to detect a downstream facing port to upstream facing port (DFP-to-UFP) connection for VBUS management and host-to-device connected relationship determination.

The configuration process is used for the following:

- DFP-to-UFP attach/detach detection
- Plug orientation/cable twist detection
- Initial DFP-to-UFP (host-to-device) and power relationships detection
- USB Type-C VBUS current detection and usage
- [USB PD](#) communication
- Discovery and configuration of functional extensions

Two pins on the USB Type-C receptacle, CC1 and CC2, are used for this purpose. Within a standard USB Type-C cable, only a single CC pin position within each plug of the cable is connected through the cable.

2.3.1 DFP-to-UFP Attach/Detach Detection

Initially, DFP-to-UFP attach is detected by a host or hub port (DFP) when one of the CC pins at its USB Type-C receptacle senses a specified resistance to GND. Subsequently, DFP-to-UFP detach is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer terminated to GND.

Power is not applied to the USB Type-C host or hub receptacle (VBUS or VCONN) until the DFP detects the presence of an attached device (UFP) port. When a DFP-to-UFP attach is detected, the DFP is expected to enable power to the receptacle and proceed to normal USB operation with the attached device. When a DFP-to-UFP detach is detected, the port sourcing VBUS removes power.

2.3.2 Plug Orientation/Cable Twist Detection

The USB Type-C plug can be inserted into a receptacle in either one of two orientations, therefore the CC pins enable a method for detecting plug orientation in order to determine which SuperSpeed USB data signal pairs are functionally connected through the cable. This allows for signal routing, if needed, within a DFP or UFP to be established for a successful connection.

2.3.3 Initial DFP-to-UFP (host-to-device) and Power Relationships Detection

Unlike existing USB Type-A and Type-B receptacles and plugs, the mechanical characteristics of the USB Type-C receptacle and plug do not inherently establish the relationship of USB

host and device ports. The CC pins on the receptacle also serve to establish an initial DFP-to-UFP and power relationships prior to the normal USB enumeration process.

For the purpose of defining how the CC pins are used to establish the initial DFP-to-UFP relationship, the following port behavior modes are defined.

- 1) Host-only – for this mode, the port exclusively behaves as a DFP
- 2) Device-only – for this mode, the port exclusively behaves as a UFP
- 3) Dual-role – for this mode, the port can behave either as a DFP or UFP

The host-only and device-only ports behaviorally map to traditional USB host ports and USB device ports, respectively. When a host-only port is attached to a device-only port, the behavior from the user's perspective follows the traditional USB host-to-device port model. However, the USB Type-C connector solution does not physically prevent host-to-host or device-to-device connections. In this case, the resulting host-to-host or device-to-device connection results in a safe but non-functional situation.

Initially, the DFP sources VBUS and the UFP sinks VBUS. [USB PD](#) may then be used to independently swap both the data and power roles of the ports.

USB hubs have two types of ports, a single UFP that is connected up to a host or another hub and one or more DFPs for connecting other devices.

A port that supports dual-role operation by being able to shift to the appropriate connected mode when attached to either a host-only or device-only port is a DRP. In the special case of a DRP being attached to another DRP, an initialization protocol across the CC pins is used to establish the initial host-to-device relationship, and in this case, the determination of which is DFP or UFP is random from the user's perspective.

Two methods are defined to allow a USB Type-C DRP to functionally swap data roles, one managed using [USB PD](#) DR_Swap and the other emulating a disconnect/reconnect sequence (see Figure 4-16). As an alternative to role swapping, a USB Type-C DRP may provide useful functionality by when operating as a host, exposing a CDC/network (preferably TCP/IP) stack or when operating as a device, exposing a CDC/network interface.

2.3.4 USB Type-C VBUS Current Detection and Usage

With the USB Type-C connector solution, a DFP (host or downstream hub port) may implement higher source current over VBUS to enable faster charging of mobile devices or powering devices that require more current than is specified in the [USB 3.1 Specification](#). All USB host and hub ports advertise via the CC pins the level of current that is presently available. The USB device port is required to manage its load to stay within the current level offered by the host or hub, including dynamically scaling back the load if the host or hub port changes its advertisement to a lower level as indicated over the CC pins.

Three current levels at default VBUS are defined by [USB Type-C Current](#):

- Default values as defined by a USB Specification
- 1,5 A
- 3,0 A

The higher [USB Type-C Current](#) levels that can be advertised allows hosts and devices that do not implement [USB PD](#) to take advantage of higher charging current.

2.3.5 USB PD Communication

USB Power Delivery is a feature on products (hosts, hubs and devices). **USB PD** communications is used to:

- Establish power contracts that allow voltage and current outside that defined by the **USB 2.0** and **USB 3.1** specifications.
- Change the port sourcing VBUS.
- Change the port sourcing VCONN.
- Swap DFP and UFP roles.
- Communicate with cables.

The USB Type-C connector solution provides a new path for **USB PD** communications. Rather than superimposing a Binary Frequency Shift Keying (BFSK) on VBUS, the **USB PD** Bi-phase Mark Coded (BMC) communications are carried on the CC wire. In USB Type-C to legacy applications, the use of **USB PD** BFSK is allowed.

2.3.6 Functional Extensions

Functional extensions (see Chapter 5) are enabled via a communications channel across CC using methods defined by the **USB Power Delivery Specification**.

2.4 Vbus

VBUS provides a path to deliver power between a host and a device, and between a charger and a host/device. A simplified high-current supply capability is defined for hosts and chargers that optionally support current levels beyond the **USB 2.0** and **USB 3.1** specifications. The **USB Power Delivery Specification** is supported.

Table 2-1 summarizes the power supply options available from the perspective of a device with the USB Type-C connector. Not all options will be available to the device from all host or hub ports – only the first two listed options are mandated by the base USB specifications and form the basis of **USB Type-C Current** at the Default USB Power level.

Table 2-1 – Summary of power supply options

Mode of Operation	Nominal Voltage	Maximum Current	Notes
USB 2.0	5 V	500 mA	Default Current, based on definitions in the base specifications
USB 3.1	5 V	900 mA	
USB BC 1.2	5 V	Up to 1,5 A	Legacy charging
USB Type-C Current @ 1,5 A	5 V	1,5 A	Supports higher power devices
USB Type-C Current @ 3,0 A	5 V	3 A	Supports higher power devices
USB PD	Configurable up to 20 V	Configurable up to 5 A	Directional control and power level management

The USB Type-C receptacle is specified for current capability of 5 A whereas standard USB Type-C cable assemblies are rated for 3 A. The higher rating of the receptacle enables systems to deliver more power over directly attached docking solutions or using appropriately designed chargers with captive cables when implementing **USB PD**. Also, USB Type-C cable assemblies designed for **USB PD** and appropriately identified via electronic marking are allowed to support up to 5 A.

2.5 Vconn

Once the connection between host and device is established, the CC pin (CC1 or CC2) in the receptacle that is not connected via the CC wire through the standard cable is repurposed to source VCONN to power circuits in the plug needed to implement Electronically Marked Cables (see Section 4.9). Initially, the DFP sources VCONN and the source may be swapped using [USB PD VCONN_Swap](#).

Electronically marked cables may use VBUS instead of VCONN as VBUS is available across the cable. VCONN functionally differs from VBUS in that it is isolated from the other end of the cable. VCONN is independent of VBUS and, unlike VBUS which can use [USB PD](#) to support higher voltages, VCONN voltage is fixed at 5 V.

2.6 Hubs

USB hubs implemented with USB Type-C receptacles are required to clearly identify the upstream facing port. This requirement is needed because a user can no longer know which port on a hub is the upstream facing port and which ports are the downstream facing ports by the type of receptacles that are exposed, i.e., USB Type-B is the upstream facing port and USB Type-A is a downstream facing port.

3 Mechanical

3.1 Overview

3.1.1 Compliant Connectors

The USB Type-C™ specification defines the following standard connectors:

- USB Type-C receptacle
- USB Full-Featured Type-C plug
- USB 2.0 Type-C plug

3.1.2 Compliant Cable Assemblies

Table 3-1 summarizes the USB Type-C standard cable assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. All cables that are either full-featured and/or are rated at more than 3 A current are [Electronically Marked Cables](#).

Table 3-1 – USB Type-C Standard Cable Assemblies

Cable Ref	Plug 1	Plug 2	USB Version	Cable Length	Current Rating	USB Power Delivery (BMC)	USB Type-C Electronically Marked
CC2-3	C	C	USB 2.0	≤ 4 m	3 A	Supported	Optional
CC2-5					5 A		Required
CC3G1-3	C	C	USB 3.1 Gen1	≤ 2 m	3 A	Supported	Required
CC3G1-5					5 A		
CC3G2-3	C	C	USB 3.1 Gen2	≤ 1 m	3 A	Supported	Required
CC3G2-5					5 A		

USB Type-C products are also allowed to have a captive cable. See Section 3.4.3.

3.1.3 Compliant USB Type-C to Legacy Cable Assemblies

Table 3-2 summarizes the USB Type-C legacy cable assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. Cables shall be electronically marked where indicated in Table 3-2. **USB 3.1** Type-C legacy cables assemblies that only offer performance up to **USB 3.1** Gen1 are not allowed by this specification.

Table 3-2 – USB Type-C Legacy Cable Assemblies

Cable Ref	Plug 1 ⁴	Plug 2 ⁴	USB Version	Cable Length	Current Rating	USB Type-C Electronically Marked ³
AC2-3	USB 2.0 Standard-A	USB 2.0 Type-C ¹	USB 2.0	≤ 4 m	3 A	Optional
AC2-5	USB 2.0 PD Standard-A				5 A	Required
AC3G2-3	USB 3.1 Standard-A	USB Full-Featured Type-C ¹	USB 3.1 Gen2	≤ 1 m	3 A	Optional
AC3G2-5	USB 3.1 PD Standard-A				5 A	Required
CB2-3	USB 2.0 Type-C ²	USB 2.0 Standard-B	USB 2.0	≤ 4 m	3 A	Optional
CB2-5		USB 2.0 PD Standard-B			5 A	Required
CB3G2-3	USB Full-Featured Type-C ²	USB 3.1 Standard-B	USB 3.1 Gen2	≤ 1 m	3 A	Optional
CB3G2-5		USB 3.1 PD Standard-B			5 A	Required
CmB2	USB 2.0 Type-C ²	USB 2.0 Mini-B	USB 2.0	≤ 4 m	500 mA	Optional
CmB2-3	USB 2.0 Type-C ²	USB 2.0 PD Micro-B	USB 2.0	≤ 2 m	3 A	Optional
CmB3G2-3	USB Full-Featured Type-C ²	USB 3.1 PD Micro-B	USB 3.1 Gen2	≤ 1 m	3 A	Optional

¹ USB Type-C plugs associated with the “B” end of a legacy adapter cable are required to have Rp termination incorporated into the plug assembly – see Section 4.5.3.2.2.

² USB Type-C plugs associated with the “A” end of a legacy adapter cable are required to have Rd termination incorporated into the plug assembly – see Section 4.5.3.2.1.

³ Electronic marking shall only be implemented using **USB PD** BMC.

⁴ Legacy USB plugs used in the USB Type-C cable assemblies shall comply with the low level contact resistance as specified in **USB PD** 3.6.1 for 3A or 5A cables as appropriate. Legacy USB plugs shall comply with the contact current rating as specified in **USB PD** 3.6.5.1 for 3A current and 3.6.5.2 for 5A current. For USB Type-C to **USB PD**-versions of USB Standard-B and USB Micro-B plugs, **USB PD** passive marking (cPlug) on the ID pin of the B plug is not required.

3.1.4 Compliant USB Type-C to Legacy Adapter Assemblies

Table 3-3 summarizes the USB Type-C legacy adapter assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements.

Table 3-3 – USB Type-C Legacy Adapter Assemblies

Adapter Ref	Plug	Receptacle ³	USB Version	Cable Length	Current Rating	USB Legacy Receptacle Type	USB Type-C Electronically Marked
CμBR2-3	USB 2.0 Type-C ¹	USB 2.0 Micro-B	USB 2.0	≤ 0,15 m	3 A	PD Receptacle Not Allowed	Optional
CAR3G1-3	USB Full-Featured Type-C ²	USB 3.1 Standard-A	USB 3.1 Gen1	≤ 0,15 m	3 A	PD Receptacle Not Allowed	Optional

- ¹ USB Type-C plugs associated with the “B” end of a legacy adapter are required to have Rp termination incorporated into the plug assembly – see Section 4.5.3.2.2. The [USB PD](#) version of the USB Micro-B receptacle shall not be implemented.
- ² USB Type-C plugs associated with the “A” end of a legacy adapter are required to have Rd termination incorporated into the plug assembly – see Section 4.5.3.2.1. The [USB PD](#) version of the USB Standard-A receptacle shall not be implemented.
- ³ Legacy USB receptacles shall to comply with the low level contact resistance as specified in [USB PD](#) 3.6.1 for 3A. Legacy USB receptacles shall comply with the contact current rating specified in [USB PD](#) 3.6.5.1 measured for 3A current.

3.2 USB Type-C Connector Mating Interfaces

This section defines the connector mating interfaces, including the connector interface drawings, pin assignments, and descriptions.

3.2.1 Interface Definition

Figure 3-1 and Figure 3-3 show, respectively, the USB Type-C receptacle and USB Full-Featured Type-C plug interface dimensions.

Figure 3-9 shows the [USB 2.0](#) Type-C plug interface dimensions. The dimensions that govern the mating interoperability are specified. All the REF dimensions are provided for reference only, not hard requirements.

Key features, configuration options, and design areas that need attention:

- 1) Figure 3-1 shows a vertical-mount receptacle. Other PCB mounting types such as right-angle mount and mid-mount are allowed.
- 2) A mid-plate is required between the top and bottom signals inside the receptacle tongue to manage crosstalk in full-featured applications. The mid-plate shall be connected to the PCB ground with at least two grounding points. A reference design of the mid-plate is provided in Section 3.2.2.1.
- 3) Retention of the cable assembly in the receptacle is achieved by the side-latches in the plug and features on the sides of the receptacle tongue. Side latches are required for all plugs except plugs used for docking with no cable attached. Side latches shall be connected to ground inside the plug. A reference design of the side latches is provided in Section 3.2.2.2 along with its grounding scheme. Docking applications may not have side latches, requiring special consideration regarding EMC (Electromagnetic Compatibility).
- 4) The EMC shielding springs are required inside the cable plug. The shielding spring shall be connected to the plug shell. Section 3.2.2.3 shows reference designs of the EMC spring.
- 5) Shorting of any signal or power contact spring to the plug metal shell is not allowed. The spring in the deflected state should not touch the plug shell. An isolation layer (e.g., Kapton tape placed on the plug shell) is recommended to prevent accidental shorting due to plug shell deformation.

- 6) The USB Type-C receptacle shall provide an EMC ground return path through one of the following options:

- Fingers in the receptacle outer shell
- Internal EMC pads
- Both external fingers in the shell and internal EMC pads

If fingers in the receptacle outer shell are used, then the receptacle springs shall contact the mated plug within the zones defined in Figure 3-2. A minimum of four separate contact points are required. Additional fingers and points of contact are allowed. See Section 3.2.2.4 for a reference design of receptacle outer shell fingers.

If internal EMC pads are present in the receptacle, then they shall comply with the requirements defined in Figure 3-1. The shielding pads shall be connected to the receptacle shell. If no receptacle shell is present, then the receptacle shall provide a means to connect the shielding pad to ground. See Section 3.2.2.3 for a reference design of the shielding pad and ground connection.

- 7) This specification defines the USB Type-C receptacle shell length (6.20 ± 0.02 mm) as a reference dimension. The receptacle shell length of 6.2 mm provides proper mechanical and electrical mating of the plug to the receptacle in addition to providing both the plug and receptacle a defined configuration to design to for the wrenching and contact mating requirements. The USB Type-C receptacle at the system level should be implemented such that the USB Type-C receptacle connector mounted in the associated system hardware has an effective shell length equal to the reference dimension.
- 8) The USB Type-C connector mating interface is defined so that the electrical connection may be established without the receptacle shell. To prevent excessive misalignment of the plug when it enters or exits the receptacle, the enclosure should have features to guide the plug for insertion and withdrawal when a modified receptacle shell is present. If the USB Type-C receptacle shell is modified from the specified dimension, then the recommended lead in from the receptacle tongue to the plug point of entry is 1,5 mm minimum when mounted in the system.
- 9) A paddle card (e.g., PCB) may be used in the USB Type-C plug to manage wire termination and electrical performance. Section 3.2.2.5 includes the guidelines and a design example for a paddle card.
- 10) This specification does not define standard footprints. Figure 3-4 shows an example SMT (surface mount) footprint for the vertical receptacle shown in Figure 3-1. Additional reference footprints and mounting configurations are shown in Figure 3-5, Figure 3-6, Figure 3-7, and Figure 3-8.
- 11) The receptacle shell shall be connected to the PCB ground plane.
- 12) All VBUS pins shall be connected together in the USB Type-C plug.
- 13) All Ground return pins shall be connected together in the USB Type-C plug.
- 14) All VBUS pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all VBUS pins bussed together in the PCB).
- 15) All Ground return pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all Ground return pins bussed together in the PCB).

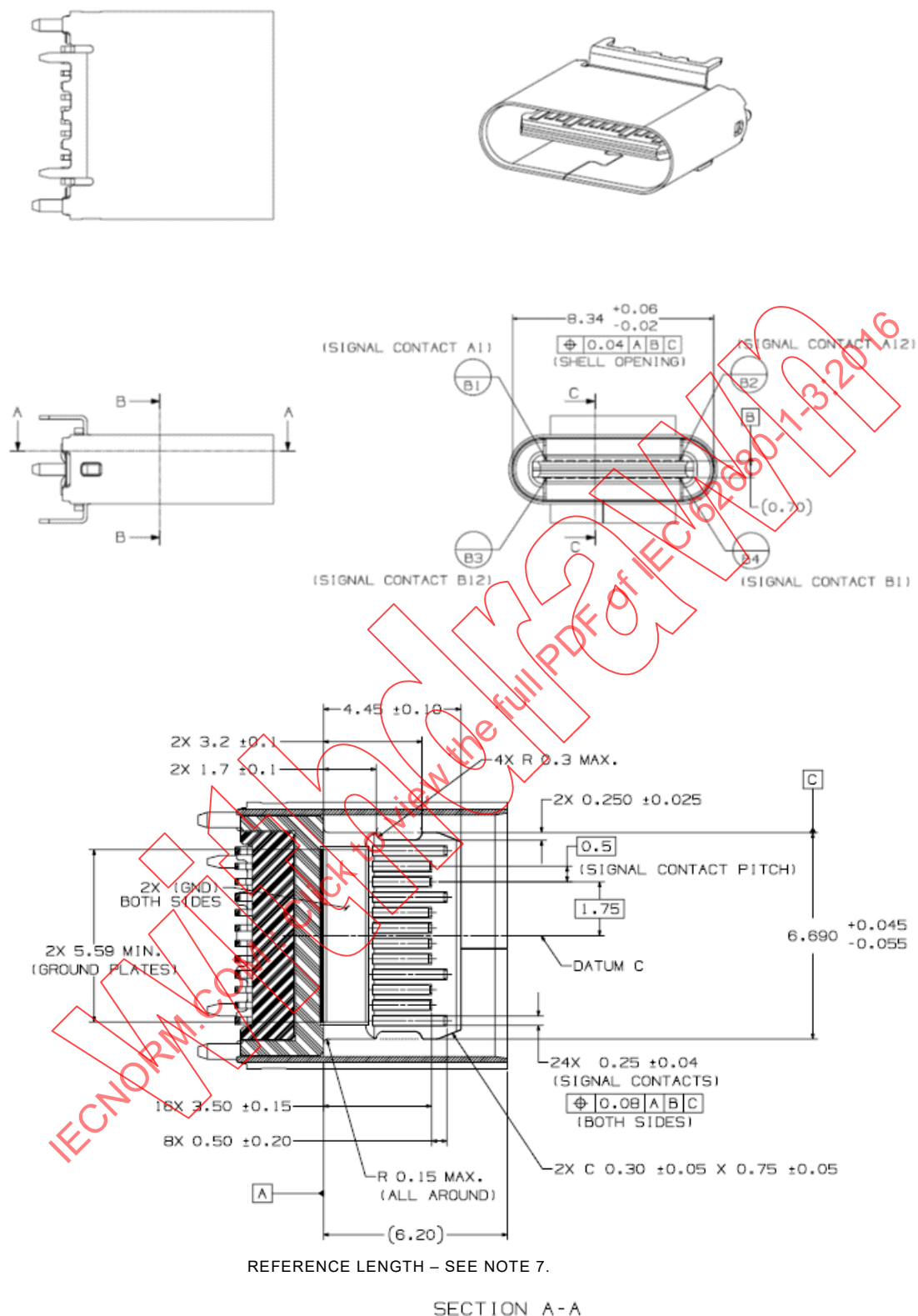


Figure 3-1 – USB Type-C Receptacle Interface Dimensions

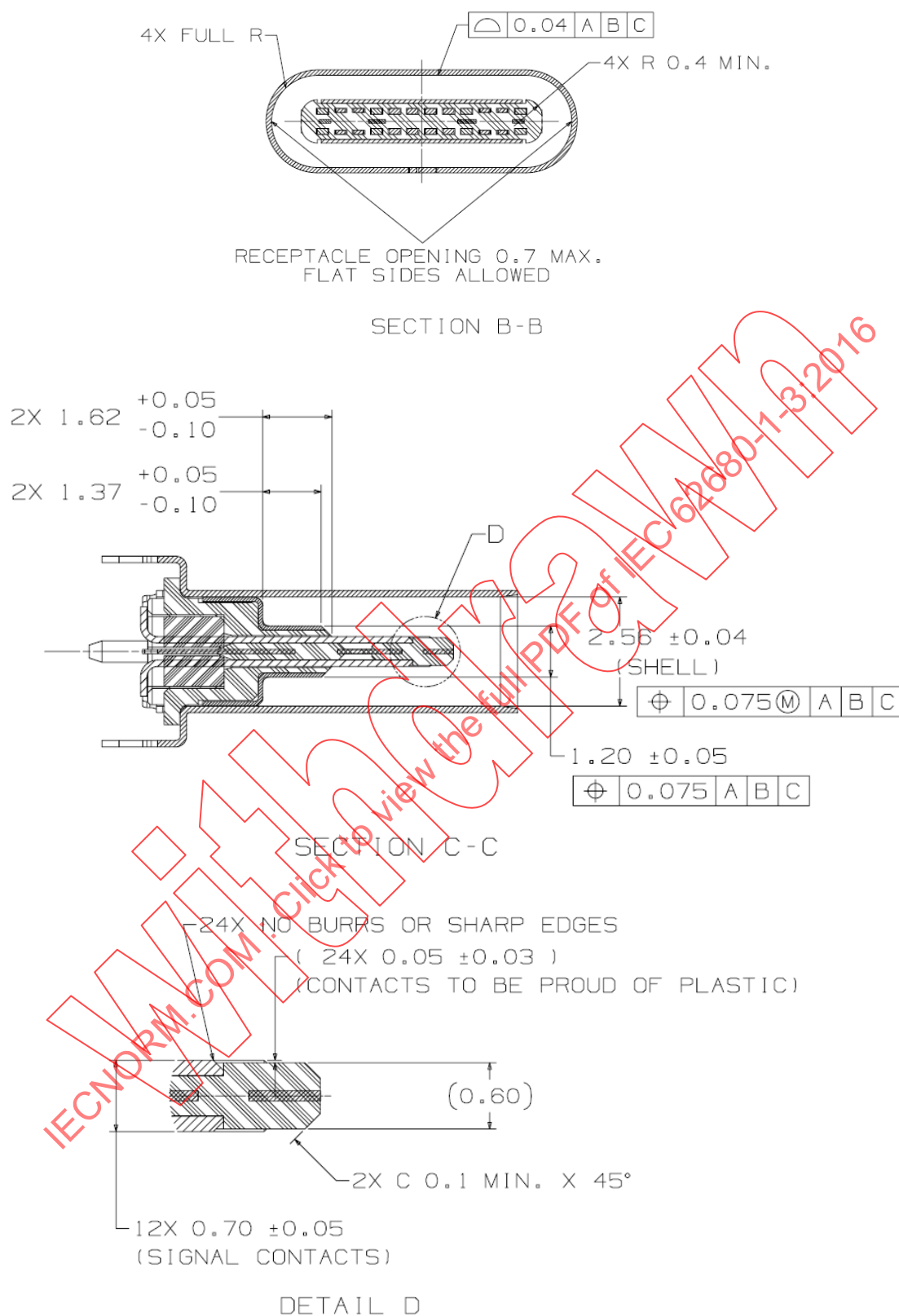


Figure 3–1 (cont)

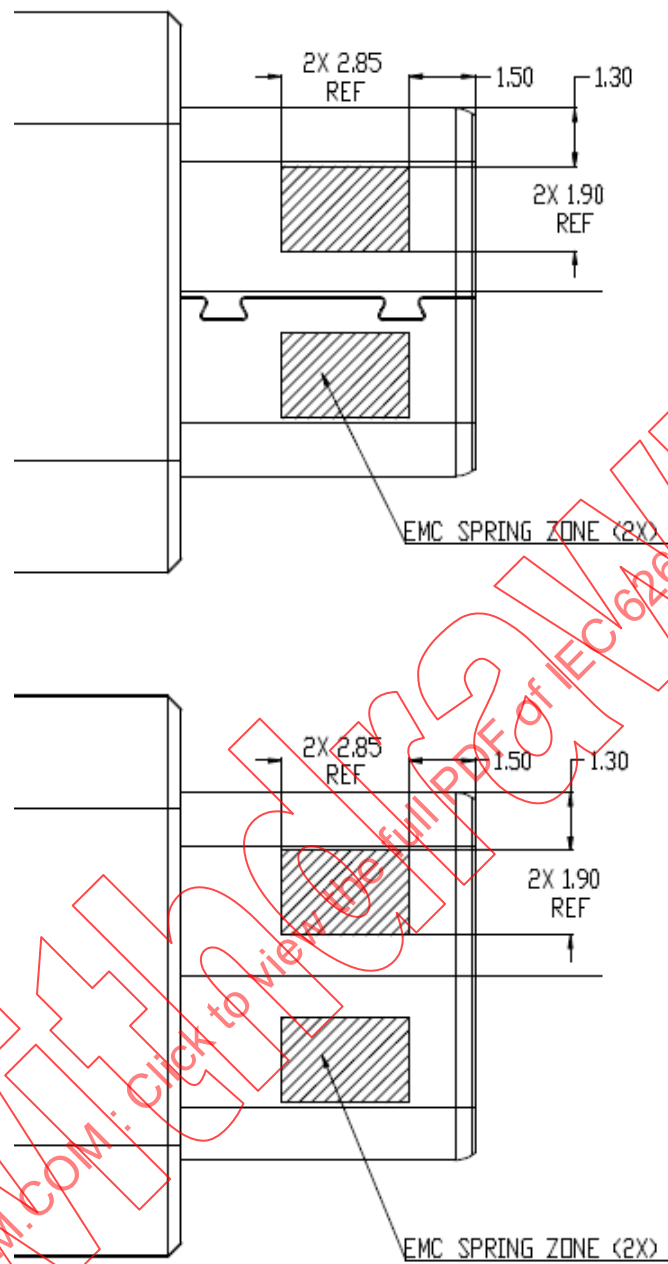


Figure 3-2 – Reference Design USB Type-C Plug External EMC Spring Contact Zones

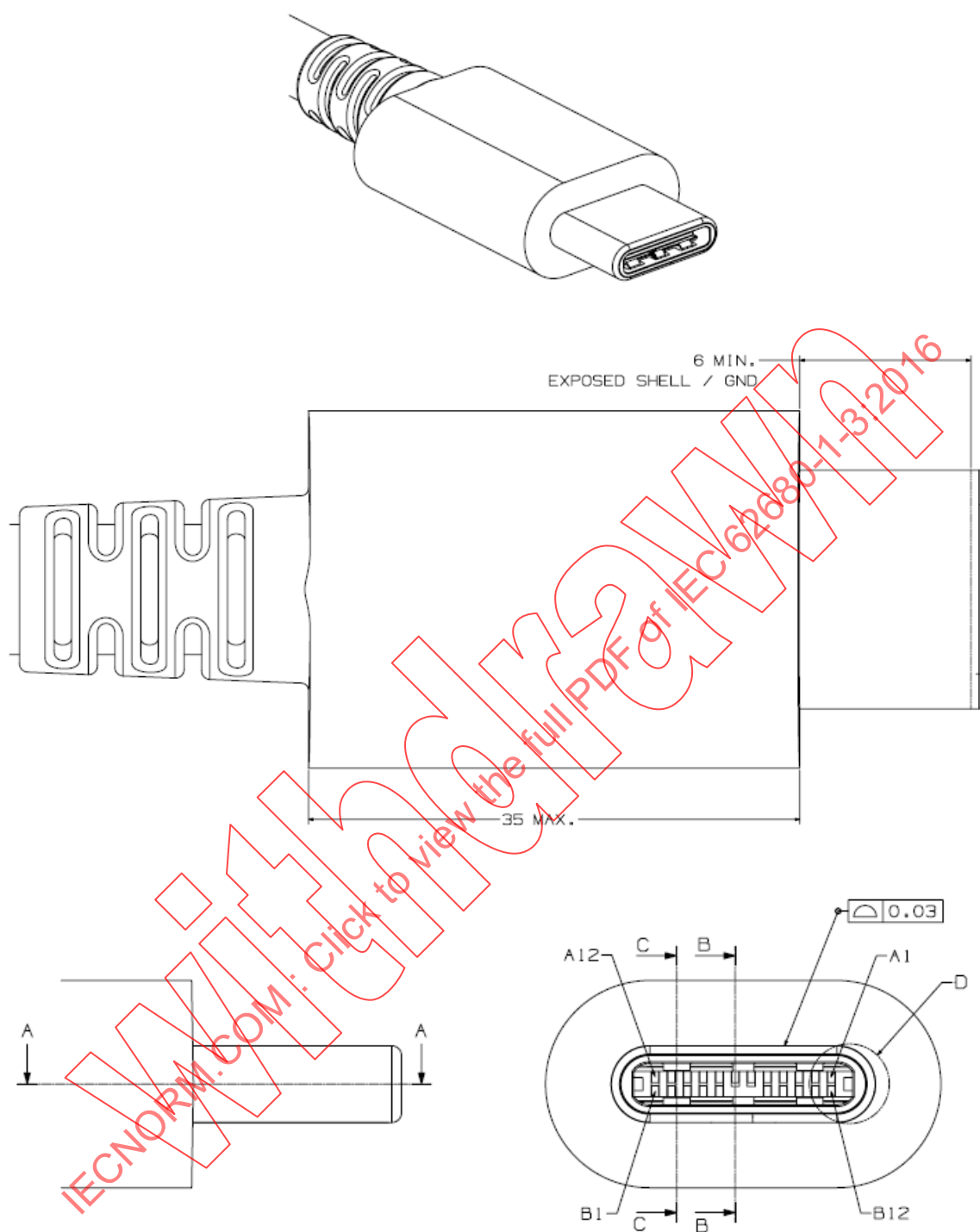


Figure 3-3 – USB Full-Featured Type-C Plug Interface Dimensions

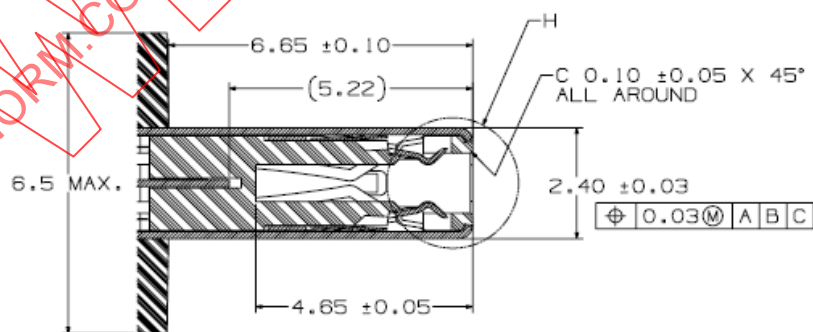
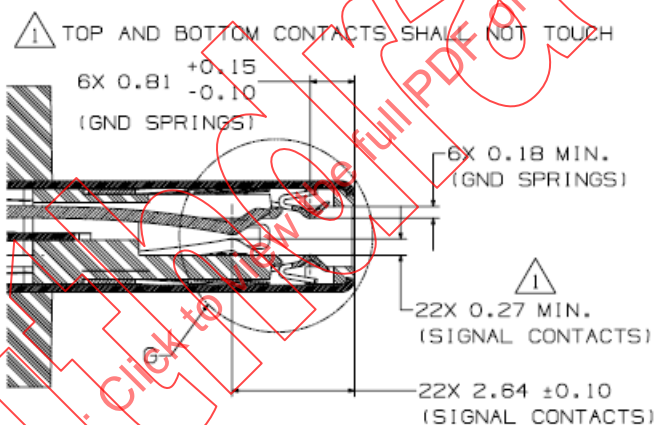
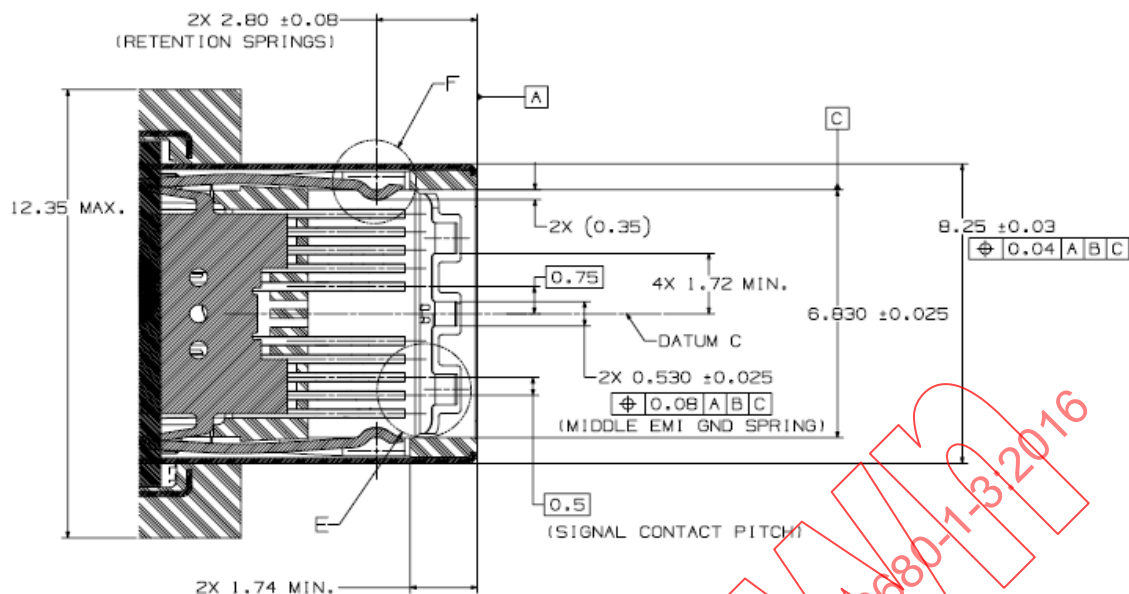


Figure 3-3 (cont.)

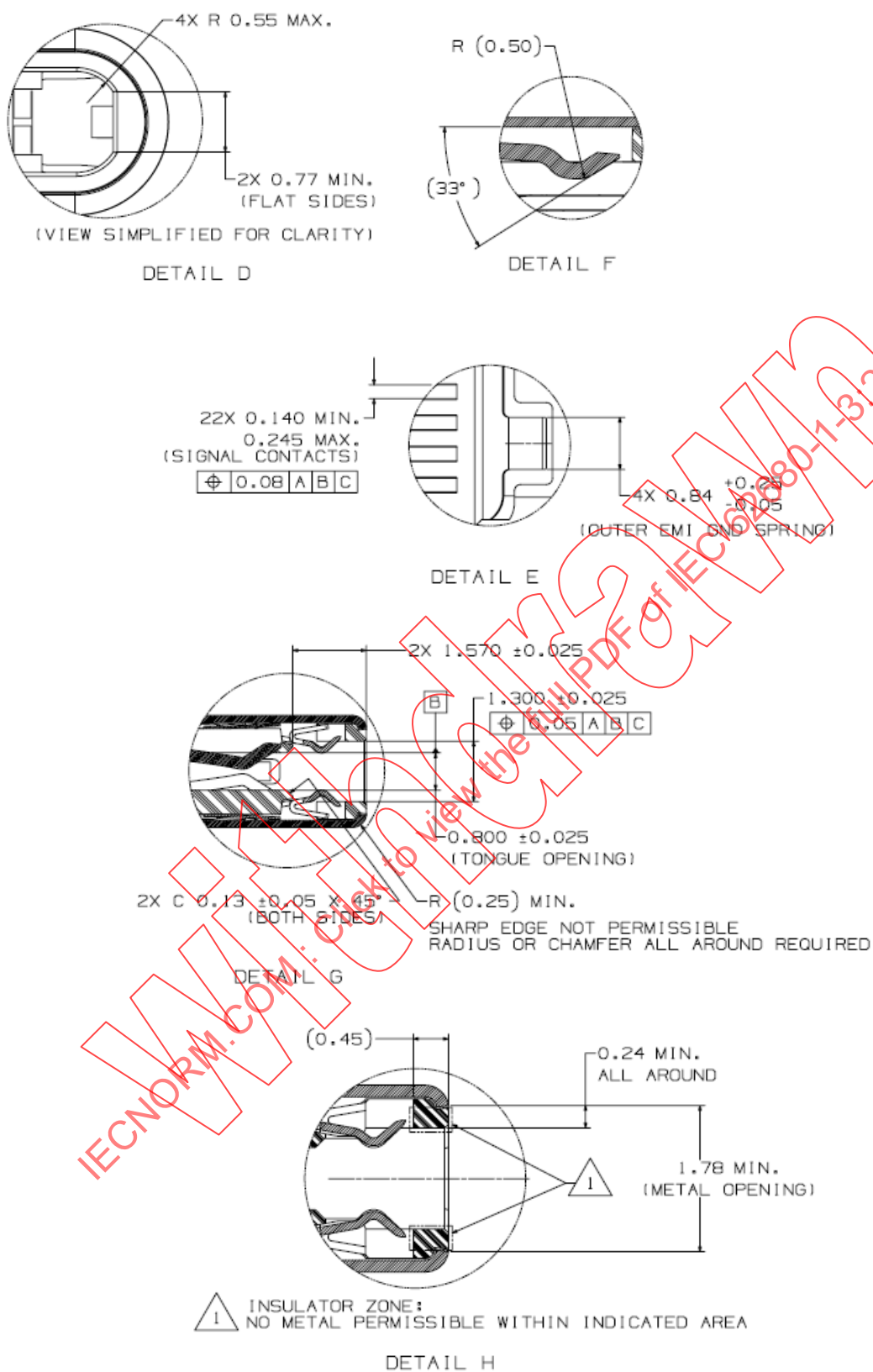


Figure 3-3 (cont.)

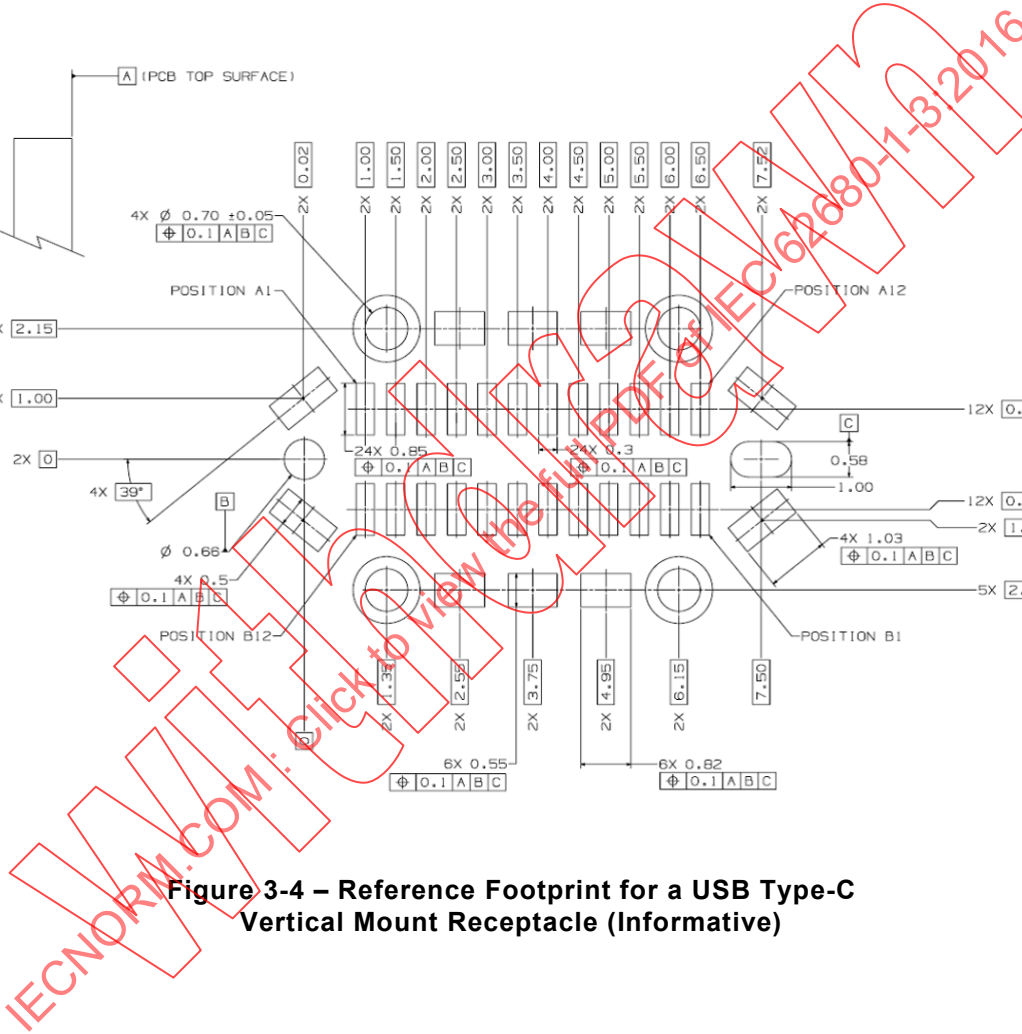


Figure 3-4 – Reference Footprint for a USB Type-C Vertical Mount Receptacle (Informative)



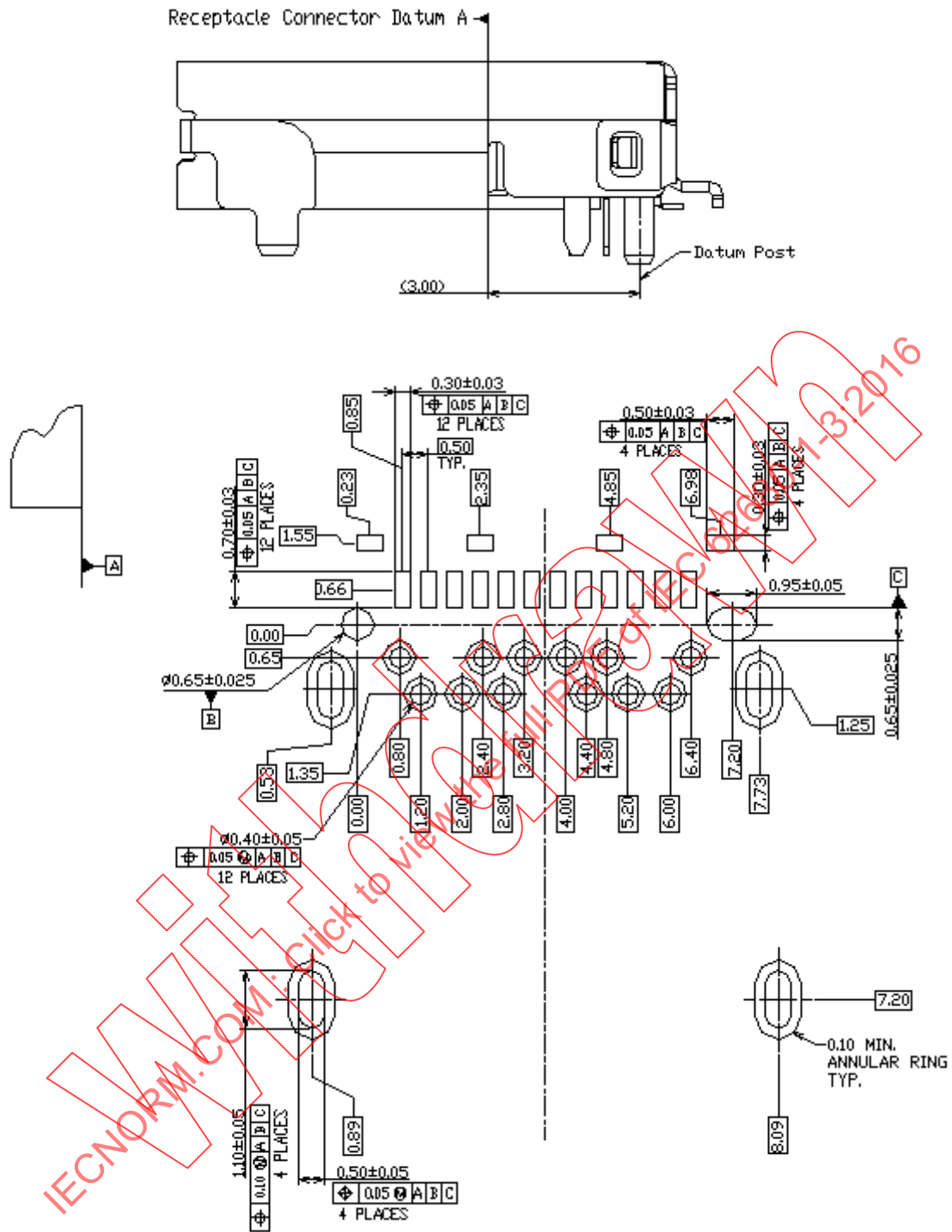
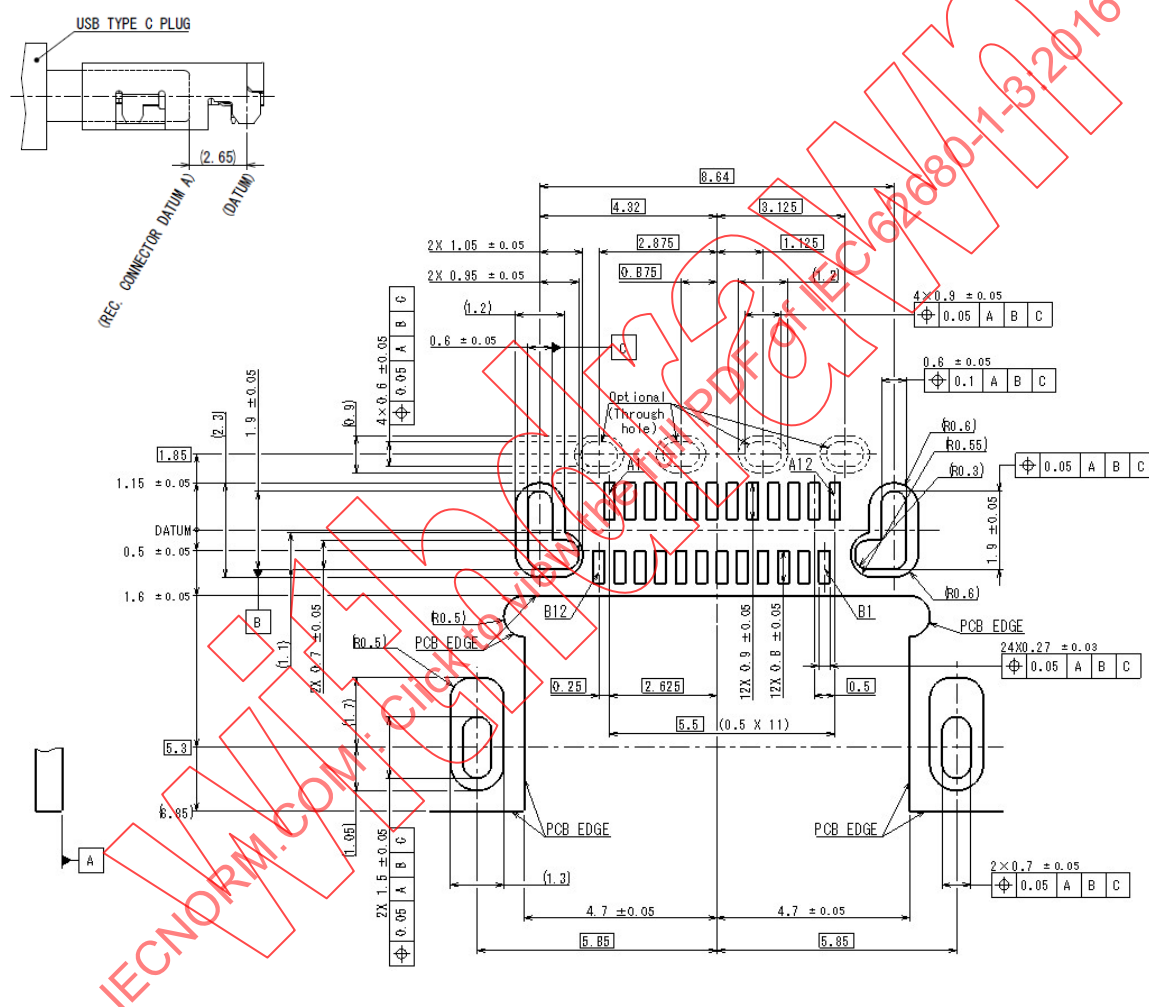


Figure 3-6 – Reference Footprint for a USB Type-C Hybrid Right-Angle Receptacle (Informative)



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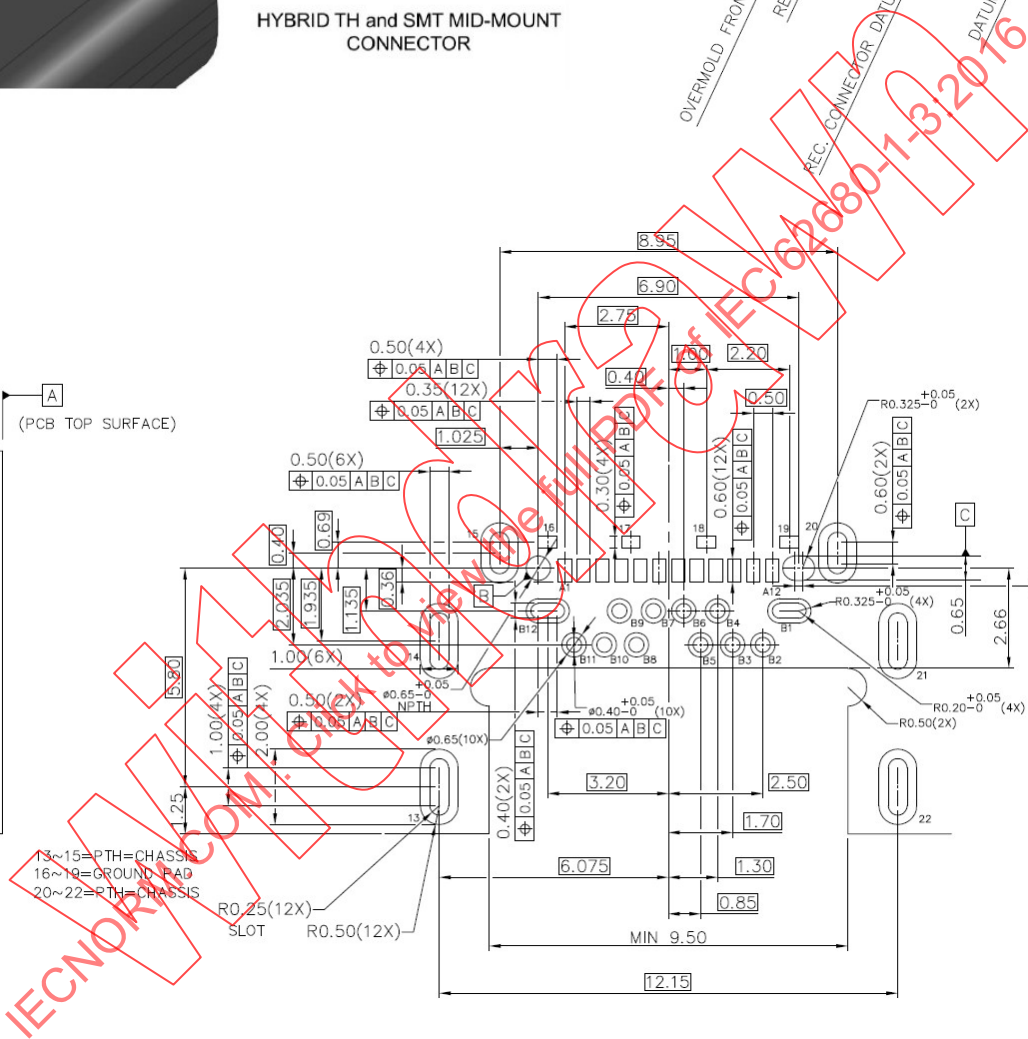


Figure 3-8 – Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (Informative)

This specification requires that all contacts be present in the mating interface of the USB Type-C receptacle connector, but allows the plug to include only the contacts required for **USB PD** and **USB 2.0** functionality for applications that only support **USB 2.0**. The **USB 2.0** Type-C plug is shown in Figure 3-9. The following design simplifications may be made when only **USB 2.0** is supported:

- Only the contacts necessary to support **USB PD** and **USB 2.0** are required in the plug. All other pin locations may be unpopulated. See Table 3-5. All contacts are required to be present in the mating interface of the USB Type-C receptacle connector.

- Unlike the USB Full-Featured Type-C plug, the internal EMC springs may be formed from the same strip as the signal, power, and ground contacts. The internal EMC springs contact the inner surface of the plug shell and mate with the receptacle EMC pads when the plug is seated in the receptacle. Alternately, the [USB 2.0](#) Type-C plug may use the same EMC spring configuration as defined for the USB Full-Featured Type-C plug. The [USB 2.0](#) Type-C plug four EMC spring locations are defined in Figure 3-9. The alternate configuration using the six spring locations is defined in Figure 3-1. Also refer to the reference designs in 3.2.2.3 for further clarification.
- A paddle card inside the plug may not be necessary if wires are directly attached to the contact pins.

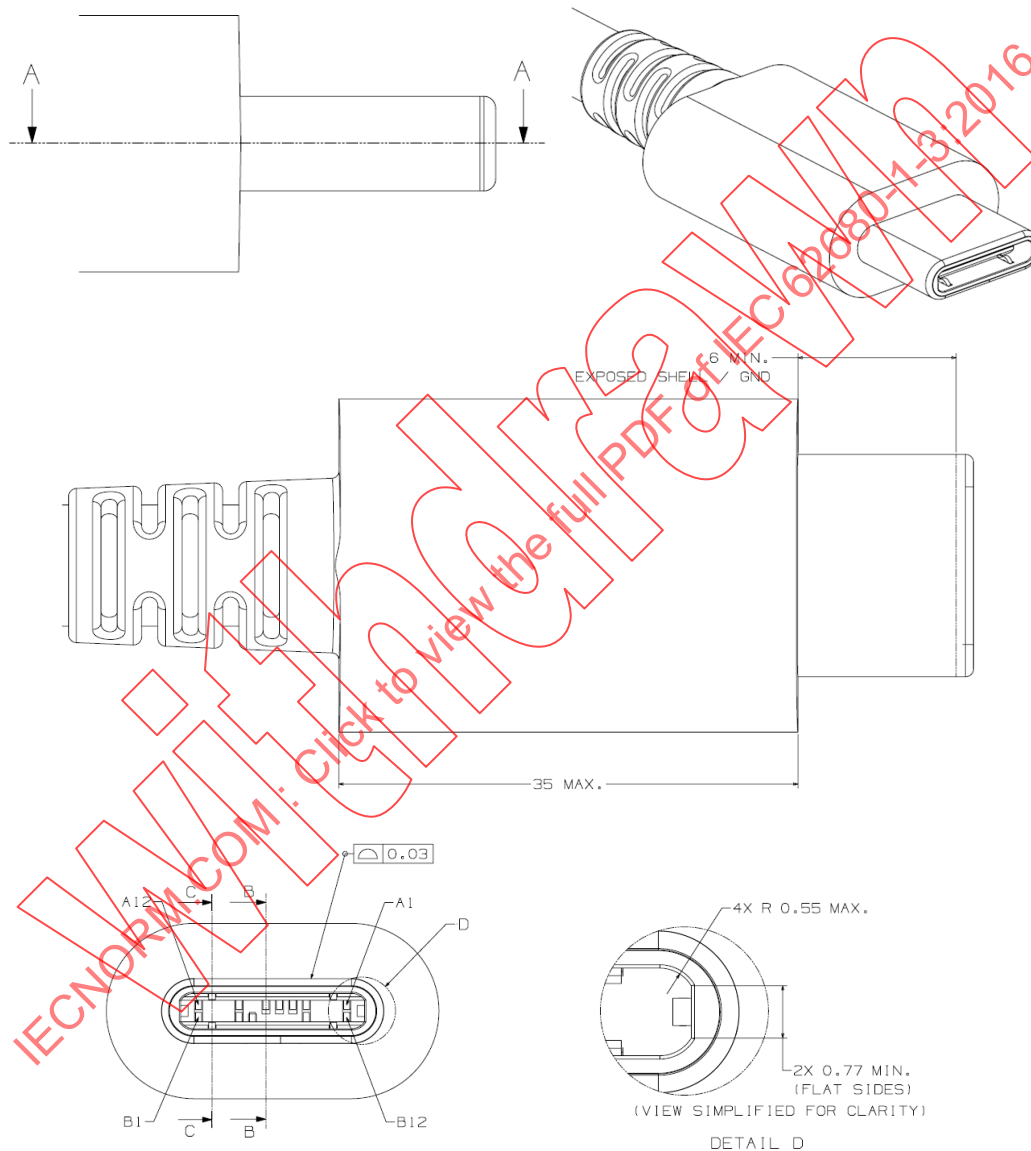


Figure 3-9 – [USB 2.0](#) Type-C Plug Interface Dimensions

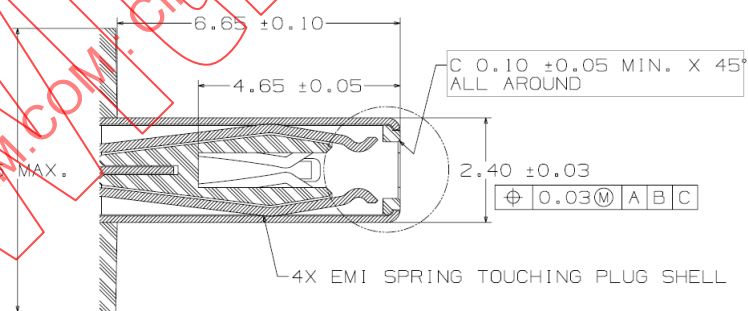
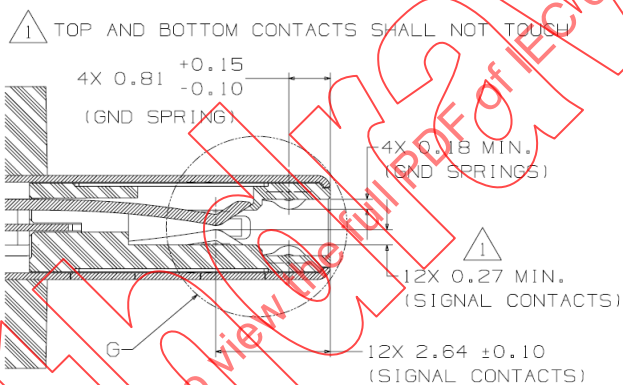
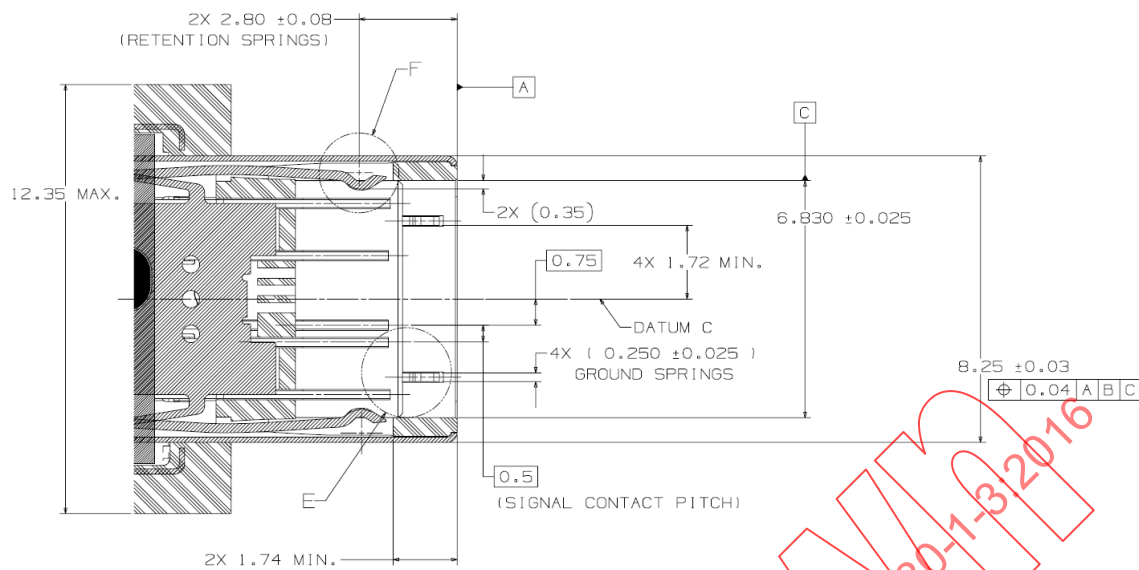


Figure 3-9 (cont.)

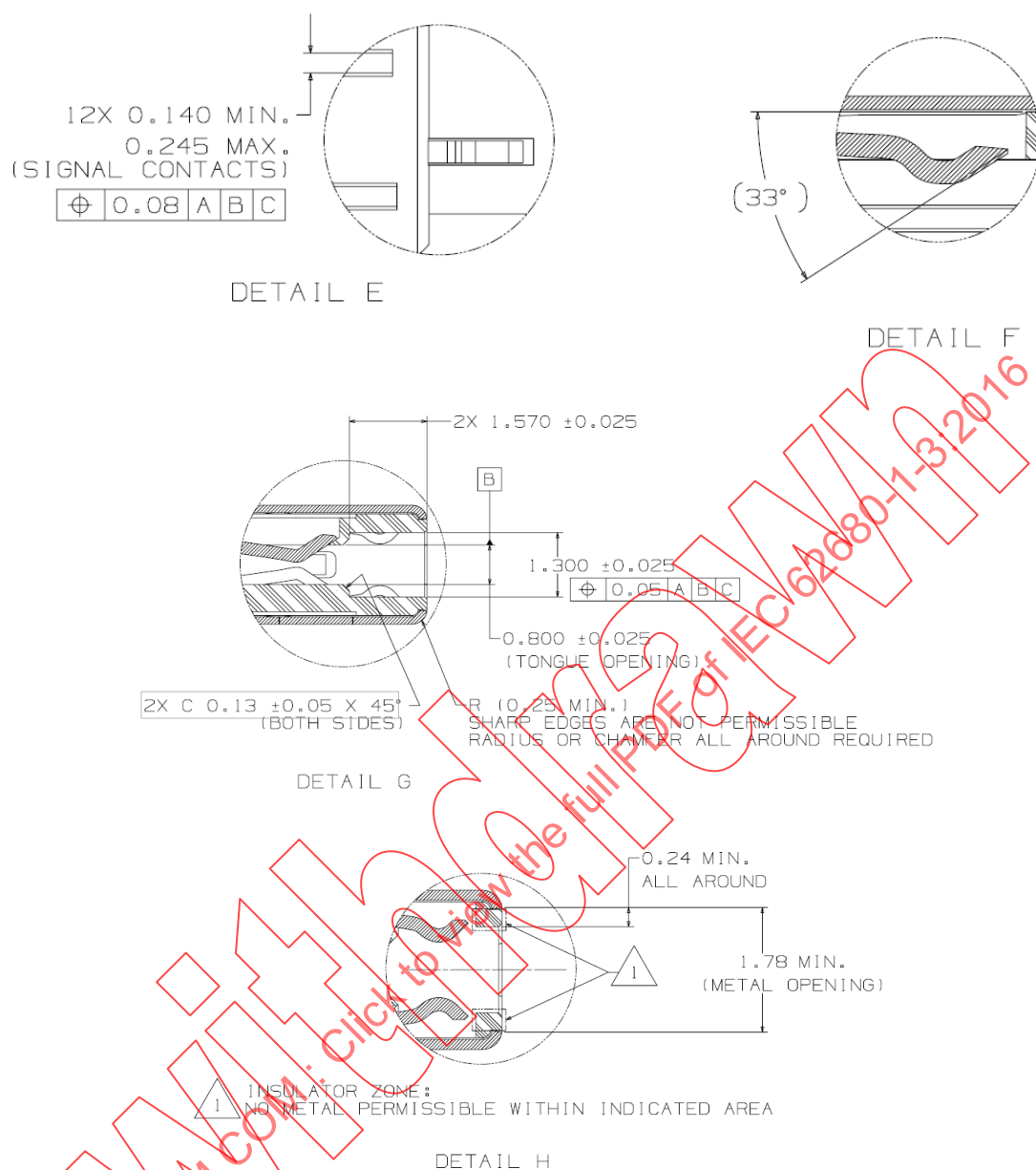


Figure 3-9 (cont.)

3.2.2 Reference Designs

This section provides reference designs for a few key features of the USB Type-C connector. The reference designs are provided as acceptable design examples. They are not normative.

3.2.2.1 Receptacle Mid-Plate (Informative)

The signals between the top and bottom of the receptacle tongue are isolated by a mid-plate inside the tongue. Figure 3-10 shows a reference design of the mid-plate. It is important to pay attention to the following features of the middle plate:

- The distance between the signal contacts and the mid-plate should be accurately controlled since the variation of this distance may significantly impact impedance of the connector.

- The mid-plate in this particular design protrudes slightly beyond the front surface of the tongue. This is to protect the tongue front surface from damage caused by miss-insertion of small objects into the receptacle.
- The mid-plate is required to be directly connected to the PCB ground with at least two grounding points.
- The sides of the mid-plate mate with the plug side latches, making ground connections to reduce EMC. Proper surface finishes are necessary in the areas where the side latches and mid-plate connections occur.

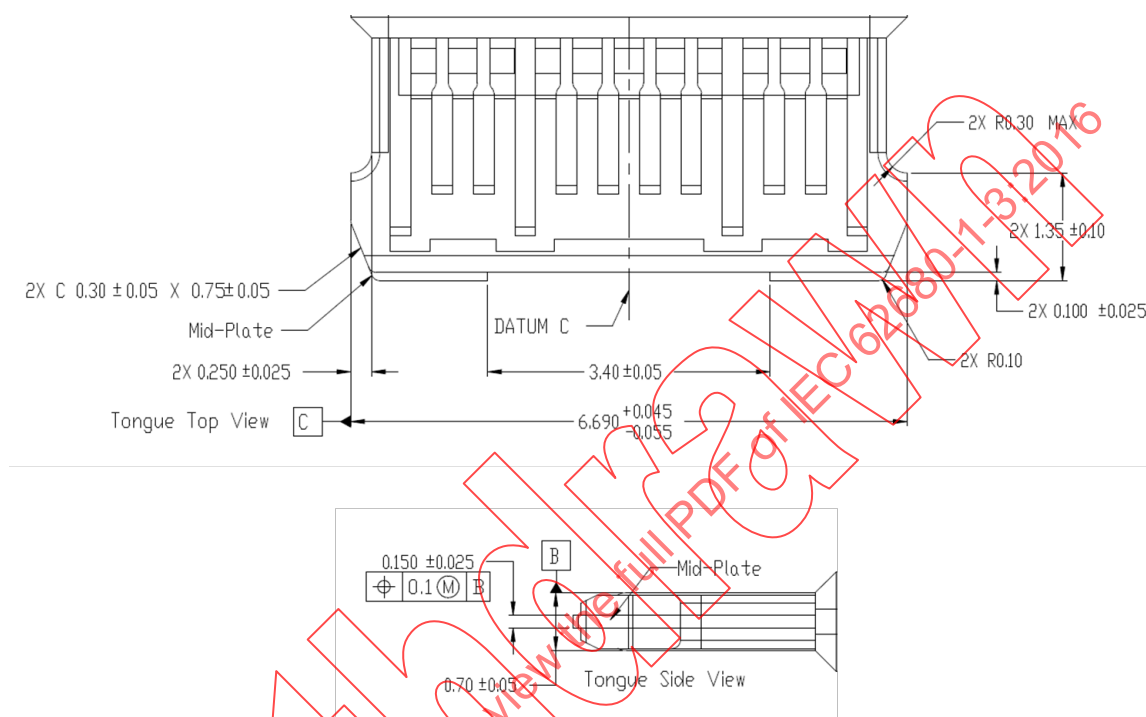


Figure 3-10 – Reference Design of Receptacle Mid-Plate

3.2.2.2 Side Latch (informative)

The side latches (retention latches) are located in the plug. Figure 3-11 shows a reference design of a blanked side latch. The plug side latches should contact the receptacle mid-plate to provide an additional ground return path.

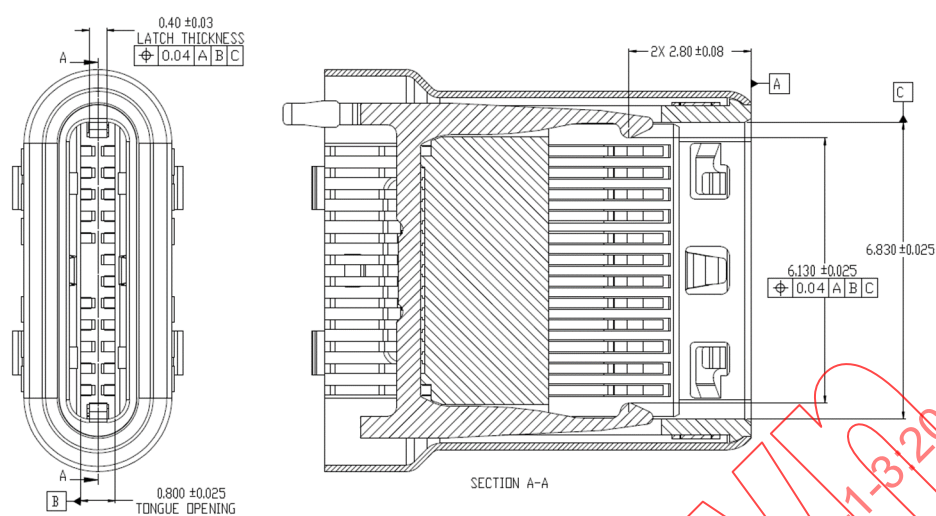


Figure 3-11 – Reference Design of the Retention Latch

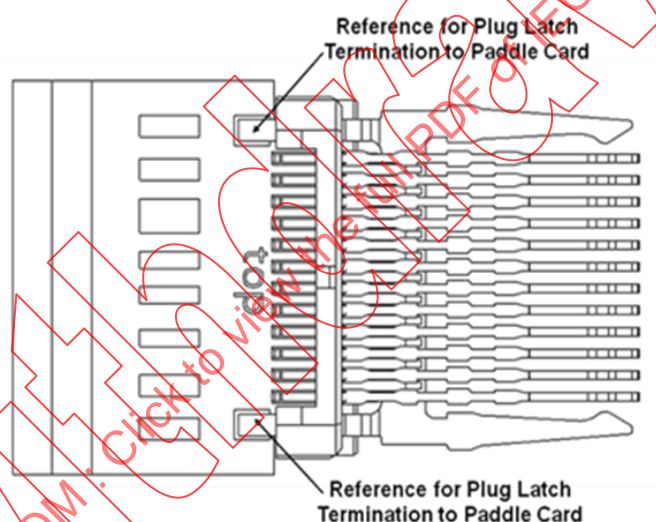


Figure 3-12 – Illustration of the Latch Soldered to the Paddle Card Ground

3.2.2.3 Internal EMI Springs and Pads (Informative)

Figure 3-13 is a reference design of the internal EMC spring located inside the USB Full-Featured Type-C plug. Figure 3-14 is a reference design of the internal EMC spring located inside the [USB 2.0](#) Type-C plug.

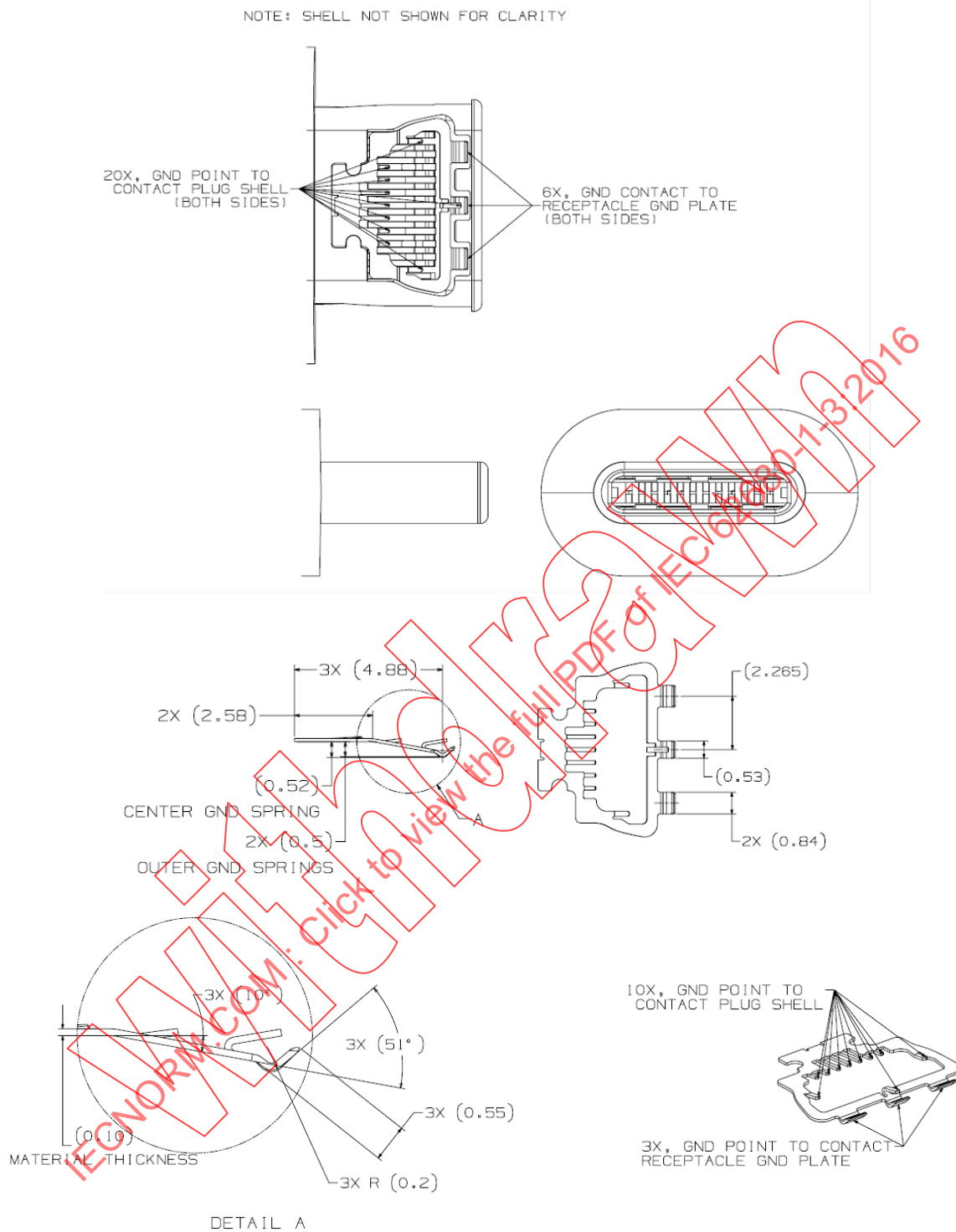


Figure 3-13 – Reference Design of the USB Full-Featured Type-C Plug Internal EMC Spring

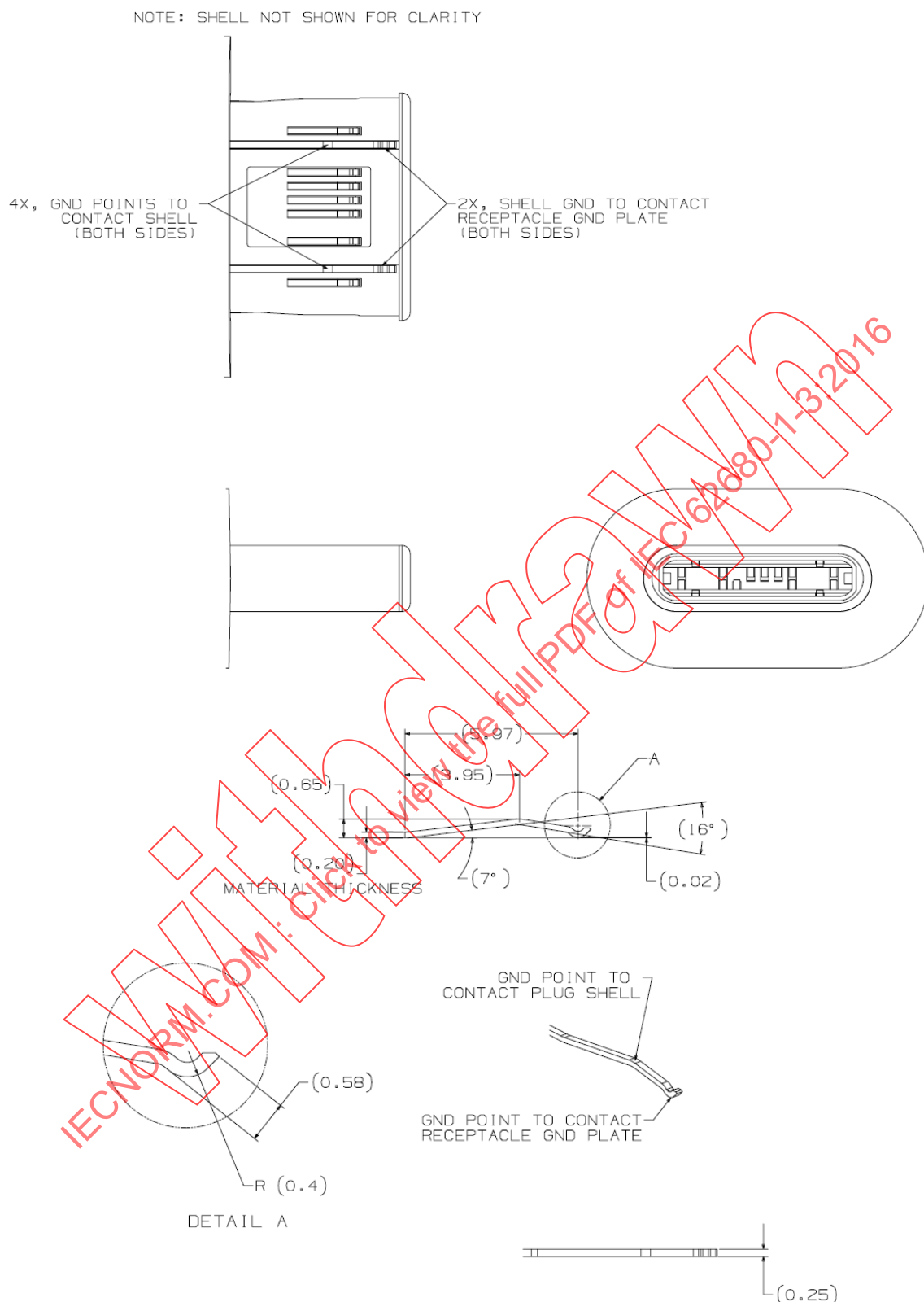
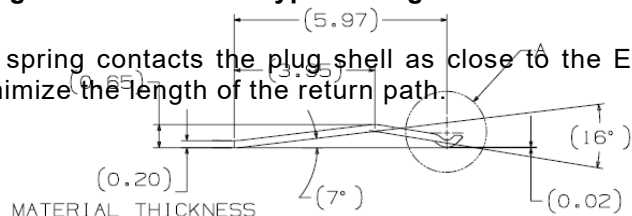


Figure 3-14 – Reference Design of the USB 2.0 Type-C Plug Internal EMC Spring

It is critical that the internal EMC spring contacts the plug shell as close to the EMC spring mating interface as possible to minimize the length of the return path.



The internal EMC pad (i.e., ground plate) shown in Figure 3-15 is inside the receptacle. It mates with the EMC spring in the plug. To provide an effective ground return, the EMC pads should have multiple connections with the receptacle shell.

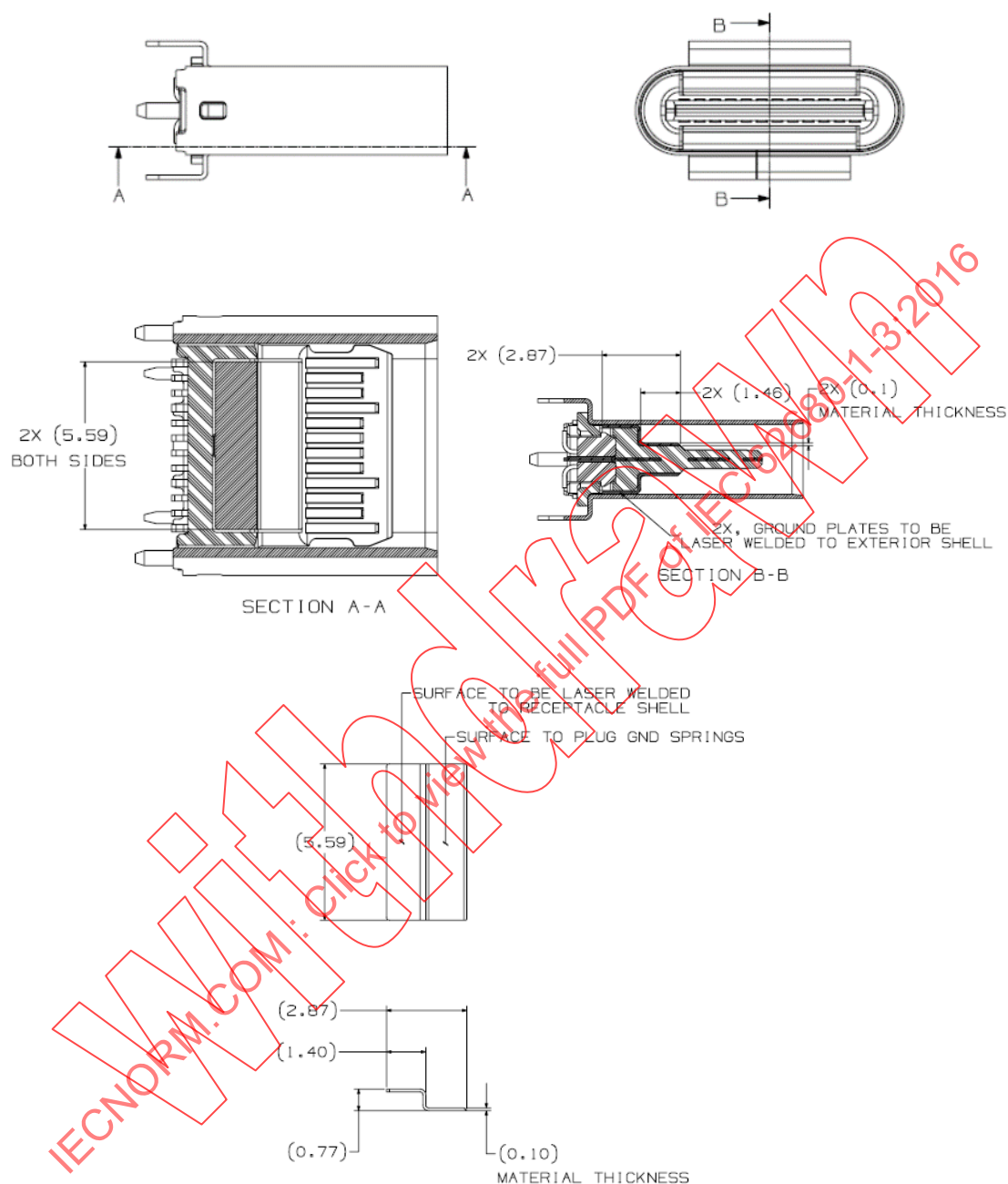


Figure 3-15 – Reference Design of Internal EMC Pad

3.2.2.4 Optional External Receptacle EMC Springs (Informative)

Some applications may use receptacles with EMC springs that contact the outside of the plug shell. Figure 3-16 shows a reference receptacle design with external EMC springs. The EMC spring contact landing zones for the fully mated condition are normative and defined in Section 3.2.1.

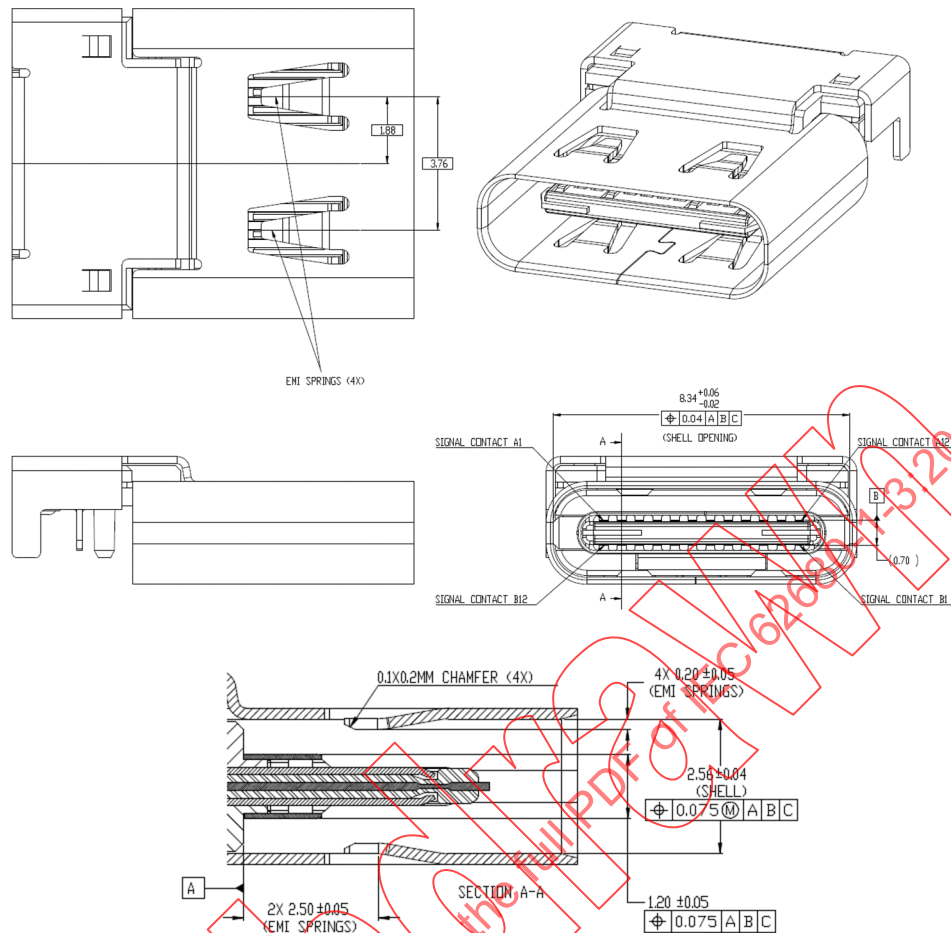


Figure 3-16 – Reference Design of a USB Type-C Receptacle with External EMC Springs

3.2.2.5 USB Full-Featured Type-C Plug Paddle Card (Informative)

The use of a paddle card is expected in the USB Full-Featured Type-C Plug. Figure 3-17 illustrates the paddle card pin assignment and contact spring connection location for a USB Full-Featured Type-C plug. The following guidelines are provided for the paddle card design:

- The paddle card should use high performance substrate material. The recommended paddle card thickness should have a tolerance less than or equal to $\pm 10\%$.
- The USB SuperSpeed traces should be as short as possible and have a nominal differential characteristic impedance of $85\ \Omega$.
- The differential pairs should have a minimum pair-to pair separation of $0,5\ \text{mm}$.
- It is recommended that a grounded coplanar waveguide (CPWG) system be selected as a transmission line method.
- Use of vias should be minimized.
- VBUS pins should be bussed together on the paddle card.
- GND pins should be bussed together on the paddle card.

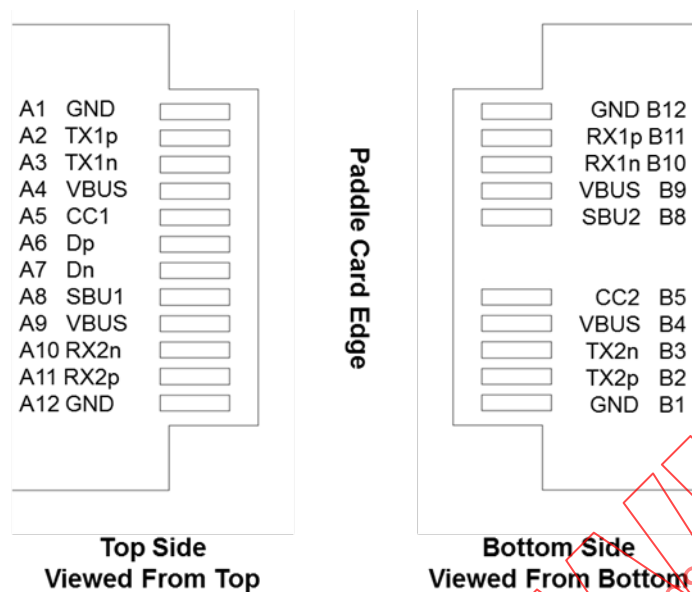


Figure 3-17 – Reference Design for a USB Full-Featured Type-C Plug Paddle Card

3.2.3 Pin Assignments and Descriptions

The usage and assignments of the 24 pins for the USB Type-C receptacle interface are defined in Table 3-4.

Table 3-4 – USB Type-C Receptacle Interface Pin Assignments

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2	SSTXp1	Positive half of first SuperSpeed TX differential pair	Second	B11	SSRXp1	Positive half of first SuperSpeed RX differential pair	Second
A3	SSTXn1	Negative half of first SuperSpeed TX differential pair	Second	B10	SSRXn1	Negative half of first SuperSpeed RX differential pair	Second
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the USB 2.0 differential pair – Position 1	Second	B7	Dn2	Negative half of the USB 2.0 differential pair – Position 2	Second
A7	Dn1	Negative half of the USB 2.0 differential pair – Position 1	Second	B6	Dp2	Positive half of the USB 2.0 differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10	SSRXn2	Negative half of second SuperSpeed RX differential pair	Second	B3	SSTXn2	Negative half of second SuperSpeed TX differential pair	Second
A11	SSRXp2	Positive half of second SuperSpeed RX differential pair	Second	B2	SSTXp2	Positive half of second SuperSpeed TX differential pair	Second
A12	GND	Ground return	First	B1	GND	Ground return	First

NOTES:

- 1) Contacts B6 and B7 should not be present in the USB Type-C plug. The receptacle side shall support the **USB 2.0** differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 may be shorted on the host/device as close to the receptacle as possible to minimize stub length. Dn1 and Dn2 may also be shorted. The maximum shorting trace length should not exceed 3,5 mm.
- 2) All VBUS pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
- 3) All Ground return pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).

The usage and assignments of the signals necessary for the support of only **USB 2.0** with the USB Type-C mating interface are defined in Table 3-5.

Table 3-5 – USB Type-C Receptacle Interface Pin Assignments for USB 2.0-only Support

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2				B11			
A3				B10			
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the USB 2.0 differential pair – Position 1	Second	B7	Dn2	Negative half of the USB 2.0 differential pair – Position 2	Second
A7	Dn1	Negative half of the USB 2.0 differential pair – Position 1	Second	B6	Dp2	Positive half of the USB 2.0 differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	Vbus	Bus Power	First
A10				B3			
A11				B2			
A12	GND	Ground return	First	B1	GND	Ground return	First

NOTES:

- 1) The unused contacts shall not be physically depopulated in the USB Type-C receptacle. Unused contact locations shall be electrically isolated from power, ground or signaling (i.e., not connected).
- 2) Contacts B6 and B7 should not be present in the USB Type-C plug. The receptacle side shall support the [USB 2.0](#) differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 may be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 may also be shorted. The maximum shorting trace length should not exceed 3,5 mm.
- 3) Contacts A8 and B8 (SBU1 and SBU2) shall be not connected unless required for a specified purpose (e.g., [Audio Adapter Accessory Mode](#)).
- 4) All VBUS pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
- 5) All Ground return pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).

3.3 Cable Construction and Wire Assignments

This section discusses the USB Type-C cables, including cable construction, wire assignments, and wire gauges.

3.3.1 Cable Construction (Informative)

Figure 3-18 illustrates an example of USB Full-Featured Type-C cable cross-section, using micro-coaxial wires for USB SuperSpeed. There are four groups of wires: USB D+/D- (typically unshielded twisted pairs (UTP)), USB SuperSpeed signal pairs (coaxial wires, twin-axial or shielded twisted pairs), sideband signal wires, and power and ground wires. In this example, the optional VCONN wire is shown whereas in Figure 3-19 the example is shown with the VCONN wire removed – the inclusion of VCONN or not relates to the implementation approach chosen for electronically marked cables (See Section 4.9).

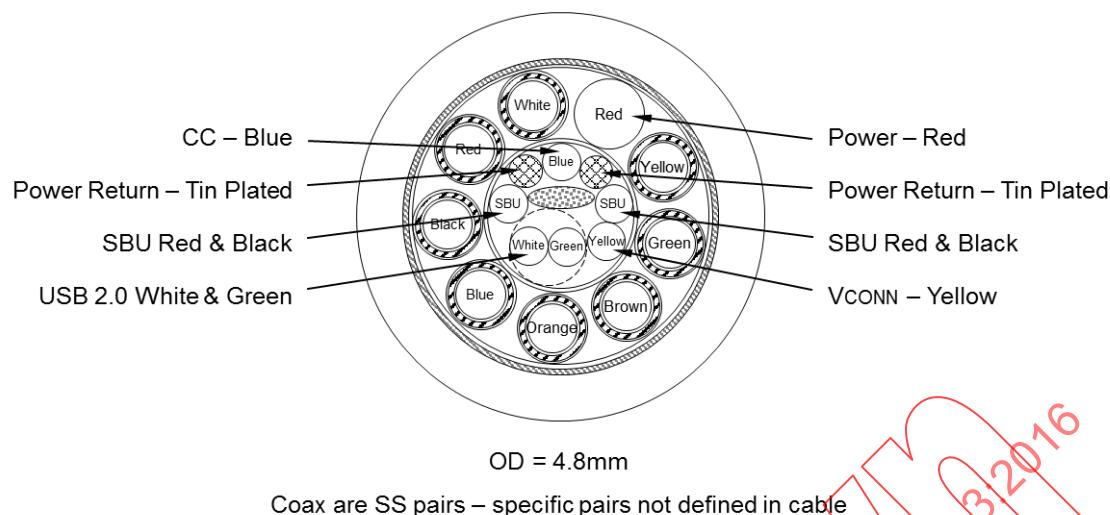


Figure 3-18 – Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example with VCONN

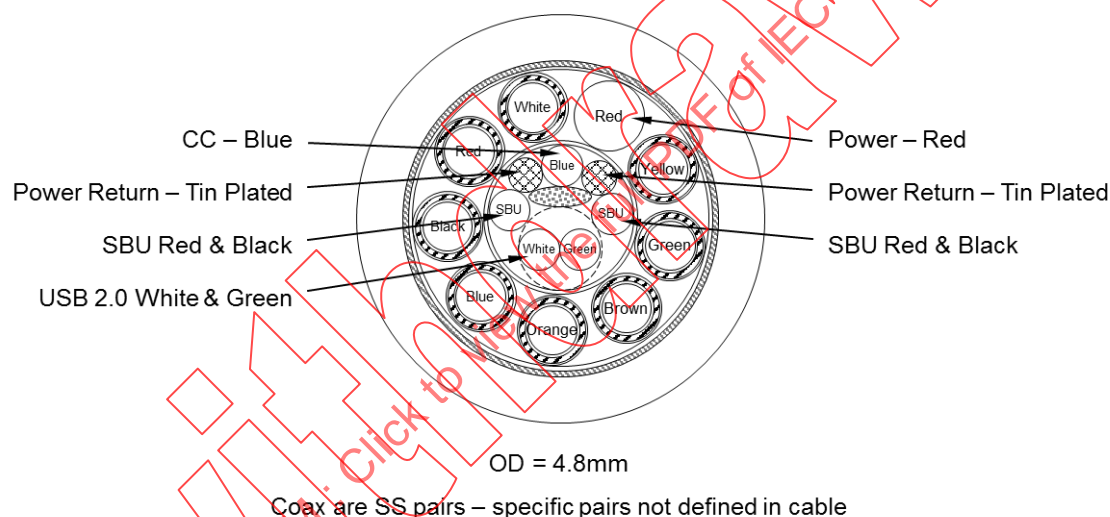


Figure 3-19 – Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example without VCONN

The USB D+/D– signal pair is intended to transmit the [USB 2.0](#) Low-Speed, Full-Speed and High-Speed signaling while the SuperSpeed signal pairs are used for [USB 3.1](#) SuperSpeed signaling. Shielding is needed for the SuperSpeed differential pairs for signal integrity and EMC performance.

3.3.2 Wire Assignments

Table 3-6 defines the full set of possible wires needed to produce all standard USB Type-C cables assemblies. For some cable assemblies, not all of these wires are used. For example, a USB Type-C cable that only provides [USB 2.0](#) functionality will not include wires 6–15.

Table 3-6 – USB Type-C Standard Cable Wire Assignments

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	CC	Configuration Channel
4	UTP_Dp	Unshielded twist pair, positive
5	UTP_Dn	Unshielded twist pair, negative
6	SDPp1	Shielded differential pair #1, positive
7	SDPn1	Shielded differential pair #1, negative
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDPp3	Shielded differential pair #3, positive
11	SDPn3	Shielded differential pair #3, negative
12	SDPp4	Shielded differential pair #4, positive
13	SDPn4	Shielded differential pair #4, negative
14	SBU_A	Sideband Use
15	SBU_B	Sideband Use
16	GND_PWRrt2	Ground for power return (optional)
17	PWR_VBUS2	VBUS power (optional)
18	PWR_VCONN	VCONN power (optional, see Section 4.9)
Braid	Shield	Cable external braid
NOTE:		
1) This table is based on the assumption that coaxial wire construction is used for all SDP's and there are no drain wires. The signal ground return is through the shields of the coaxial wires. If shielded twisted or twin-axial pairs are used, then drain wires are needed.		

Table 3-7 defines the full set of possible wires needed to produce USB Type-C to legacy cable assemblies. For some cable assemblies, not all of these wires are needed. For example, a USB Type-C to [USB 2.0](#) Standard-B cable will not include wires 5–10.

Table 3-7 – USB Type-C Cable Wire Assignments for Legacy Cables/Adapters

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	UTP_Dp	Unshielded twist pair, positive
4	UTP_Dn	Unshielded twist pair, negative
5	SDPp1	Shielded differential pair #1, positive
6	SDPn1	Shielded differential pair #1, negative
7	SDP1_Drain	Drain wire for SDPp1 and SDPn1
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDP2_Drain	Drain wire for SDPp2 and SDPn2
Braid	Shield	Cable external braid
NOTE:		
1) This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are needed and the signal ground return is through the shields of the coaxial wires.		

3.3.3 Wire Gauges and Cable Diameters (Informative)

This specification does not specify wire gauge. Table 3-8 and Table 3-9 list typical wire gauges for reference purposes only. A large gauge wire incurs less loss, but at the cost of cable diameter and flexibility. Multiple wires may be used for a single wire such as for VBUS or Ground. It is recommended to use the smallest possible wire gauges that meet the cable assembly electrical and mechanical requirements.

To maximize cable flexibility, all wires should be stranded and the cable outer diameter should be minimized as much as possible. A typical USB Full-Featured Type-C cable outer diameter may range from 4 mm to 6 mm while a typical [USB 2.0](#) Type-C cable outer diameter may range from 2 mm to 4 mm. A typical USB Type-C to [USB 3.1](#) legacy cable outer diameter may range from 3 mm to 5 mm.

Table 3-8 – Reference Wire Gauges for standard USB Type-C Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	CC	32-34
4	UTP_Dp	28-34
5	UTP_Dn	28-34
6	SDPp1	26-34
7	SDPn1	26-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDPp3	26-34
11	SDPn3	26-34
12	SDPp4	26-34
13	SDPn4	26-34
14	SBU_A	32-34
15	SBU_B	32-34
16	GND_PWRrt2	20-28
17	PWR_VBUS2	20-28
18	PWR_VCONN	32-34

Table 3-9 – Reference Wire Gauges for USB Type-C to Legacy Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	UTP_Dp	28-34
4	UTP_Dn	28-34
5	SDPp1	26-34
6	SDPn1	26-34
7	SDP1_Drain	28-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDP2_Drain	28-34

3.4 Standard USB Type-C Cable Assemblies

Two standard USB Type-C cable assemblies are defined and allowed by this specification. In addition, captive cables are allowed (see Section 3.4.3). Shielding (braid) is required to enclose all the wires in the USB Type-C cable. The shield shall be terminated to the plug metal shells. The shield should be physically connected to the plug metal shell as close to 360° as possible, to control EMC.

3.4.1 USB Full-Featured Type-C Cable Assembly

Figure 3-20 shows a USB Full-Featured Type-C standard cable assembly.

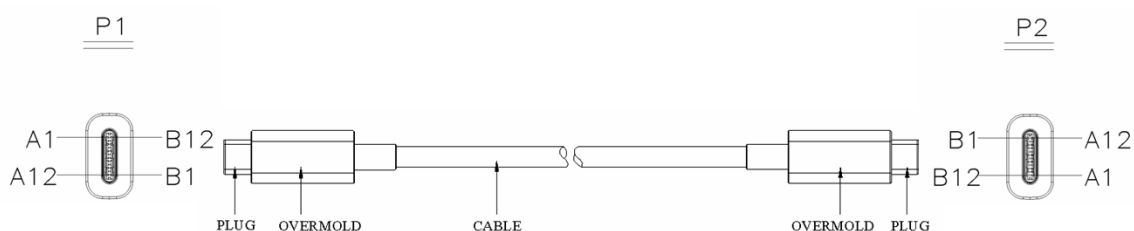


Figure 3-20 – USB Full-Featured Type-C Standard Cable Assembly

Table 3-10 defines the wire connections for the USB Full-Featured Type-C standard cable assembly.

Table 3-10 – USB Full-Featured Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	SSTXp1	6	SDPp1	B11	SSRXp1
A3	SSTXn1	7	SDPn1	B10	SSRXn1
B11	SSRXp1	8	SDPp2	A2	SSTXp1
B10	SSRXn1	9	SDPn2	A3	SSTXn1
B2	SSTXp2	10	SDPp3	A11	SSRXp2
B3	SSTXn2	11	SDPn3	A10	SSRXn2
A11	SSRXp2	12	SDPp4	B2	SSTXp2
A10	SSRXn2	13	SDPn4	B3	SSTXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Shell	Shield	Braid	Shield	Shell	Shield

NOTES:

- 1) This table is based on the assumption that coaxial wire construction is used for all SDP's and there are no drain wires. The shields of the coaxial wires are connected to the ground pins. If shielded twisted pair is used, then drain wires are needed and shall be connected to the GND pins.
- 2) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
- 3) Contacts B6 and B7 should not be present in the USB Type-C plug.
- 4) All VBUS pins shall be connected together within the USB Type-C plug. A 10 nF bypass capacitor (minimum voltage rating of 30 V) is required for the VBUS pin in the full-featured cable at each end of the cable. The bypass capacitor should be placed as close as possible to the power supply pad.
- 5) All GND pins shall be connected together within the USB Type-C plug.

3.4.2 USB 2.0 Type-C Cable Assembly

A **USB 2.0** Type-C standard cable assembly has the same form factor shown in Figure 3-20.

Table 3-11 defines the wire connections for the **USB 2.0** Type-C standard cable assembly.

Table 3-11 – USB 2.0 Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1	GND_PWRrt1	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
Shell	Shield	Braid	Shield	Shell	Shield
NOTES: 1) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9. 2) Contacts B6 and B7 should not be present in the USB Type-C plug. 3) All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is not required for the VBUS pin in the USB 2.0 Type-C cable. 4) All GND pins shall be connected together within the USB Type-C plug. 5) All USB Type-C plug pins that are not listed in this table shall be open (not connected).					

3.4.3 USB Type-C Captive Cable Assemblies

A captive cable assembly is a cable assembly that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end. The cable assembly that is hardwired is not detachable from the device.

The assembly wiring for captive USB Type-C cables follow the same wiring assignments as the standard cable assemblies (see Table 3-10 and Table 3-11) with the exception that the hardwired attachment on the device side substitutes for the USB Type-C Plug #2 end.

The CC wire in a captive cable shall be terminated and behave as appropriate to the function of the product to which it is captive (e.g. host or device).

This specification does not define how the hardwired attachment is physically done on the device side.

3.5 Legacy Cable Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy cable assemblies are defined. Only the cables defined within this specification are allowed.

For all legacy cable assemblies that support **USB PD** BFSK usage, the legacy plug shall be the **USB PD** version of the plug and appropriate **USB PD** cable marking is required.

3.5.1 USB Type-C to **USB 3.1** Standard-A Cable Assembly

Figure 3-21 shows a USB Type-C to **USB 3.1** Standard-A cable assembly.



Figure 3-21 – USB Type-C to USB 3.1 Standard-A Cable Assembly

Table 3-12 defines the wire connections for the USB Type-C to **USB 3.1** Standard-A cable assembly.

Table 3-12 – USB Type-C to **USB 3.1 Standard-A Cable Assembly Wiring**

USB Type-C Plug		Wire		USB 3.1 Standard-A plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC				
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D-
A2	SSTXp1	5	SDPp1	6	StdA_SSRX+
A3	SSTXn1	6	SDPn1	5	StdA_SSRX-
B11	SSRXp1	8	SDPp2	9	StdA_SSTX+
B10	SSRXn1	9	SDPn2	8	StdA_SSTX-
Shell	Shield	Braid	Shield	Shell	Shield

Notes:

- 1) This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
- 2) Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor R_p . See Section 4.5.3.2.2 and Table 4-13 for the functional description and value of R_p .
- 3) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
- 4) Contacts B6 and B7 should not be present in the USB Type-C plug.
- 5) All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be $10 \text{ nF} \pm 20 \%$ in cables which incorporate a USB Standard-A plug. The bypass capacitor shall be $100 \text{ pF} \pm 20 \%$ (minimum voltage rating of 30 V) in cables which incorporate a **USB PD** Standard-A plug. The bypass capacitor shall be placed as close as possible to the power supply pad.
- 6) All Ground return pins shall be connected together within the USB Type-C plug.
- 7) All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.2 USB Type-C to **USB 2.0** Standard-A Cable Assembly

Figure 3-22 shows a USB Type-C to **USB 2.0** Standard-A cable assembly.

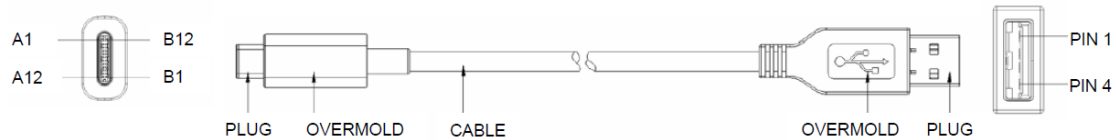


Figure 3-22 – USB Type-C to *USB 2.0* Standard-A Cable Assembly

Table 3-13 defines the wire connections for the USB Type-C to *USB 2.0* Standard-A cable assembly.

Table 3-13 – USB Type-C to *USB 2.0* Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Standard-A plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC				
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D-
Shell	Shield	Braid	Shield	Shell	Shield

NOTES:

1) Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp. See Section 4.5.3.2.2 and Table 4-13 for the functional description and value of Rp.

2) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.

3) Contacts B6 and B7 should not be present in the USB Type-C plug.

4) All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.

5) All Ground return pins shall be connected together within the USB Type-C plug.

6) All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.3 USB Type-C to *USB 3.1* Standard-B Cable Assembly

Figure 3-23 shows a USB Type-C to *USB 3.1* Standard-B cable assembly.

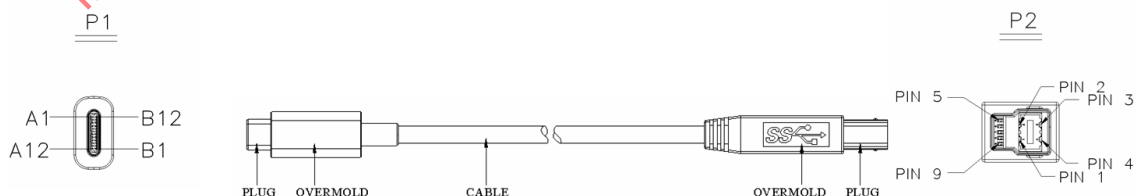


Figure 3-23 – USB Type-C to *USB 3.1* Standard-B Cable Assembly

Table 3-14 defines the wire connections for the USB Type-C to *USB 3.1* Standard-B cable assembly.

Table 3-14 – USB Type-C to *USB 3.1* Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Standard-B plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC				
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D-
A2	SSTXp1	5	SDPp1	9	StdB_SSRX+
A3	SSTXn1	6	SDPn1	8	StdB_SSRX-
B11	SSRXp1	8	SDPp2	6	StdB_SSTX+
B10	SSRXn1	9	SDPn2	5	StdB_SSTX-
Shell	Shield	Braid	Shield	Shell	Shield

NOTES:

- 1) Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor R_d . See Section 4.5.3.2.1 and Table 4-14 for the functional description and value of R_d .
- 2) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
- 3) This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
- 4) Contacts B6 and B7 should not be present in the USB Type-C plug.
- 5) All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be $10\text{nF} \pm 20\%$ in cables which incorporate a USB Standard-B plug. The bypass capacitor shall be $100\text{pF} \pm 20\%$ (minimum voltage rating of 30V) in cables which incorporate a *USB PD* Standard-B plug. The bypass capacitor shall be placed as close as possible to the power supply pad.
- 6) All Ground return pins shall be connected together within the USB Type-C plug.
- 7) All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.4 USB Type-C to *USB 2.0* Standard-B Cable Assembly

Figure 3-24 shows a USB Type-C to *USB 2.0* Standard-B cable assembly.

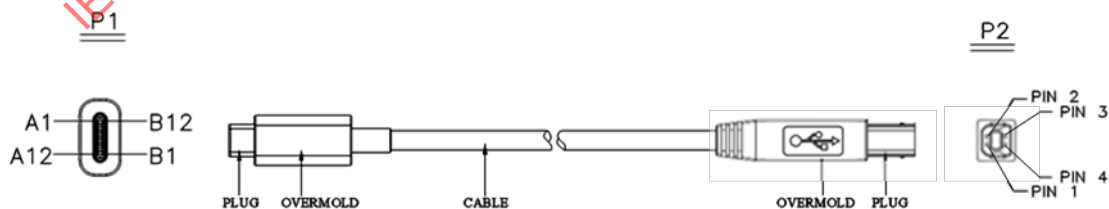


Figure 3-24 – USB Type-C to *USB 2.0* Standard-B Cable Assembly

Table 3-15 defines the wire connections for the USB Type-C to *USB 2.0* Standard-B cable assembly.

Table 3-15 – USB Type-C to *USB 2.0* Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Standard-B plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC				
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D-
Shell	Shield	Braid	Shield	Shell	Shield

NOTES:

- 1) Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor R_d . See Section 4.5.3.2.1 and Table 4-14 for the functional description and value of R_d .
- 2) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
- 3) Contacts B6 and B7 should not be present in the USB Type-C plug.
- 4) All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
- 5) All Ground return pins shall be connected together within the USB Type-C plug.
- 6) All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.5 USB Type-C to *USB 2.0* Mini-B Cable Assembly

Figure 3-25 shows a USB Type-C to *USB 2.0* Mini-B cable assembly.

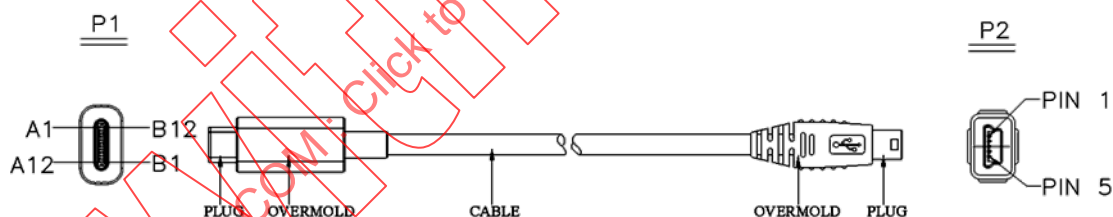


Figure 3-25 – USB Type-C to *USB 2.0* Mini-B Cable Assembly

Table 3-16 defines the wire connections for the USB Type-C to *USB 2.0* Mini-B cable assembly.

Table 3-16 – USB Type-C to *USB 2.0* Mini-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Mini-B plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D–
				4	ID
Shell	Shield	Braid	Shield	Shell	Shield

NOTES:

- 1) Pin A5 of the USB Type-C plug shall be connected to GND through a resistor R_d . See Section 4.5.3.2.1 and Table 4-14 for the functional description and value of R_d .
- 2) Contacts B6 and B7 should not be present in the USB Type-C plug.
- 3) All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
- 4) All Ground return pins shall be connected together within the USB Type-C plug.
- 5) Pin 4 (ID) of the *USB 2.0* Mini-B plug shall be terminated as defined in the applicable specification for the cable type.
- 6) All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.6 USB Type-C to *USB 3.1* Micro-B Cable Assembly

Figure 3-26 shows a USB Type-C to *USB 3.1* Micro-B cable assembly.

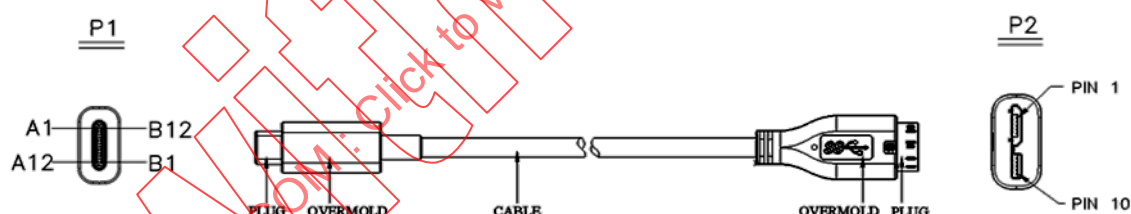


Figure 3-26 – USB Type-C to *USB 3.1* Micro-B Cable Assembly

Table 3-17 defines the wire connections for the USB Type-C to *USB 3.1* Micro-B cable assembly.

Table 3-17 – USB Type-C to *USB 3.1* Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Micro-B plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	5 8	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC				
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D-
A2	SSTXp1	5	SDPp1	10	MicB_SSRX+
A3	SSTXn1	6	SDPn1	9	MicB_SSRX-
B11	SSRXp1	8	SDPp2	7	MicB_SSTX+
B10	SSRXn1	9	SDPn2	6	MicB_SSTX-
				4	ID
Shell	Shield	Braid	Shield	Shell	Shield

NOTES:

- 1) Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor R_d . See Section 4.5.3.2.1 and Table 4-14 for the functional description and value of R_d .
- 2) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
- 3) This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
- 4) Contacts B6 and B7 should not be present in the USB Type-C plug.
- 5) All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be $10\text{nF} \pm 20\%$ in cables which incorporate a USB Micro-B plug. The bypass capacitor shall be $100\text{pF} \pm 20\%$ (minimum voltage rating of 30V) in cables which incorporate a *USB PD* Micro-B plug. The bypass capacitor should be placed as close as possible to the power supply pad.
- 6) All Ground return pins shall be connected together within the USB Type-C plug.
- 7) Pin 4 (ID) of the *USB 3.1* Micro-B plug shall be terminated as defined in the applicable specification for the cable type.
- 8) All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.7 USB Type-C to *USB 2.0* Micro-B Cable Assembly

Figure 3-27 shows a USB Type-C to *USB 2.0* Micro-B cable assembly.

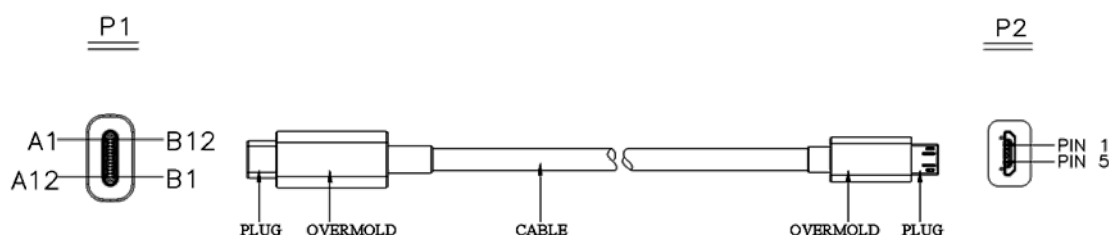


Figure 3-27 – USB Type-C to *USB 2.0* Micro-B Cable Assembly

Table 3-18 defines the wire connections for the USB Type-C to **USB 2.0** Micro-B cable assembly.

Table 3-18 – USB Type-C to **USB 2.0 Micro-B Cable Assembly Wiring**

USB Type-C Plug		Wire		USB 2.0 Micro-B plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC				
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D-
				4	ID
Shell	Shield	Braid	Shield	Shell	Shield
NOTES: 1) Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor R_d. See Section 4.5.3.2.1 and Table 4-14 for the functional description and value of R_d. 2) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9. 3) Contacts B6 and B7 should not be present in the USB Type-C plug. 4) All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable. 5) All Ground return pins shall be connected together within the USB Type-C plug. 6) Pin 4 (ID) of the USB 2.0 Micro-B plug shall be terminated as defined in the applicable specification for the cable type. 7) All USB Type-C plug pins that are not listed in this table shall be open (not connected).					

3.6 Legacy Adapter Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy adapter assemblies are defined. Only the adapter assemblies defined in this specification are allowed.

3.6.1 USB Type-C to **USB 3.1** Standard-A Receptacle Adapter Assembly

Figure 3-28 shows a USB Type-C to **USB 3.1** Standard-A receptacle adapter assembly. This cable assembly is defined for direct connect to a USB device (e.g., a thumb drive). System functionality of using this adaptor assembly together with another USB cable assembly is not guaranteed.

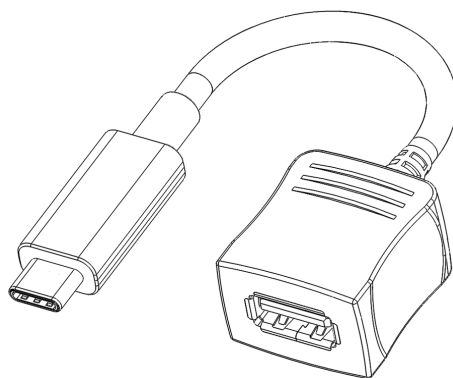


Figure 3-28 – USB Type-C to **USB 3.1 Standard-A Receptacle Adapter Assembly**

Table 3-19 defines the wire connections for the USB Type-C to **USB 3.1** Standard-A receptacle adapter assembly.

Table 3-19 – USB Type-C to **USB 3.1 Standard-A Receptacle Adapter Assembly Wiring**

USB Type-C Plug		USB 3.1 Standard-A receptacle	
Pin	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC		
B5	VCONN		
A6	Dp1	3	D+
A7	Dn1	2	D-
A2	SSTXp1	9	StdA_SSTX+
A3	SSTXn1	8	StdA_SSTX-
B11	SSRXp1	6	StdA_SSRX+
B10	SSRXn1	5	StdA_SSRX-
Shell	Shield	Shell	Shield

NOTES:

- 1) Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor R_d . See Section 4.5.3.2.1 and Table 4-14 for the functional description and value of R_d .
- 2) Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this adapter. See Section 4.9.
- 3) This table is based on the assumption that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present and the shields of the coaxial wires are connected to the ground pins.
- 4) Contacts B6 and B7 should not be present in the USB Type-C plug.
- 5) All VBUS pins shall be connected together within the USB Type-C plug. A 10 nF bypass capacitor is required for the VBUS pin in the USB Type-C plug end of the cable. The bypass capacitor should be placed as close as possible to the power supply pad. A bypass capacitor is not required for the VBUS pin in the Standard-A receptacle.
- 6) All Ground return pins shall be connected together within the USB Type-C plug.
- 7) All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.6.2 USB Type-C to **USB 2.0** Micro-B Receptacle Adapter Assembly

Figure 3-29 shows a USB Type-C to **USB 2.0** Micro-B receptacle adapter assembly.

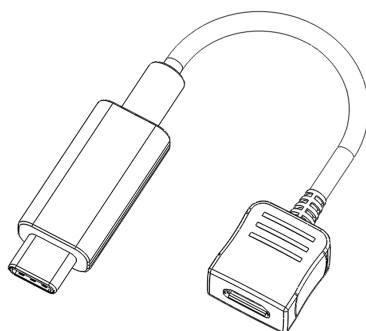


Figure 3-29 – USB Type-C to **USB 2.0 Micro-B Receptacle Adapter Assembly**

Table 3-20 defines the wire connections for the USB Type-C to **USB 2.0** Micro-B receptacle adapter assembly.

Table 3-20 – USB Type-C to **USB 2.0 Micro-B Receptacle Adapter Assembly Wiring**

USB Type-C Plug		USB 2.0 Micro-B receptacle	
Pin	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	5	GND
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC		
A6	Dp1	3	D+
A7	Dn1	2	D–
		4	ID
Shell	Shield	Shell	Shield
NOTES: 1) Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor R_p . See Section 4.5.3.2.2 and Table 4-13 for the functional description and value of R_p . 2) Contacts B6 and B7 should not be present in the USB Type-C plug. 3) All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins at the Micro-B receptacle end of this cable. 4) All Ground return pins shall be connected together within the USB Type-C plug. 5) All USB Type-C plug pins that are not listed in this table shall be open (not connected).			

3.7 Electrical Characteristics

This section defines the USB Type-C raw cable, connector, and cable assembly electrical requirements, including signal integrity, shielding effectiveness, and DC requirements. Chapter 4 defines additional requirements regarding functional signal definition, host/device discovery and configuration, and power delivery.

Unless otherwise specified, all measurements are made at a temperature of 15° to 35 °C, a relative humidity of 25 % to 85 %, and an atmospheric pressure of 86 to 106 kPa and all S-parameters are normalized with an 85 Ω differential impedance.

3.7.1 Raw Cable (Informative)

Informative raw cable electrical performance targets are provided to help cable assembly manufacturers manage the procurement of raw cable. These targets are not part of the USB Type-C compliance requirements. The normative requirement is that the cable assembly meets the performance characteristics specified in Sections 3.7.3, 3.7.4, and 3.7.5.

The differential characteristic impedance for shielded differential pairs is recommended to be $90 \Omega \pm 5 \Omega$. The single-ended characteristic impedance of coaxial wires is recommended to be $45 \Omega \pm 3 \Omega$. The impedance should be evaluated using a 200 ps (10%-90%) rise time; a faster rise time is not necessary for raw cable since it will make cable test fixture discontinuities more prominent.

3.7.1.1 Intra-Pair Skew (Informative)

The intra-pair skew for a differential pair is recommended to be less than 10 ps/m. It should be measured with a Time Domain Transmission (TDT) in a differential mode using a 200 ps (10 %-90 %) rise time with a crossing at 50 % of the input voltage.

3.7.1.2 Differential Insertion Loss (Informative)

Cable loss depends on wire gauges, plating and dielectric materials. Table 3-21 and Table 3-22 show examples of differential insertion losses.

Table 3-21 – Differential Insertion Loss Examples for USB SuperSpeed with Twisted Pair Construction

Frequency	34AWG	32AWG	30AWG	28AWG
0,625 GHz	–1,8 dB/m	–1,4 dB/m	–1,2 dB/m	–1,0 dB/m
1,25 GHz	–2,5 dB/m	–2,0 dB/m	–1,7 dB/m	–1,4 dB/m
2,50 GHz	–3,7 dB/m	–2,9 dB/m	–2,5 dB/m	–2,1 dB/m
5,00 GHz	–5,5 dB/m	–4,5 dB/m	–3,9 dB/m	–3,1 dB/m
7,50 GHz	–7,0 dB/m	–5,9 dB/m	–5,0 dB/m	–4,1 dB/m
10,00 GHz	–8,4 dB/m	–7,2 dB/m	–6,1 dB/m	–4,8 dB/m
12,50 GHz	–9,5 dB/m	–8,2 dB/m	–7,3 dB/m	–5,5 dB/m
15,00 GHz	–11,0 dB/m	–9,5 dB/m	–8,7 dB/m	–6,5 dB/m

Table 3-22 – Differential Insertion Loss Examples for USB SuperSpeed with Coaxial Construction

Frequency	34AWG	32AWG	30AWG	28AWG
0,625 GHz	–1,8 dB/m	–1,5 dB/m	–1,2 dB/m	–1,0 dB/m
1,25 GHz	–2,8 dB/m	–2,2 dB/m	–1,8 dB/m	–1,3 dB/m
2,50 GHz	–4,2 dB/m	–3,4 dB/m	–2,7 dB/m	–1,9 dB/m
5,00 GHz	–6,1 dB/m	–4,9 dB/m	–4,0 dB/m	–3,1 dB/m
7,50 GHz	–7,6 dB/m	–6,5 dB/m	–5,2 dB/m	–4,2 dB/m
10,0 GHz	–8,8 dB/m	–7,6 dB/m	–6,1 dB/m	–4,9 dB/m
12,5 GHz	–9,9 dB/m	–8,6 dB/m	–7,1 dB/m	–5,7 dB/m
15,0 GHz	–12,1 dB/m	–10,9 dB/m	–9,0 dB/m	–6,5 dB/m

3.7.2 Mated Connector (Normative)

The mated connector as defined in this specification for USB Type-C consists of a receptacle mounted on a PCB, representing how the receptacle is used in a product, and a test plug also mounted on a PCB (paddle card) without cable. This is illustrated in Figure 3-30. Note that the test plug is used in host/device TX/RX testing also.

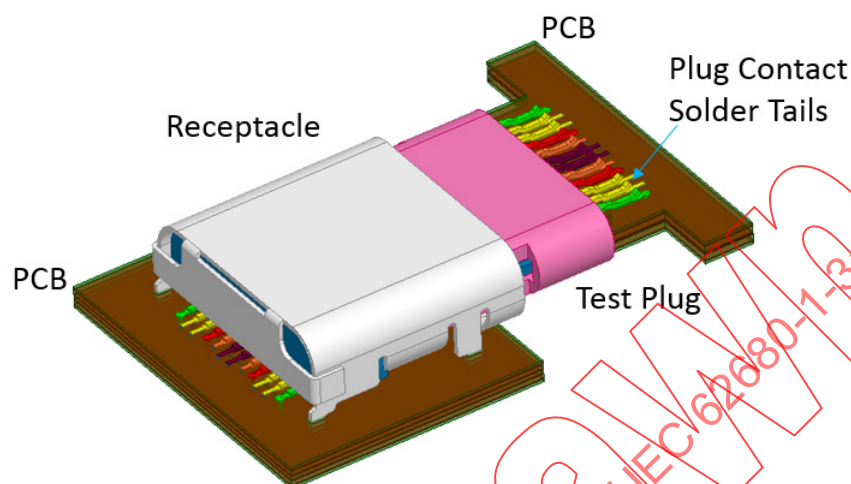


Figure 3-30 – Illustration of USB Type-C Mated Connector

3.7.2.1 Differential Impedance (Informative)

The mated connector impedance target is specified to minimize reflection from the connector. The differential impedance of a mated connector should be within $85\ \Omega \pm 9\ \Omega$, as seen from a 40 ps (20 %-80 %) rise time. The impedance profile of a mated connector should fall within the limits shown in Figure 3-31.

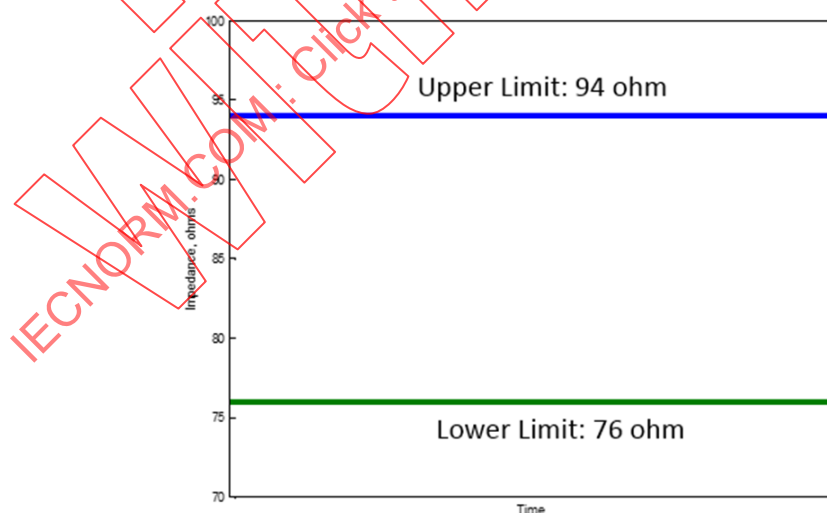
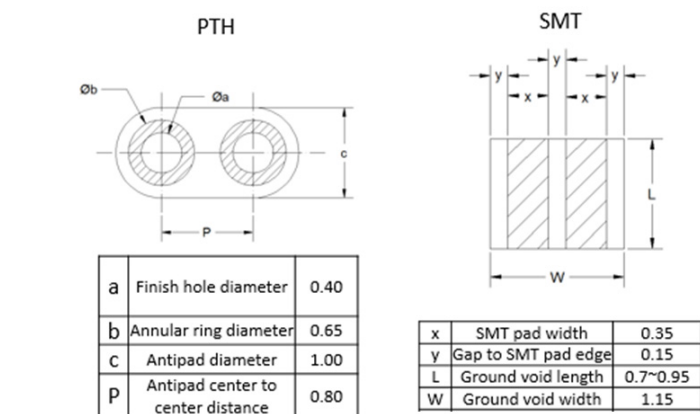


Figure 3-31 – Recommended Impedance Limits of a USB Type-C Mated Connector

The PCB stack up, lead geometry, and solder pad geometry should be modeled in 3D field-solver to optimize electrical performance. Example ground voids under signal pads are shown in Figure 3-32 based on pad geometry, mounting type, and PCB stack-up shown.



Unit: mm

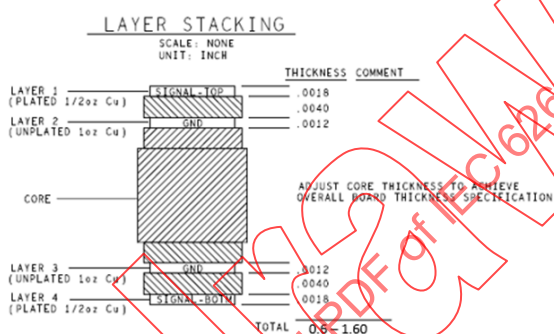


Figure 3-32 – Recommended Ground Void Dimensions for USB Type-C Receptacle

3.7.2.2 Differential Insertion Loss (Informative)

The differential insertion loss measures the differential signal energy transmitted through the mated connector. Figure 3-33 shows the differential insertion loss limit, which is defined by the following vertices: (100 MHz, -0.25 dB), (2.5 GHz, -0.35 dB), (5 GHz, -0.45 dB), (10 GHz, -0.75 dB) and (15 GHz, -1.85 dB).

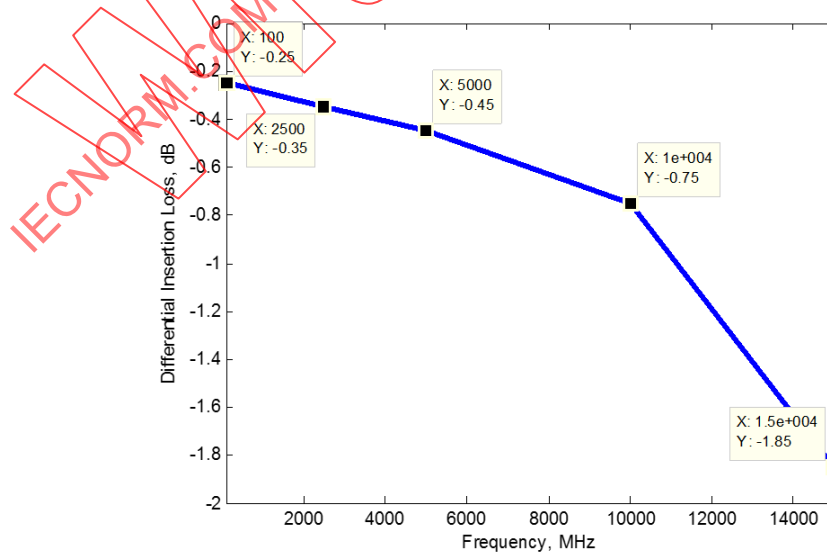


Figure 3-33 – Recommended Differential Insertion Loss Limits

3.7.2.3 Differential Return Loss (Informative)

The differential return loss measures the differential signal reflection from the mated connector. Figure 3-34 shows the differential return loss limits as defined by the following vertices: (100 MHz, -20 dB), (5 GHz, -20 dB), (10 GHz, -13 dB), and (15 GHz, -6 dB).

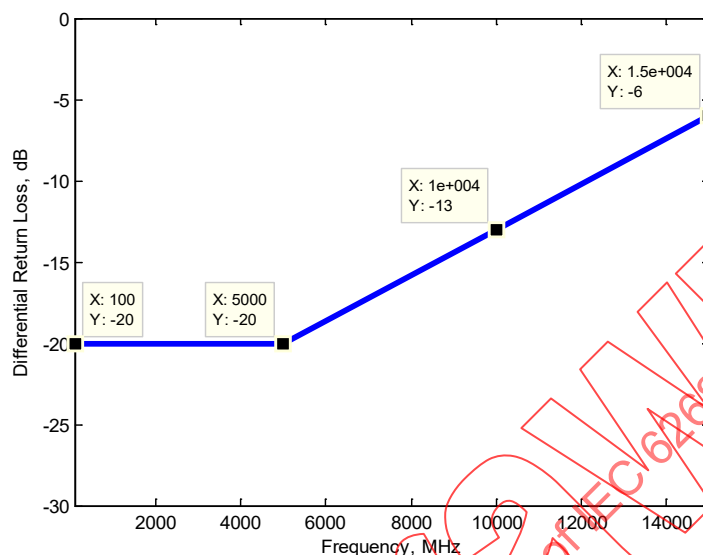


Figure 3-34 – Recommended Differential Return Loss Limits

3.7.2.4 Differential Near-End and Far-End Crosstalk between SuperSpeed Pairs (Informative)

The differential crosstalk measures the unwanted coupling between differential pairs. Both near-end crosstalk and far-end crosstalk for mated connector pairs are specified, as shown in Figure 3-35. The recommended limit is defined by the following vertices: (100 MHz, -40 dB), (5 GHz, -40 dB), (10 GHz, -36 dB), and (15 GHz, -30 dB).

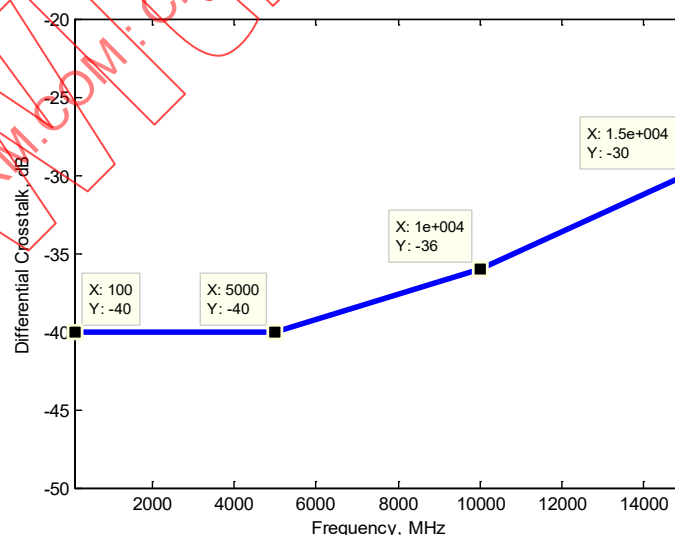


Figure 3-35 – Recommended Differential Crosstalk Limits between SuperSpeed Pairs

3.7.2.5 Differential Crosstalk between D+/D– and SuperSpeed Pairs (Informative)

The differential near-end and far-end crosstalk between the D+/D– pair and the SuperSpeed pairs in mated connectors should be managed not to exceed the limit shown in Figure 3-36; the limit is defined by the following points: (100 MHz, –40 dB), (5 GHz, –40 dB), and (7,5 GHz, –36 dB).

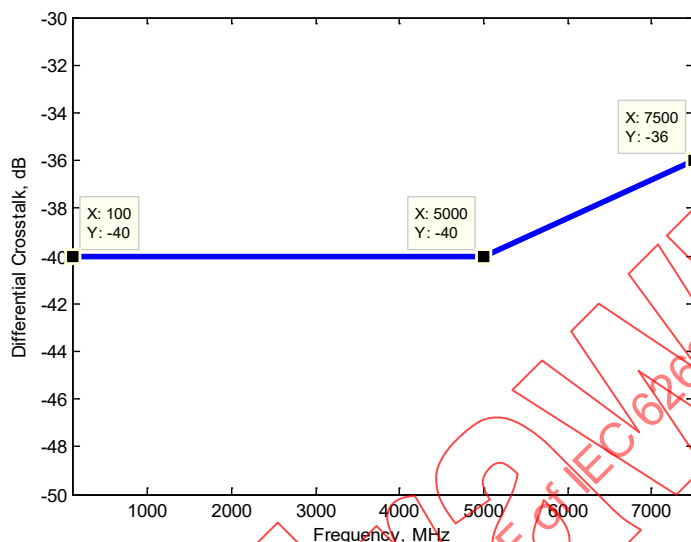


Figure 3-36 – Recommended Differential Near-End and Far-End Crosstalk Limits between D+/D– Pair and SuperSpeed Pairs

3.7.2.6 Differential-to-Common-Mode Conversion (Informative)

Common mode noise is related to EMC performance. Figure 3-37 illustrates the recommended mode conversion limits for mated connector pairs as defined by the following vertices: (100 MHz, –30 dB), (6 GHz, –30 dB), and (10 GHz, –25 dB).

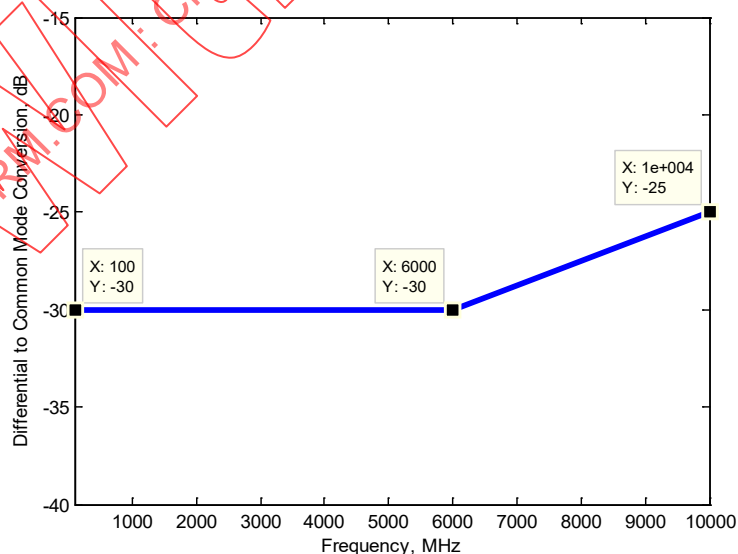


Figure 3-37 – Recommended Limits for Differential-to-Common-Mode Conversion

3.7.3 USB Type-C to Type-C Passive Cable Assemblies (Normative)

A USB Type-C to Type-C cable assembly shall be tested using a test fixture with the receptacle tongue fabricated in the test fixture. This is illustrated in Figure 3-38. The USB Type-C receptacles are not present in the test fixture. Hosts and devices should account for the additional signal degradation the receptacle introduces.

The requirements are for the entire signal path of the cable assembly mated with the fixture PCB tongues, not including lead-in PCB traces. As illustrated in Figure 3-38, the measurement is between TP1 (test point 1) and TP2 (test point 2). Refer to documentation located at [Cable Assembly and Connector Test Requirements](#) page on the [USB-IF](#) website for a detailed description of a standardized test fixture.

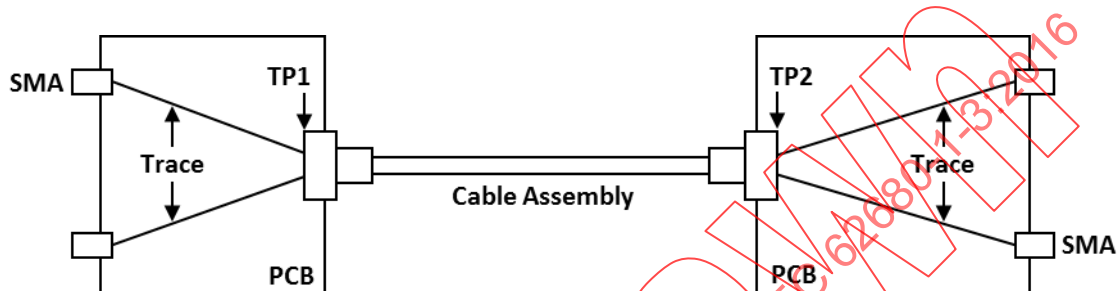


Figure 3-38 – Illustration of Test Points for a Mated Cable Assembly

The cable assembly requirements are divided into informative and normative requirements. The informative requirements are provided as design targets for cable assembly manufacturers. The normative requirements are the pass/failure criteria for cable assembly compliance.

3.7.3.1 Recommended USB SuperSpeed Passive Cable Assembly Characteristics

3.7.3.1.1 Differential Insertion Loss (Informative)

Figure 3-39 shows the differential insertion loss limit for a [USB 3.1](#) Gen 2 Type-C cable assembly, which is defined by the following vertices: (100 MHz, -2 dB), (2,5 GHz, -4 dB), (5,0 GHz, -6 dB), (10 GHz, -11 dB) and (15 GHz, -20 dB).

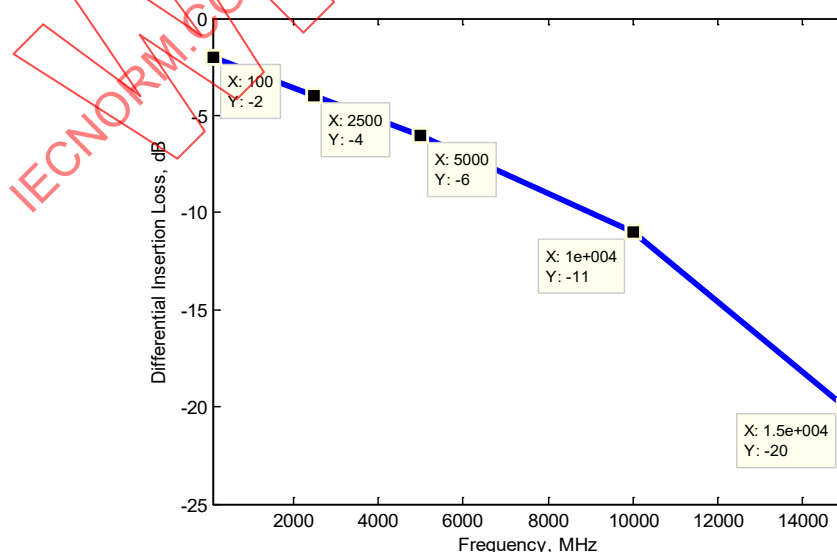


Figure 3-39 – Recommended Differential Insertion Loss Requirement

3.7.3.1.2 Differential Return Loss (Informative)

Figure 3-40 shows the differential return loss limit, which is defined by the following points: (100 MHz, -18 dB), (5 GHz, -18 dB), (10 GHz, -12 dB), and (15 GHz, -5 dB).

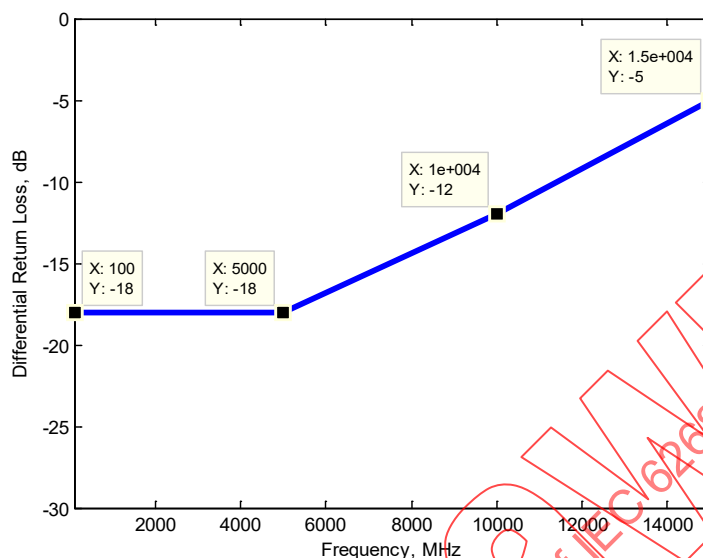


Figure 3-40 – Recommended Differential Return Loss Requirement

3.7.3.1.3 Differential Near-End and Far-End Crosstalk between SuperSpeed Pairs (Informative)

Both the near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are specified, as shown in Figure 3-41. The DDNEXT/DDFEXT limits are defined by the following vertices: (100 MHz, -37 dB), (5 GHz, -37 dB), (10 GHz, -32 dB), and (15 GHz, -25 dB).

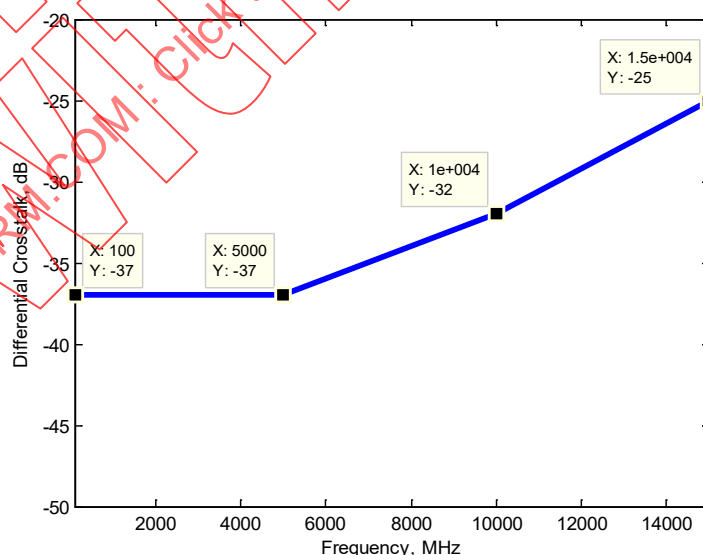


Figure 3-41 – Recommended Differential Crosstalk Requirement

3.7.3.1.4 Differential Crosstalk between USB D+/D– and USB SuperSpeed Pairs (Informative)

The differential near-end and far-end crosstalk between the USB D+/D– pair and the USB SuperSpeed pairs should be managed not to exceed the limits shown in Figure 3-42. The limits are defined by the following points: (100 MHz, –35 dB), (5 GHz, –35 dB), and (7,5 GHz, –30 dB).

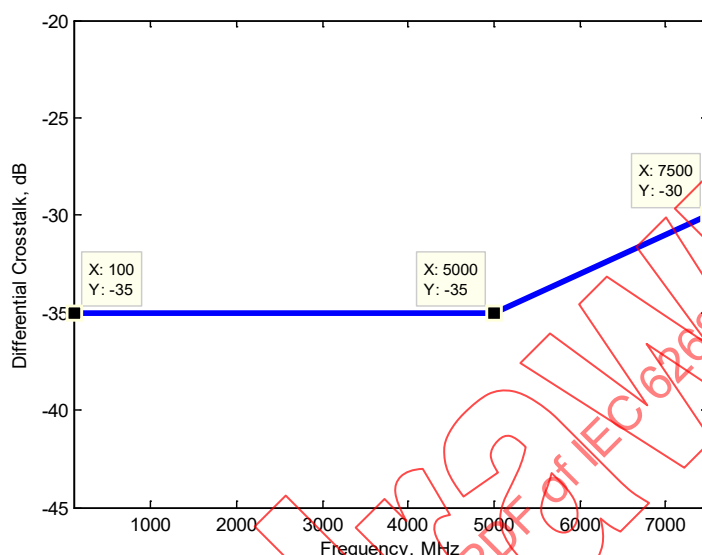


Figure 3-42 – Recommended Differential Near-End and Far-End Crosstalk Requirement between USB D+/D– Pair and USB SuperSpeed Pair

3.7.3.2 Normative SuperSpeed Passive Cable Assembly Requirements

The integrated parameters are used for cable assembly compliance (except for insertion loss and differential-to-common-mode conversion) to avoid potential rejection of a functioning cable assembly that may fail the traditional S-parameters spec at a few frequencies.

3.7.3.2.1 Insertion Loss Fit at Nyquist Frequencies (Normative)

The insertion loss fit at Nyquist frequency measures the attenuation of the cable assembly. To obtain the insertion loss fit at Nyquist frequency, the measured cable assembly differential insertion loss is fitted with a smooth function. A standard fitting algorithm and tool shall be used to extract the insertion loss fit at Nyquist frequencies. Refer to documentation located at [Cable Assembly and Connector Test Requirements](#) page on the [USB-IF](#) website for a more detailed description about insertion loss fit.

Figure 3-43 illustrates an example of a measured cable assembly insertion loss fitted with a smooth function; the insertion loss fit at the Nyquist frequency of USB SuperSpeed Gen 2 (5,0 GHz) is –5,8 dB.

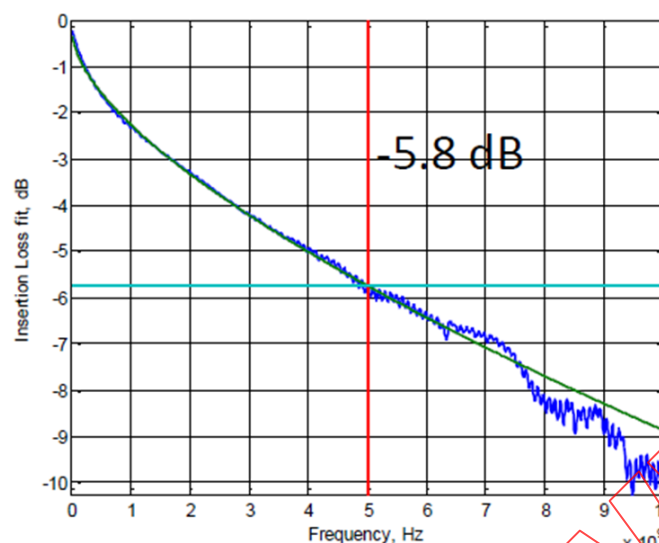


Figure 3-43 – Illustration of Insertion Loss Fit at Nyquist Frequency

The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:

- ≥ -4 dB at 2,5 GHz,
- ≥ -6 dB at 5 GHz, and
- ≥ -11 dB at 10 GHz.

2,5 GHz, 5,0 GHz and 10 GHz are the Nyquist frequencies for USB SuperSpeed Gen 1, USB SuperSpeed Gen 2, and a possible future 20 Gbps USB data rate, respectively.

The USB SuperSpeed Gen 1-only Type-C to Type-C cable assembly is allowed by this specification and shall comply with the following insertion loss fit at Nyquist frequency requirements:

- $\geq -7,0$ dB at 2,5 GHz, and
- > -12 dB at 5 GHz.

This insertion fit at Nyquist frequency allows the USB SuperSpeed Gen 1-only Type-C to Type-C cable assembly to achieve an overall length of approximately 2 meters.

3.7.3.2.2 Integrated Multi-reflection (Normative)

The insertion loss deviation, ILD, is defined as

$$ILD(f) = IL(f) - ILfit(f)$$

It measures the ripple of the insertion loss, caused by multiple reflections inside the cable assembly (mated with the fixture). The integration of $ILD(f)$ is called the integrated multi-reflection (IMR):

$$IMR = dB \left(\sqrt{\frac{\int_0^{f_{max}} |ILD(f)|^2 |V_{in}(f)|^2 df}{\int_0^{f_{max}} |V_{in}(f)|^2 df}} \right)$$

where $f_{max} = 12.5$ GHz and $V_{in}(f)$ is the input trapezoidal pulse spectrum, defined in Figure 3-44.

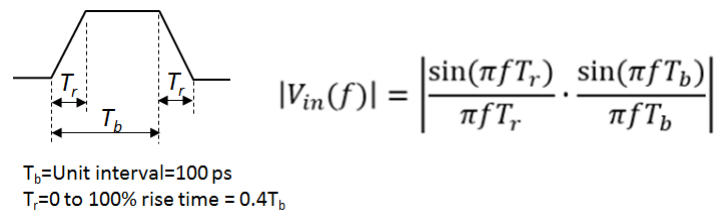


Figure 3-44 – Input Pulse Spectrum

IMR has dependency on ILfitatNq. More IMR may be tolerated when ILfitatNq decreases. The IMR limit is specified as a function of ILfitatNq:

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 23.392$$

This is plotted in Figure 3-45.

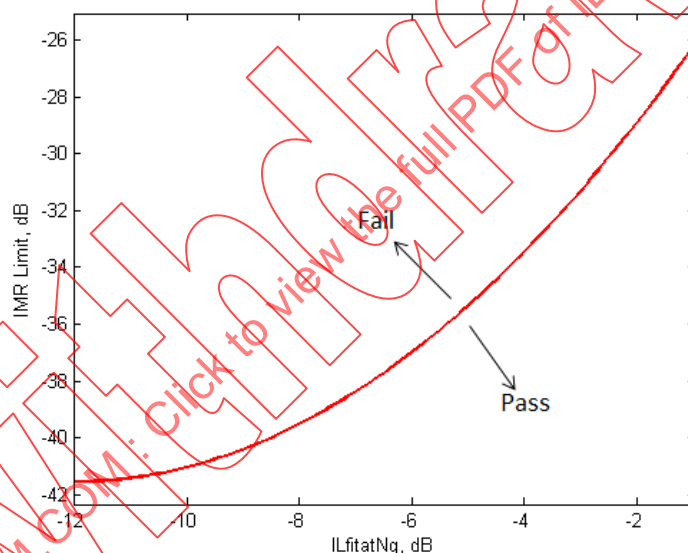


Figure 3-45 – IMR Limit as Function of ILfitatNq

3.7.3.2.3 Integrated Crosstalk between SuperSpeed Pairs (Normative)

The integrated crosstalk between all USB SuperSpeed pairs is calculated with the equations below:

$$INEXT = dB \left(\sqrt{\frac{\int_0^{f_{max}} |V_{in}(f)|^2 (|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) df + |V_{dd}(f)|^2 |NEXT_d(f)|^2 df}{\int_0^{f_{max}} |V_{in}(f)|^2 df}} \right)$$

$$IFEXT = dB \left(\sqrt{\frac{\int_0^{f_{max}} |V_{in}(f)|^2 (|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) df + |V_{dd}(f)|^2 |FEXT_d(f)|^2 df}{\int_0^{f_{max}} |V_{in}(f)|^2 df}} \right)$$

where $NEXT(f)$, $FEXT(f)$, and $C2D(f)$ are the measured near-end and far-end crosstalk between USB SuperSpeed pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude. $NEXT_d(f)$ and $FEXT_d(f)$ are, respectively, the near-end and far-end crosstalk from the D+/D- pair to SuperSpeed pairs. $V_{dd}(f)$ is the input pulse spectrum evaluated using the equation in Figure 3-44 with $T_b=2.08$ ns.

The integration shall be done for each NEXT and FEXT between USB SuperSpeed pairs located at A2, A3 to B10, B11 and B2, B3 to A10, A11 (See Figure 2-2). Coupling between other combinations of USB SuperSpeed pairs is comparatively lower. The largest values of INEXT and IFEXT shall meet the following requirements:

- $INEXT \leq -40$ dB,
- $IFEXT \leq -40$ dB.

3.7.3.2.4 Integrated Return Loss (Normative)

The integrated return loss (IRL) manages the reflection between the cable assembly and the rest of the system (host and device). It is defined as:

$$IRL = dB \left(\sqrt{\frac{\int_0^{f_{max}} |V_{in}(f)|^2 |SDD_{21}(f)|^2 (|SDD_{11}(f)|^2 + |SDD_{22}(f)|^2) df}{\int_0^{f_{max}} |V_{in}(f)|^2 df}} \right)$$

where $SDD_{21}(f)$ is the measured cable assembly differential insertion loss, $SDD_{11}(f)$ and $SDD_{22}(f)$ are the measured cable assembly return losses on the left and right sides, respectively, of a differential pair.

The IRL also has a strong dependency on $IL_{fitatNq}$, and its limit is specified as a function of $IL_{fitatNq}$:

$$IRL \leq 0.046 \cdot IL_{fitatNq}^2 + 1.812 \cdot IL_{fitatNq} - 10.784.$$

It is shown in Figure 3-46.

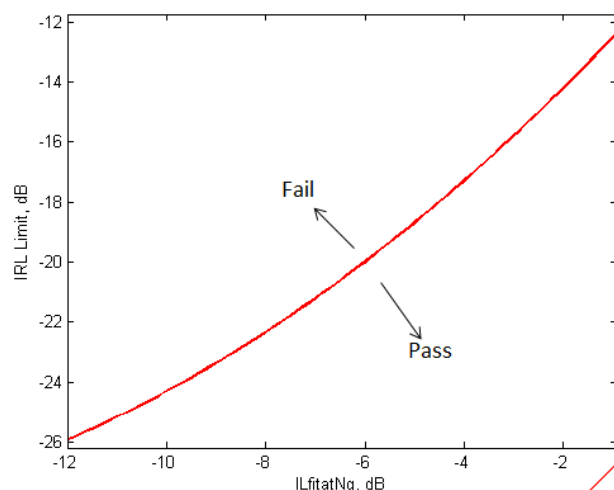


Figure 3-46 – IRL Limit as Function of ILfitatNg

3.7.3.2.5 Differential-to-Common-Mode Conversion (Normative)

The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Figure 3-47 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to -20 dB from 100 MHz to 10 GHz.

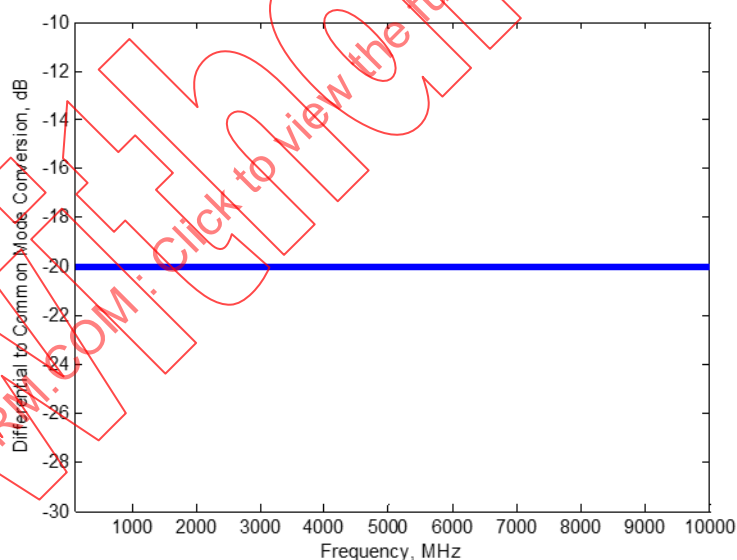


Figure 3-47 – Differential-to-Common-Mode Conversion Requirement

3.7.3.3 Low-Speed Signal Requirements (Normative)

This section specifies the low speed signal requirements including the impedance for CC and SBU wires and the coupling among CC, USB D+/D-, VBUS and SBU.

The CC wire shall have a characteristic impedance of 32 Ω to 93 Ω . The SBU wire shall have a characteristic impedance of 32 Ω to 53 Ω . The CC and SBU wires may be unshielded or shielded.

Coupling or crosstalk, both near-end and far-end, among the low speed signals shall be controlled. Table 3-23 shows the matrix of couplings specified.

Table 3-23 – Coupling Matrix for Low Speed Signals

Coupling Matrix	D+/D- (DF)	V _{bus}	SBU_B/SBU_A
CC	FF, CT	FF, CT	FF
D+/D- (DF)	N/A	FF, CT	FF
SBU_A/SBU_B	FF	FF	FF

DF: Differential; FF: Full-featured cable; CT: Charge-through cable (including USB 2.0 function).

3.7.3.3.1 CC to USB D+/D- (Normative)

The differential coupling between the CC and D+/D- shall be below the limit shown in Figure 3-48. The limit is defined with the vertices of (0.3 MHz, -60.5 dB), (1 MHz, -50 dB), (10 MHz, -30 dB), (16 MHz, -26 dB) and (100 MHz, -26 dB).

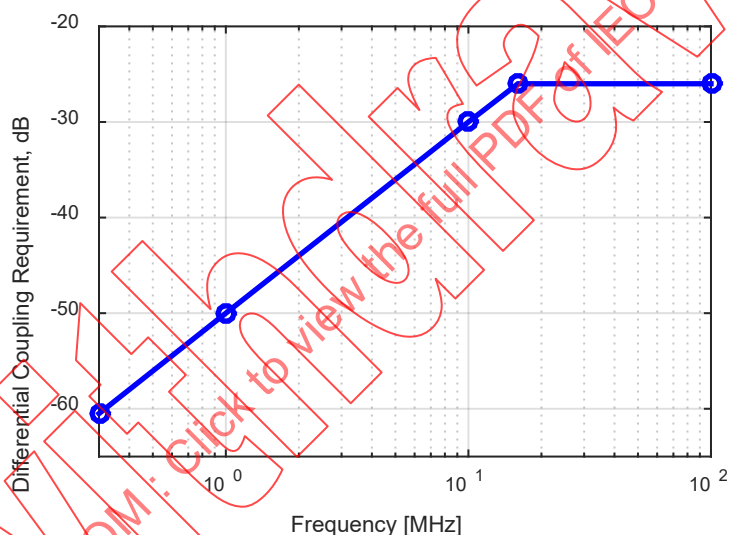


Figure 3-48 – Requirement for Differential Coupling between CC and D+/D-

For USB 2.0 Type-C cables, the singled-ended coupling between the CC and D- shall be below the limit shown in Figure 3-49. The limit is defined with the vertices of (0,3 MHz, -48,5 dB), (1 MHz, -38 dB), (10 MHz, -18 dB) and (100 MHz, -18 dB).

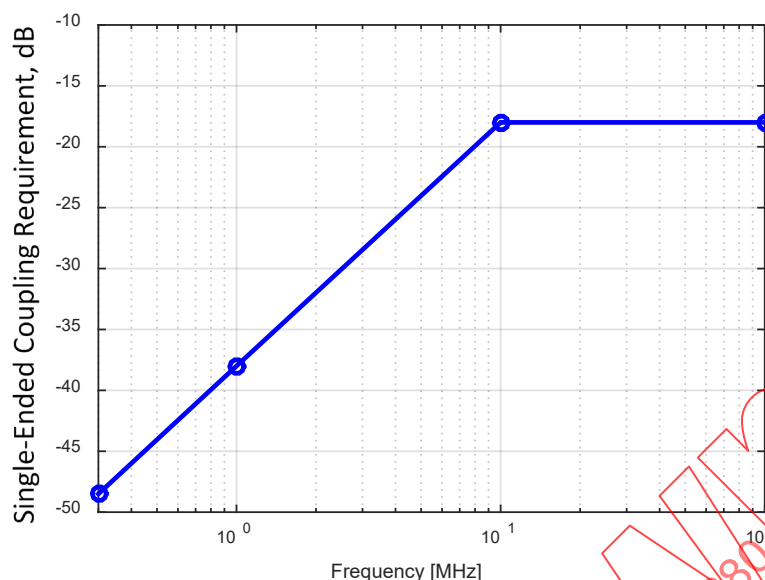


Figure 3-49 – Requirement for Single-Ended Coupling between CC and D- in USB 2.0 Type-C Cables

For USB Full-Featured Type-C cables, the singled-ended coupling between the CC and D- shall be below the limit shown in Figure 3-50. The limit is defined with the vertices of (0,3 MHz, -8 dB), (10 MHz, -27,5 dB), (11,8 MHz, -26 dB) and (100 MHz, -26 dB).

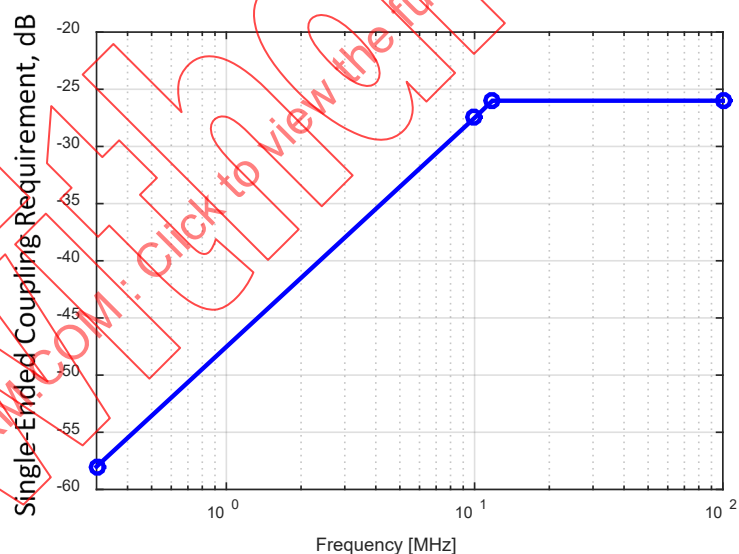


Figure 3-50 – Requirement for Single-Ended Coupling between CC and D- in USB Full-Featured Type-C Cables

3.7.3.3.2 Vbus Coupling to SBU_A/SBU_B, CC, and USB D+/D- (Normative)

The differential coupling between VBUS and USB D+/D- shall be less than the limit shown in Figure 3-51. The limit is defined by the following vertices: (0.3 MHz, -40 dB), (1 MHz, -40 dB), (30 MHz, -40 dB), and (100 MHz, -30 dB).

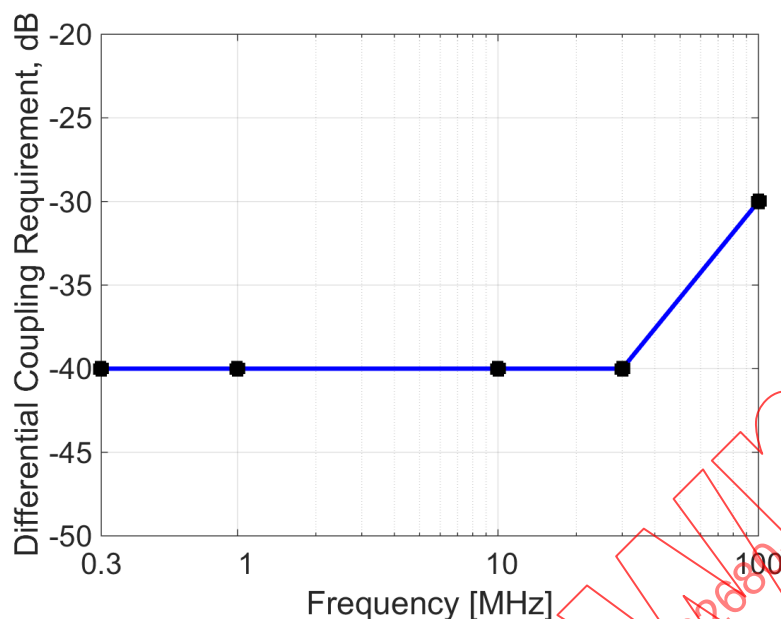


Figure 3-51 – Requirement for Differential Coupling between VBUS and D+/D-

The loop inductance of VBUS and its coupling factor to low speed lines is controlled to limit noise induced on low speed signaling lines. The maximum loop inductance of VBUS shall be 900 nH and the maximum mutual inductance coupling factor (k) between VBUS and low speed signal lines (CC, SBU_A, SBU_B, D+, D-) shall be 0.3. For fully featured cables, the range of VBUS bypass capacitance shall be 9nF up to 500nF as any of the values in the range is equally effective for high-speed return-path bypassing.

3.7.3.3.3 Coupling between SBU_A and SBU_B (Normative)

The single-ended coupling between SBU_A and SBU_B shall be less than the limit shown in Figure 3-52. The limit is defined with the vertices of (0,3 MHz, -56,5 dB), (1 MHz, -46 dB), (10 MHz, -26 dB), (11,2 MHz, -25 dB), and (100 MHz, -25 dB).

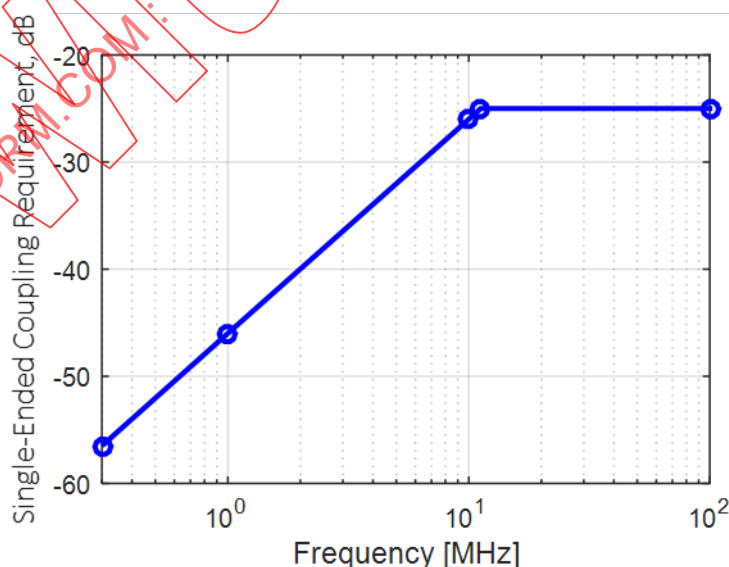


Figure 3-52 – Requirement for Single-Ended Coupling between SBU_A and SBU_B

3.7.3.3.4 Coupling between SBU_A/SBU_B and CC (Normative)

The single-ended coupling between SBU_A and CC, and between SBU_B and CC shall be less than the limit shown in Figure 3-53. The limit is defined with the vertices of (0,3 MHz, -65 dB), (1 MHz, -55 dB), (18 MHz, -30 dB), and (100 MHz, -30 dB).

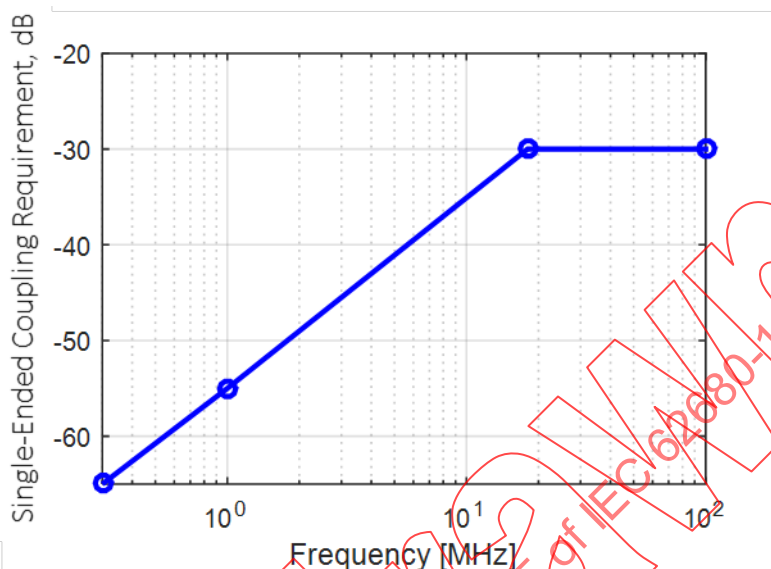


Figure 3-53 – Requirement for Single-Ended Coupling between SBU_A/SBU_B and CC

3.7.3.3.5 Coupling between SBU_A/SBU_B and USB D+/D- (Normative)

The coupling between SBU_A and differential D+/D-, and between SBU_B and differential D+/D- shall be less than the limit shown in Figure 3-54. The limit is defined with the vertices of (0,3 MHz, -80 dB), (30 MHz, -40 dB), and (100 MHz, -40 dB).

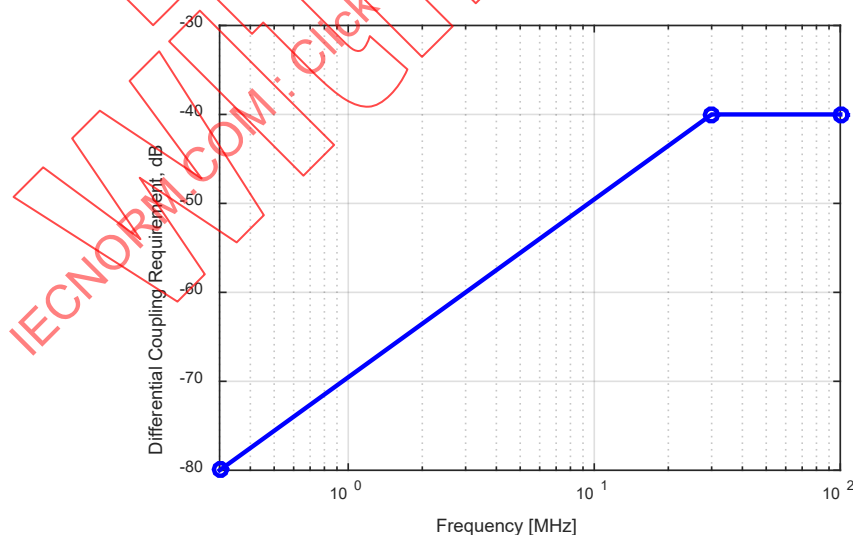


Figure 3-54 – Requirement for Coupling between SBU_A and differential D+/D-, and SBU_B and differential D+/D-

3.7.3.4 USB D+/D– Signal Requirements (Normative)

The USB D+/D– lines of the USB Type-C to Type-C cable assembly shall meet the requirements defined in Table 3-24.

Table 3-24 – USB D+/D– Signal Integrity Requirements

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D– lines of the cable assembly have the proper impedance.	75 ohms min and 105 ohms max.
	For the entire cable assembly.	400 ps rise time (20 %-80 %).
Propagation Delay	EIA 364-103	20 ns max.
	The purpose of the test is to verify the end-to-end propagation of the D+/D– lines of the cable assembly.	400 ps rise time (20 %-80 %).
Intra-pair Skew	EIA 364 – 103	100 ps max.
	This test ensures that the signal on both the D+ and D– lines of cable assembly arrive at the receiver at the same time.	400 ps rise time (20 %-80 %).
D+/D– Pair Attenuation	EIA 364 – 101 This test ensures the D+/D– pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	$\geq -1,02$ dB @ 50 MHz $\geq -1,43$ dB @ 100 MHz $\geq -2,40$ dB @ 200 MHz $\geq -4,35$ dB @ 400 MHz

3.7.4 USB Type-C to Legacy Cable Assemblies (Normative)

The USB Type-C to legacy cable assemblies may support [USB 2.0](#) only or [USB 3.1](#) Gen 2; [USB 3.1](#) Gen 1-only Type-C to legacy cable assemblies are not allowed.

3.7.4.1 USB 2.0-only Cable Assemblies (Normative)

The [USB 2.0](#)-only Type-C to legacy USB cable assemblies include:

- USB Type-C plug to [USB 2.0](#) Standard-A plug
- USB Type-C plug to [USB 2.0](#) Standard-B plug
- USB Type-C plug to [USB 2.0](#) Micro-B plug
- USB Type-C plug to [USB 2.0](#) Mini-B plug

The USB D+/D– signal integrity requirements are specified in Table 3-25.

Table 3-25 – USB D+/D– Signal Integrity Requirements for USB Type-C to Legacy USB Cable Assemblies

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D– lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20 %-80 %).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D– lines of the cable assembly.	10 ns max for USB Type-C to Micro-B cable assembly; 20 ns max for all other USB Type-C to legacy USB cable assemblies. 400 ps rise time (20 %-80 %)
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D– lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20 %-80 %).
D+/D– Pair Attenuation	EIA 364 – 101 This test ensures the D+/D– pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	$\geq -1,02$ dB @ 50 MHz $\geq -1,43$ dB @ 100 MHz $\geq -2,40$ dB @ 200 MHz $\geq -4,35$ dB @ 400 MHz

3.7.4.2 **USB 3.1 Gen 2 Cable Assemblies (Normative)**

The USB Type-C to **USB 3.1** Gen 2 legacy cable assemblies include:

- USB Type-C plug to **USB 3.1** Standard-A plug
- USB Type-C plug to **USB 3.1** Standard-B plug
- USB Type-C plug to **USB 3.1** Micro-B plug

The informative design targets for these cables are provided in Table 3-26.

Table 3-26 – Design Targets for USB Type-C to **USB 3.1 Gen 2 Legacy Cable Assemblies (Informative)**

Items	Design Targets
Differential Impedance	76 ohms min and 96 ohms max. 40 ps rise time (20 %-80 %).
Differential Insertion Loss	≥ -2 dB @ 100 MHz ≥ -4 dB @ 2,5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is $\geq -3,5$ dB @ 2,5 GHz $-6,0$ dB max @ 5.0 GHz
Differential NEXT between SuperSpeed Pairs	≤ -34 dB to 5 GHz
Differential NEXT and FEXT between D+/D– and SuperSpeed Pairs	≤ -30 dB to 5 GHz

The normative requirements include the USB D+/D– signaling as specified in Table 3-25, and the USB SuperSpeed parameters specified in Table 3-27.

Table 3-27 – USB Type-C to *USB 3.1* Gen 2 Legacy Cable Assembly Signal Integrity Requirements (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at both the SuperSpeed Gen 1 and Gen 2 Nyquist frequencies.	≥ -4 dB @ 2,5 GHz, except for the USB Type-C plug to USB 3,1 Standard-A plug cable assembly which is $\geq -3,5$ dB @ 2,5 GHz $\geq -6,0$ dB at 5,0 GHz
Integrated Differential Multi-reflection (IMR)	$dB \left(\frac{\int_0^{f_{max}} ILD(f) ^2 V_{in}(f) ^2 df}{\int_0^{f_{max}} V_{in}(f) ^2 df} \right)$	$\leq 0.126 \cdot ILfitatNq^2 + 3.0$ See Figure 3-55.
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB \left(\frac{\int_0^{f_{max}} (V_{in}(f) ^2 NEXT_s(f) ^2 + V_{dd}(f) ^2 NEXT_d(f) ^2) df}{\int_0^{f_{max}} V_{in}(f) ^2 df} \right)$ where: NEXT_s = NEXT between SuperSpeed pairs NEXT_d = NEXT between D+/D- and SuperSpeed pairs V_{dd}(f) = Input pulse spectrum on D+/D- pair, evaluated using equation shown in Figure 3-44 with T_b (UI) = 2.08 ns.	≤ -38 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB \left(\frac{\int_0^{f_{max}} (V_{in}(f) ^2 NEXT(f) ^2 + V_{in}(f) ^2 FEXT(f) ^2) df}{\int_0^{f_{max}} V_{in}(f) ^2 df} \right)$ where: NEXT = Near-end crosstalk from SuperSpeed to D+/D- FEXT = Far-end crosstalk from SuperSpeed to D+/D- f_{max} = 7.5 GHz	≤ -34 dB
Integrated Return Loss (IRL)	$dB \left(\frac{\int_0^{f_{max}} V_{in}(f) ^2 (SDD21(f) ^2 + SDD11(f) ^2 + SDD22(f) ^2) df}{\int_0^{f_{max}} V_{in}(f) ^2 df} \right)$	$\leq 0.046 \cdot ILfitatNq^2 + 1.8$ See Figure 3-56.
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ -20 dB

NOTE f_{max} = 10 GHz (unless otherwise specified); V_{in}(f) is defined in Figure 3-44 with T_b (UI) = 100 ps; and V_{dd}(f) is also defined in Figure 3-44 with T_b (UI) = 2.08 ns.

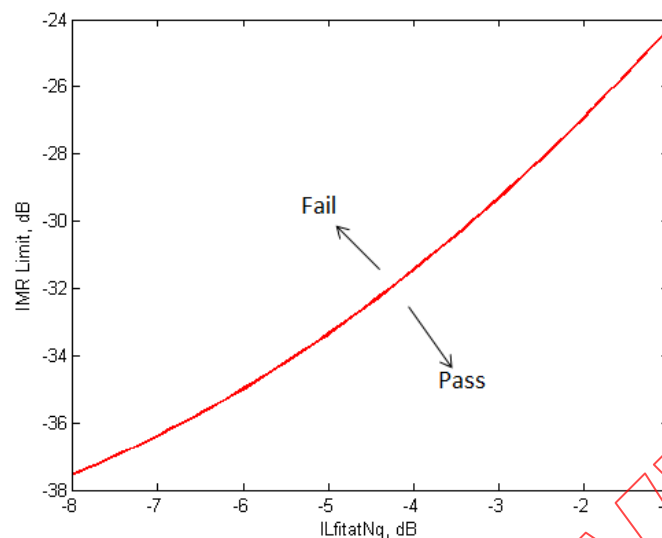


Figure 3-55 – IMR Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly

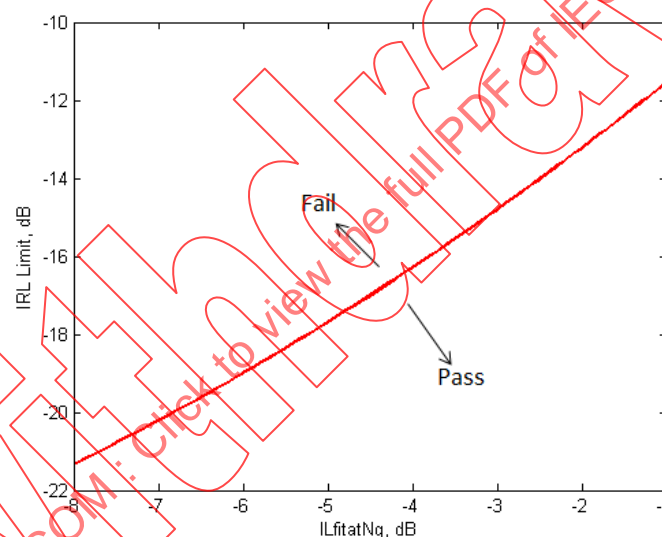


Figure 3-56 – IRL Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly

3.7.5 USB Type-C to USB Legacy Adapter Assemblies (Normative)

Only the following standard legacy adapter assemblies are defined:

- **USB 2.0** Type-C plug to **USB 2.0** Micro-B receptacle
- USB Full-Featured Type-C plug to **USB 3.1** Standard-A receptacle

3.7.5.1 USB 2.0 Type-C Plug to **USB 2.0** Micro-B Receptacle Adapter Assembly (Normative)

This adapter assembly supports only the **USB 2.0** signaling. It shall not exceed 150 mm total length, measured from end to end. Table 3-28 defines the electrical requirements.

Table 3-28 – USB D+/D– Signal Integrity Requirements for USB Type-C to Legacy USB Adapter Assemblies (Normative)

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D– lines of the adapter assembly have the proper impedance. For the entire adaptor assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20 %-80 %).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D– lines of adapter assembly arrive at the receiver at the same time.	20 ps max. 400 ps rise time (20 %-80 %).
Differential Insertion Loss	EIA 364 – 101 This test ensures the D+/D– pair of an adapter assembly can provide adequate signal strength to the receiver.	–0,7 dB max @ 400 MHz

3.7.5.2 USB Full-Featured Type-C Plug to [USB 3.1](#) Standard-A Receptacle Adapter Assembly (Normative)

The USB Full-Featured Type-C plug to [USB 3.1](#) Standard-A receptacle adapter assembly is intended to be used with a direct-attach device (e.g., USB thumb drive). A system is not guaranteed to function when using an adapter assembly together with a Standard USB cable assembly.

To minimize the impact of the adapter assembly to system signal integrity, the adapter assembly should meet the informative design targets in Table 3-29.

Table 3-29 – Design Targets for USB Type-C to [USB 3.1](#) Standard-A Adapter Assemblies (Informative)

Items	Design Targets
Differential Return Loss	≤ -15 dB to 5 GHz Normalized with 85 ohms.
Differential Insertion Loss	$\geq -2,4$ dB to 2,5 GHz, $\geq -3,5$ dB to 5 GHz
Differential NEXT between SuperSpeed Pairs	≤ -40 dB to 2,5 GHz ≤ -34 dB at 5 GHz
Differential NEXT and FEXT between D+/D– and SuperSpeed Pairs	≤ -30 dB to 2,5 GHz

The normative requirements for the adapter assembly are defined in Table 3-28 and Table 3-30. The adapter assembly total length is limited to 150 mm max.

Table 3-30 – USB Type-C to [USB 3.1](#) Standard-A Receptacle Adapter Assembly Signal Integrity Requirements (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequency (ILfitatNq)	ILfitatNq is evaluated at the SuperSpeed Gen 1 Nyquist frequency.	$\geq -2,4$ dB at 2,5 GHz $\geq -3,5$ dB at 5 GHz
Integrated Differential Multi-reflection (IMR)	$dB \left(\sqrt{\frac{\int_0^{f_{max}} ILD(f) ^2 V_{in}(f) ^2 df}{\int_0^{f_{max}} V_{in}(f) ^2 df}} \right)$	≤ -38 dB, Tb = 200 ps ≤ -27 dB, Tb = 100 ps
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB \left(\sqrt{\frac{\int_0^{f_{max}} (V_{in}(f) ^2 NEXT_s(f) ^2 + V_{dd}(f) ^2 NEXT_d(f) ^2) df}{\int_0^{f_{max}} V_{in}(f) ^2 df}} \right)$ where: NEXTs = NEXT between SuperSpeed pairs NEXTd = NEXT between D+/D- and SuperSpeed pairs Vdd(f) = Input pulse spectrum on D+/D- pair, evaluated using equation shown in Figure 3-44 with Tb (UI) = 2,08 ns.	≤ -37 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB \left(\sqrt{\frac{\int_0^{f_{max}} (V_{in}(f) ^2 NEXT(f) ^2 + V_{in}(f) ^2 FEXT(f) ^2) df}{\int_0^{f_{max}} V_{in}(f) ^2 df}} \right)$ where: NEXT = Near-end crosstalk from SuperSpeed to D+/D- FEXT = Far-end crosstalk from SuperSpeed to D+/D- f_{max} = 7.5 GHz	≤ -23 dB
Integrated Return Loss (IRL)	$dB \left(\sqrt{\frac{\int_0^{f_{max}} V_{in}(f) ^2 (SDD11(f) ^2 + SDD12(f) ^2 + SDD21(f) ^2 + SDD22(f) ^2) df}{\int_0^{f_{max}} V_{in}(f) ^2 df}} \right)$	$\leq -14,5$ dB, Tb = 200 ps $\leq -12,0$ dB, Tb = 100 ps
Diff to Comm mode	Differential to Common Mode conversion (SCD12, SCD21)	≤ -15 dB

NOTE f_{max} = 7.5 GHz; V_{in}(f) is defined in Figure 3-44 with Tb (UI) = 200 ps; and Vdd(f) is also specified in Figure 3-44 with Tb (UI) = 2,08 ns.

3.7.6 Shielding Effectiveness Requirements (Normative)

The cable assembly shielding effectiveness (SE) test measures the EMI and RFI levels from the cable assembly. To perform the measurement, the cable assembly shall be installed in the cable SE test fixture as shown in Figure 3-57. The coupling factors from the cable to the fixture are characterized with a VNA.

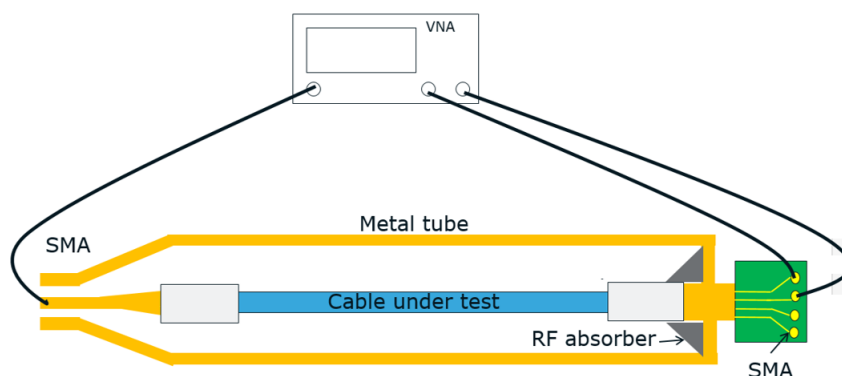
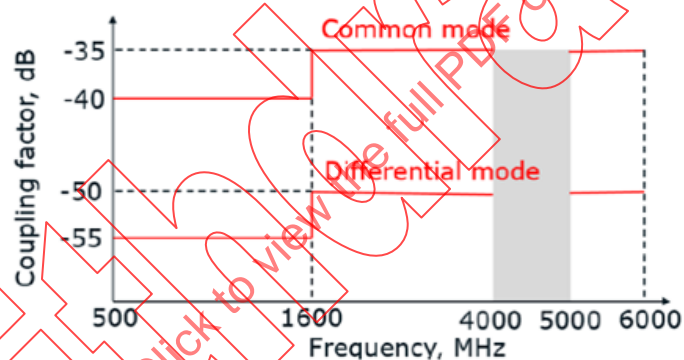
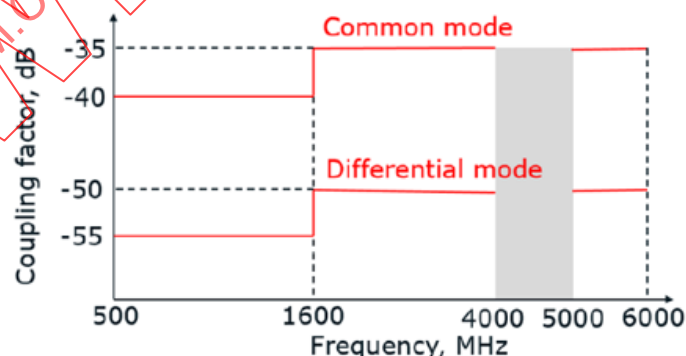


Figure 3-57 – Cable Assembly Shielding Effectiveness Testing

All USB Type-C cable assemblies shall pass the shielding effectiveness test for compliance. The pass/fail criteria for the USB Type-C to USB Type-C cable assemblies is shown in Figure 3-58a while the pass/fail criteria for the USB Type-C to legacy USB cable assemblies is shown in Figure 3-58b. Note that the shielding effectiveness for the frequency band from 4 GHz to 5 GHz is not specified since there is no antenna operating in this frequency range.



(a) For USB Type-C to USB Type-C Cable Assemblies



(b) For USB Type-C to legacy USB cable assemblies

Figure 3-58 – Shielding Effectiveness Pass/Fail Criteria

3.7.7 DC Electrical Requirements (Normative)

Unless otherwise stated, the tests in this section are performed on mated connector pairs.

3.7.7.1 Low Level Contact Resistance (EIA 364-23B)

The low level contact resistance (LLCR) measurement is made from the solder tail of the receptacle to the soldering point of the plug (including any internal paddle cards, contacts and substrates of the plug and receptacle). See Figure 3-59. The following requirements apply to the power and signal contacts:

- 40 mΩ (Max) initial for VBUS, GND and all other contacts.
- Maximum change (delta) of +10 mΩ after environmental stresses.
- Measure at 20 mV (Max) open circuit at 100 mA.

Refer to Section 3.8 for environmental requirements and test sequences.

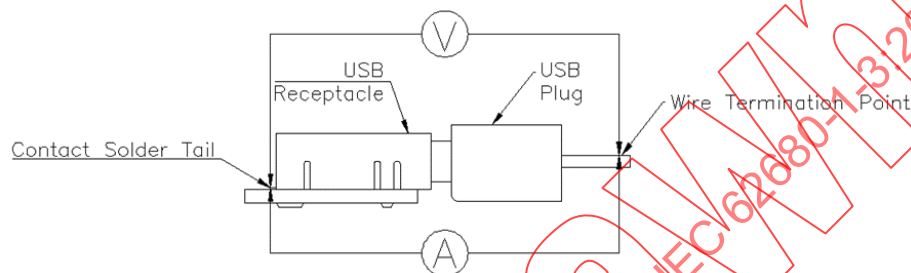


Figure 3-59 – LLCR Measurement Diagram

3.7.7.2 Dielectric Strength (EIA 364-20)

No breakdown shall occur when 100 Volts AC (RMS) is applied between adjacent contacts of unmated and mated connectors.

3.7.7.3 Insulation Resistance (EIA 364-21)

A minimum of 100 MΩ insulation resistance is required between adjacent contacts of unmated and mated connectors.

3.7.7.4 Contact Current Rating (EIA 364-70, Method 2)

A current of 5.0 A shall be applied collectively to VBUS pins (i.e., pins A4, A9, B4, and B9) and 1.25 A applied to the VCONN pin (i.e., B5 of the plug connector) with the return path through the corresponding GND pins (i.e., pins A1, A12, B1, and B12). A minimum current of 0.25 A shall also be applied individually to all the other contacts. When the currents are applied to the contacts, the temperature rise shall not exceed 30 °C at any point on the USB Type-C mated plug and receptacle under test, when measured at an ambient temperature of 25 °C.

3.8 Mechanical and Environmental Requirements (Normative)

The requirements in this section apply to all USB Type-C connectors and/or cable assemblies unless otherwise specified. For USB Type-C plug connectors and cable assemblies, the test methods are based on an assumption that the cable exits the overmold in line with mating direction to a USB Type-C receptacle (i.e., straight out the back of the overmold). For USB Type-C plug connectors and cable assemblies with the cable exiting the overmold in a different direction than straight out the back (e.g., right angle to the mating direction), test fixtures and procedures shall be modified as required to accomplish the measurement.

3.8.1 Mechanical Requirements

3.8.1.1 Insertion Force (EIA 364-13)

The initial connector insertion force shall be within the range from 5 N to 20 N at a maximum rate of 12,5 mm (0,492") per minute. This requirement does not apply when the connectors are used in a docking application.

It is recommended to use a non-silicone based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.

3.8.1.2 Extraction Force (EIA 364-13)

The connector extraction force shall be within the range of 8 N to 20 N up to 1,000 mating cycles and within the range of 6 N to 20 N after the specified insertion/extraction or durability cycles (at a maximum rate of 12,5 mm (0,492") per minute). This requirement does not apply when the connectors are used in a mechanical docking application.

It is recommended to use a non-silicone based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.

3.8.1.3 Durability or Insertion/Extraction Cycles (EIA 364-09)

The durability rating shall be 10,000 cycles minimum for the USB Type-C connector family. The durability test shall be done at a maximum rate of 200 cycles per hour and no physical damage to any part of the connector and cable assembly shall occur.

3.8.1.4 Cable Flexing (EIA 364-41, Condition 1)

No physical damage or discontinuity over 1ms during flexing shall occur to the cable assembly with Dimension X = 3,7 times the cable diameter and 100 cycles in each of two planes.

3.8.1.5 Cable Pull-Out (EIA 364-38, Method A)

No physical damage to the cable assembly shall occur when it is subjected to a 40 N axial load for a minimum of 1 minute while clamping one end of the cable plug.

3.8.1.6 4-Axis Continuity Test

The USB Type-C connector family shall be tested for continuity under stress using the test configurations shown in Figure 3-60. Plugs shall be supplied in a cable assembly with a representative overmold. A USB Type-C receptacle shall be mounted on a 2-layer printed circuit board (PCB) between 0,8 mm and 1,0 mm thickness. The PCB shall be clamped on either side of the receptacle no further than 5 mm away from the solder tails. The PCB shall initially be placed in a horizontal plane, and an 8 N tensile force shall be applied to the cable in a downward direction, perpendicular to the axis of insertion, for a period of at least 10 seconds. For receptacle designs that do not have a full length shell, the test shall be done with the connector and associated hardware mounted as in the final product configuration.

The continuity across each contact shall be measured throughout the application of the tensile force. Each non-ground contact shall also be tested to confirm that it does not short to the shell during the stresses. The PCB shall then be rotated 90 degrees such that the cable is still inserted horizontally and the 8 N tensile force shall be applied again in the downward direction and continuity measured as before. This test is repeated for 180 degree and 270 degree rotations. Passing parts shall not exhibit any discontinuities or shorting to the shell greater than 1 µs duration in any of the four orientations.

One method for measuring the continuity through the contacts is to short all the wires at the end of the cable pigtail and apply a voltage through a pull-up to each of VBUS, USB D+, USB D-, SBU, CC, and USB SuperSpeed pins, with the GND pins connected to ground.

Alternate methods are allowed to verify continuity through all pins.

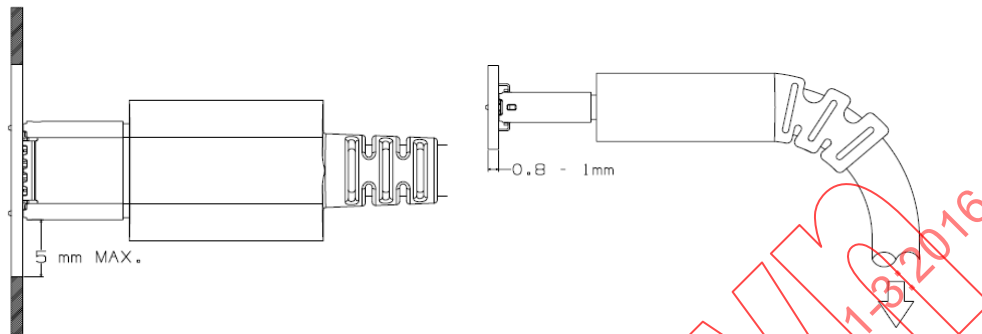


Figure 3-60 – 4-Axis Continuity Test

3.8.1.7 Wrenching Strength

USB Type-C plugs shall be tested using the mechanical wrenching test fixture defined in the Universal Serial Bus Type-C Connectors and Cable Assemblies Compliance Document. Perpendicular moments are applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds when inserted in the test fixture to achieve the defined moments in four directions of up or down (i.e., perpendicular to the long axis of the plug opening) and left or right (i.e., in the plane of the plug opening). Compliant connectors shall meet the following force thresholds:

- A moment of 0-0,75 Nm (e.g., 50 N at 15 mm from the edge of the receptacle) is applied to a plug inserted in the test fixture in each of the four directions. A single plug shall be used for this test. Some mechanical deformation may occur. The plug shall be mated with the continuity test fixture after the test forces have been applied to verify no damage has occurred that causes discontinuity or shorting. The continuity test fixture shall provide a planar surface on the mating side located $6,20 \pm 0,20$ mm from the receptacle Datum A, perpendicular to the direction of insertion. No moment forces are applied to the plug during this continuity test.

Figure 3-61 illustrates an example continuity test fixture to perform the continuity test. The Dielectric Withstanding Voltage test shall be conducted after the continuity test to verify plug compliance.

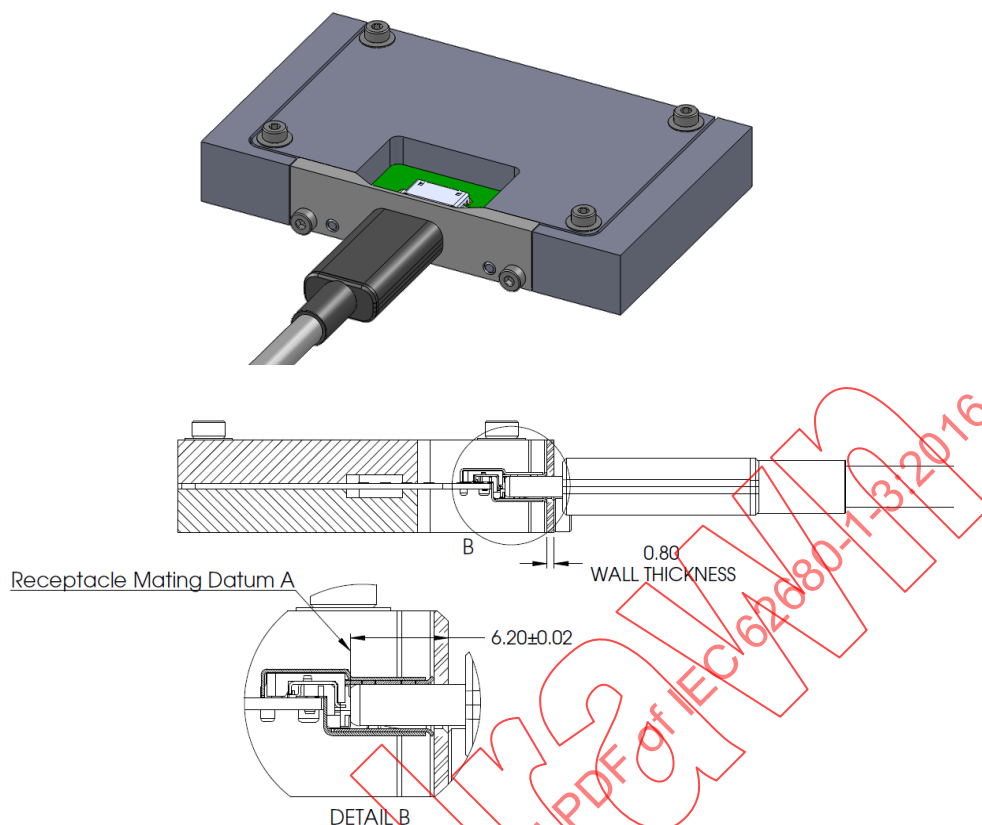


Figure 3-61 – Reference Wrenching Strength Continuity Test Fixture

- The plug shall disengage from the test fixture or demonstrate mechanical failure (i.e., the force applied during the test procedure peaks and drops off) when a moment of 2.0 Nm is applied to the plug in the up and down directions and a moment 3.5 Nm is applied to the plug in the left and right directions. A new plug is required for each of the four test directions. An example of the mechanical failure point and an illustration of the wrenching test fixture are shown in Figure 3-62 and Figure 3-63, respectively.

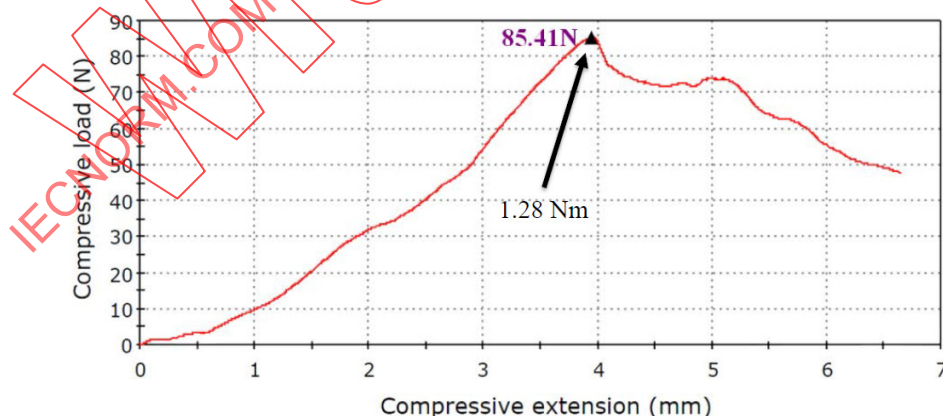


Figure 3-62 – Example of Wrenching Strength Test Mechanical Failure Point

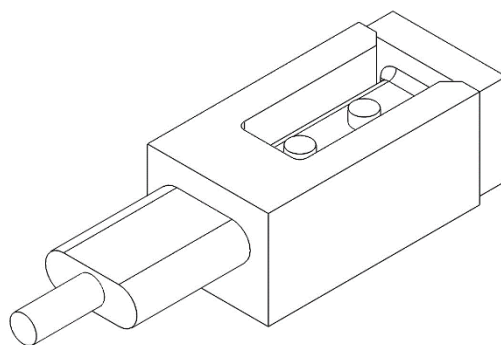


Figure 3-63 – Wrenching Strength Test with Cable in Fixture

3.8.1.8 Restriction of Hazardous Substances

It is recommended that components be RoHS compliant.

3.8.2 Environmental Requirements

The connector interface environmental tests shall follow EIA 364-1000.01, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications.

Since the connector defined has more than 0.127 mm wipe length, Test Group 6 in EIA 364-1000.01 is not required. The temperature life test duration and the mixed flowing gas test duration values are derived from EIA 364-1000.01 based on the field temperature per the following.

Table 3-31 – Environmental Test Conditions

Temperature Life test temperature and duration	105 °C for 120 hours
Temperature Life test temperature and duration for preconditioning	105 °C for 72 hours
Mixed flowing gas test duration	7 days

The pass/fail criterion for the low level contact resistance (LLCR) is as defined in Section 3.7.7.1. The durability ratings are defined in Section 3.8.1.3.

3.8.2.1 Reference Materials (Informative)

This specification does not specify materials for connectors and cables. Connector and cable manufacturers should select appropriate materials based on performance requirements. The information below is provided for reference only.

NOTE Connector and cable manufacturers should comply with contact plating requirements per the following options:

Option I

Receptacle

Contact area: (Min) 0,05 µm Au + (Min) 0,75 µm Ni-Pd on top of (Min) 2,0 µm Ni

Plug

Contact area: (Min) 0,05 µm Au + (Min) 0,75 µm Ni-Pd on top of (Min) 2,0 µm Ni

Option II

Receptacle

Contact area: (Min) 0,75 μm Au on top of (Min) 2,0 μm Ni

Plug

Contact area: (Min) 0,75 μm Au on top of (Min) 2,0 μm Ni

Other reference materials that connector and cable manufacturers select based on performance parameters listed in Table 3-32 are for reference only.

Table 3-32 – Reference Materials

Component	Materials
Cable	Conductor: copper with tin or silver plating
	SDP Shield: AL foil or AL/mylar foil
	Coaxial shield: copper strand
	Braid: Tin plated copper or aluminum
	Jacket: PVC or halogen free substitute material
Cable Overmold	Thermoset or thermoplastic
Connector Shells	Stainless steel or phosphor bronze
Plug Side Latches	Stainless steel
Receptacle Mid-Plate	Stainless steel
Plug Internal EMC Spring	Stainless steel or high yield strength copper alloy
Receptacle EMC Pad	Stainless steel or phosphor bronze
Receptacle Shell	Stainless steel or phosphor bronze
Receptacle Tongue	Glass-filled nylon
Housing	Thermoplastics capable of withstanding lead-free soldering temperature

NOTE Halogen-free materials should be considered for all plastics

3.9 Docking Applications (Informative)

In this specification, docking refers to plugging a device directly into a dock without using a cable assembly. The USB Type-C connector is defined to support such applications.

The connector is only part of a docking solution. A complete docking solution at the system level may also include retention or locking mechanisms, alignment mechanisms, docking plug mounting solutions, and protocols supported through the connector. This specification does not attempt to standardize system docking solutions, therefore there is no interoperability requirement for docking solutions.

The following list includes the requirements and guidelines when using the USB Type-C connector for docking:

- 1) The USB Type-C plug used for docking shall work with compliant USB Type-C receptacle. It shall comply with all dimensional, electrical and mechanical requirements.
- 2) If the plug on the dock does not include the side latches, then the dock should provide a retention or locking mechanism to secure the device to the plug. The retention latches also serve as one of the ground return paths for EMC. The docking design should ensure adequate EMC performance without the side latches if they are not present.
- 3) The internal EMC fingers are not required for the docking plug as long as the receptacle and plug shells have adequate electrical connection.

- 4) Alignment is critical for docking. Depending on system design, standard USB Type-C connectors alone may not provide adequate alignment for mating. System level alignment is highly recommended. Alignment solutions are implementation-specific.
- 5) Fine alignment is provided by the connector. The receptacle front face may have lead-in features for fine alignment. Figure 3-64 shows an example of a USB Type-C receptacle with a lead-in flange compared to a receptacle without the flange.

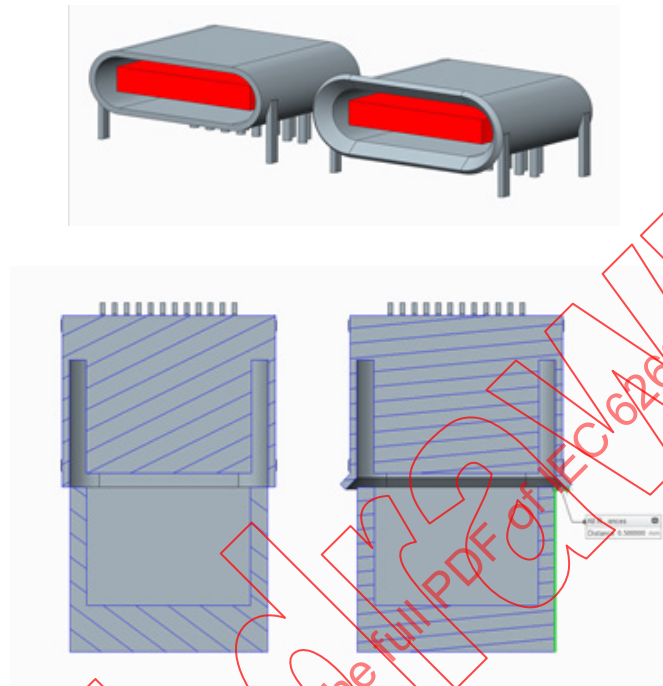


Figure 3-64 – USB Type-C Cable Receptacle Flange Example

3.10 Implementation Notes and Design Guides

This section discusses a few implementation notes and design guides to help users design and use the USB Type-C connectors and cables.

3.10.1 EMC Management (Informative)

Connector and cable assembly designers, as well as system implementers should pay attention to receptacle and cable assembly shielding to ensure a low-impedance grounding path. The following are guidelines for EMC management:

- The quality of raw cables should be ensured. The intra-pair skew or the differential to common mode conversion of the SuperSpeed pairs has a significant impact on cable EMC and should be controlled within the limits of this specification.
- The cable external braid should be physically connected to the plug metal shell as close to 360° as possible to control EMC. Without appropriate shielding termination, even a perfect cable with zero intra-pair skew may not meet EMC requirements. Copper tape may be needed to shield off the braid termination area.
- The wire termination contributes to common-mode noise. The breakout distance for the wire termination should be kept as small as possible to optimize EMC and signal integrity performance. If possible, symmetry should be maintained for the two lines within a differential pair.
- Besides the mechanical function, the side latches on the plug and the mid-plate in the receptacle also play a role for EMC. This is illustrated in Figure 3-65:

- 1) The side latch should have electrical connection to the receptacle mid-plate (a docking plug may not have side latches).
- 2) The side latches should be terminated to the paddle card GND plane inside the plug.
- 3) The mid-plate should be directly connected to system PCB GND plane with 3 or more solder leads/tails.

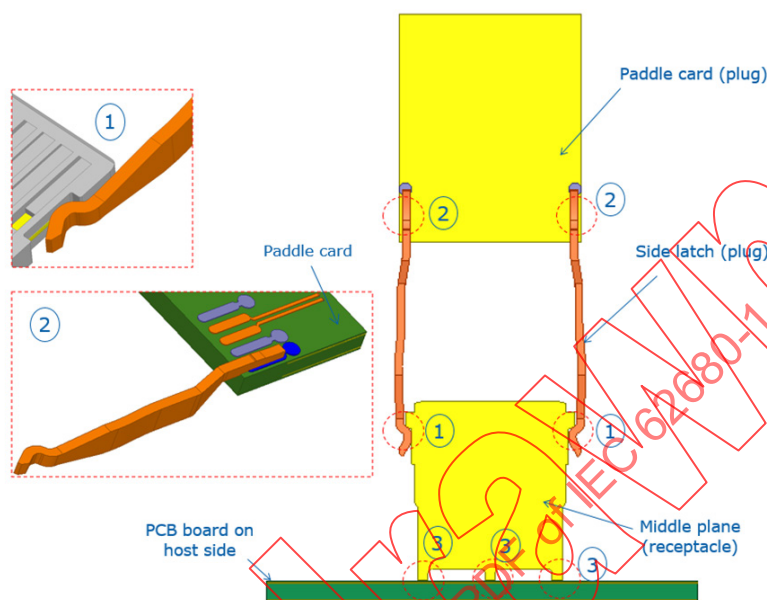


Figure 3-65 – EMC Guidelines for Side Latch and Mid-plate

- The internal RFI finger inside the plug should have adequate connection points to the inner surface of the plug shell. Four or more connection points are recommended as illustrated in Figure 3-66.

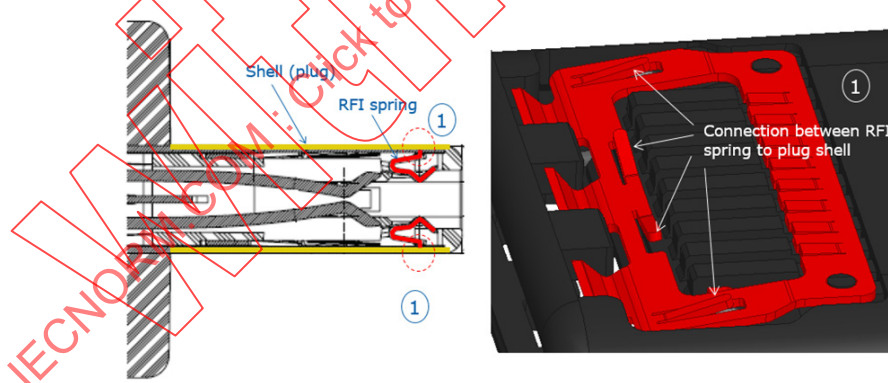


Figure 3-66 – EMC Finger Connections to Plug Shell

- The EMC fingers inside the plug mates with the EMC pad in the receptacle. It is important for the EMC pad to have adequate connections to the receptacle shell. As illustrated in Figure 3-67, there are multiple laser welding points between the EMC pads and the receptacle shell, top and bottom.
- The receptacle shell should have sufficient connection points to the system PCB GND plane with apertures as small as possible. Figure 3-67 illustrates an example with multiple solder tails to connect the receptacle shell to system PCB GND.

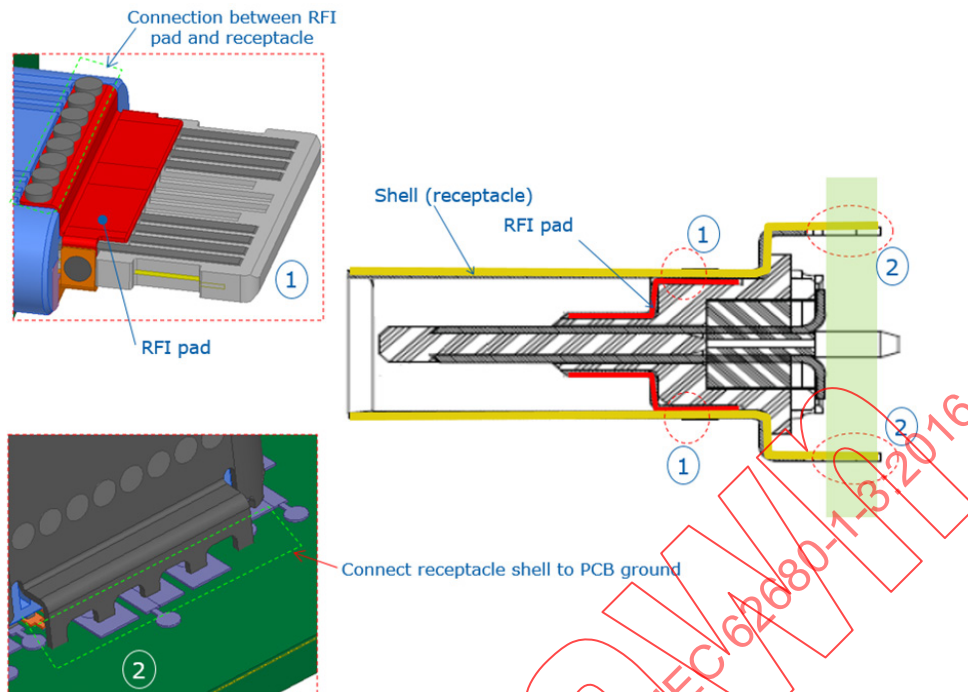


Figure 3-67 – EMC Pad Connections to Receptacle Shell

- Apertures in the receptacle and plug shells should be minimized. If apertures are unavoidable, a maximum aperture size of 1.5 mm is recommended. See Figure 3-68 for aperture illustrations. Copper tape may be applied to seal the apertures inside the cable plug.



Figure 3-68 – Examples of Connector Apertures

- The receptacle connectors should be connected to metal chassis or enclosures through grounding fingers, screws, or any other way to manage EMC.

3.10.2 Stacked and Side-by-Side Connector Physical Spacing (Informative)

Stacked and side-by-side USB connectors are commonly used in PC systems. Figure 3-69 illustrates the recommended spacing between connectors for stacked and side-by-side configurations.

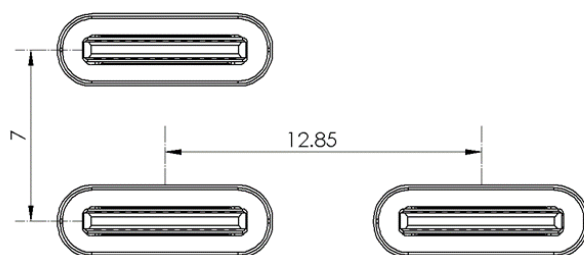


Figure 3-69 – Recommended Minimum Spacing between Connectors

3.10.3 Cable Mating Considerations (Informative)

The receptacle mounting location, exterior product surfaces, cable overmold, and plug mating length need to be considered to ensure the USB Type-C plug is allowed to fully engage the USB Type-C receptacle. Figure 3-70 illustrates the recommended minimum plug overmold clearance to allow the cable plug to fully seat in the product receptacle.

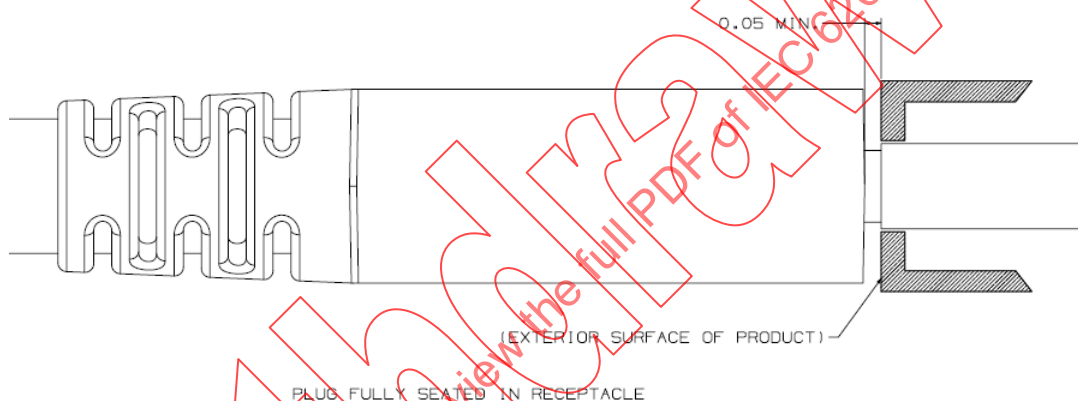


Figure 3-70 – Recommended Minimum Plug Overmold Clearance

Figure 3-71 illustrates special considerations required when external walls are angled. For such applications, the USB Type-C receptacle shell may not provide as much mechanical alignment protection to the receptacle tongue as in the full shell design. Design options to allow the receptacle to pass mechanical test requirements include relief in the exterior wall surface to allow use of a full shell receptacle or use of a receptacle specifically designed for the application.

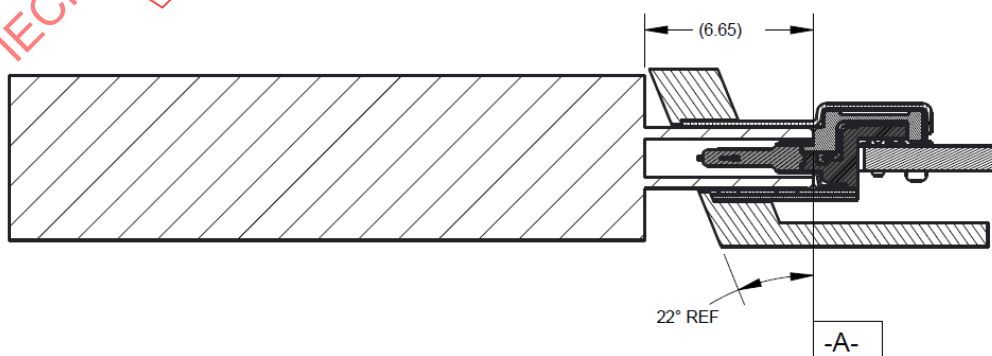


Figure 3-71 – Cable Plug Overmold and an Angled Surface

4 Functional

This chapter covers the functional requirements for the signaling across the USB Type-C™ cables and connectors. This includes functional signal definition, discovery and configuration processes, and power delivery.

For purposes of this description, a USB port operating as a host is referred to as the Downstream Facing Port (DFP) and a USB port operating as a device is referred to as the Upstream Facing Port (UFP).

Chapter 5 defines functional extensions that are optional.

4.1 Signal Summary

Table 4-1 summarizes the list of signals used on the USB Type-C connectors.

Table 4-1 – USB Type-C List of Signals

Signal Group	Signal	Description
USB 3.1	SSTXp1, SSTXn1 SSRXp1, SSRXn1 SSTXp2, SSTXn2 SSRXp2, SSRXn2	SuperSpeed USB serial data interface defines 1 differential transmit pair and 1 differential receive pair. On a USB Type-C receptacle, two sets of SuperSpeed USB signal pins are defined to enable plug flipping feature
USB 2.0	Dp1, Dn1 Dp2, Dn2	USB 2.0 serial data interface defines a differential pair. On a USB Type-C receptacle, two set of USB 2.0 signal pins are defined to enable plug flipping feature
Configuration	CC1, CC2 (receptacle) CC (plug)	CC channel in the plug used for connection detect, interface configuration and VCONN
Auxiliary signals	SBU1, SBU2	Sideband Use
Power	VBUS	USB cable bus power
	VCONN (plug)	USB plug power
	GND	USB cable return current path

4.2 Signal Pin Descriptions

4.2.1 SuperSpeed USB Pins

SSTXp1, SSTXn1
(**SSTXp2, SSTXn2**) These pins are required to implement the system's transmit path of a [USB 3.1](#) SuperSpeed interface. The transmitter differential pair in a port are routed to the receiver differential pair in the port at the opposite end of the path. The [USB 3.1 Specification](#) defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

SSRXp1, SSRXn1
(**SSRXp2, SSRXn2**) These pins are required to implement the system's receive path of a [USB 3.1](#) SuperSpeed interface. The receiver differential pair in a port are routed to the transmitter differential pair in the port at the opposite end of the path. The [USB 3.1 Specification](#) defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

4.2.2 USB 2.0 Pins

Dp1, Dn1
(Dp2, Dn2)

These pins are required to implement [USB 2.0](#) functionality. [USB 2.0](#) in all three modes (LS, FS, and HS) is supported. The [USB 2.0 Specification](#) defines all electrical characteristics, enumeration, and bus protocol and bus management features for this interface.

Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

4.2.3 Auxiliary Signal Pins

SBU1, SBU2

These pins are assigned to sideband use. Refer to Section 4.3 for the functional requirements.

4.2.4 Power and Ground Pins

Vbus

These pins are for USB cable bus power as defined by the USB specifications. This source is only present when a DFP-to-UFP connection across the CC channel is present – see Section 4.5.1.2.1. Refer to Section 4.4.2 for the functional requirements for Vbus.

Vconn

Vconn is applied to the unused CC pin to supply power to the local plug. Refer to Section 4.4.3 for the functional requirements for Vconn.

GND

Return current path.

4.2.5 Configuration Pins

CC1, CC2, CC

These pins are used to detect connections and configure the interface across the USB Type-C cables and connectors. Refer to Section 4.5 for the functional definition. Once a connection is established, CC1 or CC2 will be reassigned for providing power over the VCONN pin of the plug – see Section 4.5.1.2.1.

4.3 Sideband Use (SBU)

The Sideband Use pins (SBU1 and SBU2) are limited to the uses as defined by this specification and additional functionality will be defined in future versions of the USB specifications. See Section 5.1 and A for use of the SBU pins in Alternate Modes and Audio Adapter Accessory Mode.

The SBU pins on a port shall either be open circuit or have a weak pull-down to ground no stronger than [zSBU Termination](#).

These pins are pre-wired in the standard USB Full-Featured Type-C cable as individual single-ended wires (SBU_A and SBU_B). Note that SBU1 and SBU2 are cross-connected in the cable.

4.4 Power and Ground

4.4.1 IR Drop

The maximum allowable cable IR drop for ground shall be 250 mV and for VBUS shall be 500 mV through the cable to the cable's maximum rated VBUS current capacity. When VCONN is being sourced, the IR drop for the ground shall still be met considering any additional VCONN return current.

Figure 4-1 illustrates what parameters contribute to the IR drop and where it shall be measured. The IR drop includes the contact resistance of the mated plug and receptacles at each end.

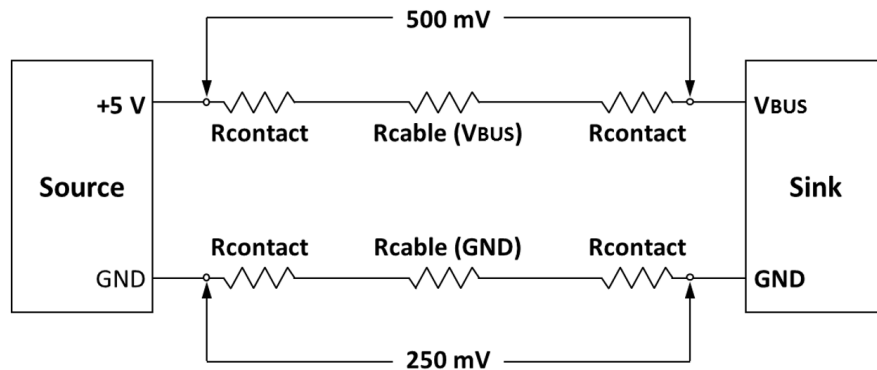


Figure 4-1 – Cable IR Drop

Figure 4-2 illustrates what parameters contribute to the IR drop for a powered cable and where it shall be measured. Note that the powered cable includes isolation elements (Iso) and loads (L1 and L2) for the functions in the powered cable such as [USB PD](#) controllers. The IR drop shall remain below 250 mV in all cases.

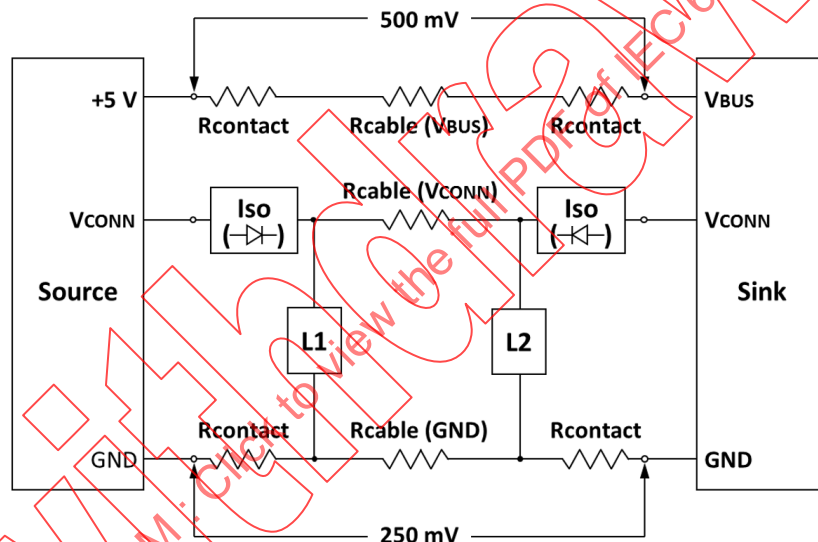


Figure 4-2 – Cable IR Drop for powered cables

4.4.2 VBUS

The allowable default range for VBUS as measured at the DFP receptacle shall be as defined by the [USB 2.0 Specification](#) and [USB 3.1 Specification](#). Note that due to higher currents allowed, legacy devices may experience a higher voltage (up to 5.5V maximum) at light loads.

The DFP's USB Type-C receptacle VBUS pin shall remain unpowered until a UFP is attached. The VBUS pin shall return to the unpowered state when the UFP is detached. See Table 4-18 for VBUS timing values. Legacy hosts/chargers that by default source VBUS when connected using any legacy USB connector (Standard-A, Micro-B, etc.) to USB Type-C cable or adapter are exempted from these two requirements.

A DRP or DFP or UFP with Accessory Support implementing an R_p pull-up as its method of connection detection shall provide an impedance between VBUS and GND on its receptacle pins as specified in Table 4-2 when not sourcing power on VBUS (i.e., when in states [Unattached.SRC](#) or [Unattached.Accessory](#)).

Table 4-2 – VBUS Leakage

	Minimum	Maximum	Notes
VBUS Leakage Impedance	72,4 kΩ		Leakage between VBUS pins and GND pins on receptacle when VBUS is not being Sourced.

4.4.3 VCONN

VCONN is provided by the DFP to power cables with electronics in the plug. VCONN is provided over the CC pin that is determined not to be connected to the CC wire of the cable.

Initially, VCONN shall be sourced on all DFP USB Type-C receptacles that utilize the SSTX and SSRX pins during specific connection states as described in Section 4.5.2.2. VCONN may be sourced on DFP USB Type-C receptacles that do not utilize the SSTX and SSRX pins as described in Section 4.5.2.2. **USB PD** VCONN_Swap command also provides the DFP a means to request that the attached UFP source VCONN.

Table 4-3 provides the voltage and power requirements that shall be met for VCONN. See Section 4.9 for more details about Electronically Marked Cables. See Section 4.10 for a wider VCONN voltage operating range for VCONN-powered accessories. See Section 5.1 regarding optional support for an increased VCONN power range in Alternate Modes.

Table 4-3 – VCONN Source Characteristics

	Minimum	Maximum	Notes
Voltage	4,75 V	5,5 V	Ports that support VCONN-powered accessories are allowed to supply at a lower minimum of 2,7 V when operating in the PoweredAccessory state.
Power	1,0 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage.
Bulk Capacitance	10 μF	220 μF	The VCONN source shall disconnect the bulk capacitance from the receptacle when VCONN is powered off.

To aid in reducing the power associated with supplying VCONN, a DFP is allowed to either not source VCONN or turn off Vconn under any of the following conditions:

- **Ra** is not detected on the CC pin after **tCCDebounce** when the other CC pin is in the **SRC.Rd** state
- **Ra** is not detected on the CC pin after **tCCDebounce** when the other CC pin is in the **SRC.Open** state and the port supports VCONN-powered accessories
- After completing the **USB PD** Discover Identity process and determining that VCONN is not needed
- If there is no GoodCRC response to **USB PD** Discover Identity messages

Table 4-4 provides the requirements that shall be met for cables that consume VCONN power.

Table 4-4 – VCONN Sink Characteristics

	Minimum	Maximum	Notes
Inrush Capacitance		10 μ F	A cable shall not present more than the equivalent inrush capacitance to the VCONN source. The active cable is responsible for discharging its capacitance.
Power for Electronically Marked Cables		70 mW	See Section 4.9.
Power for Active Cables		1.0 W	See Section 5.2.
tVCONNDischarge		250 ms	The time from the point that the cable is detached until vVCONNDischarge shall be met.
vVCONNDischarge		150 mV	The VCONN voltage following cable detach and self-discharge.

The cable may remove or weaken **Ra** when VCONN is above 1.0 V as long as the other requirements are met. See Section 4.5.1.2.1.

4.5 Configuration Channel (CC)

4.5.1 Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the DFP-to-UFP connection. Note that in this section, “direct connect” is used to refer to a device connected directly to a host (e.g., a thumb drive). When the device is connected through a hub, the connection between a UFP on the hub and the host port and the connection between the device port and a DFP on the hub, are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a DFP to a UFP
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish DFP and UFP roles between two attached ports
- Discover and configure VBUS: USB Type-C Current modes or [USB Power Delivery](#)
- Configure VCONN
- Discover and configure optional Alternate and Accessory modes

4.5.1.1 USB Data Bus Interface and USB Type-C Plug Flip-ability

Since the USB Type-C plug can be inserted in either right-side-up or upside-down position, the hosts and devices that support USB data bus functionality must operate on the signal pins that are actually connected end-to-end. In the case of USB 2.0, this is done by shorting together the two D+ signal pins and the two D– signal pins in the DFP and UFP receptacles. In the case of USB SuperSpeed signals, it requires the functional equivalent of a switch in both the DFP and UFP to appropriately route the SuperSpeed TX and RX signal pairs to the connected path through the cable.

Figure 4-3 illustrates the logical data bus model for a USB Type-C-based DFP connected to a USB Type-C-based UFP. The USB cable that sits between a DFP and UFP can be in one of four possible connected states when viewed by the DFP:

- Un-flipped straight through – Position ① ⇔ Position ①
- Un-flipped twisted through – Position ① ⇔ Position ②
- Flipped straight through – Position ② ⇔ Position ②

- Flipped twisted through – Position ② ⇔ Position ①

To establish the proper routing of the active USB data bus from DFP to UFP, the standard USB Type-C cable is wired such that a single CC wire is position aligned with the first USB SuperSpeed signal pairs (SSTXp1/SSTXn1 and SSRXp1/SSRXn1) – in this way, the CC wire and USB SuperSpeed data bus wires that are used for signaling within the cable track with regard to the orientation and twist of the cable. By being able to detect which of the CC pins (CC1 or CC2) at the receptacle is terminated by the UFP, the DFP is able to determine which SuperSpeed USB signals are to be used for the connection and the DFP can use this to control the functional switch for routing the SuperSpeed USB signal pairs. Similarly in the UFP, detecting which of the CC pins at the receptacle is terminated by the DFP allows the UFP to control the functional switch that routes its SuperSpeed USB signal pairs.

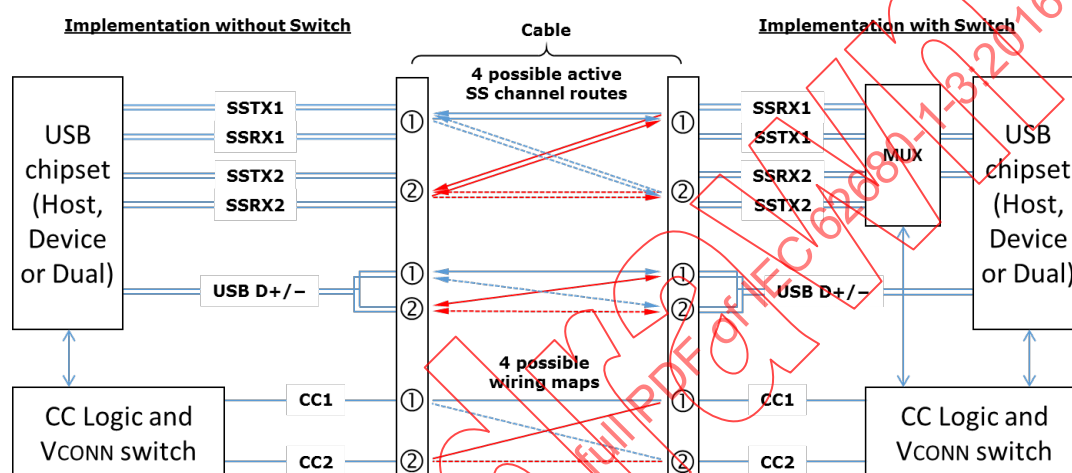


Figure 4-3 – Logical Model for Data Bus Routing across USB Type-C-based Ports

While Figure 4-3 illustrates the functional model as a DFP connected to a UFP, this model equally applies to a USB hub's DFPs as well.

Figure 4-4 illustrates the logical data bus model for a USB Type-C-based UFP (implemented with a USB Type-C plug either physically incorporated into the device or permanently attached as a captive cable) connected directly to a USB Type-C-based DFP. For the UFP, the location of the USB SuperSpeed data bus, **USB 2.0** data bus, CC and VCONN pins are fixed by design. Given that the UFP pin locations are fixed, only two possible connected states exist when viewed by the DFP.

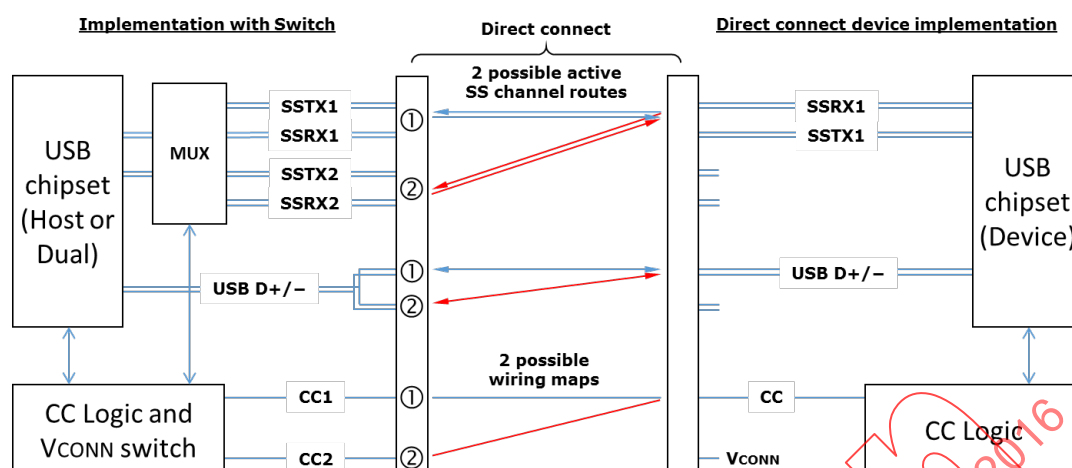


Figure 4-4 – Logical Model for USB Type-C-based Ports for the Direct Connect Device

The functional requirements for implementing SuperSpeed USB data bus routing for the USB Type-C receptacle are not included in the scope of this specification. There are multiple host, device and hub architectures that can be used to accomplish this which could include either discrete or integrated switching, and could include merging this functionality with other USB 3.1 design elements, e.g. a bus repeater.

4.5.1.2 Connecting DFPs and UFPs

Given that the USB Type-C receptacle and plug no longer differentiate host and device roles based on connector shape, e.g., as was the case with USB Type-A and Type-B connectors, any two ports that have USB Type-C receptacles can be connected together with a standard USB Type-C cable. Table 4-5 summarizes the expected results when interconnecting DFP, UFP and DRP ports.

Table 4-5 – USB Type-C-based Port Interoperability

	DFP	UFP	DRP
DFP	Non-functional	Functional	Functional
UFP	Functional	Non-functional	Functional
DRP	Functional	Functional	Functional ¹

¹ Resolution of roles may be automatic or manually driven

In the cases where no function results, neither port shall be harmed by this connection. The user has to independently realize the invalid combination and take appropriate action to resolve. While these two invalid combinations mimic traditional USB where DFP-to-DFP and UFP-to-UFP connections are not intended to work, the non-keyed USB Type-C solution does not prevent the user from attempting such interconnects. VBUS and VCONN shall not be applied by a DFP in these cases.

The typical flow for the configuration of the interface in the general USB case of a DFP to a UFP is as follows:

- 1) Detect a valid connection between the ports (including determining cable orientation and DFP/UFP relationship)
- 2) Optionally discover the cable's capabilities
- 3) Optionally establish alternatives to traditional USB power (See Section 4.6.2)

- a) **USB PD** communication over CC for advanced power delivery negotiation
- b) USB Type-C Current modes
- c) USB BC 1.2

4) USB Device Enumeration

For cases of DRPs connecting to either DFP, UFP or another DRP, the process is essentially the same except that during the detecting a valid connection step, the DRP alternates between operating as a DFP for detecting an attached UFP and presenting as a UFP to be detected by an attached DFP. Ultimately this results in a DFP-to-UFP connection.

4.5.1.2.1 Detecting a Valid DFP-to-UFP Connection

The general concept for setting up a valid connection between a DFP and UFP is based on being able to detect terminations residing in the product being attached.

To aid in defining the functional behavior of CC, a pull-up (**R_p**) and pull-down (**R_d**) termination model is used – actual implementation in hosts and devices may vary, for example, the pull-up termination could be replaced by a current source. Figure 4-5 and Figure 4-6 illustrates two models, the first based on a pull-up resistor in the DFP and the second replacing this with a current source.

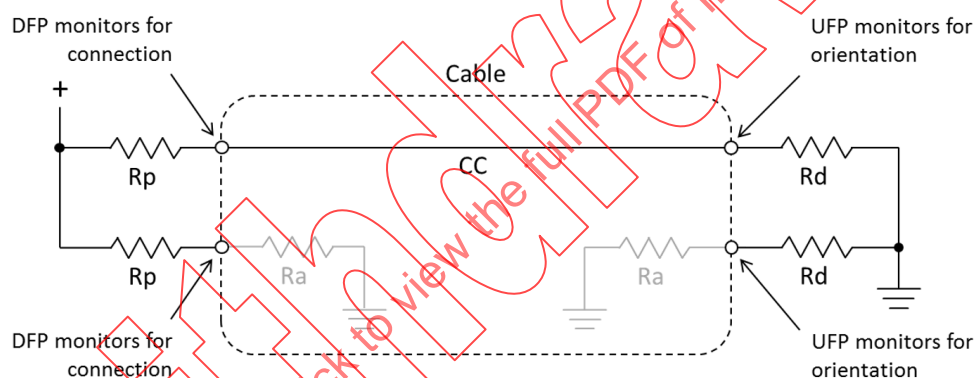


Figure 4-5 – Pull-Up/Pull-Down CC Model

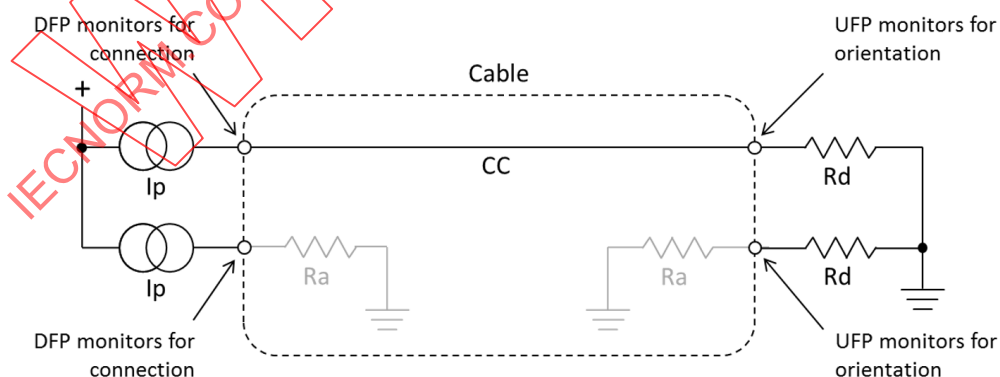


Figure 4-6 – Current Source/Pull-Down CC Model

Initially, a DFP exposes **R_p** terminations on its CC pins and a UFP exposes **R_d** terminations on its CC pins, the DFP-to-UFP combination of this circuit configuration represents a valid connection. To detect this, the DFP monitors both CC pins for a voltage lower than its unterminated voltage – the choice of **R_p** is a function of the pull-up termination voltage and

the DFP's detection circuit. This indicates that either a UFP, a powered cable, or a UFP connected via a powered cable has been attached.

Prior to application of VCONN, a powered cable exposes **Ra** on its VCONN pin. **Ra** represents the load on VCONN plus any resistive elements to ground. In some cable plugs it might be a pure resistance and in others it may be simply the load.

The DFP has to be able to differentiate between the presence of **Rd** and **Ra** to know whether there is a UFP attached and where to apply VCONN. The DFP is not required to source VCONN unless **Ra** is detected.

Two special termination combinations on the CC pins as seen by a DFP are defined for directly attached Accessory Modes: **Ra/Ra** for Audio Adapter Accessory Mode (A) and **Rd/Rd** for Debug Accessory Mode (B).

The DFP uses de-bounce timers to reliably detect states on the CC pins to de-bounce the connection (**tCCDebounce**), and hide **USB PD** BMC communications (**tPDDebounce**).

Table 4-6 summarizes the port state from the DFP's perspective.

Table 4-6 – Source Perspective

CC1	CC2	State	Position
Open	Open	Nothing attached	N/A
Rd	Open	Sink attached	①
Open	Rd		②
Open	Ra	Powered cable without Sink attached	①
Ra	Open		②
Rd	Ra	Powered cable with Sink or Vconn-powered Accessory attached	①
Ra	Rd		②
Rd	Rd	Debug Accessory Mode attached (Appendix B)	N/A
Ra	Ra	Audio Adapter Accessory Mode attached (Appendix A)	N/A

When the UFP senses VBUS, the UFP monitors both CC pins for a voltage greater than its local ground. The CC pin that is at a higher voltage (i.e. pulled up by **Rp** in the DFP) indicates the orientation of the plug.

Table 4-7 summarizes the typical behaviors for simple DFPs and UFPs for each state in Table 4-6.

Table 4-7 – Source and Sink Behaviors by State

State	Source Behavior	Sink Behavior
Nothing attached	– Sense CC pins for attach – Do not apply VBUS or VCONN	– Sense VBUS for attach
Sink attached	– Sense CC for orientation – Sense CC for detach – Apply VBUS and VCONN	– Sense CC pins for orientation – Sense loss of VBUS for detach
Powered cable without Sink attached	– Sense CC pins for attach – Do not apply VBUS or VCONN	– Sense VBUS for attach
Powered cable with Sink or Vconn-powered Accessory attached	– Sense CC for orientation – Sense CC for detach – Apply VBUS and VCONN	– If accessories are supported, see Source Behavior with exception that VBUS is not applied, otherwise, N/A.
Debug Accessory Mode attached	– Sense CC pins for detach – Reconfigure for debug	– If accessories are supported, see Source Behavior, otherwise, N/A
Audio Adapter Accessory Mode attached	– Sense CC pins for detach – Reconfigure for analog audio	– If accessories are supported, see Source Behavior, otherwise, N/A

Figure 4-3 shows how the inserted plug orientation is detected at the DFP's receptacle by noting on which of the two CC pins in the receptacle an R_d termination is sensed. Now that the DFP has recognized that a UFP is attached and the plug orientation is determined, it configures the SuperSpeed USB data bus routing to the receptacle.

The DFP then turns on VBUS. For the CC pin that does not connect DFP-to-UFP through the cable, the DFP supplies VCONN and may remove the termination. With the UFP now powered, it configures the USB data path. This completes the DFP-to-UFP connection.

The DFP monitors the CC wire for the loss of pull-down termination to detect detach. If the UFP is removed, the DFP port removes any voltage applied to VBUS and VCONN, resets its interface configuration and resumes looking for a new UFP attach.

Once a valid DFP-to-UFP connection is established, alternatives to traditional USB power (VBUS as defined by either [USB 2.0](#) or [USB 3.1](#) specifications) may be available depending on the capabilities of the host and device. These include USB Type-C Current, USB Power Delivery, and [USB Battery Charging 1.2](#).

In the case where [USB PD](#) PR_Swap is used to swap the source and sink of VBUS, the source of VCONN remains unchanged during and after the VBUS power swap. The new source monitors the CC wire and the new sink monitors VBUS to detect detach. When a detach event is detected, any voltages applied to VBUS and VCONN are removed, each port resets its interface configuration and resumes looking for an attach event.

In the case where [USB PD](#) DR_Swap is used to swap the DFP and UFP, the new UFP maintains sourcing VCONN during and after the data role swap.

In the case where [USB PD](#) VCONN_Swap is used to swap the VCONN source, the VBUS source/sink and DFP/UFP roles are maintained during and after the VCONN swap.

The last step in the normal USB Type-C connect process is for the USB device to be attached and enumerated per standard [USB 2.0](#) and [USB 3.1](#) processes.

4.5.1.3 Configuration Channel Functional Models

The functional models for the configuration channel behavior based on the CC1 and CC2 pins are described in this section for each port type: DFP, UFP and DRP.

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete. In these figures, VBUS and VCONN may or may not actually be available.

4.5.1.3.1 DFP Configuration Channel Functional Model

Figure 4-7 illustrates the functional model for CC1 and CC2 for a DFP prior to attach. This illustration includes consideration for the [USB PD](#) Provider.

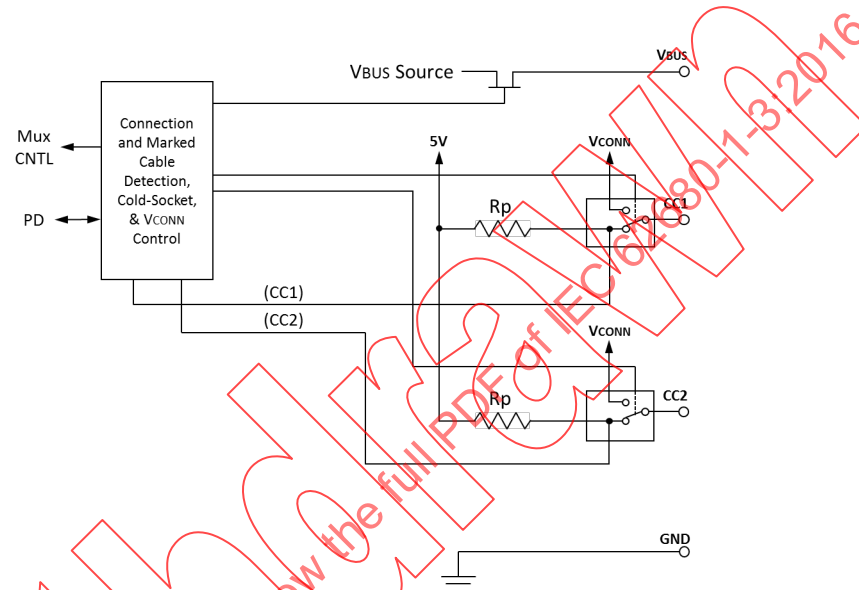


Figure 4-7 – DFP Functional Model for CC1 and CC2

Referring to Figure 4-7, a port that behaves as a DFP has the following functional characteristics:

- 1) The DFP uses a FET to enable/disable power delivery across VBUS and initially the DFP has VBUS disabled.
- 2) The DFP supplies pull-up resistors (R_p) on CC1 and CC2 and monitors both CC pins to detect a UFP – the presence of an R_d pull-down resistor on either pin indicates that a UFP is being attached. The value of R_p indicates the initial USB Type-C Current level supported by the host.
- 3) The DFP uses the CC pin pull-down characteristic to detect and establish the correct routing for the USB SuperSpeed data path and determine which CC pin is intended for supplying VCONN.
- 4) Once a UFP is detected, the DFP enables VBUS and VCONN.
- 5) The DFP can dynamically adjust the value of R_p to indicate a change in available USB Type-C Current to a UFP.
- 6) The DFP monitors the continued presence of R_d to detect UFP detach. When a detach event is detected, the DFP removes VBUS and VCONN, and returns to step 2.
- 7) If the DFP supports advanced functions (USB Power Delivery and/or Alternate Modes), [USB PD](#) communication is required.

Figure 4-8 illustrates the functional model for CC1 and CC2 for a DFP that is a [USB PD](#) Provider/Consumer (e.g., supports [USB PD](#) PR_Swap) prior to attach.

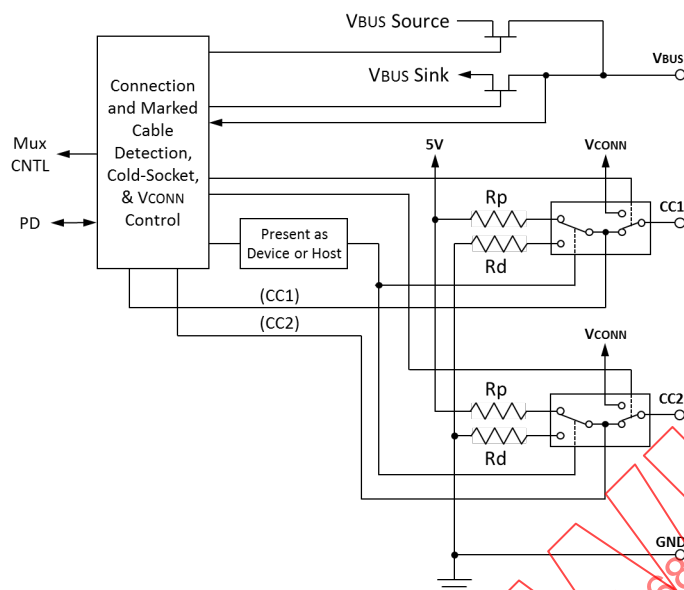


Figure 4-8 – DFP Functional Model Supporting USB PD Provider/Consumer

4.5.1.3.2 UFP Configuration Channel Functional Model

Figure 4-9 illustrates the functional model for CC1 and CC2 for a UFP. This illustration includes consideration for both USB Type-C Current and **USB PD** Consumer.

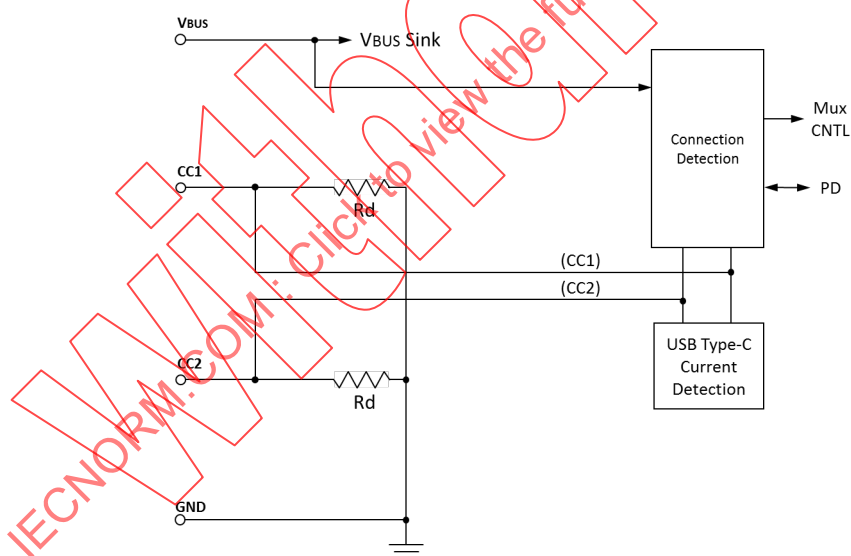


Figure 4-9 – UFP Functional Model for CC1 and CC2

Referring to Figure 4-9, a port that behaves as a UFP has the following functional characteristics:

- 1) The UFP terminates both CC1 and CC2 to GND using pull-down resistors.
- 2) The UFP determines that a DFP is attached by the presence of power on VBUS.
- 3) The UFP uses the CC pin pull-up characteristic to detect and establish the correct routing for the USB SuperSpeed data path.
- 4) The UFP can optionally monitor CC to detect an available higher USB Type-C Current from the DFP. The UFP shall manage its load to stay within the detected DFP current limit.

- 5) If the UFP supports advanced functions (USB Power Delivery and/or Alternate Modes), **USB PD** communication is required.

Figure 4-10 illustrates the functional model for CC1 and CC2 for a UFP that is a **USB PD** Consumer/Provider (e.g., supports **USB PD** PR_Swap) and supports **USB PD** VCONN_Swap prior to attach.

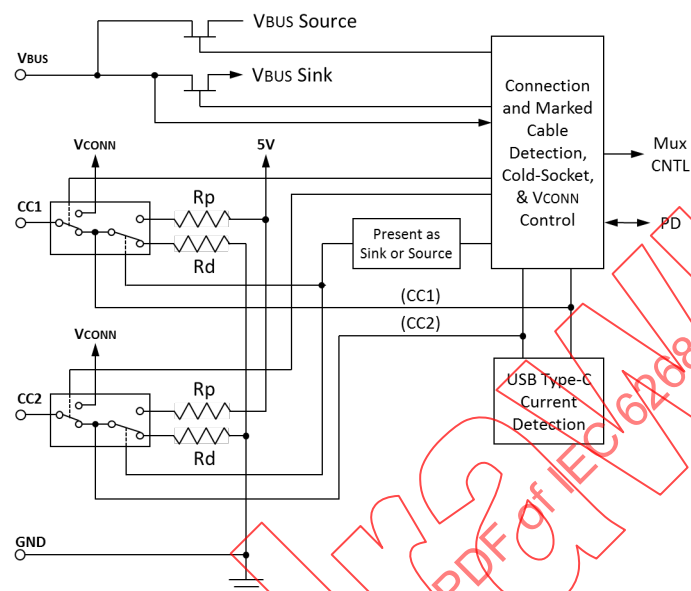


Figure 4-10 – UFP Functional Model Supporting USB PD Consumer/Provider and VCONN_Swap

4.5.1.3.3 DRP Configuration Channel Functional Model

Figure 4-11 illustrates the functional model for CC1 and CC2 for a DRP presenting as a DFP prior to attach. This illustration includes consideration for both the USB Type-C Current and the **USB PD** features.

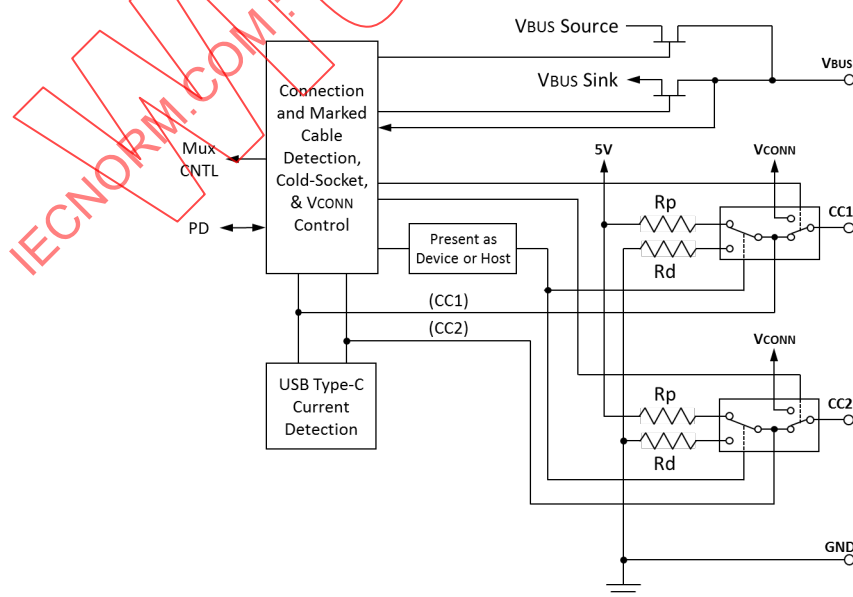


Figure 4-11 – DRP Functional Model for CC1 and CC2

Referring to Figure 4-11, a port that can alternate between DFP and UFP behaviors has the following functional characteristics:

- 1) The DRP uses a FET to enable/disable power delivery across VBUS and initially when in DFP mode has VBUS disabled.
- 2) The DRP uses switches for presenting as a DFP or UFP.
- 3) The DRP has logic used during initial attach to toggle between DFP and UFP operation:
 - a) Until a specific stable state is established, the DRP alternates between exposing itself as a DFP and UFP. The timing of this process is dictated by a period (**tDRP**), percentage of time that a DRP exposes **Rp (dcSRC.DRP)** and role transition time (**tDRPTransition**).
 - b) When the DRP is presenting as a DFP, it follows DFP operation to detect an attached UFP – if a UFP is detected, it applies VBUS, VCONN, and continues to operate as a DFP for a minimum of **tDRPHold** (e.g., cease alternating).
 - c) When the DRP is presenting as a UFP, it monitors VBUS to detect that it is attached to a DFP – if a DFP is detected, it continues to operate as a UFP (cease alternating).
- 4) If the DRP supports advanced functions (USB Power Delivery and/or Alternate Modes), **USB PD** communication is required.
 - a) If a DRP supports **USB PD**, initially the **USB PD** role follows the port role, i.e., when operating as a DFP, the **USB PD** operates as a Provider/Consumer and when operating as a UFP, the **USB PD** operates as a Consumer/Provider.

4.5.1.4 USB PD-based Power Role, Data Role and VCONN Swapping

Table 4-8 summarizes the behaviors of a port in response to the three **USB PD** swap commands.

Table 4-8 – USB PD Swapping Port Behavior Summary

	Host/Device Data Roles	Rp/Rd	VBUS Source/Sink	VCONN Source
PR_Swap	Unchanged	Swapped	Swapped	Unchanged
DR_Swap	Swapped	Unchanged	Unchanged	Unchanged
VCONN_Swap	Unchanged	Unchanged	Unchanged	Swapped ¹

¹ Swapping of VCONN source port.

4.5.2 CC Functional and Behavioral Requirements

This section provides the functional and behavioral requirements for implementing CC. The first sub-section provides connection state diagrams that are the basis for the remaining sub-sections.

The terms Source (SRC) and Sink (SNK) used in this section refer to the port's power role while the terms DFP and UFP refer to the port's data role. A DRP (Dual Role Port) is capable of acting as either a Source or Sink. Typically DFPs are found on hosts and source VBUS while a UFP is found on a device and sinks power from VBUS. When a connection is initially made, the port's initial power state and data role are established. USB PD introduces three swap commands that may alter a port's power or data role:

- The PR_Swap command changes the port's power state as reflected in the following state machines. PR_Swap does not change the port sourcing VCONN.
- The DR_Swap command has no effect on the following state machines or VCONN as it only changes the port's data role.

- VCONN_Swap command changes the port sourcing VCONN. The PR_Swap command and DR_Swap command have no effect on the port sourcing VCONN.

The connection state diagrams and CC behavior descriptions in this section describe the behavior of receptacle-based ports. The plug on a direct connect device or a device with a captive cable shall behave as a plug on a cable that is attached at its other end in normal orientation to a receptacle. These devices shall apply and sense CC voltage levels on pin A5 only and pin B5 shall have an impedance above zOPEN, unless it is a Powered Accessory, in which case B5 shall have an impedance [Ra](#).

4.5.2.1 Connection State Diagrams

This section provides reference connection state diagrams for CC-based behaviors.

Refer to Section 4.5.2.2 for the specific state transition requirements related to each state shown in the diagrams.

Refer to Section 4.5.2.4 for a description of which states are mandatory for each port type, and a list of states where [USB PD](#) communication is permitted.

Figure 4-12 illustrates a connection state diagram for a Source (Host/Hub DFP).

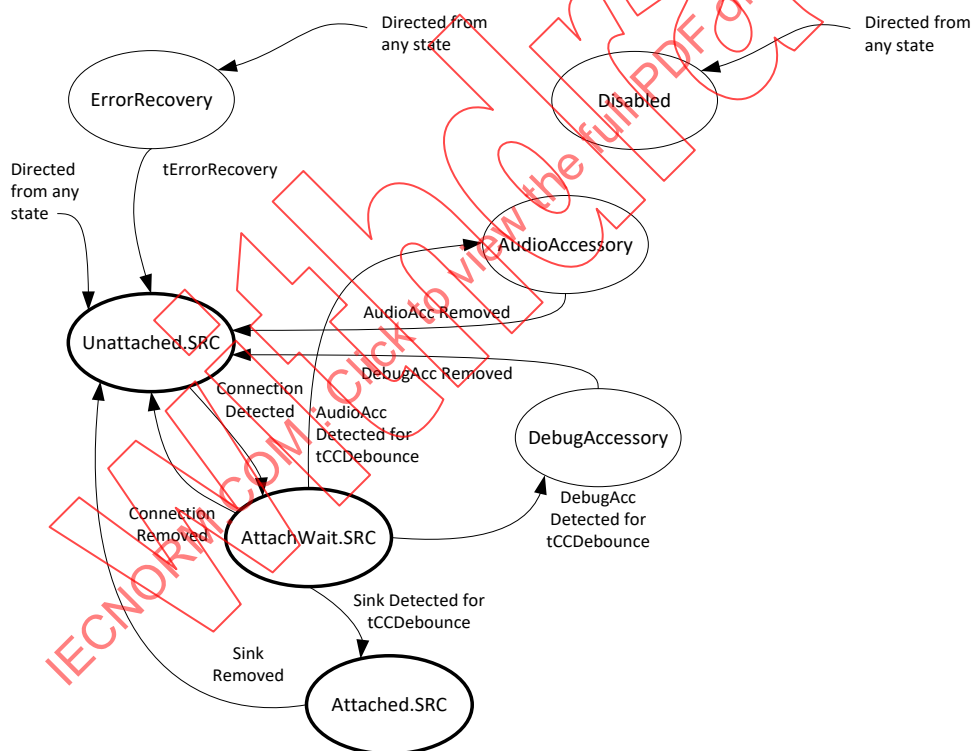


Figure 4-12 – Connection State Diagram: Source

Figure 4-13 illustrates a connection state diagram for a simple Sink (Device UFP).

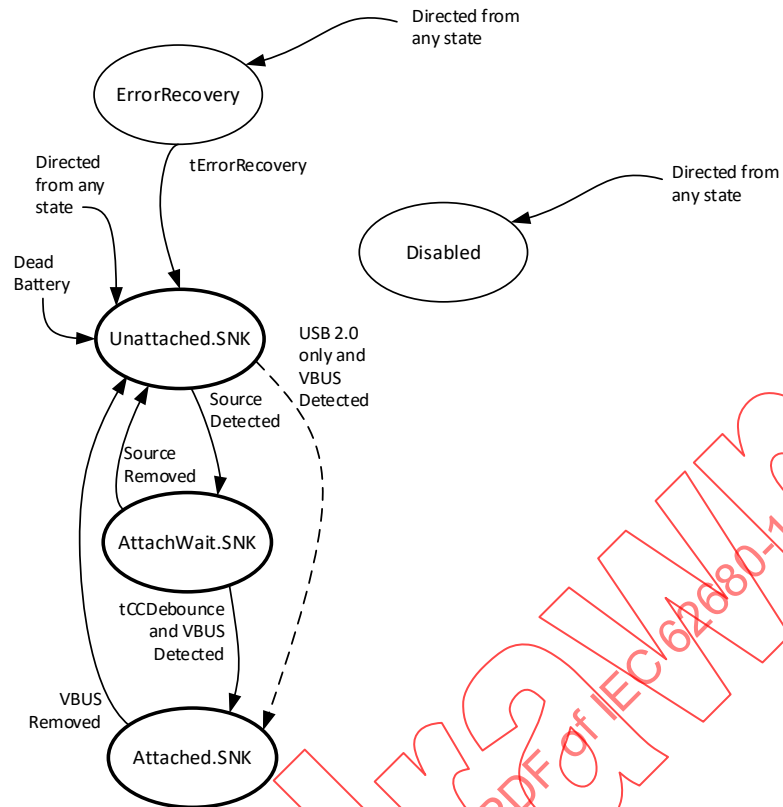


Figure 4-13 – Connection State Diagram: Sink

Figure 4-14 illustrates a connection state diagram for a Sink that supports Accessory Modes.

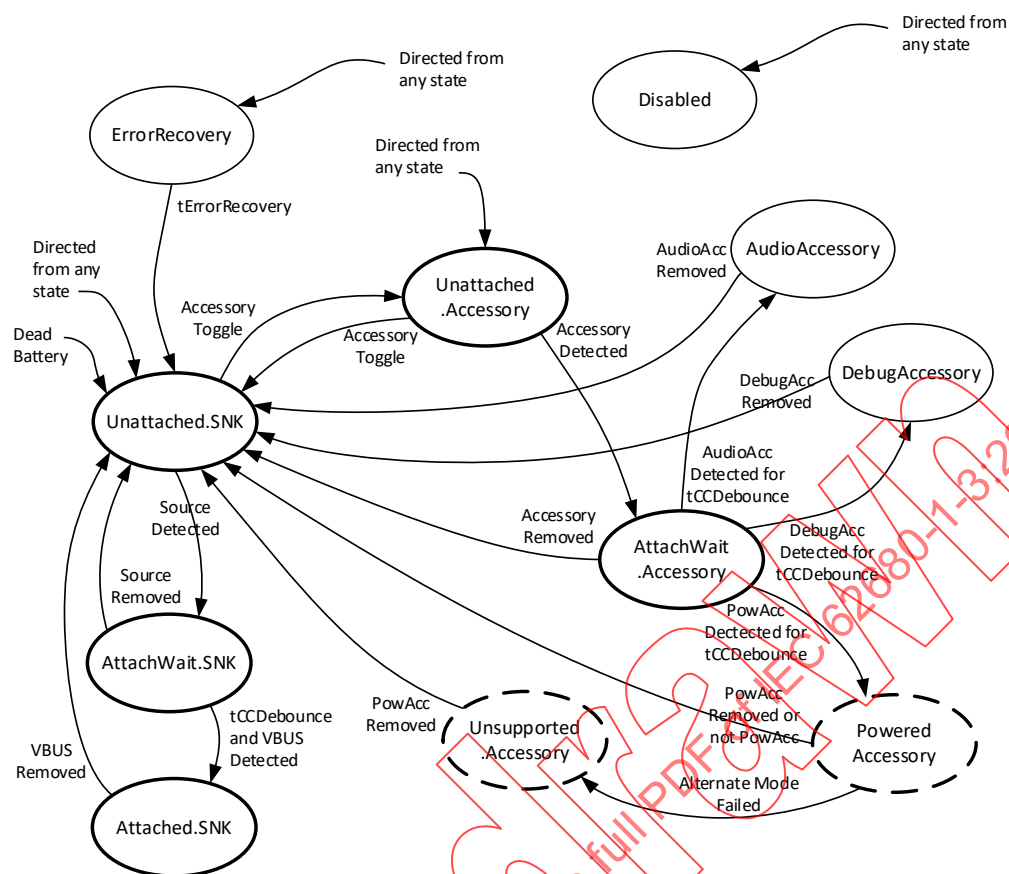


Figure 4-14 – Connection State Diagram: Sink with Accessory Support

Figure 4-15 illustrates a connection state diagram for a simple DRP.

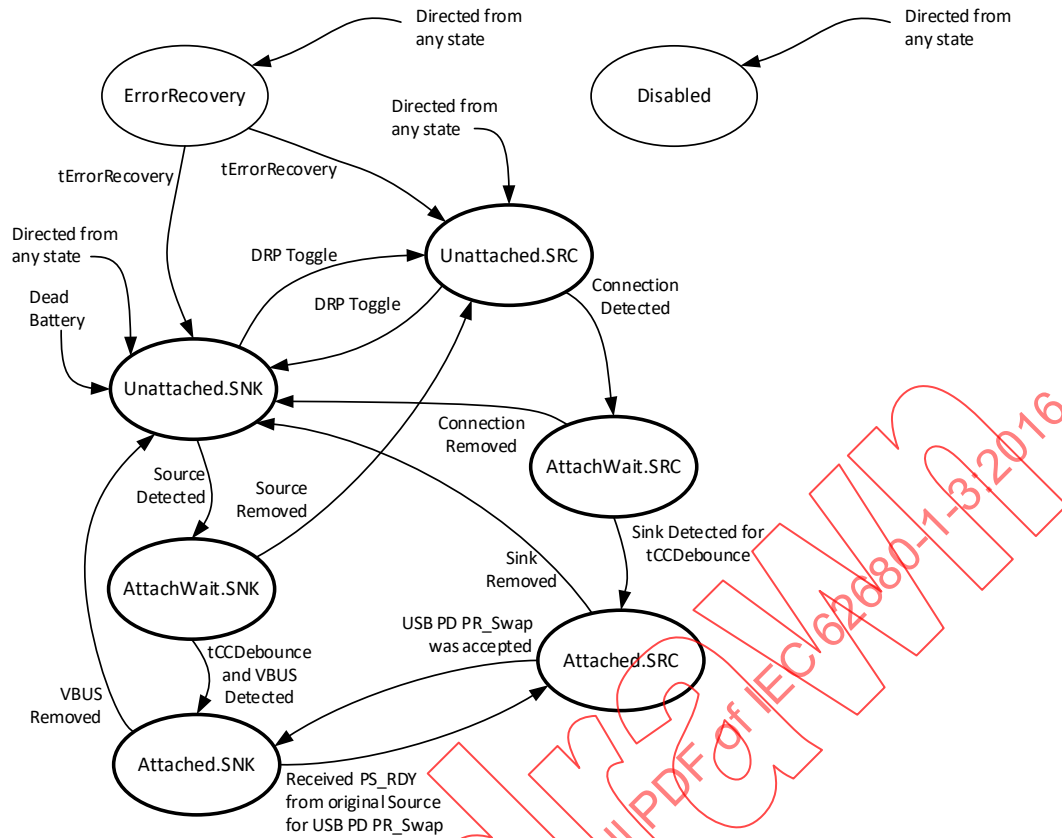


Figure 4-15 – Connection State Diagram: DRP

Figure 4-16 illustrates a connection state diagram for a DRP that supports all possible states including Accessory Modes and Try.SRC.

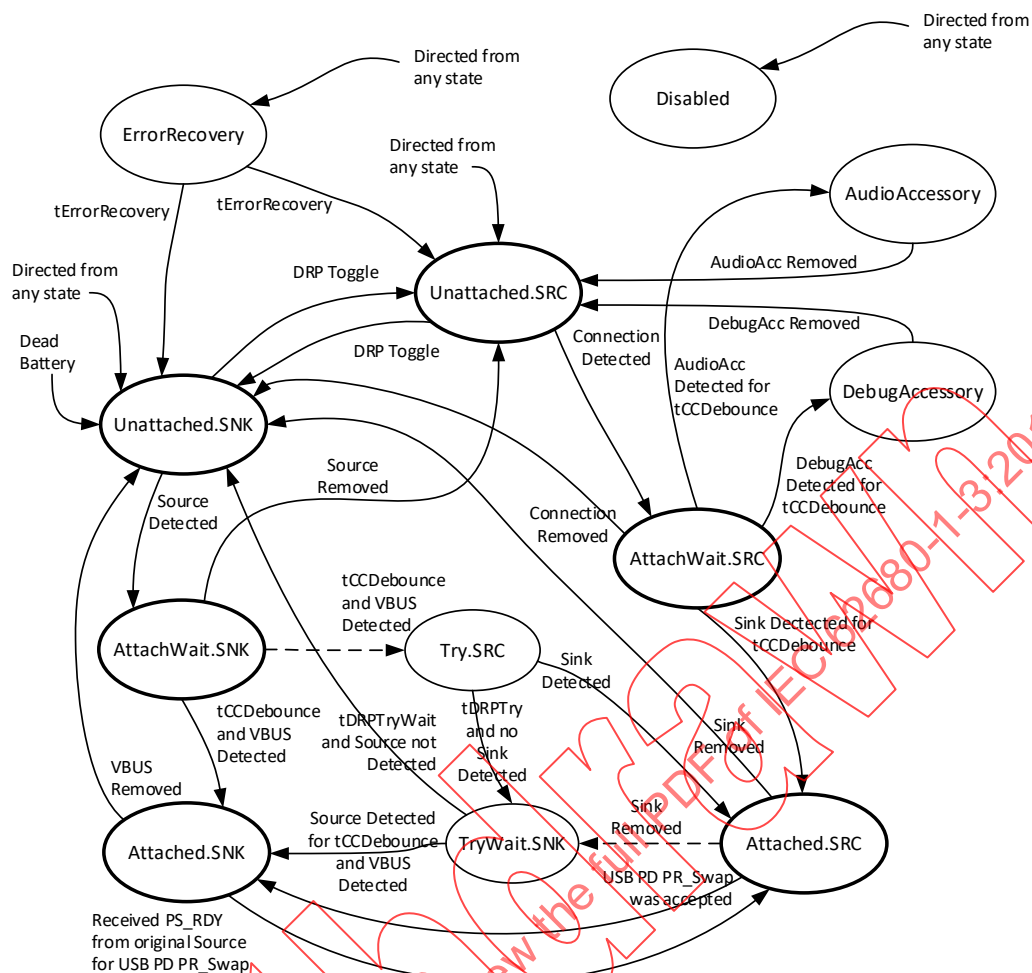


Figure 4-16 – Connection State Diagram: DRP with Accessory and Try.SRC Support

4.5.2.2 Connection State Machine Requirements

Entry into any unattached state when “directed from any state” shall not be used to override tDRP toggle.

A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has two CC pins, each with its own individual CC pin state. The combination of a port’s two CC pin states are be used to define the conditions under which a port transitions from one state to another.

Table 4-9 – Source Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	Open, Rp	Above vOPEN
SRC.Rd	Rd	Within the vRd range (i.e., between minimum vRd and maximum vRd)
SRC.Ra	Ra	Below maximum vRa

Table 4-10 – Sink Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	Rp	Above minimum vRd-Connect
SNK.Open	Open, Ra, Rd	Below maximum vRa

4.5.2.2.1 Disabled State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15 and Figure 4-16.

The Disabled state is where the port prevents connection from occurring by removing all terminations from the CC pins.

The port should transition to the Disabled state from any other state when directed.

A port may choose not to support the Disabled state. If the Disabled state is not supported, the port shall be directed to either the **Unattached.SNK** or **Unattached.SRC** states after power-on.

4.5.2.2.1.1 Disabled State Requirements

The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above **zOPEN**) on its CC pins.

4.5.2.2.1.2 Exiting From Disabled State

A Sink shall transition to **Unattached.SNK** when directed.

A Source shall transition to **Unattached.SRC** when directed.

A DRP shall transition to either **Unattached.SNK** or **Unattached.SRC** when directed.

4.5.2.2.2 ErrorRecovery State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15 and Figure 4-16.

The ErrorRecovery state is where the port cycles its connection by removing all terminations from the CC pins for **tErrorRecovery** followed by transitioning to the appropriate **Unattached.SNK** or **Unattached.SRC** state based on port type.

The port should transition to the ErrorRecovery state from any other state when directed.

A port may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the port shall be directed to the Disabled state if supported. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states.

4.5.2.2.2.1 ErrorRecovery State Requirements

The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC pins.

4.5.2.2.2.2 Exiting From ErrorRecovery State

A Sink shall transition to Unattached.SNK after tErrorRecovery.

A Source shall transition to Unattached.SRC after tErrorRecovery.

A DRP shall transition to either Unattached.SNK or Unattached.SRC after tErrorRecovery.

4.5.2.2.3 Unattached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15 and Figure 4-16.

When in the Unattached.SNK state, the port is waiting to detect the presence of a Source.

A port with a dead battery shall enter this state while unpowered.

4.5.2.2.3.1 Unattached.SNK Requirements

The port shall not drive VBUS or VCONN.

Both CC pins shall be independently terminated to ground through Rd.

4.5.2.2.3.2 Exiting from Unattached.SNK State

The port shall transition to AttachWait.SNK when a Source connection is detected, as indicated by the SNK.Rp state on one of its CC pins.

A USB 2.0 only Sink without Accessory support that is self-powered or requires only default power and does not support USB PD may transition directly to Attached.SNK when VBUS is detected.

A DRP shall transition to Unattached.SRC within tDRPTransition after the state of both CC pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.

A Sink with Accessory support shall transition to Unattached.Accessory within tDRPTransition after the state of both CC pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.

4.5.2.2.4 AttachWait.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15 and Figure 4-16.

When in the AttachWait.SNK state, the port has detected the SNK.Rp state on one CC pin and is waiting for VBUS.

4.5.2.2.4.1 AttachWait.SNK Requirements

The port shall not drive VBUS or VCONN.

Both CC pins shall be independently terminated to ground through [Rd](#).

It is strongly recommended that a USB 3.1 SuperSpeed device hold off VBUS detection to the device controller until the [Attached.SNK](#) state is reached, i.e. one CC pin is in the [SNK.Rp](#) state. Otherwise, it may connect as USB 2.0 when attached to a legacy host or hub's DFP.

4.5.2.2.4.2 Exiting from AttachWait.SNK State

A Sink shall transition to [Unattached.SNK](#) when the state of both CC pins is [SNK.Open](#) for at least [tPDDebounce](#).

A DRP shall transition to [Unattached.SRC](#) when the state of both CC pins is [SNK.Open](#) for at least [tPDDebounce](#).

The port shall transition to [Attached.SNK](#) if the state of exactly one CC pin has been [SNK.Open](#) for at least [tCCDebounce](#) and VBUS is detected. Note the Source may initiate [USB PD](#) communications which will cause brief periods of the [SNK.Open](#) state on both CC pins, but this event will not exceed [tPDDebounce](#).

A DRP that strongly prefers the Source role may optionally transition to [Try.SRC](#) instead of [Attached.SNK](#) when the state of one CC pin has been [SNK.Rp](#) for at least [tCCDebounce](#) and VBUS is detected.

4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15 and Figure 4-16.

When in the [Attached.SNK](#) state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using [USB PD](#) commands.

A port that entered this state directly from [Unattached.SNK](#) due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use [USB PD](#).

4.5.2.2.5.1 Attached.SNK Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which CC pin is connected through the cable (i.e., the CC pin that is in the [SNK.Rp](#) state).

If the port supports signaling on USB SuperSpeed pairs, it shall functionally connect the USB SuperSpeed pairs and maintain the connection during and after a [USB PD](#) PR_Swap.

If the port has entered the [Attached.SNK](#) state from the [AttachWait.SNK](#) or [TryWait.SNK](#) states, only one CC pin will be in the [SNK.Rp](#) state. The port shall continue to terminate this CC pin to ground through [Rd](#).

If the port has entered the [Attached.SNK](#) state from the [Attached.SRC](#) state following a [USB PD](#) PR_Swap, the port shall terminate the connected CC pin to ground through [Rd](#).

The port shall meet the [Sink Power Sub-State](#) requirements specified in Section 4.5.2.3.

The port may negotiate a **USB PD** PR_Swap, DR_Swap or VCONN_Swap.

By default, upon entry from **AttachWait.SNK** or **Unattached.SNK**, VCONN shall not be supplied in the **Attached.SNK** state. If **Attached.SNK** is entered from **Attached.SRC** as a result of a **USB PD** PR_Swap, it shall maintain VCONN supply state, whether on or off, and its data role/connections. A **USB PD** DR_Swap has no effect on which port sources VCONN.

The port may negotiate a **USB PD** VCONN_Swap. When the port successfully executes **USB PD** VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within **tVCONNON**. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes **USB PD** VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within **tVCONNOFF**.

4.5.2.2.5.2 Exiting from Attached.SNK State

A port that is not in the process of a **USB PD** PR_Swap or a **USB PD** Hard Reset shall transition to **Unattached.SNK** when VBUS is no longer present. If supplying VCONN, the port shall cease to supply it within **tVCONNOFF** of exiting **Attached.SNK**.

After receiving a **USB PD** PS_RDY from the original Source during a **USB PD** PR_Swap, the port shall transition directly to the **Attached.SRC** state (i.e., remove **Rd** from CC, assert **Rp** on CC and supply VBUS), but shall maintain its VCONN supply state, whether off or on, and its data role/connections.

4.5.2.2.6 Unattached.SRC State

This state appears in Figure 4-12, Figure 4-15 and Figure 4-16.

When in the **Unattached.SRC** state, the port is waiting to detect the presence of a Sink or an Accessory.

4.5.2.2.6.1 Unattached.SRC Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both CC pins independently.

The port shall provide an **Rp** as specified in Table 4-13.

4.5.2.2.6.2 Exiting from Unattached.SRC State

The port shall transition to **AttachWait.SRC** when:

- The **SRC.Rd** state is detected on at least one CC pin or
- The **SRC.Ra** state is detected on both CC pins.

NOTE A cable without an attached device can be detected, when the **SRC.Ra** state is detected on one CC pin and the **SRC.Open** state is detected on the other CC pin. However in this case, the port shall not transition to **AttachWait.SRC**.

A DRP shall transition to **Unattached.SNK** within **tDRPTransition** after **dcSRC.DRP** · **tDRP**, or if directed.

4.5.2.2.7 AttachWait.SRC State

This state appears in Figure 4-12, Figure 4-15 and Figure 4-16.

The AttachWait.SRC state is used to ensure that the state of both of the CC pins is stable after a Sink is connected.

4.5.2.2.7.1 AttachWait.SRC Requirements

The requirements for this state are identical to [Unattached.SRC](#).

4.5.2.2.7.2 Exiting from AttachWait.SRC State

The port shall transition to [Attached.SRC](#) when VBUS is at vSafe0V and the [SRC.Rd](#) state is detected on exactly one of the CC pins for at least [tCCDebounce](#).

If the port supports Audio Adapter Accessory Mode, it shall transition to [AudioAccessory](#) when the [SRC.Ra](#) state is detected on both CC pins for at least [tCCDebounce](#).

If the port supports Debug Accessory Mode, it shall transition to [DebugAccessory](#) when the [SRC.Rd](#) state is detected on both CC pins for at least [tCCDebounce](#).

A Source shall transition to [Unattached.SRC](#) and a DRP to [Unattached.SNK](#) when the [SRC.Open](#) state is detected on both CC pins.

A Source shall transition to [Unattached.SRC](#) and a DRP to [Unattached.SNK](#) when the [SRC.Open](#) state is detected on one CC pin and the [SRC.Ra](#) state is detected on the other CC pin.

4.5.2.2.8 Attached.SRC State

This state appears in Figure 4-12, Figure 4-15 and Figure 4-16.

When in the [Attached.SRC](#) state, the port is attached and operating as a Source. When the port initially enters this state it is also operating as a DFP. Subsequently, the initial power and data roles can be changed using [USB PD](#) commands.

4.5.2.2.8.1 Attached.SRC Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to the [Attached.SRC](#) state by detecting which CC pin is connected through the cable, i.e., which CC pin is in the [SRC.Rd](#) state.

If the port has entered this state from the [AttachWait.SRC](#) state or the [Try.SRC](#) state, the [SRC.Rd](#) state will be on only one CC pin. The port shall source current on this CC pin and monitor its state.

If the port has entered this state from the [Attached.SNK](#) state as the result of a [USB PD](#) PR_Swap, the port shall source current on the connected CC pin and monitor its state.

The port shall provide an [Rp](#) as specified in Table 4-13.

The port shall supply VBUS current at the level it advertises on [Rp](#).

The port shall supply VBUS within [tVBUSON](#) of entering this state, and for as long as it is operating as a power source.

The port shall not initiate any [USB PD](#) communications until VBUS reaches vSafe5V.

If the port supports signaling on USB SuperSpeed pairs, it shall:

- Functionally connect the USB SuperSpeed pairs
- For VCONN, do one of two things:
 - Apply VCONN unconditionally to the CC pin not in the **SRC.Rd** state, or
 - Apply VCONN to the CC pin in the **SRC.Ra** state.

A port that does not support signaling on USB SuperSpeed pairs may supply VCONN in the same manner described above.

The port may negotiate a **USB PD** PR_Swap, DR_Swap or VCONN_Swap.

If the port supplies VCONN, it shall do so within **tVCONNON**.

The port shall not supply VCONN if it has entered this state as a result of a **USB PD** PR_Swap and was not previously supplying VCONN. A **USB PD** DR_Swap has no effect on which port sources VCONN.

The port may negotiate a **USB PD** VCONN_Swap. When the port successfully executes **USB PD** VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within **tVCONNOFF**. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes **USB PD** VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within **tVCONNON**.

4.5.2.2.8.2 Exiting from Attached.SRC State

A Source shall transition to **Unattached.SRC** when the **SRC.Open** state is detected on the monitored CC pin.

When the **SRC.Open** state is detected on the monitored CC pin, a DRP shall transition to **Unattached.SNK** unless it strongly prefers the Source role. In that case, it shall transition to **TryWait.SNK**. This transition to **TryWait.SNK** is needed so that two devices that both prefer the Source role do not loop endlessly between Source and Sink. In other words, a DRP that would enter **Try.SRC** from **AttachWait.SNK** shall enter **TryWait.SNK** for a Sink detach from **Attached.SRC**.

A port shall cease to supply VBUS within **tVBUSOFF** of exiting **Attached.SRC**.

A port that is supplying VCONN shall cease to supply it within **tVCONNOFF** of exiting **Attached.SRC**, unless it is exiting as a result of a **USB PD** PR_Swap.

After a **USB PD** PR_Swap is accepted (i.e., either an Accept message is received or acknowledged), a DRP shall transition directly to the **Attached.SNK** state (i.e., remove **Rp** from CC, assert **Rd** on CC and stop supplying VBUS) and maintain its current data role, connection and VCONN supply state.

4.5.2.2.9 Try.SRC State

This state appears in Figure 4-16.

When in the Try.SRC state, the port is querying to determine if the port partner supports the Sink role.

4.5.2.2.9.1 Try.SRC Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both CC pins independently.

The port shall provide an **R_p** as specified in Table 4-13.

4.5.2.2.9.2 Exiting from Try.SRC State

The port shall transition to **Attached.SRC** when the **SRC.Rd** state is detected on exactly one of the CC pins for at least **tPDDebounce**.

The port shall transition to **TryWait.SNK** after **tDRPTry** and the **SRC.Rd** state has not been detected.

4.5.2.2.10 TryWait.SNK State

This state appears in Figure 4-16.

When in the **TryWait.SNK** state, the port has failed to become a Source and is waiting to attach as a Sink. Alternatively the port is responding to Sink being removed while in the **Attached.SRC** state.

4.5.2.2.10.1 TryWait.SNK Requirements

The port shall not drive VBUS or VCONN.

Both CC pins shall be independently terminated to ground through **R_d**.

4.5.2.2.10.2 Exiting from TryWait.SNK State

The port shall transition to **Attached.SNK** if the state of exactly one CC pin has been **SNK.Open** for at least **tCCDebounce** and VBUS is detected. Note the Source may initiate **USB PD** communications which will cause brief periods of the **SNK.Open** state on both CC pins, but this event will not exceed **tPDDebounce**.

The port shall transition to **Unattached.SNK** after **tDRPTryWait** if the state of both of the CC pins is **SNK.Open**.

4.5.2.2.11 Unattached.Accessory State

This state appears in Figure 4-14.

The Unattached.Accessory state allows accessory-supporting Sinks to connect to accessories.

This state is functionally equivalent to the **Unattached.SRC** state in a DRP, except that **Attached.SRC** is not supported.

4.5.2.2.11.1 Unattached.Accessory Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both CC pins independently.

The port shall provide an **R_p** as specified in Table 4-13.

4.5.2.2.11.2 Exiting from Unattached.Accessory State

The port shall transition to [AttachWait.Accessory](#) when the state of neither of the CC pins is [SRC.Open](#).

The port shall transition to [Unattached.SNK](#) within [tDRPTransition](#) after $dcSRC.DRP \cdot tDRP$, and the state of at least one CC pin is [SRC.Open](#) or if directed.

4.5.2.2.12 AttachWait.Accessory State

This state appears in Figure 4-14.

The AttachWait.Accessory state is used to ensure that the state of both of the CC pins is stable after a cable is plugged in.

4.5.2.2.12.1 AttachWait.Accessory Requirements

The requirements for this state are identical to [Unattached.Accessory](#).

4.5.2.2.12.2 Exiting from AttachWait.Accessory State

If the port supports Audio Adapter Accessory Mode, it shall transition to [AudioAccessory](#) when the state of both CC pins is [SRC.Ra](#) for at least [tCCDebounce](#).

If the port supports Debug Accessory Mode, it shall transition to [DebugAccessory](#) when the state of both CC pins is [SRC.Rd](#) for at least [tCCDebounce](#).

The port shall transition to [Unattached.SNK](#) when the state of either CC pin is [SRC.Open](#) for at least [tCCDebounce](#).

If the port supports VCONN-powered accessories, it shall transition to [PoweredAccessory](#) state if the state of one of its CC pins is [SRC.Rd](#) and the state of the other CC pin is [SRC.Ra](#) concurrently for at least [tCCDebounce](#).

4.5.2.2.13 AudioAccessory State

This state appears in Figure 4-12, Figure 4-14 and Figure 4-16.

The AudioAccessory state is used for the [Audio Adapter Accessory Mode](#) specified in A.

4.5.2.2.13.1 AudioAccessory Requirements

The port shall reconfigure its pins as detailed in A.

The port shall not drive VBUS or VCONN. A port that sinks current from the audio accessory over VBUS shall not draw more than 500 mA.

The port shall provide an [Rp](#) as specified in Table 4-13.

The port shall source current on at least one of the CC pins and monitor to detect when the CC pin state is no longer [SRC.Ra](#). If the port sources and monitors only one CC pin, then it shall ensure that the termination on the unmonitored CC pin does not affect the monitored signal when the port is connected to an Audio Accessory that may short both CC pins together.

4.5.2.2.13.2 Exiting from AudioAccessory State

If the port is a Sink or DRP, the port shall transition to [Unattached.SNK](#) when the state of the monitored CC pin(s) is [SRC.Open](#) for at least [tCCDebounce](#).

If the port is a Source, the port shall transition to [Unattached.SRC](#) when the state of the monitored CC pin(s) is [SRC.Open](#) for at least [tCCDebounce](#).

4.5.2.2.14 DebugAccessory

This state appears in Figure 4-12, Figure 4-14 and Figure 4-16.

The DebugAccessory state is used for the [Debug Accessory Mode](#) specified in B.

4.5.2.2.14.1 DebugAccessory Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall not drive VBUS or VCONN.

The port shall provide an [Rp](#) as specified in Table 4-13.

The port shall source current on at least one of the CC pins and monitor to detect when the CC pin state is no longer [SRC.Rd](#). If the port monitors only one CC pin, it shall source current on the monitored pin and may source current or not on the unmonitored pin.

4.5.2.2.14.2 Exiting from DebugAccessory State

If the port is a Sink or DRP, the port shall transition to [Unattached.SNK](#) when the [SRC.Open](#) state is detected on the monitored CC pin(s).

If the port is a Source, the port shall transition to [Unattached.SRC](#) when the [SRC.Open](#) state is detected on the monitored CC pin(s).

4.5.2.2.15 PoweredAccessory State

This state appears in Figure 4-14.

When in the PoweredAccessory state, the port is powering a [VCONN-Powered Accessory](#).

4.5.2.2.15.1 PoweredAccessory Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to the PoweredAccessory state by detecting which CC pin is connected through the cable (i.e., which CC pin is in the [SRC.Rd](#) state).

The [SRC.Rd](#) state is detected on only one CC pin. The port shall advertise either 1.5 A or 3.0 A (see Table 4-13) on this CC pin and monitor its state.

The port shall supply VCONN (2.7 V minimum) on the unused CC pin within [tvconnON-PA](#) of entering the PoweredAccessory state.

The port shall not drive VBUS.

When the port initially enters the PoweredAccessory state it shall operate as a DFP.

The port shall use **USB Power Delivery** Structured Vendor Defined Messages (Structured VDMs) to identify the accessory and enter an Alternate Mode.

4.5.2.2.15.2 Exiting from PoweredAccessory State

The port shall transition to **Unattached.SNK** when the **SRC.Open** state is detected on the monitored CC pin.

The port shall transition to **Unattached.SNK** if the attached device is not a **VCONN-Powered Accessory**. For example, the attached device does not support **USB PD** or does not respond to **USB PD** commands required for a **VCONN-Powered Accessory** (e.g., Discover SVIDs, Discover Modes, etc.).

The port shall transition to **Unsupported.Accessory** if it does not successfully enter an Alternate Mode within **tAMETimeout** (see Section 5.1).

The port shall cease to supply VCONN within **tVCONNOFF** of exiting the PoweredAccessory state.

4.5.2.2.16 Unsupported.Accessory State

This state appears in Figure 4-14.

If a VCONN-powered accessory does not enter an Alternate Mode, the Unsupported.Accessory state is used to wait until the accessory is unplugged before continuing.

4.5.2.2.16.1 Unsupported.Accessory Requirements

Only one CC pin shall be in the **SRC.Rd** state. The port shall advertise Default USB Power (see Table 4-13) on this CC pin and monitor its voltage.

The port shall not drive VBUS or VCONN.

4.5.2.2.16.2 Exiting from Unsupported.Accessory

The port shall transition to **Unattached.SNK** when the **SRC.Open** state is detected on the monitored CC pin.

4.5.2.3 Sink Power Sub-State Requirements

When in the **Attached.SNK** state and the Source is supplying default VBUS, the port shall operate in one of the sub-states shown in Figure 4-17. The initial Sink Power Sub-State is **PowerDefault.SNK**. Subsequently, the Sink Power Sub-State is determined by Source's USB Type-C current advertisement. The port in **Attached.SNK** shall remain within the Sink Power Sub-States until either VBUS is removed or a **USB PD** contract is established with the Source.

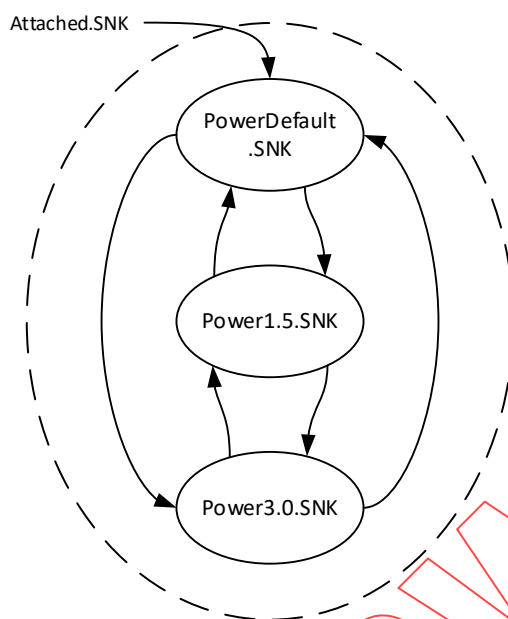


Figure 4-17 – Sink Power Sub-States

The Sink is only required to implement Sink Power Sub-State transitions if the Sink wants to consume more than default USB current.

4.5.2.3.1 PowerDefault.SNK Sub-State

This sub-state supports Sinks consuming current within the lowest range (default) of Source-supplied current.

4.5.2.3.1.1 PowerDefault.SNK Requirements

The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the port wants to consume more than the default USB power, it shall monitor **vRd** to determine if more current is available from the Source.

4.5.2.3.1.2 Exiting from PowerDefault.SNK

For any change on CC indicating a change in allowable power, the port shall not transition until the new **vRd** on CC has been stable for at least **tPDDebounce**.

For a **vRd** in the **vRd-1.5** range, the port shall transition to the **Power1.5.SNK Sub-State**.

For a **vRd** in the **vRd-3.0** range, the port shall transition to the **Power3.0.SNK Sub-State**.

4.5.2.3.2 Power1.5.SNK Sub-State

This sub-state supports Sinks consuming current within the two lower ranges (default and 1.5 A) of Source-supplied current.

4.5.2.3.2.1 Power1.5.SNK Requirements

The port shall draw no more than 1.5 A from VBUS.

The port shall monitor **vRd** while it is in this sub-state.

4.5.2.3.2.2 Exiting from Power1.5.SNK

For any change on CC indicating a change in allowable power, the port shall not transition until the new **vRd** on CC has been stable for at least **tPDDebounce**.

For a **vRd** in the **vRd-USB** range, the port shall transition to the **PowerDefault.SNK Sub-State** and reduce its power consumption to the new range within **tSinkAdj**.

For a **vRd** in the **vRd-3.0** range, the port shall transition to the **Power3.0.SNK Sub-State**.

4.5.2.3.3 Power3.0.SNK Sub-State

This sub-state supports Sinks consuming current within all three ranges (default, 1,5 A and 3,0 A) of Source-supplied current.

4.5.2.3.3.1 Power3.0.SNK Requirements

The port shall draw no more than 3,0 A from VBUS.

The port shall monitor **vRd** while it is in this sub-state.

4.5.2.3.3.2 Exiting from Power3.0.SNK

For any change on CC indicating a change in allowable power, the port shall not transition until the new **vRd** on CC has been stable for at least **tPDDebounce**.

For a **vRd** in the **vRd-USB** range, the port shall transition to the **PowerDefault.SNK Sub-State** and reduce its power consumption to the new range within **tSinkAdj**.

For a **vRd** in the **vRd-1.5** range, the port shall transition to the **Power1.5.SNK Sub-State** and reduce its power consumption to the new range within **tSinkAdj**.

4.5.2.4 Connection States Summary

Table 4-11 defines the mandatory and optional states for each type of port.

Table 4-11 – Mandatory and Optional States

	SOURCE	SINK	DRP	USB PD Communication
Disabled	Optional	Optional	Optional	Not Permitted
ErrorRecovery	Optional	Optional	Optional	Not Permitted
Unattached.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWait.SNK	N/A	Mandatory ¹	Mandatory	Not Permitted
Attached.SNK	N/A	Mandatory	Mandatory	Permitted
Unattached.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWait.SRC	Mandatory	N/A	Mandatory	Not Permitted
Attached.SRC	Mandatory	N/A	Mandatory	Permitted
Try.SRC	N/A	N/A	Optional	Not Permitted
TryWait.SNK ²	N/A	N/A	Optional	Not Permitted
Accessory.Present	N/A	Optional	Optional	Not Permitted
AudioAccessory	Optional	Optional	Optional	Not Permitted
DebugAccessory	Optional	Optional	Optional	Permitted
Unattached.Accessory	N/A	Optional	N/A	Not Permitted
AttachWait.Accessory	N/A	Optional	N/A	Not Permitted
PoweredAccessory	N/A	Optional	N/A	Permitted
Unsupported.Accessory ³	N/A	Optional	N/A	Not Permitted
PowerDefault.SNK	N/A	Mandatory	Mandatory	Permitted
Power1.5.SNK	N/A	Optional	Optional	Permitted
Power3.0.SNK	N/A	Optional	Optional	Permitted

¹ Optional for UFP applications that are USB 2.0-only, consume USB Default Power and do not support **USB PD** or accessories.

² TryWait.SNK is mandatory when Try.SRC is supported.

³ Unsupported.Accessory is mandatory when PoweredAccessory is supported.

4.5.3 USB Port Interoperability Behavior

This section describes interoperability behavior between USB Type-C to USB Type-C ports and between USB Type-C to legacy USB ports.

4.5.3.1 USB Type-C Port to USB Type-C Port Interoperability Behaviors

The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of USB Type-C DFP, UFP and DRPs as presented in Table 4-5. In all of the described behaviors, the impact of **USB PD**-based swaps (PR_Swap, DR_Swap or VCONN_Swap) are not considered.

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete.

4.5.3.1.1 DFP to UFP Behavior

Figure 4-18 illustrates the functional model for a DFP connected to a UFP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

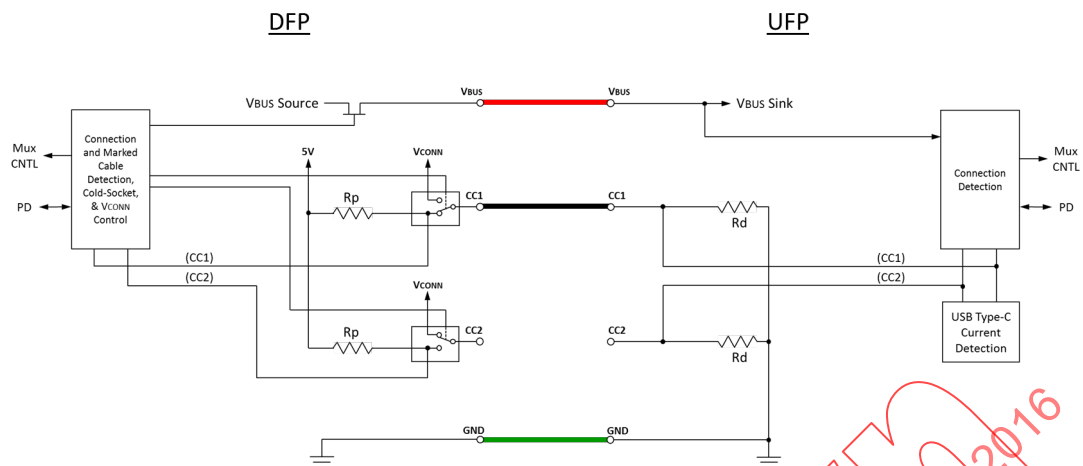


Figure 4-18 – DFP to UFP Functional Model

The following describes the behavior when a DFP is connected to a UFP.

- 1) DFP and UFP in the unattached state
- 2) DFP transitions from **Unattached.SRC** to **Attached.SRC** through **AttachWait.SRC**
 - DFP detects the UFP's pull-down on CC and enters **Attached.SRC** through **AttachWait.SRC**
 - DFP turns on VBUS and VCONN
- 3) UFP transitions from **Unattached.SNK** to **Attached.SNK** through **AttachWait.SNK**. UFP may skip **AttachWait.SNK** if it is USB 2.0 only and does not support accessories.
 - UFP detects VBUS and enters **Attached.SNK** through **AttachWait.SNK**
- 4) While the DFP and UFP are in the attached state:
 - DFP adjusts **Rp** as needed to limit the current the UFP may draw
 - UFP detects and monitors **vRd** for available current on VBUS
 - DFP monitors CC for detach and when detected, enters **Unattached.SRC**
 - UFP monitors VBUS for detach and when detected, enters **Unattached.SNK**

4.5.3.1.2 DFP to DRP Behavior

Figure 4-19 illustrates the functional model for a DFP connected to a DRP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

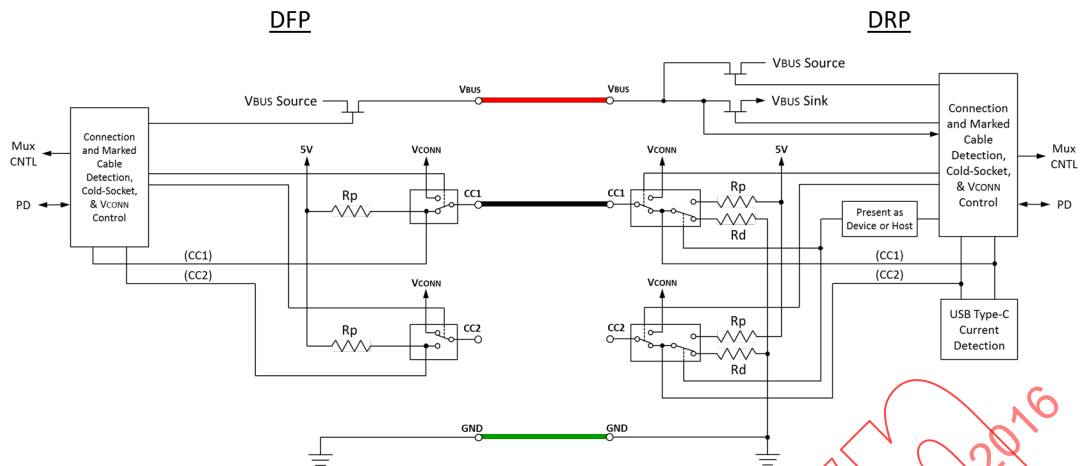


Figure 4-19 – DFP to DRP Functional Model

The following describes the behavior when a DFP is connected to a DRP.

- 1) DFP and DRP in the unattached state
 - DRP alternates between **Unattached.SRC** and **Unattached.SNK**
- 2) DFP transitions from **Unattached.SRC** to **Attached.SRC** through **AttachWait.SRC**
 - DFP detects the DRP's pull-down on CC and enters **AttachWait.SRC**. After **tCCDebounce** it then enters **Attached.SRC**.
 - DFP turns on VBUS and VCONN
- 3) DRP transitions from **Unattached.SNK** to **Attached.SNK** through **AttachWait.SNK**
 - DRP in **Unattached.SNK** detects pull up on CC and enters **AttachWait.SNK**. After that state persists for **tCCDebounce** and it detects VBUS, it enters **Attached.SNK**.
- 4) While the DFP and DRP are in their respective attached states:
 - DFP adjusts **Rp** as needed to limit the current the UFP may draw
 - DRP detects and monitors **vRd** for available current on VBUS
 - DFP monitors CC for detach and when detected, enters **Unattached.SRC**
 - DRP monitors VBUS for detach and when detected, enters **Unattached.SNK** (and resumes toggling between **Unattached.SNK** and **Unattached.SRC**)

4.5.3.1.3 DRP to UFP Behavior

Figure 4-20 illustrates the functional model for a DRP connected to a UFP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

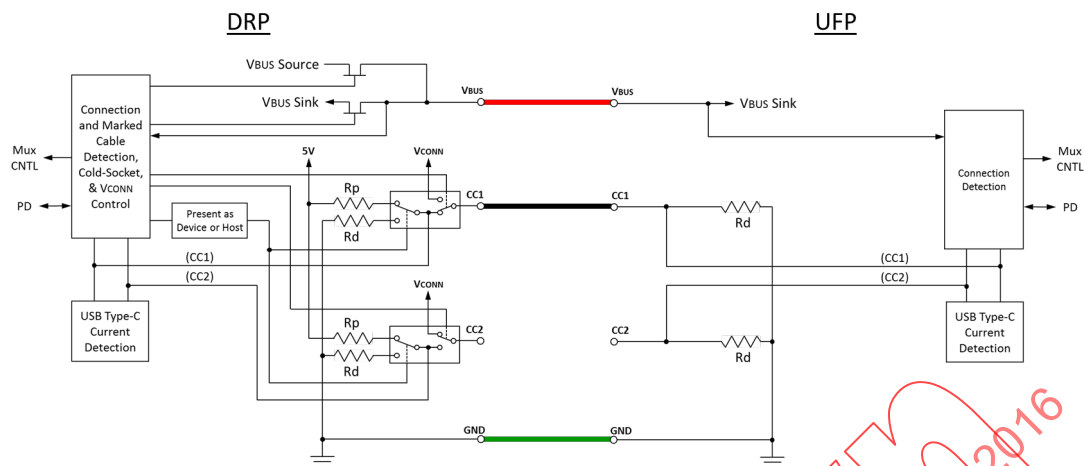


Figure 4-20 – DRP to UFP Functional Model

The following describes the behavior when a DRP is connected to a UFP.

- 1) DRP and UFP in the unattached state
 - DRP alternates between **Unattached.SRC** and **Unattached.SNK**
- 2) DRP transitions from **Unattached.SRC** to **AttachWait.SRC**
 - DRP in **Unattached.SRC** detects one of the CC pull-downs of UFP which is in **Unattached.SNK** and DRP enters **AttachWait.SRC**
 - DRP in **AttachWait.SRC** detects that pull down on CC persists for **tCCDebounce**. It then enters **Attached.SRC** and turns on VBUS and VCONN
- 3) UFP transitions from **Unattached.SNK** to **Attached.SNK** through **AttachWait.SNK** if required.
 - UFP detects VBUS and enters **Attached.SNK**
- 4) DRP transitions from **AttachWait.SRC** to **Attached.SRC**
 - DRP in **AttachWait.SRC** times out (**tDRPHold**) and transitions to **Attached.SRC**
- 5) While the DRP and UFP are in their respective attached states:
 - DRP adjusts **Rp** as needed to limit the current the UFP may draw
 - UFP detects and monitors **vRd** for available current on VBUS
 - DRP monitors CC for detach and when detected, enters **Unattached.SNK** (and resumes toggling between **Unattached.SNK** and **Unattached.SRC**)
 - UFP monitors VBUS for detach and when detected, enters **Unattached.SNK**

4.5.3.1.4 DRP to DRP Behavior

Two behavior descriptions based on the connection state diagrams are provided below. In the first case, the two DRPs accept the resulting DFP-to-UFP relationship achieved randomly whereas in the second case the DRP #2 chooses to drive the random result to the opposite result using the **Try.SRC** mechanism.

Figure 4-21 illustrates the functional model for a DRP connected to a DRP in the first case described. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

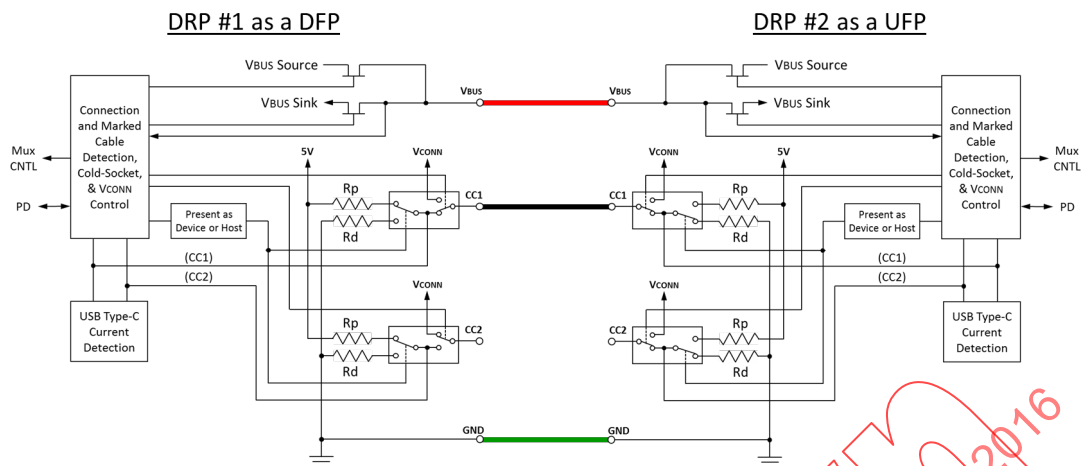


Figure 4-21 – DRP to DRP Functional Model – CASE 1

CASE 1: The following describes the behavior when a DRP is connected to another DRP. In this flow, the two DRPs accept the resulting DFP-to-UFP relationship achieved randomly.

- 1) Both DRPs in the unattached state
 - DRP #1 and DRP #2 alternate between **Unattached.SRC** and **Unattached.SNK**
- 2) DRP #1 transitions from **Unattached.SRC** to **AttachWait.SRC**
 - DRP #1 in **Unattached.SRC** detects a CC pull down of DRP #2 in **Unattached.SNK** and enters **AttachWait.SRC**
- 3) DRP #2 transitions from **Unattached.SNK** to **AttachWait.SNK**
 - DRP #2 in **Unattached.SNK** detects pull up on a CC and enters **AttachWait.SNK**
- 4) DRP #1 transitions from **AttachWait.SRC** to **Attached.SRC**
 - DRP #1 in **AttachWait.SRC** continues to see CC pull down of DRP #2 for **tCCDebounce**, enters **Attached.SRC** and turns on VBUS and VCONN
- 5) DRP #2 transitions from **AttachWait.SNK** to **Attached.SNK**.
 - DRP #2 after having been in **AttachWait.SNK** for **tCCDebounce** and having detected VBUS, enters **Attached.SNK**
- 6) While the DRPs are in their respective attached states:
 - DRP #1 adjusts **Rp** as needed to limit the current DRP #2 may draw
 - DRP #2 detects and monitors **vRd** for available current on VBUS
 - DRP #1 monitors CC for detach and when detected, enters **Unattached.SNK** (and resumes toggling between **Unattached.SNK** and **Unattached.SRC**)
 - DRP #2 monitors VBUS for detach and when detected, enters **Unattached.SNK** (and resumes toggling between **Unattached.SNK** and **Unattached.SRC**)

Figure 4-22 illustrates the functional model for a DRP connected to a DRP in the second case described.

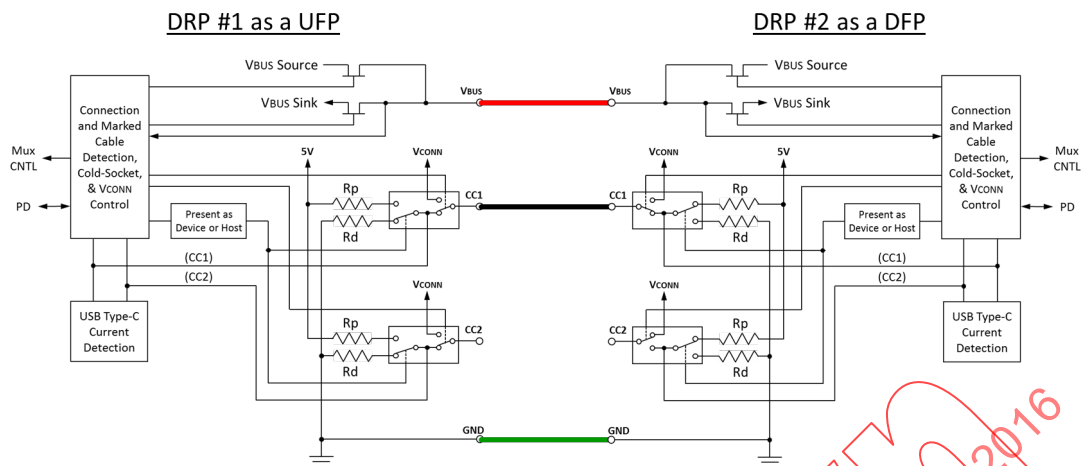


Figure 4-22 – DRP to DRP Functional Model – CASE 2

CASE 2: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #2 chooses to drive the random result to the opposite result using the [Try.SRC](#) mechanism.

- 1) Both DRPs in the unattached state
 - DRP #1 and DRP #2 alternate between [Unattached.SRC](#) and [Unattached.SNK](#)
- 2) DRP #1 transitions from [Unattached.SRC](#) to [AttachWait.SRC](#)
 - DRP #1 in [Unattached.SRC](#) detects a CC pull down of DRP #2 in [Unattached.SNK](#) and enters [AttachWait.SRC](#)
- 3) DRP #2 transitions from [Unattached.SNK](#) to [AttachWait.SNK](#)
 - DRP #2 in [Unattached.SNK](#) detects pull up on a CC and enters [AttachWait.SNK](#)
- 4) DRP #1 transitions from [AttachWait.SRC](#) to [Attached.SRC](#)
 - DRP #1 in [AttachWait.SRC](#) continues to see CC pull down of DRP #2 for [tCCDebounce](#), enters [Attached.SRC](#) and turns on VBUS and VCONN
- 5) DRP #2 transitions from [AttachWait.SNK](#) to [Try.SRC](#).
 - DRP #2 in [AttachWait.SNK](#) has been in this state for [tCCDebounce](#) and detects VBUS but strongly prefers the Source role, so transitions to [Try.SRC](#)
 - DRP #2 in [Try.SRC](#) asserts a pull-up on CC and waits
- 6) DRP #1 transitions from [Attached.SRC](#) to [Unattached.SNK](#) to [AttachWait.SNK](#)
 - DRP #1 in [Attached.SRC](#) no longer detects DRP #2's pull-down on CC and transitions to [Unattached.SNK](#).
 - DRP #1 in [Unattached.SNK](#) turns off VBUS and VCONN and applies a pull-down on CC
 - DRP #2 in [Unattached.SNK](#) detects pull up on a CC and enters [AttachWait.SNK](#)
- 7) DRP #2 transitions from [Try.SRC](#) to [Attached.SRC](#) via [AttachWait.SRC](#)
 - DRP #2 in [Try.SRC](#) detects the DRP #1 in [Unattached.SNK](#)'s pull-down on CC and enters [AttachWait.SRC](#)
 - DRP #2 in [AttachWait.SRC](#) times out ([tCCDebounce](#)) and transitions to [Attached.SRC](#)
 - DRP #2 in [Attached.SRC](#) turns on VBUS and VCONN
- 8) DRP #1 transitions from [AttachWait.SNK](#) to [Attached.SNK](#)
 - DRP #1 in [AttachWait.SNK](#) after [tCCDebounce](#) and detecting VBUS, enters [Attached.SNK](#)

9) While the DRPs are in their respective attached states:

- DRP #2 adjusts R_p as needed to limit the current DRP #1 may draw
- DRP #1 detects and monitors vR_d for available current on VBUS
- DRP #2 monitors CC for detach and when detected, enters **Unattached.SRC** (and resumes toggling between **Unattached.SNK** and **Unattached.SRC**)
- DRP #1 monitors VBUS for detach and when detected, enters **Unattached.SNK** (and resumes toggling between **Unattached.SNK** and **Unattached.SRC**)

4.5.3.1.5 DFP to DFP Behavior

Figure 4-23 illustrates the functional model for a DFP connected to a DFP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

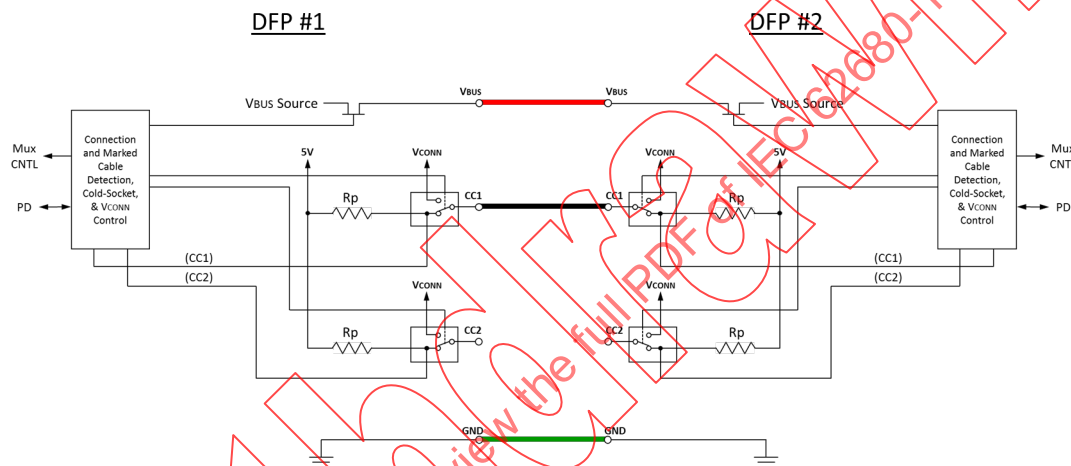


Figure 4-23 – DFP to DFP Functional Model

The following describes the behavior when a DFP is connected to another DFP.

1) Both DFPs in the unattached state

- DFP #1 fails to detect a UFP's pull-down on CC and remains in **Unattached.SRC**
- DFP #2 fails to detect a UFP's pull-down on CC and remains in **Unattached.SRC**

4.5.3.1.6 UFP to UFP Behavior

Figure 4-24 illustrates the functional model for a UFP connected to a UFP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.