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Thermal standardization on semiconductor packages – Part 2-1: 3D thermal simulation models of semiconductor packages for steady-state analysis – Discrete packages

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THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES –

Part 2-1: 3D thermal simulation models of semiconductor packages for steady-state analysis – Discrete packages

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IEC 63378-2-1 has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47D/976/FDIS	47D/982/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 63378 series, published under the general title *Thermal standardization on semiconductor packages*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES –

Part 2-1: 3D thermal simulation models of semiconductor packages for steady-state analysis – Discrete packages

1 Scope

This part of IEC 63378 specifies three-dimensional (3D) thermal models of discrete semiconductor packages (TO-243, TO-252 and TO-263), utilized in the steady-state thermal analysis of electronic devices to estimate junction temperatures accurately.

This model is assumed to be made by semiconductor suppliers and to be used by assembly makers of electronic devices.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1
detailed model
semiconductor package model which has both the structures of each portion, such as die or moulding or terminal, and the material properties for thermal analysis

Note 1 to entry: This model is often simplified to some extent.

4 Attributes of 3D thermal models

4.1 General

Clause 4 shows the attributes such as dimensions and thermal properties of three different type of TO-packages. These attributes are used to estimate junction temperatures.

4.2 TO-243

Figure 1 and Table 1 show the attributes which TO-243 thermal simulation models shall have.

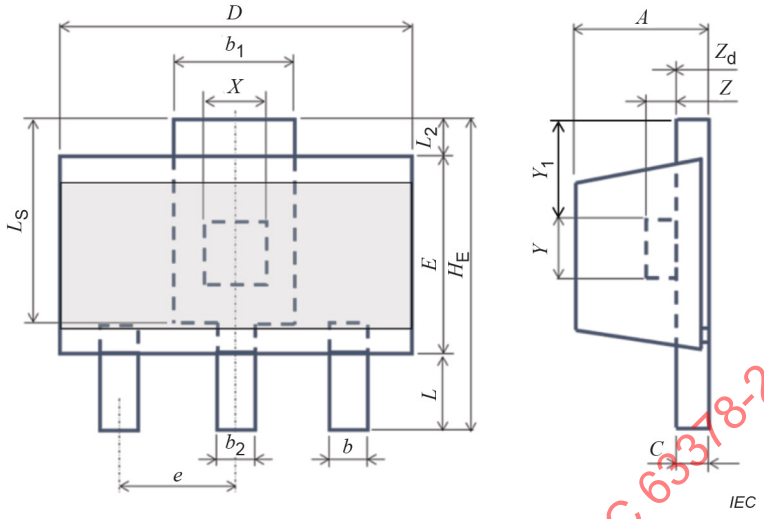

Figure 1 – Dimensions of TO-243

Table 1 – Attributes for TO-243

	Attribute	Symbol	Value	Unit
Dimension	Package thickness	A		m
	Terminal width	b		m
	Heat spreader width	b_1		m
	Centre terminal width	b_2		m
	Terminal thickness	C		m
	Package width	D		m
	Package body length	E		m
	Terminal pitch	e		m
	Span	H_E		m
	Terminal length	L		m
	Exposed terminal length	L_2		m
	Heat spreader length	L_S		m
	Die width	X		m
	Die length	Y		m
	Die length offset	Y_1		m
	Die thickness	Z		m
	Die attach thickness	Z_d		m
Thermal conductivity	Thermal conductivity of die	k_d		W/(m × K)
	Thermal conductivity of die attach	k_{da}		W/(m × K)
	Thermal conductivity of molding	k_m		W/(m × K)
	Thermal conductivity of heat spreader	k_s		W/(m × K)

NOTE 1 The default thermal conductivity of molding is 0,6 W/(m·K) and that of heat spreader is 300 W/(m × K). The thermal conductivity of die and die attach varies a lot according to the material adopted.

NOTE 2 The thickness of molding is the same as package thickness "A".

NOTE 3 The length and width of the die attach are the same as those of die X and Y.

NOTE 4 The columns for "Value" shall be filled in.

4.3 TO-252

Figure 2 and Table 2 show the attributes which TO-252 thermal simulation models shall have. (A contribution analysis in the case of TO-252 is given in Annex A.)

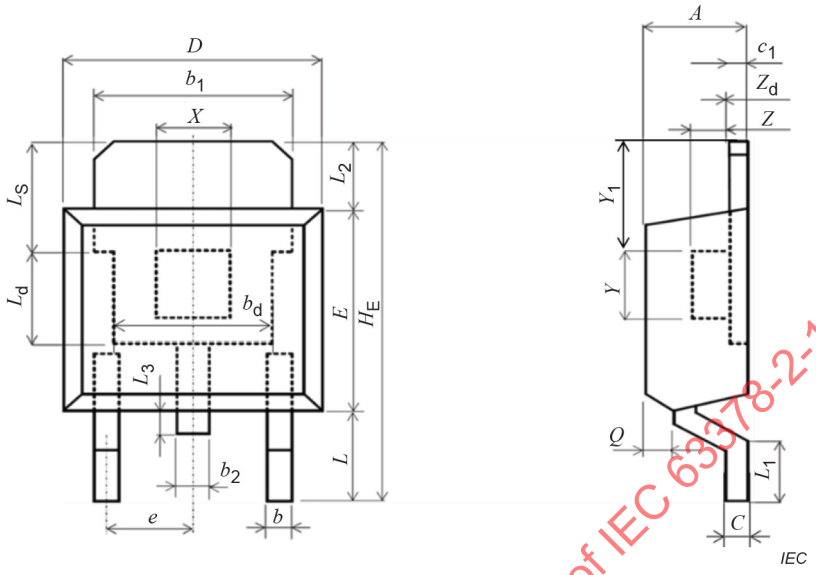

Figure 2 – Dimensions of TO-252

Table 2 – Attributes for TO-252

	Attribute	Symbol	Value	Unit
Dimension	Package thickness	A		m
	Terminal width	b		m
	Heat spreader width	b_1		m
	Centre terminal width	b_2		m
	Terminal thickness	C		m
	Heat spreader thickness	c_1		m
	Package width	D		m
	Package body length	E		m
	Terminal pitch	e		m
	Span	H_E		m
	Terminal length	L		m
	Terminal contact area	L_1		m
	Exposed terminal length	L_2		m
	Convex region length of centre terminal	L_3		m
	Top side of terminal	Q		m
	Die pad width	b_d		m
	Die pad length	L_d		m
	Heat spreader length	L_S		m
	Die width	X		m
	Die length	Y		m
	Die length offset	Y_1		m
	Die thickness	Z		m
	Die attach thickness	Z_d		m
Thermal conductivity	Thermal conductivity of die	k_d		W/(m × K)
	Thermal conductivity of die attach	k_{da}		W/(m × K)
	Thermal conductivity of molding	k_m		W/(m × K)
	Thermal conductivity of heat spreader	k_s		W/(m × K)

NOTE 1 The default thermal conductivity of molding is 0,6 W/(m·K) and that of heat spreader is 300 W/(m × K). The thermal conductivity of die and die attach varies a lot according to the material adopted.

NOTE 2 The length and width of die attach are the same as those of die X and Y.

NOTE 3 The columns for "Value" shall be filled in.

4.4 TO-263

Figure 3 and Table 3 show the attributes which TO-263 thermal simulation models shall have.

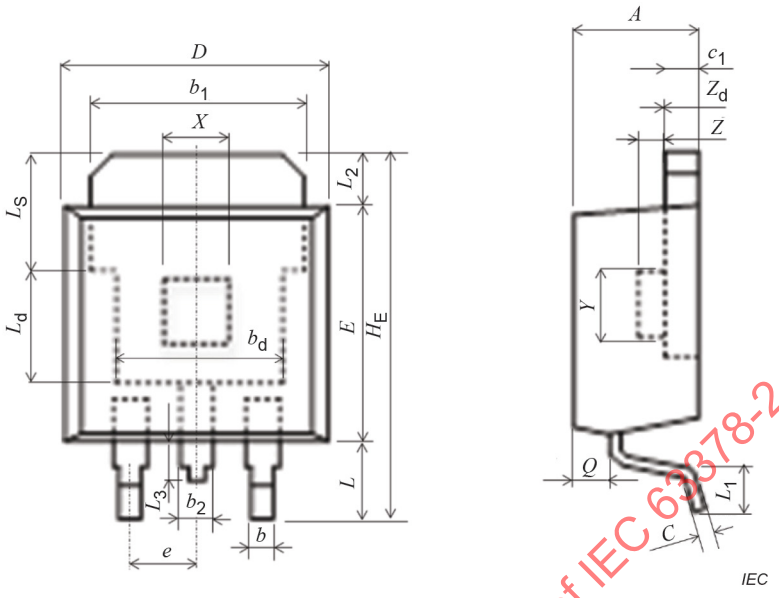

Figure 3 – Dimensions of TO-263

Table 3 – Attributes for TO-263

	List	Symbol	Value	Unit
Dimension	Package thickness	A		m
	Terminal width	b		m
	Heat spreader width	b_1		m
	Centre terminal width	b_2		m
	Terminal thickness	C		m
	Heat spreader thickness	c_1		m
	Package width	D		m
	Package body length	E		m
	Terminal pitch	e		m
	Span	H_E		m
	Terminal length	L		m
	Terminal contact area	L_1		m
	Exposed terminal length	L_2		m
	Convex region length of centre terminal	L_3		m
	Top side of terminal	Q		m
	Die pad width	b_d		m
	Die pad length	L_d		m
	Heat spreader length	L_S		m
	Die width	X		m
	Die length	Y		m
	Die length offset	Y_1		m
	Die thickness	Z		m
	Die attach thickness	Z_d		m
Thermal conductivity	Thermal conductivity of die	k_d		W/(m × K)
	Thermal conductivity of die attach	k_{da}		W/(m × K)
	Thermal conductivity of molding	k_m		W/(m × K)
	Thermal conductivity of heat spreader	k_s		W/(m × K)

NOTE 1 The default thermal conductivity of molding is 0,6 W/(m × K) and that of heat spreader is 300 W/(m × K). The thermal conductivity of die and die attach varies a lot according to the material adopted.

NOTE 2 The length and width of die attach are the same as those of die "X and Y".

NOTE 3 The columns for "Value" shall be filled in.

Annex A
(normative)

Contribution analysis in the case of TO-252

A.1 Attributes of a sample package

A sample package's attributes were determined by contribution analysis. In Annex A, an example of contribution analysis is introduced.

Table A.1 lists a typical range of thermal properties and dimensions regarding the example of a TO-252 package.

Table A.1 – Attributes and their range of a sample package

Item	Attribute	Range
1	Thermal conductivity of molding (k_m)	0,6 W/m × K to 1,0 W/m × K
2	Die width and length (X and Y)	1,296 mm to 3,024 mm
3	Die thickness (Z)	50 ∝m to 500 ∝m
4	Thermal conductivity of die attach (k_d)	5 W/m × K to 50 W/m × K
5	Die attach thickness (Z_d)	5 ∝m to 30 ∝m
6	Thermal conductivity of heat spreader (k_s)	300 W/m × K to 398 W/m × K

A TO-252 indicated in Figure A.1 was prepared. The attributes of this package are within the range of Table A.1.

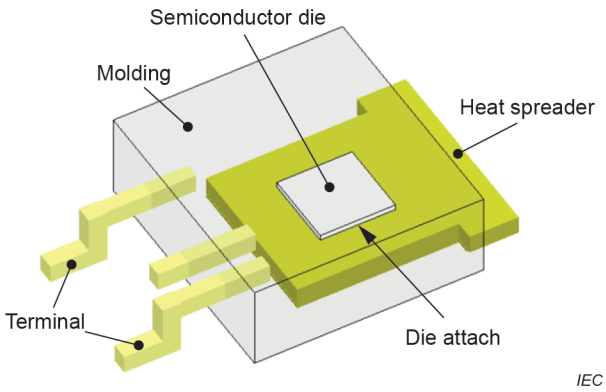

Figure A.1 – Sample package of TO-252

JEDEC 2s2p, where this package was mounted, was selected as a motherboard and the test environment of JEDEC was adopted. These detailed conditions are shown in [1] to [3][1].

Plural simulations were then done, and the result of the contribution analysis is shown in Figure A.2. Here the thermal resistance of the die attach (R_{th_da}) was calculated using both the thermal conductivity of the die attach and the die attach thickness as indicated in Formula (A.1).

$$R_{th\_da} = \frac{Z_d}{k_d \times X \times Y} \tag{A.1}$$

where

Z_d is the die attach thickness;

k_d is the thermal conductivity of the die attach;

X is the die width;

Y is the die length.

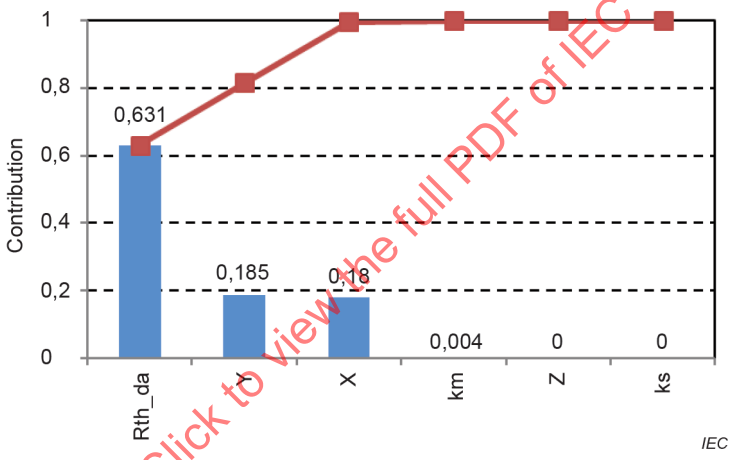

Figure A.2 – Results of contribution analysis

In Figure A.2, the vertical axis shows the contribution which is defined as Formula (A.2).

$$Contribution = \frac{V_{item,n}}{V_{total}} \tag{A.2}$$

where

$V_{item,n}$ is the variance when only the item n varies;

V_{total} is the variance when all the items vary.

[1] Numbers in square brackets refer to the Bibliography.

Variance V is defined as in Formula (A.3).

$$V = \frac{1}{n}\sum_{i=1}^{n}(X_i - X_{ave})^2 \quad \text{(A.3)}$$

where

X_i is the value when the combination i was selected;

X_{ave} is the average value of all combinations.

The thermal resistance of the die attach has the highest influence on the temperature of the semiconductor die. In addition, the die sizes are an important factor to estimate the temperature.

Using this contribution analysis, the attributes of this standardized model are defined.

A.2 Simulation validation

The accuracy of this new thermal model was validated by comparing to the detailed model. The attributes of the new model were collected in accordance with 4.3. On the other hand, the detailed model includes some of the undisclosed attributes such as bonding wire information which semiconductor suppliers have as confidential data.

The temperature of both thermal models were calculated by thermal analysis.

As a motherboard, JEDEC 1s and 2s2p were selected and test environment of JEDEC was adopted in this thermal simulation. Figure A.3 shows the accuracy comparison between the models. It is confirmed that this newly standardized model can predict the temperature of semiconductor die precisely.

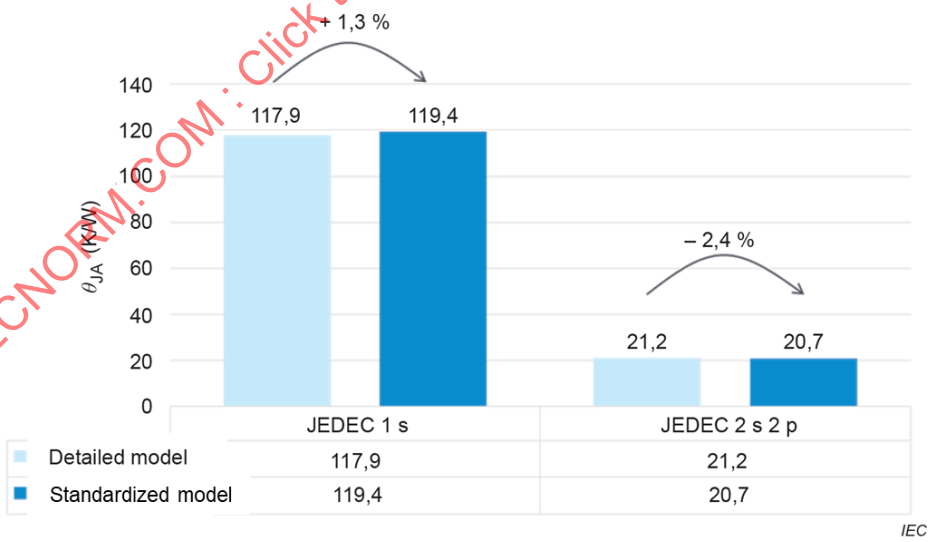

Figure A.3 – Accuracy comparison