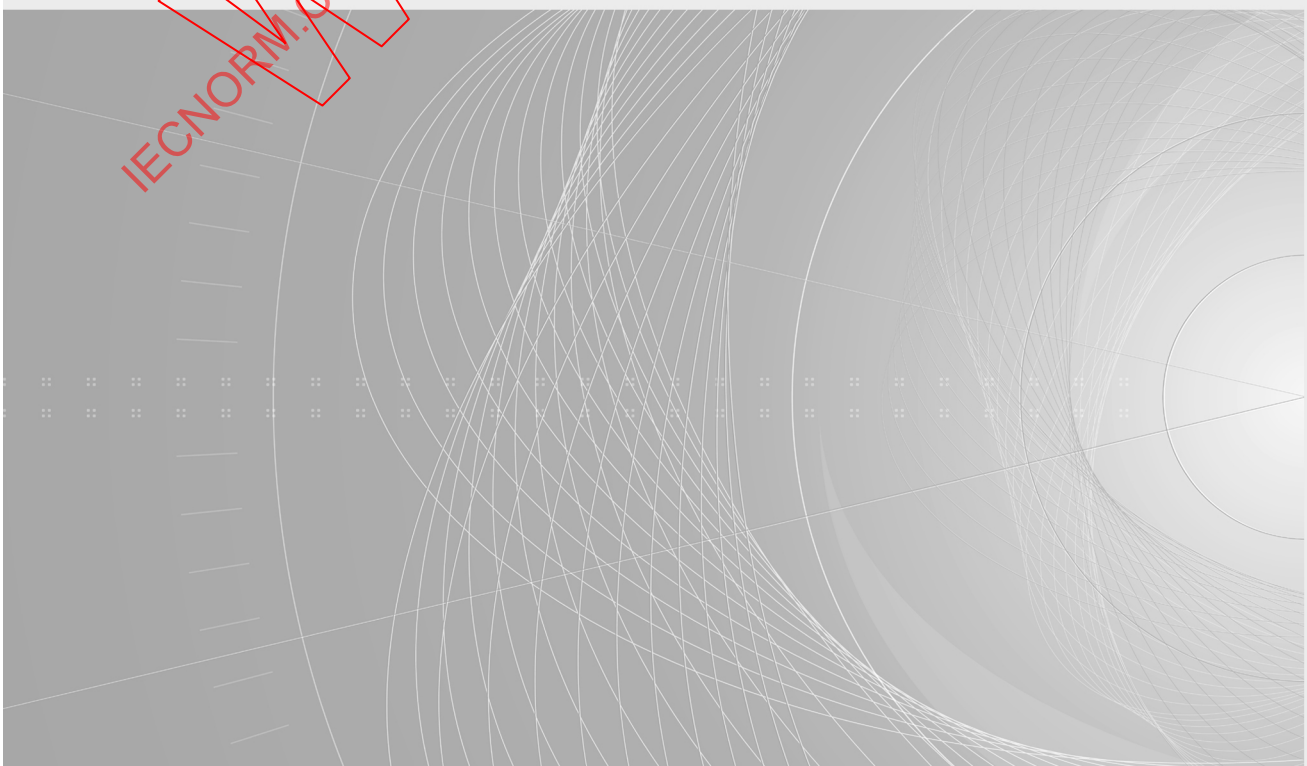
IEC/PAS 62326-20

Edition 1.0 2011-01

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD

Printed boards –
Part 20: Electronic circuit board for high-brightness LEDs



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CONTENTS

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PRINTED BOARDS –

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FOREWORD

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It is based on JPCA-TMC-LED01S-2010. It is published as a double-logo PAS and JPCA.

The text of this PAS is based on the following document:	This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document
Draft PAS	**Report on voting**
91/926/PAS	91/942A/RVD

Following publication of this PAS, which is a pre-standard publication, the technical committee or subcommittee concerned may transform it into an International Standard.

This PAS shall remain valid for an initial maximum period of 3 years starting from the publication date. The validity may be extended for a single period up to a maximum of 3 years, at the end of which it shall be published as another type of normative document, or shall be withdrawn.

A list of all the parts in the IEC 62326 series, under the general title *Printed boards*, can be found on the IEC website.

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PRINTED BOARDS –

Part 20: Electronic circuit board for high-brightness LEDs

1 Scope

This PAS specifies the properties of the electronic circuit board for high-brightness LEDs (hereafter described as “ECB”).

NOTE Standards relevant to the present standards are given below.

JPCA-TD01 Terms and definitions for printed circuits

JIS C 5603 Terms and definitions for printed circuits

2 Terms and definitions

For the purpose of this document, the terms used in this PAS shall be in accordance with JPCA-TD01 and JIS C 5603, unless otherwise specified.

3 Classification and class of the ECB

The ECB specified in this PAS shall satisfy the specification of (A) to (C) in Table 1 in the following way. The materials used in the materials of PWB are not specified; however, they shall be agreed upon between user and supplier depending on the application area of the boards in question.

Table 1 – Application and classification

Classification (thermal conductivity)	Definition	Small classification (insulation property)	Definition	Thermal conductivity parameter W/(mK)	Heat transfer parameter W/(m^{2}K)
A	Standard boards	Ⅰ	No specification	<1	<10
		Ⅱ	Electric strength <1,000 V		
		Ⅲ	Electric strength 1,000 V≤		
B	Thermal conductive boards	Ⅰ	No specification	1≤	<10
		Ⅱ	Electric strength <1,000 V		
		Ⅲ	Electric strength 1,000 V≤		
C	High thermal conductive boards	Ⅰ	No specification	1≤	10≤
		Ⅱ	Electric strength <1,000 V		
		Ⅲ	Electric strength 1,000 V≤		

Heat Radiation	A	B	C
Classsification by base materials	Resin type substrate (CEM-3, FR-4, FR-5) Flexible type substrate	Resin type substrate (with thermal via) High thermal conductive resin substrate	Metal core substrate Metal base substrate Ceramic type substrate
Classification by electronic circuit boards	Conventional substrate for discreat type electronic parts mounted boards	Substrate for semiconductor package Substrate for Chip on Board	
Classification by final products	Assistant lighting lamp	Lamp substitute for halogen lamp amp substitute for fluorescent lamp substitutio Lamp substitute for filament lamp Street lamp	Lamp substitute for HID
Insulation class	I II III	I II III	I II III

Figure 1 – Example of classification and their application by base materials, electronic circuit boards and final products

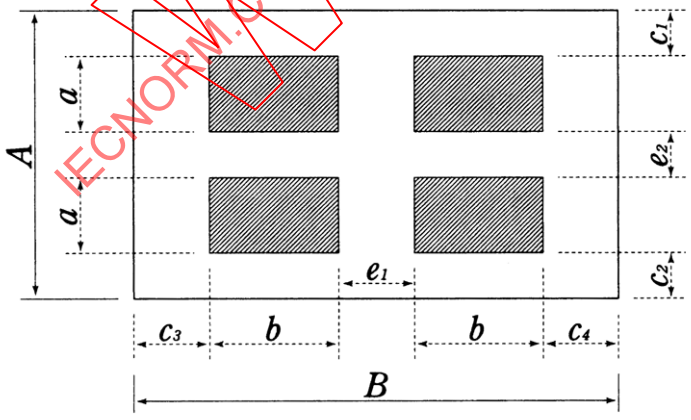
4 Design rules and allowance

4.1 Panel and board sizes

4.1.1 Board size (for reference only)

The size of the board of the product (axb) illustrated in Figure 2 shall be selected so that the boards can be arranged efficiently within a panel with a size specified in Table 2. Or, a proper panel with a size given in the table shall be selected so as to satisfy the required efficient arrangement of the boards.

Table 1. PWB



Board size of the product: a x b
Space between board and panel edges: c_1, c_2, c_3, c_4
Space between boards: e_1, e_2

Figure 2 – Board arrangement in a panel

Table 2 – Panel dimensions (informative purpose)

mm

Size of CCL (copper clad laminate) panel	Division			
	4	6	8	9
1 000 × 1 000	500 × 500	333 × 500	250 × 500	333 × 333
1 000 × 1 200	500 × 600	333 × 600 400 × 500	300 × 500	333 × 400

4.1.2 Allowance of dimensions

The allowance of dimensions of a board or a panel is given in Table 3.

Table 3– Allowance of dimensions

mm

Longitudinal size	Allowance
≤ 100	±0,2
100<	Add 0,1 for each 50 exceeding a length of 100.

4.1.3 Perforation and slit

The perforation and slit are shown in Figure 3. The allowance of the distances from the datum point to the center of the cut of the perforation and slit is given in Table 4.

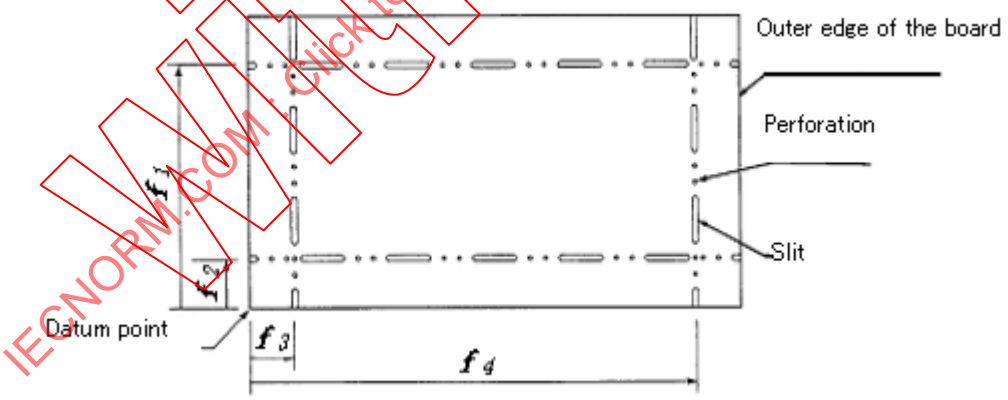


Figure 3 – Distances from the datum point to perforation and slit

Table 4 – Allowance of the distances from the datum point to perforation and slit

mm

Distances from the datum point to perforation and slit	Allowance
≤ 100	±0,2
100 <	Add 0,1 for each 50 beyond a length of 100.

4.1.4 V-cut

The V-cut is shown in Figure 4. The allowance of the distance from the reference datum to the center of cut of the V (g_1 to g_4) is given in Table 5. The allowance of the deviation of the position of the V-cut on the front and back planes is 0,2 mm, and the allowance of the uncut thickness of the board is the sum of the allowance of the board thickness ±0,1 mm.

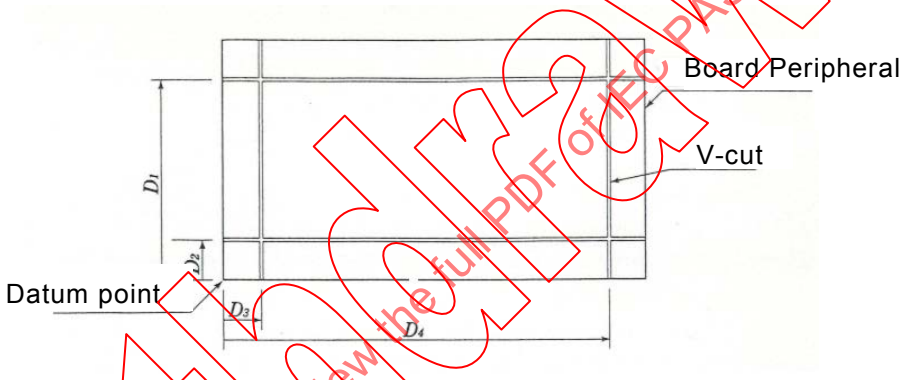


Figure 4 – Distance from the datum point to V-cut

mm

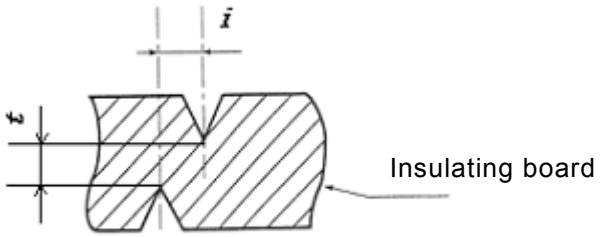


Figure 5 – Allowance of position off-set of V-cuts on front and back surfaces

Table 5 – Allowance for the distance from the datum point to the center of the V-cut

Distance from the datum point to the center of the V-cut	Allowance
≤100	±0,2
>100	Add 0,1 for each 50 mm exceeding a length over 100 mm

4.2 Total board thickness

4.2.1 Total board thickness and its allowance

The allowance of the total board thickness (*t*) of a board with solder resist and symbol marks as shown in Figure 6 is given in Table 6.

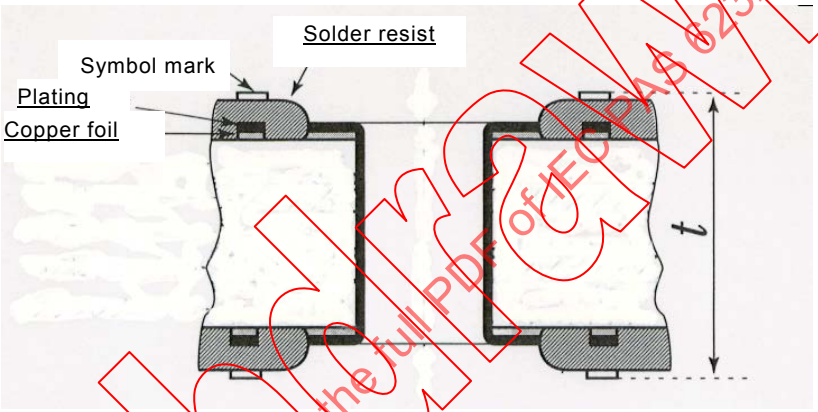


Figure 6 – PWB board with symbol mark, solder resist, copper foil and plating

Table 6 – Total thickness and its allowance

mm

Total thickness (center value of the final board) mm	**Allowance**
≤ 0,3 to < 0,5	+ 0,10 - 0,05
≤ 0,5 to < 0,8	±0,10
≤ 0,8 to < 1,10	±0,15
≤ 1,10 to < 1,40	±0,17
≤ 1,40 to < 2,00	±0,19
≤ 2,00	±10 %

4.3 Holes

4.3.1 Insertion holes and vias

(1) Allowance of component insertion holes

Allowance of component insertion holes is given in Table 7. The allowance given in this table is not applicable to vias (through-hole vias, buried vias and blind vias). The allowance of through-holes with a diameter less than 0,6 mm for insertion of a component and holes for press-fit of a component is to be agreed between user and supplier.

Table 7 – Allowance of holes for component insertion

mm

Item		Allowance
Plated through-hole	0,6 ≤ <2,0	±0,10
	2,0 ≤	±0,15
Non-plated through-hole		±0,10

(2) Position of a hole for component insertion

The center of a hole for component insertion should be at the cross point of the grid for pattern design including the complementary grid lines used. The allowance of a component insertion hole position, ($|\vec{\ }, j|$), the deviation from the designed position in respect to the datum point as shown in Figure 7 is given in Table 8.

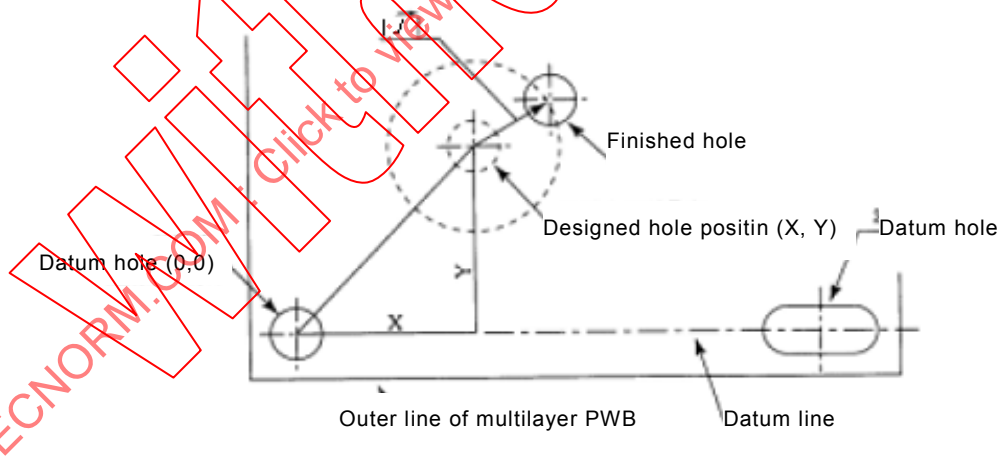


Figure 7 – Positions of component insertion holes

Table 8 – Position allowance of component insertion holes

mm

Longer dimension of rectangular board	Allowance
≤ 400	0,10
400<	For board exceeding 400, add 0,05 for each additional 100

(3) Distance from the board edge to the wall of a hole

Distance from the board edge to the wall of a hole (*d*) is shown in Figure 8. The distance (*d*) between the walls of a through-hole before plating and of a hole for component insertion shall be larger than either 1,0 mm. The distance in the case of press hole formation shall be in accordance with Table 9.

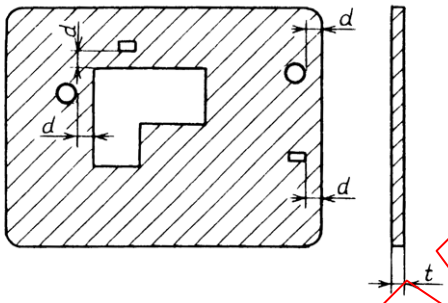


Figure 8 – Distance between the wall of a hole to the board edge

Table 9 – Distance between a hole wall and board edge

mm

Item	Distance (*j*) between a component hole before plating and the via wall
HDI PWB	≤ 1,0 mm and also longer than the board thickness (*t*)
Standard PWB	≤ 1,5 mm and also longer than the board thickness (*t*)

(4) Minimum clearance between hole wall and the inner conductor

The minimum clearance between the hole wall and the inner conductor (*k*) as illustrated in Figure 9 shall be 0,325 mm. If the distance 0,325 mm is guaranteed in the design of the pattern, the minimum separation is guaranteed.

Table 10 – Minimum clearance between the hole wall and the inner layer conductor

Item		Minimum clearance between hole wall and the inner layer conductor	
		Standard value	Minimum value
HDI PWB	Component hole	0,5	0,25
	Via	0,30	
Standard PWB	Component hole	0,5	0,30
	Via	0,35	

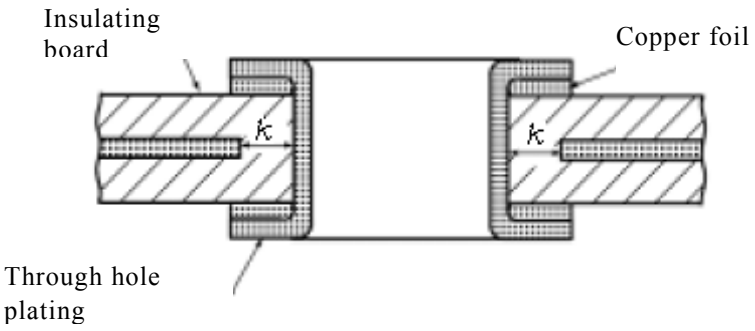


Figure 9 – Hole wall and the minimum designed spacing to the inner conductor

4.3.2 Datum hole

(1) Allowance of a datum hole

The allowance of a datum hole shall be ±0,05 mm, or $^{+0,10}_{-0,00}$ mm. A through hole without wall plating shall be used as a datum hole.

4.3.3 Assembly hole (a through-hole without wall plating)

(1) Allowance of an assembly hole

The allowance of an assembly hole shall be ±0,10 mm.

(2) Allowance of the position of an assembly hole

The allowance of the position of an assembly hole shall be in accordance with the Table 8 of 4.3.1 (2).

(3) Distance between an assembly hole and the board edge

The distance between an assembly hole and the board edge shall be larger than 2,0 mm. In case the distance is less than 2,0 mm, the distance shall be agreed between user and supplier.

(4) The distance between an assembly hole and the inner conductor

The distance between the wall of an assembly hole and the inner conductor shall be larger than 1,0 mm.

4.4 Conductor

4.4.1 Width of conductor pattern and its allowance

The allowance of the formed conductor width as illustrated in Figure 10 shall be in accordance with Table 11. The allowance of the finishied conductor pattern specifically designed for impedance control shall be agreed between the user and supplier.

Table 11 – Allowance of conductor width

Conductor thickness [a]	Allowance (mm)	Conductor with for reference
50 <75	± 25	15 to 20
7500 <100	± 30	20 to 40
100 <300	± 50	30 to 50
300	± 100	40 to 70
Thick copper foil circuits	± 150	70
	± 200	105
	± 300	140

[a] The conductor thickness is the copper foil thickness plus the thickness of plated copper.

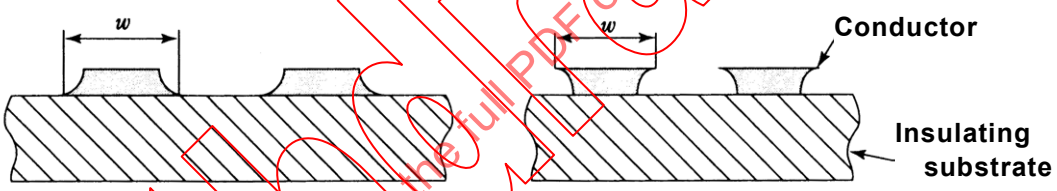


Figure 10 – Width of finished conductor

4.4.2 Distance between conductors and its allowance

The allowance of the distance between conductors (*m*) shall be as given in Table 12. The allowance of the finished conductor pattern specifically designed for impedance control shall be agreed between the user and supplier.

Table 12 – Allowance of the distance between conductors

Conductor thickness [a]	Allowance (mm)	Conductor with for reference
50 <75	± 25	15 to 20
7500 <100	± 30	20 to 40
100 <300	± 50	30 to 50
300	± 100	40 to 70

[a] The conductor thickness is the copper foil thickness plus the thickness of plated copper.

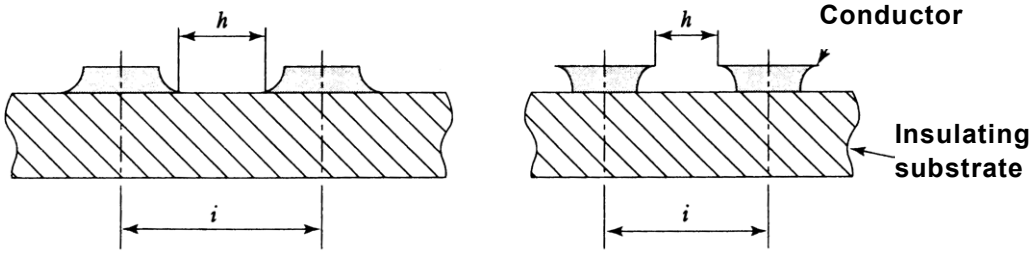


Figure 11 – Distance between finished conductors

4.4.3 Distance between conductor and board edge

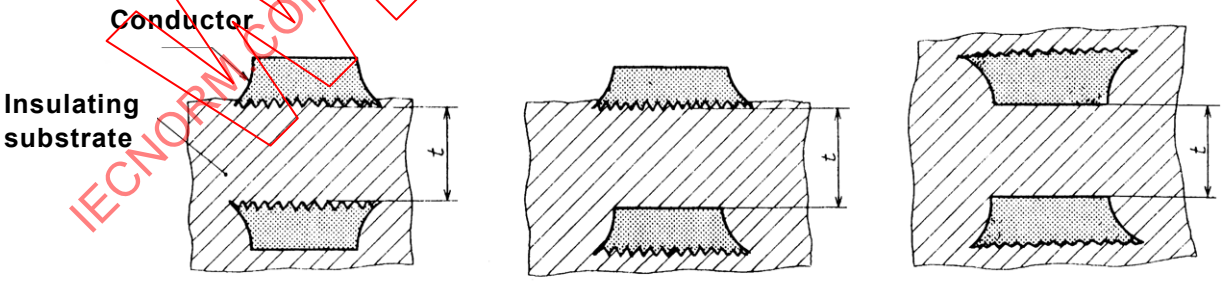
The distance between conductor and board edge shall be larger than 0,5 mm. The distance for the case of pressing shall be as given in Table 13 excluding the board printed contact portions.

Table 13 – Distance between conductor and board edge

Board thickness	Distance between conductor and board edge
< 0,8	0,5≤
0,8≤ ≤2,0	More than the board thickness

4.4.4 Thickness of the insulating layer

The thickness of an insulating layer is illustrated in Figure 12.



NOTE In case the surface of copper foil is roughened, the thickness of t he insulating substrate is the minimum distance applicable to the substrate.

Figure 12 – Thickness of the insulating layer

4.5 Printed contact

4.5.1 Allowance of the distance between the centres of two adjacent printed contacts

The allowance of the distance between the centres of two adjacent printed contacts (p, p_n) as illustrated in Figure 13 shall be ±0,10 mm. Add 0,01 mm for each additional 20 mm in case the distance between the centres of terminals exceeds 100 mm.

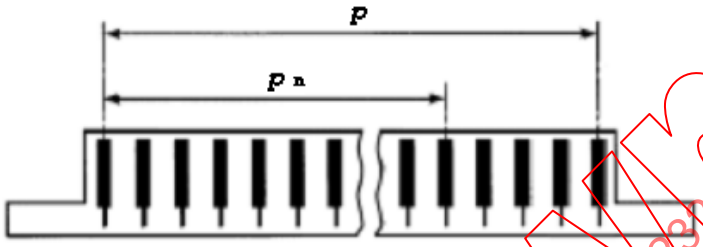


Figure 13 – Distance between centres of terminals of printed contacts

4.5.2 Allowance of the terminal width of printed contacts

The allowance of the terminal width of printed contacts (w) as illustrated in Figure 14 is specified in Table 14.

Figure 14 – Terminal width of a printed contact

Table 14 – Allowance of the terminal width of a printed contact

mm

Terminal width	Allowance
≤ 1,0	±0,05
1,0<	±0,10

4.5.3 Shift of the centre of printed contacts on front and back sides of a board

The allowance of the shift of the centre of printed contacts on front and back sides of a board (q) as illustrated in Figure 15 shall be ±0,20 mm.

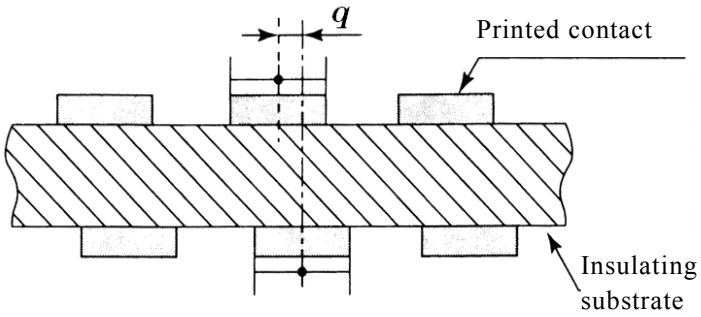


Figure 15 – Shift of the centre of printed contacts on front and back sides of a board

4.6 Footprint

4.6.1 Allowance of the distance between the centers of two pads

The allowance of the distance between the centres of two adjacent pads (S_1) and of two adjascent parallel pads (S) as illustrated in Figure 16 is specified in Table 15.

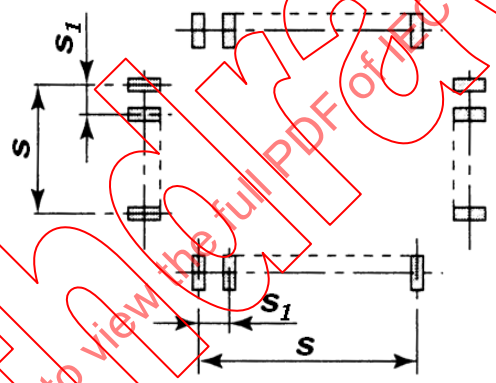


Figure 16 – Foot print

Table 15 – Allowance of the distance between the centres of two pads

mm

Distance between centres	Allowance
S_1	±0,03
S	±0,05

4.6.2 Allowance of the width of a pad

The allowance of the width of a pad of a footprint (w) as illustrated in Figure 17 is specified in Table 16. The allowance for a pad narrower than 0,15 mm shall be agreed between the user and supplier.

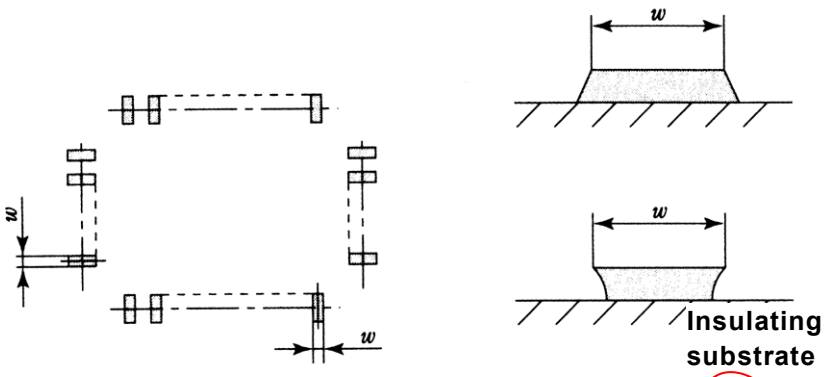


Figure 17– Pad width of a footprint

Table 16 – Allowance of the width of a pad of a footprint

mm

Pad width	Allowance
0,15 < ≤0,35	±0,04
0,35<	±0,06

4.6.3 Pad diameter and its allowance for BGA/CSP

The allowance of pad diameter for BGA/CSP is specified in 4.6.3 (1) and 4.6.3 (2) specified below.

(1) The pattern is shown in Figure 18. The allowance of the pad diameter (*d*) of BGA/CSP made of conductor only is given in Table 17.

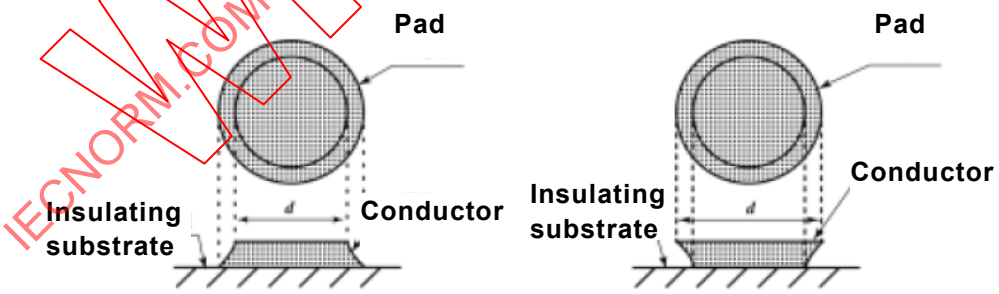


Figure 18 – Allowance of pad diameter of BGA/CSP formed of conductor only

Table 17 – Pad diameter and its allowance for BGA/CSP

Item	Allowance of pad diameter (mm)	Conductor thickness (μm, for reference)
HDI PWB	+ 0,02 – 0,03	20 to 30
Standard PWB	+ 0,03 – 0,05	30 to 50

(2) The pattern is shown in Figure 19. The allowance of the pad diameter (*d*) of BGA/CSP formed at the opening of solder resist is given in Table 18.

Table 18 – Allowance of the pad diameter (*d*) of BGA/CSP formed at the opening of solder resist

mm

Item	Allowance
HDI PWB	± 0,03
Standard PWB	± 0,05

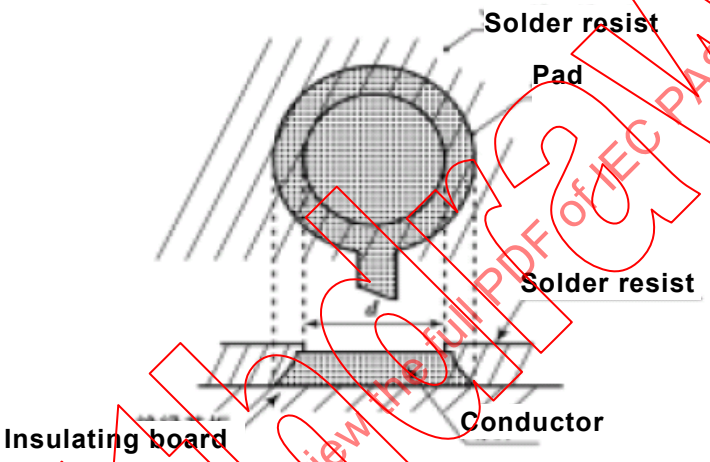


Figure 19 – Pad diameter (*d*) of BGA/CSP formed at the opening of solder resist

4.7 Fiducial mark and the mark for component positioning

4.7.1 The typical form and the size of the fiducial mark and the mark for component positioning as illustrated in Figure 20 are specified in Table 19.

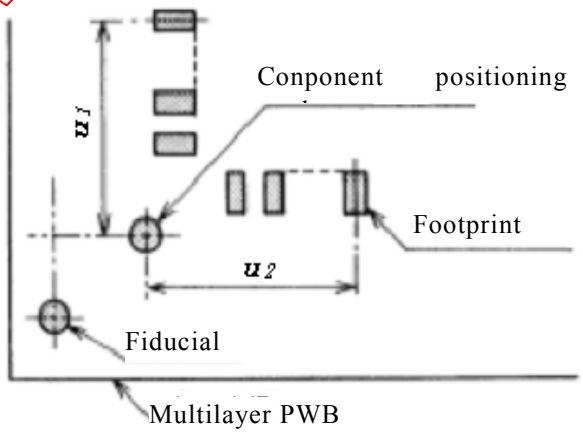


Figure 20 – Examples of fiducial mark and component positioning mark

Table 19 – Shapes and sizes of typical fiducial marks and component positioning marks

mm

Item	Shape	Diameter
Fiducial and component positioning marks	Circle	1,0

4.7.2 Dimensional allowance of fiducial mark and component positioning mark

The dimensional allowance of fiducial mark and component positioning mark as illustrated in Figure 21 is ±0,1 mm.

4.7.3 Position allowance of the component positioning mark and the farthest footprint from the mark (u_1, u_2) as illustrated in Figure 21 shall be ±0,05 mm.

4.8 Interlayer connection

(1) Copper plating

The minimum thickness of copper plating on the wall of via and component insertion holes is given in Table 20.

Table 20 – Minimum thickness of copper plating

Board thickness, or layer thickness (mm)	Minimum thickness of copper plating [a] (μm)
2,4<	Thickness shall be agreed between the user and supplier.
1,0 < ≤2,4	15
0,5 < ≤1,0	12
0,5≤	10

[a] The measurement shall be made by optical observation of a microsectioned vertical cross section. Local surface deviation is not accounted.

5 Quality

5.1 Gap between conductor and the wall of a component insertion hole or a via

The gap between conductor and the wall of a component insertion hole or a via, or the gap between the inner conductor and the wall of a hole shall be larger than 0,13 mm.

5.2 Positional deviation between conductor layers of multilayer board

The deviation of conductor layers of multilayer board shall satisfy the conditions specified in 4.5.3, 5.1, and 5.3.

5.3 Minimum land width

The minimum land width on the most outer layer (w_1) caused by the shift of land and the hole, and the minimum land width on an inner layer (w_2) are specified in Table 21 (also see Figures 21-1 to 21-3).

Table 21 – Minimum land width

mm

Item [a]		Minimum land width
Minimum land width on outer layer w_1 [b]	At the joint of land and conductor	$w_1 \geqq 0{,}03$
	Other area	$\theta \leqq 90°$
	Case of non-conductive component insertion hole	$w_1 \geqq 0{,}05$
Minimum land width on inner layer w_2 [c]	At the joint of land and conductor	$w_2 \geqq 0{,}03$
	Others (except laser drilled hole) [d]	$\theta \leqq 90°$

a Regardless of the shape of a land.

b Includes the thickness of through-hole plating.

c Does not include the thickness of through-hole plating.

d No break of inner land is allowed for a laser drilled hole.

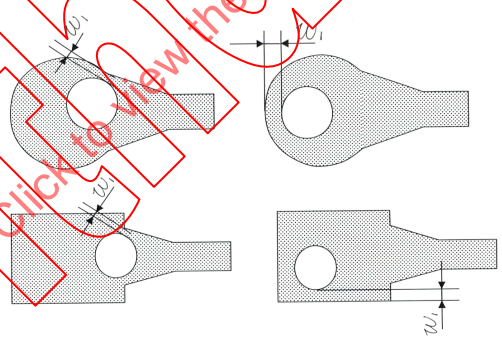


Figure 21-1 – Minimum land width on the outer layer

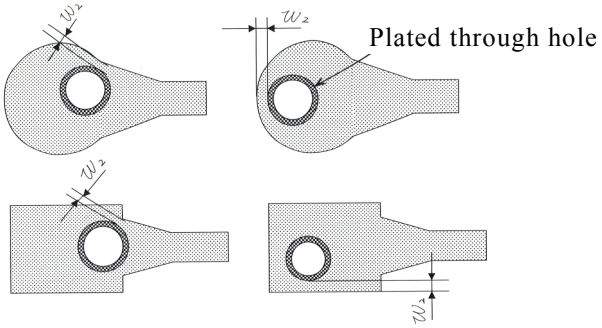


Figure 21-2 – Minimum land width on the inner layer with a plated through-hole

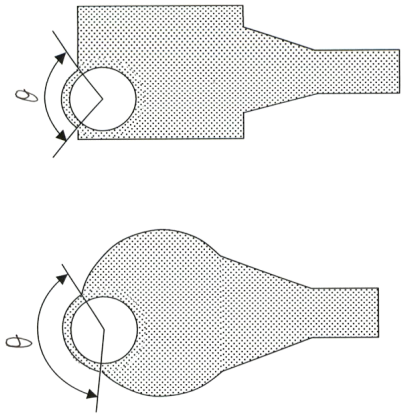


Figure 21-3 – Allowable area of land break

5.4 Surface treatment

5.4.1 Gold plating for printed contact

The gold plating for printed contact is generally plated of hard gold on the nickel plating.

1) Nickel plating: the thickness of nickel plating on a printed contact shall be more than 2,0 μm.
2) Gold plating: the hard gold shall be used for plating on a printed contact with a plating thickness of more than 0,1 μm.

5.4.2 Other surface treatment

The details of other surface treatment including gold flush plating and solder coating depends on the methods for interconnection (such as soldering or wire bonding). These details shall be agreed by the user and supplier.

5.5 Defects of solder resist

1) The defects in a pad for BGA/CSP shall be in accordance with 4.6.3 (diameter and allowance of pads for BGA/CCP).
2) Solder resist shall not have scratch, peeling, pin-hole, or foreign material. Solder resist shall not have any bubble extending to two conductors.
3) Exposure of conductor after application of solder resist shall be in conformance to the illustrations in Figure 22.

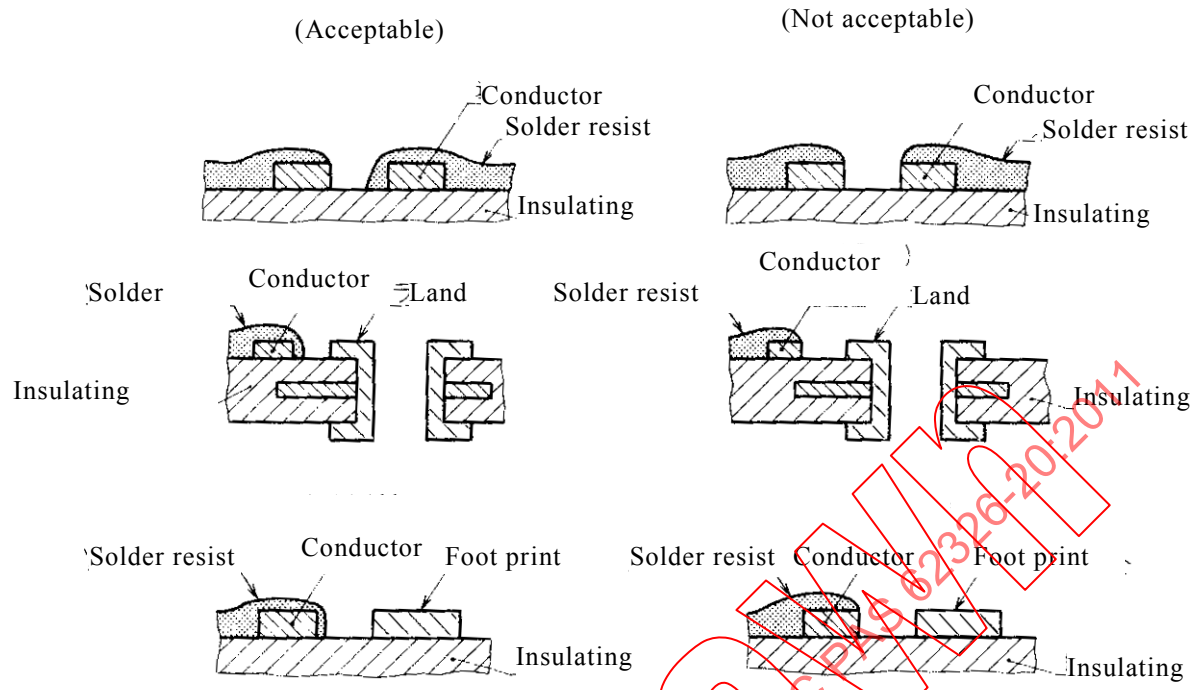


Figure 22 – Exposure of conductor

4) The minimum land width caused by the shift of solder resist (*w*) on the land on the outer conductor layer of PWB used for component insertion as illustrated in Figure 23 shall be in accordance with the specification given in Table 22.

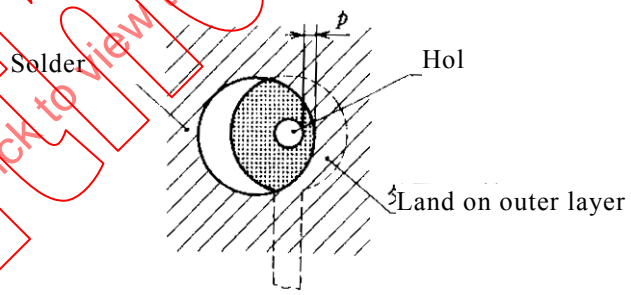


Figure 23 – Minimum land width caused by the shift of solder resist

Table 22 – Minimum land width

Item	Minimum land width
Facing to component	To the edge of a hole
Facing to solder	0,03 mm ≤ the area effective for soldering shall be larger than 70 %.

5) The overlap, smear and shift of solder resist on a land [width direction (*v*) and length direction (*x*)] on the outer conductor layer of PWB used for component insertion as illustrated in Figure 24 shall comply with the specification given in Table 23. The displacement in the case solder resist is designed to cover the entire footprint as illustrated in Figure 24-2 shall be agreed between the user and supplier.

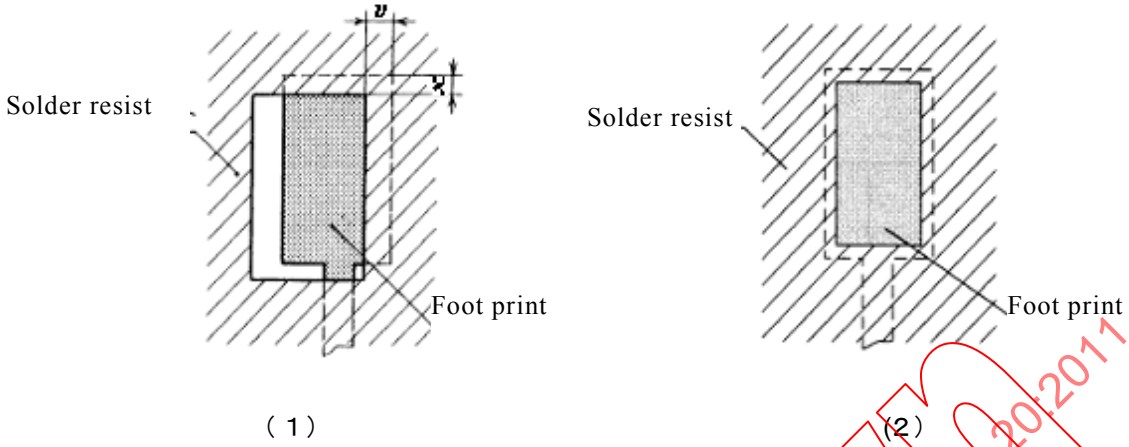


Figure 24 – The overlap, smear and shift of solder resist

Table 23 – The overlap, smear and shift of solder resist over a fool print

mm

Item	Overlap, smear and shift
Width (v)	≤ 0,05
Longitudinal (x)	≤ 0,05

6) The overlap, smear and shift of solder resist on a ball-pad or a pad for wire-bonding shall not exist unless the solder resist is designed to cover a pad.

5.6 Symbol mark

1) A printed symbol mark shall not have smear or blur affecting readability of the mark.

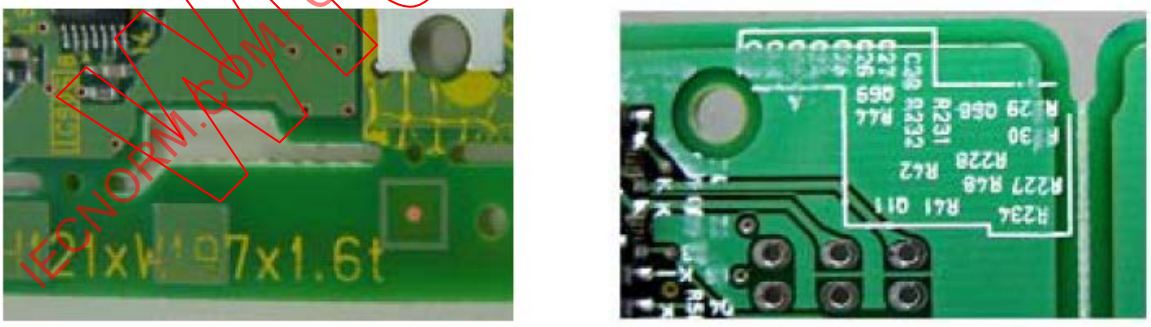


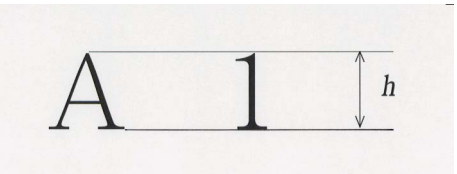
Figure 25 – Examples

2) A symbol mark shall be printed more than 0,2 mm away from a via land, a through hole land, or a footprint.

3) A symbol mark with a height (h) (see note below) of less than 1,5 mm may not be legible to identify the mark as a letter or a mark (except Chinese character).

Remark 1: The line width of thicker than 0,15 mm for a symbol is recommended.

Remark 2: A symbol mark should be designed as right on the conductor pattern, or completely away from the conductor.



NOTE An example of the height of a symbol mark is shown above.

5.7 Appearance

5.7.1 Conductor surface

There shall be no swell, wrinkle, crack, separation of conductor from the substrate, nor a metal fracture at an edge of a conductor. There shall be no colour change that may cause a defect in assembly, fouling nor foreign material on the conductor surface. The exposure of the bare conductor that is treated with plating, the surface treatment or coated is not allowed.

5.7.2 Between conductors

There shall be no foreign material that bridges two conductors and may cause an insulation problem.

5.7.3 Defects within insulating layers

1) Measling and crazing

There shall be no measling nor crazing that overlaps conductors, holes for component insertion or between vias.

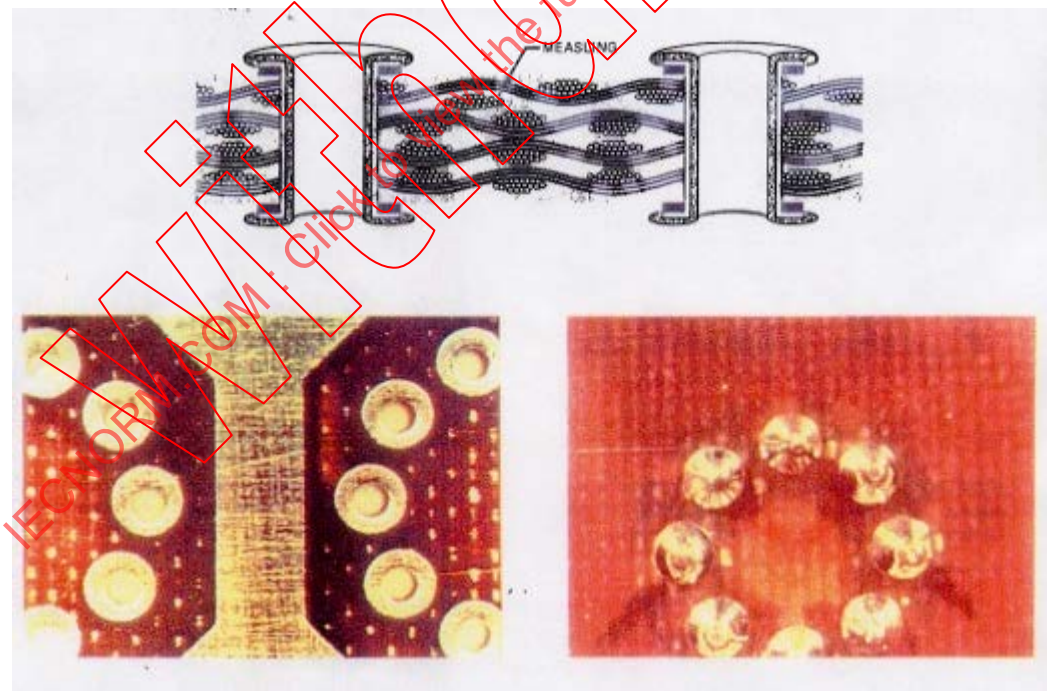


Figure 26 – Example of measling

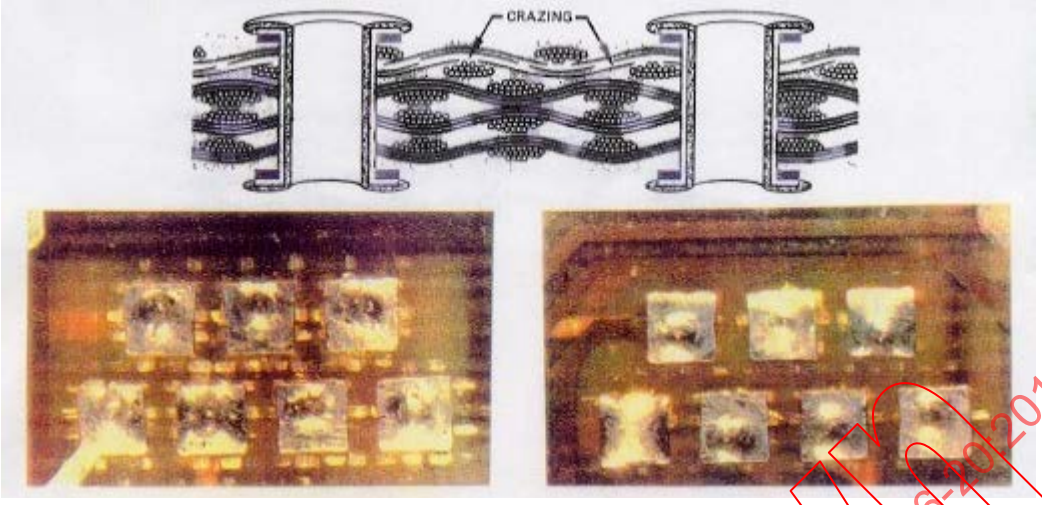


Figure 27 – Examples of crazing

2) Delamination, swell and void: there shall not be delamination nor swell and stacked voids that may result in a reliability problem of a product in a multilayer board.

3) Inclusion of foreign materials: there shall be no foreign material nor imperfection such as delamination that may result in a problem in assembly process.

5.7.4 Routing and drilling: cracks caused by press machine of routing and hole drilling, and hallowing shall be agreed between the user and supplier.

5.7.5 Conductor pattern:

1) Missing of conductor: the width of a missing part of a conductor (*w*) shall be less than 30 % of the final conductor width, and the length (*l*) of less than the width of conductor pattern.

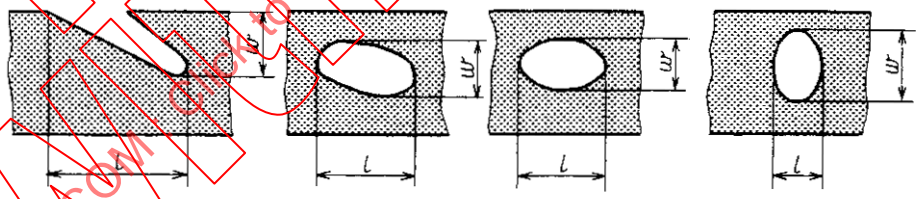


Figure 28 – Missing of conductor

2) Residue of conductor in conductor gaps: the width (*w*) of a residue of conductor between conductors as illustrated in Figure 29 (protrusion or residure in etching) shall be less than 30 % of the final separation of conductors, or, less than 0,30 mm. The length of a residue (*l*) shall be less than the final separation of the conductor.

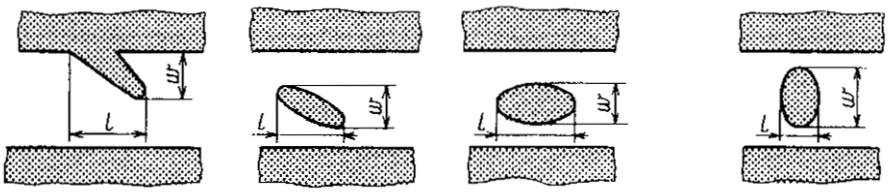
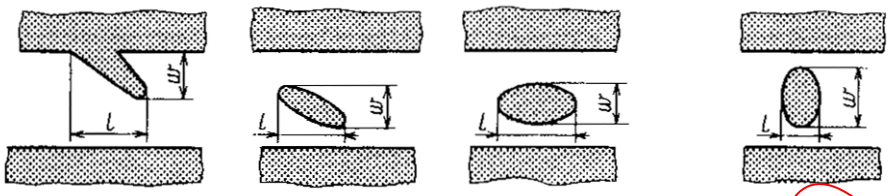


Figure 29 – Conductor residue

5.8 Land

The allowance of the area, remaining width (w_1, w_2), and protrusion (y) of a defect caused by missing of a part of a land shall comply with the specification given in Table 24.



(1) Width of remaining land (2) Widths of remaining land and edge to conductor (3) Protrusion of land

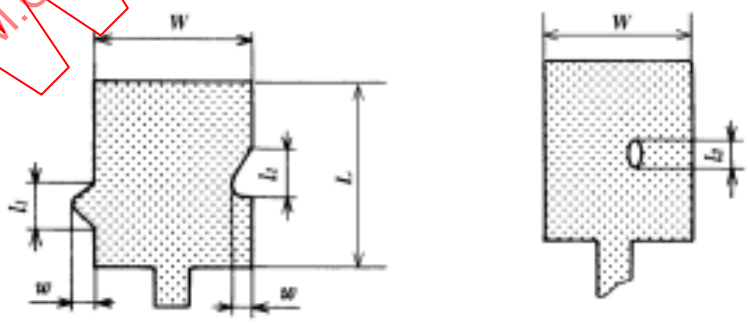
Figure 30 – Land

Table 24 – Allowance of the area of a defect, remaining width and protrusion of a land

Item		Area of a defect, remaining width and protrusion of a land
Ratio of the missing area to the area of a land		≤ 20 %
Remaining width resulted from a defect of a land	W_1	No defect shall reach to the wall of a hole.
	W_2	More than 70 % of the final conductor width
Protrusion	y	As specified in 5.7.5 (2) – Width of residue in the conductor gap w.

5.9 Pad of a footprint

The width (w) and the length (l_1, l_2) of a defect as illustrated in Figure 31 in a pad shall comply with the specification given in Table 25. The maximum number of defects in a pad shall be no more than one.



(1) Crack and protrusion (2) Pin hole

Figure 31 – Defects in a pad of a footprint

Table 25 – Defect of a pad of a footprint

mm

Item		Width of completed pad of a footprint w	
		< 0,8	0,8≤
Crack and protrusion a	Width *w*	Less than 20 % of *w*	≤ 0,15
	Length l_1	Less than 50 % of *L*	
Pinhole (longer dimension l_2)		Less than 20 % of *w*	≤ 0,15

[a] The protrusion shall satisfy the minimum separation betweeen a neighbouring conductor specified in 4.4.2.

5.10 Defects in a pad for BGA/CSP mounting

The defects in a pad for BGA/CSP mounting as illustrated in Figure 26 shall comply with what is given in Table 26, and shall not exceed 1 for one pad.

(1) Chipping and protrusion (2) Pin-hole

Figure 32 – Defects in BGA/CSP mounting pads

Table 26 – Defects in BGA/CSP mounting pads

Item	Defects in BGA/CSP mounting pads
Chipping and protrusion [a]	Effective pad area shall be over 80 % of the designed area
Pin holes (long diameter l_2)	There shall be no pin hole showing the insulation layer

[a] The length of protrusion shall satisfy the minimum separation between conductors (see 4.4.2).

5.11 Printed contact

5.11.1 Printed contact that is to be electrically connected

The allowance of the defects in the areas ① and ② of a printed contact (see Figure 33) that is to be electrically connected as illustrated in Figure 33 shall comply with the specification given Table 27.

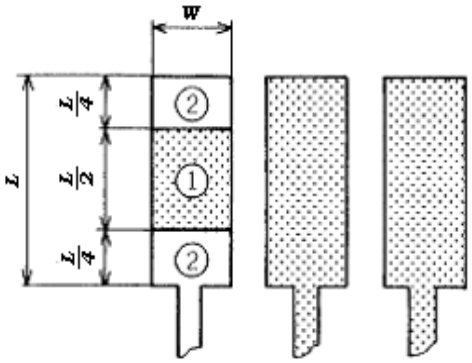


Figure 33 – The areas to be checked for defects of a printed contact

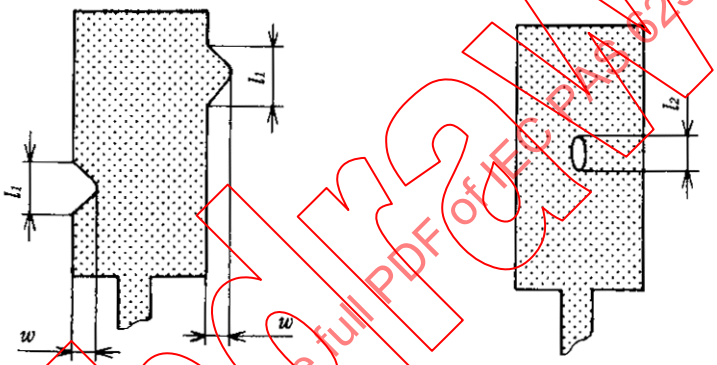


Figure 34 – Defects in a printed contact

Table 27 – Defects in a printed contact

mm

<table>
<tr><th rowspan="2">Item</th><th colspan="3">Area [b]</th></tr>
<tr><th>Area ①</th><th colspan="2">Area ②</th></tr>
<tr><td>Exposure of underlying plating (Ni, Co, etc.)
Swell and separation of plated film</td><td colspan="3">No defect is allowed that may affect the realibility of a product</td></tr>
<tr><td>Hit trace</td><td>No trace larger than φ 0,2 is allowed</td><td colspan="2">No trace larger than φ 0,5 is allowed</td></tr>
<tr><td>Scratch</td><td>No scratch larger than a width of 0,1 is allowed</td><td colspan="2">No scratch larger than a width of 0,5 is allowed</td></tr>
<tr><td>Lump protrusion</td><td colspan="3">No protrusion larger than a width of φ 0,1 is allowed.</td></tr>
<tr><td rowspan="2">Crack and protrutsion [a], l_1, w</td><td>$l_1 \leq 0{,}1\ L$ $w \leq 0{,}1\ W$
l_1 shall be smaller than 1,0, and w shall be smaller than 0,2</td><td colspan="2">$l_1 \leq 0{,}2\ L$ $w \leq 0{,}2\ W$
l_1 shall be smaller than 2,0, and w shall be smaller than 0,3</td></tr>
<tr><td colspan="3">The protrusion shall satisfy the minimum separation betweeen a neighbouring conductor specified in 4.4.2</td></tr>
<tr><td rowspan="3">Pin hole [a] (longer dimention l_2)</td><td rowspan="3">There shall be no pin hole.</td><td>φ0,05≤ ≤φ0,10</td><td>One defect per terminal and less than 10 % of the total terminals</td></tr>
<tr><td>φ0,10< ≤φ0,20</td><td>One defect per terminal and less than 2 % of the total terminals</td></tr>
<tr><td>φ0,20<</td><td>No pin hole allowed</td></tr>
<tr><td>Colour change</td><td colspan="3">No colour change that affects the performance of a product is allowed.</td></tr>
</table>

[a] See Figures 31 and 32.

[b] The defects for printed contacts not electrically connected are considered as defects in the area ② in Figure 31 for the entire contacts. The specification given in Table 22 for such an area is applicable to these contacts.

6 Performance and test methods

The performance of PWB is specified in 6.1 and Table 29. Test methods for characterization are by those specified in Table 29 and JIS C 5012.

6.1 Observation of component mounting for and vias

6.1.1 Observation with standard conditions

The holes and vias shall satisfy the following specifications when observed by a naked eye, using a magnifying glass or by means of microsectionning.

(1) The holes for component insertion shall be satisfactory for lead insersion and following soldering. The size of a lack of plating on the wall of a hole as illustrated in Figure 35 shall be less than 25 % of the cirrcumference of a hole (l_1) and less than 25% of the thickness direction of the board (l_2). The number of holes with defects shall be less than 5 % of the total number of holes.

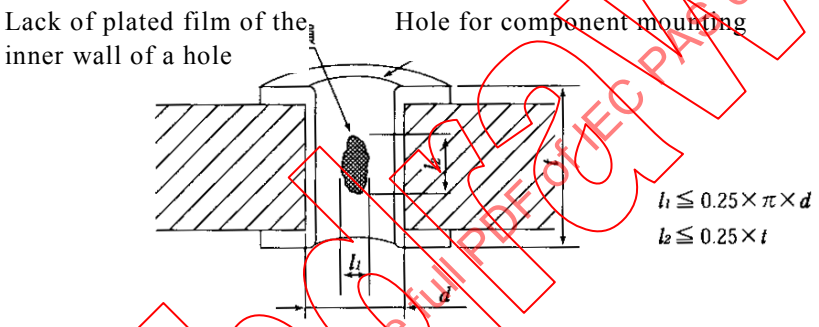


Figure 35 – Defect on a plating of a component mounting hole

(2) Vias for electrical connection between conductor layers. Vias are for electrical connections. Neither defect in via formation nor defect in electric conduction (plating or filling of metal paste) shall be allowed and shall comply with the specifications 11 and 12 in Table 29.

(3) Resin smear: The allowance in the vertical microsection of resin smear as illustrated in Figure 37-1 shall comply with the following equation. The allowance in the horizontal microsection of a smer shall be as specified in Table 28.

$l_1 , l_2 > 1/3t$, and $l_1 + l_2 > t$

l_1, l_2: effective thickness of an inner layer excluding resin smear (μm).

t: the thickness of the inner layer relevant to resin smear (μm).

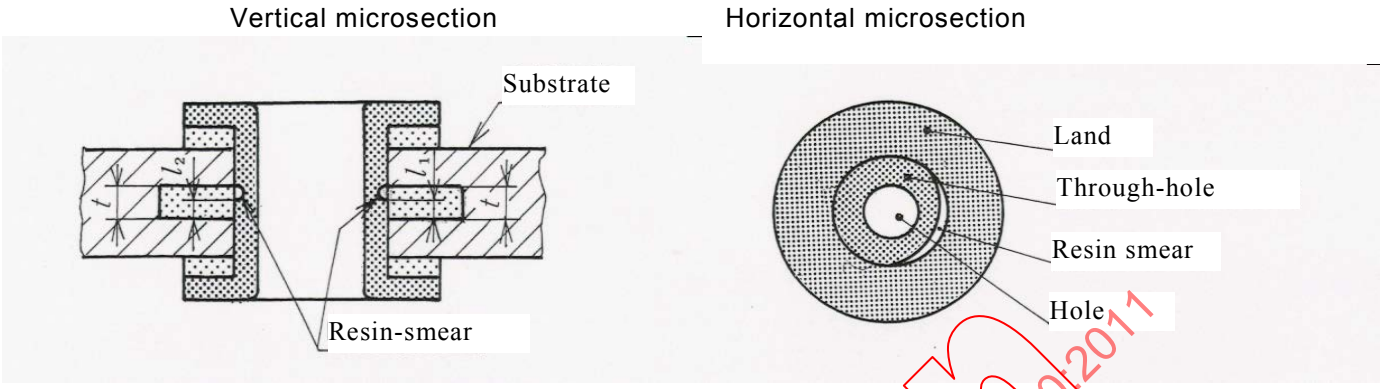


Figure 36-1 – Resin smear

Table 28 – Allowance in horizontal sectioning

HDI PWG	Less than 10 % of hole circumference
Standard PWB	Less than 25 % of hole circumference

6.1.2 Observation after thermal shock test

The specimens for the thermal shock test described in 11 and 12 of Table 29 shall be observed by microsectioning as specified in 6.2 of JIS C 5012 (Microsection), and shall comply with the following specification.

(1) Corner crack, parallel crack and foil crack

The allowance in the vertical microsection of resin smear as illustrated in Figures 36-2 to 36-4 shall comply with the following equation.

l_1 , $l_2 > 1/3t$, and $l_1 + l_2 > t$ Hole

l_1, l_2: effective thickness of copper foil for each side excluding resin smear (μm).
t: the total thickness of copper foil when there is no defect that can be considered as a defect (μm).

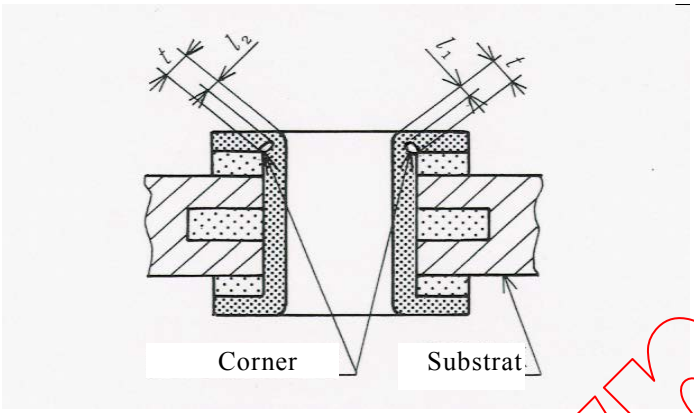


Figure 36-2 – Corner crack

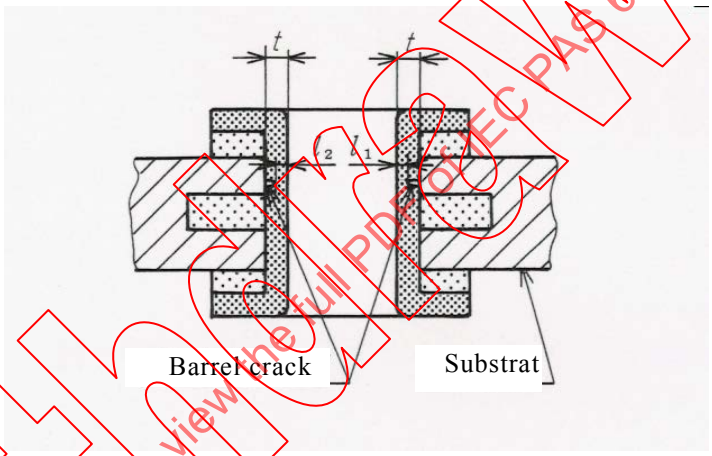


Figure 36-3 – Barrel crack

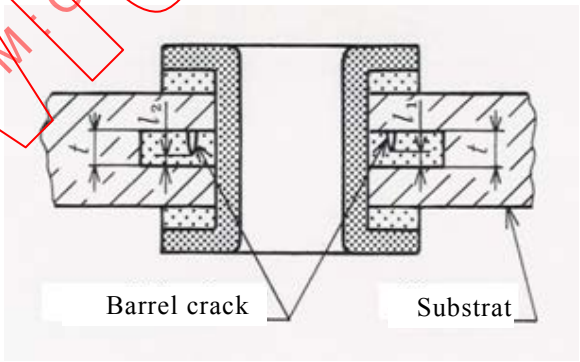
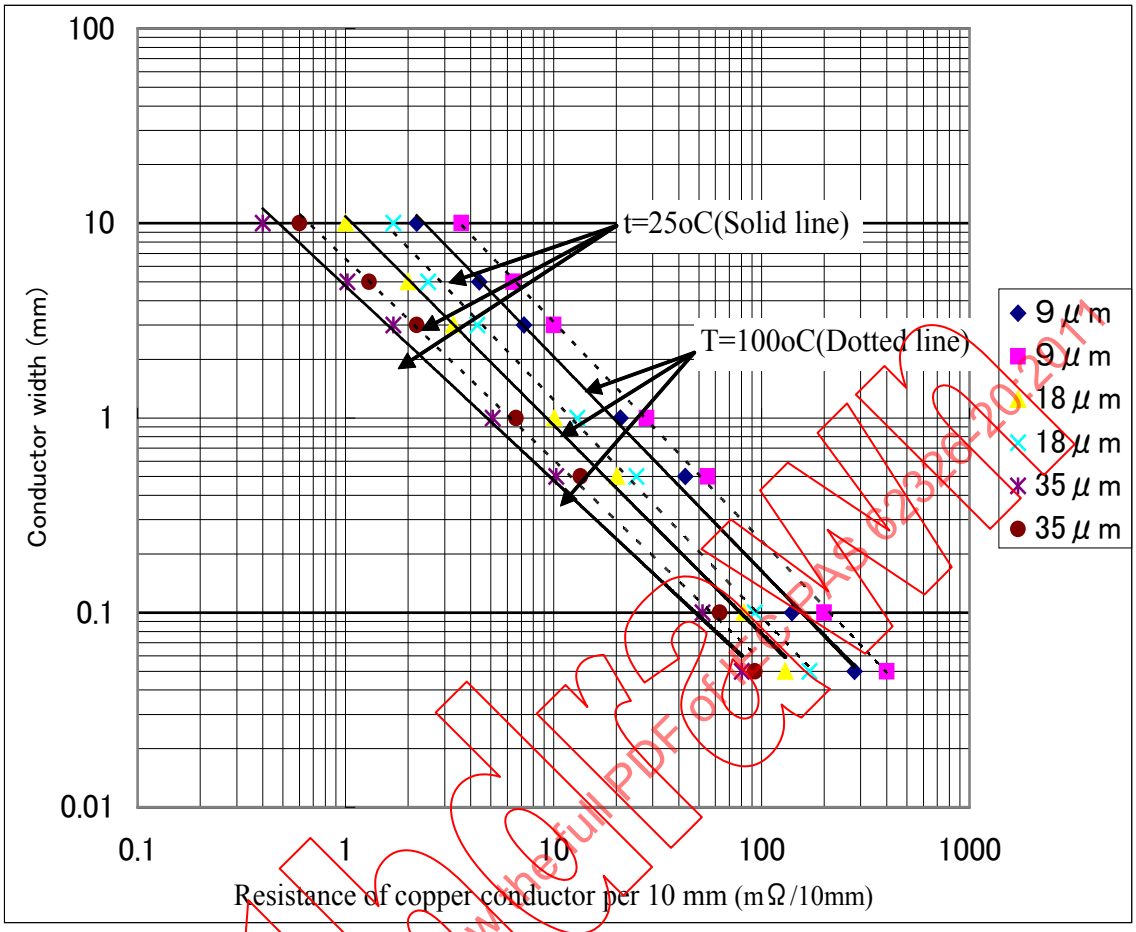


Figure 36-4 – Foil crack



NOTE The conductor width is kept constant, and the relative resistivity of copper is $\rho = 1{,}8 \times 10^{6}$ Ωcm.

Figure 37 – The relations between resistance and width, thickness and temperature of conductor

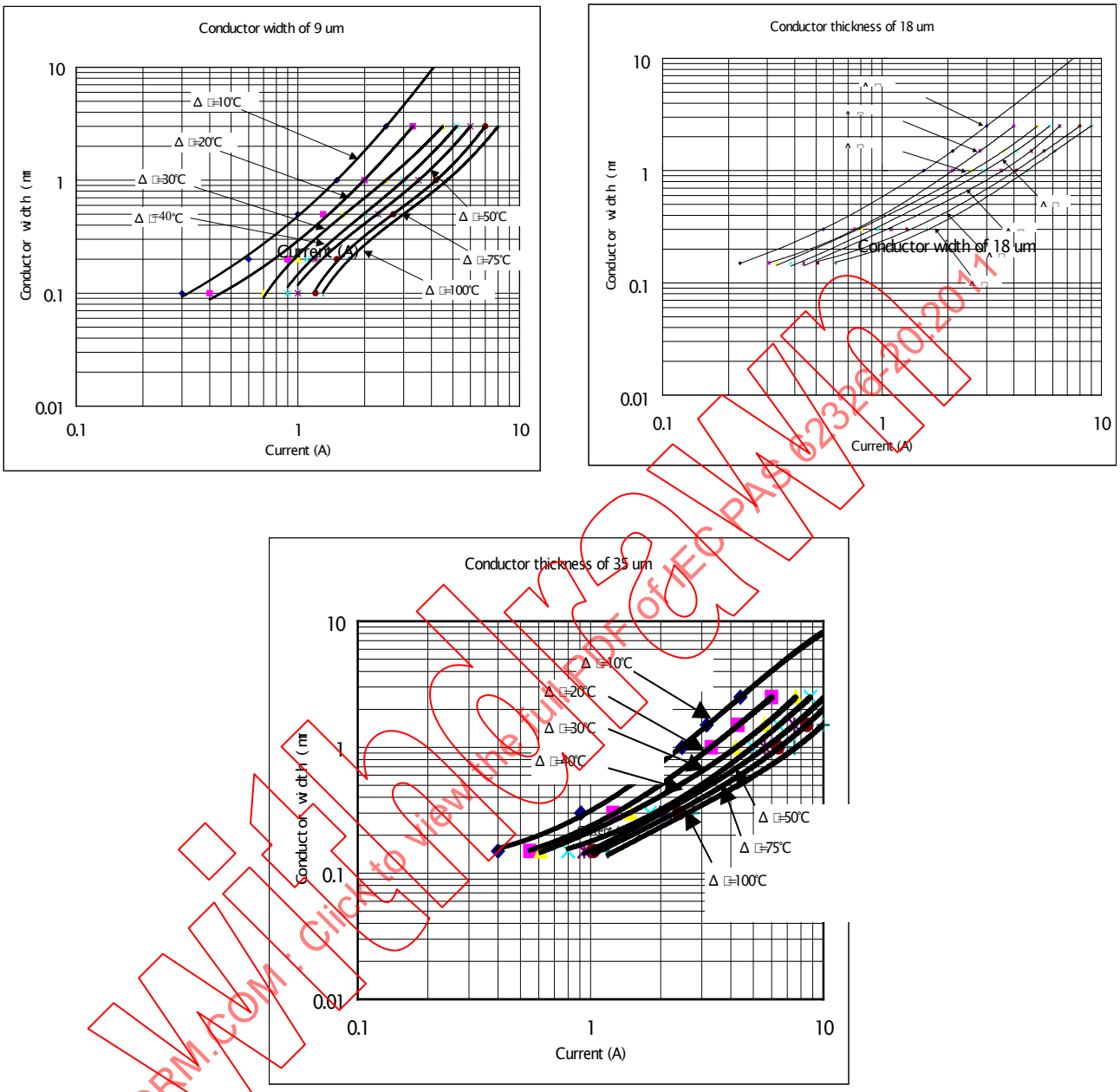


Figure 38 – Temperature rise as functions of width and thickness of conductor and current

Table 29 – Specification and test methods

No.	Item		Specification	Test method (JIS C 5012)
1	Resistance of conductor	Inner conductor	To be agreed between the user and supplier. The relations between resistance and witdth, thickness and temperature of conductor are shown in Figure 37 as a reference.	As per 7.1.1 (conductor) The shape and dimensions of specimens shall be agreed between the user and supplier.
		Outer conductor		As per 7.1.3 (inner connection)
		Plated through-hole		As per 7.1.2 (plated through-hole)
2	Tempera-ture rise	Conductor	To be agreed between the user and supplier. The relations between current and width, thickness and temperature of conductor are shown in Figure 38 as a reference.	As per 7.2 (temperature rise)
		Plated through-hole		As per 7.3 (temperature rise of plated through-hole)

Table 29 *(Continued)*

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td>3</td><td>Withstanding voltage</td><td>Within the same plane</td><td>No abnormality such as mechanical damage, flush-over or breakdown is allowed.</td><td>As per 7.4 (Withstand voltage)
Test condition for withstand voltage is given below for both outer layer (with/without solder resist) and inner layer.
<table>
<tr><th>Minimum gap between conductors, mm</th><th>Test voltage (V)</th></tr>
<tr><td>0,05≤ <0,10</td><td>50</td></tr>
<tr><td>0,10≤ <0,13</td><td>100</td></tr>
<tr><td>0,13≤ <0,25</td><td>200</td></tr>
<tr><td>0,25≤ <0,40</td><td>350</td></tr>
<tr><td>0,40≤</td><td>500</td></tr>
</table>
NOTE Solder resist is not regarded as coating.</td></tr>
<tr><td></td><td></td><td>Interlayer</td><td>No abnormality such as mechanical damage, flush-over or breakdown is allowed.</td><td>As per 7.5 (Interlayer withstand voltage)
Test condition for withstand voltage is given below for both outer layer (with/without solder resist) and inner layer.
<table>
<tr><th>Interlayer, mm</th><th>Test voltage, V</th></tr>
<tr><td>0,05≤ <0,08</td><td>250</td></tr>
<tr><td>0,08≤ <0,20</td><td>500</td></tr>
<tr><td>0,20≤</td><td>1 000</td></tr>
</table></td></tr>
</table>

Table 29 *(Continued)*

<table>
<tr><th>No.</th><th colspan="3">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td rowspan="3">4</td><td rowspan="3">Insulation resistance</td><td rowspan="2">On the same plane</td><td>Steady state</td><td>The insulation resistance shall be larger then the value specified.
<table><tr><th>Minimum gap (mm)</th><th>Insulation resistance Ω</th></tr><tr><td>0,10 ≤ < 0,13</td><td>1×10^{10}</td></tr><tr><td>0,13 ≤</td><td>5×10^{10}</td></tr></table></td><td rowspan="2">The surface insulation resistance shall be measured as specified in the Annex A of this standard.
The insulation resistance of an inner layer shall be measured as specified in the Annex B of this standard.</td></tr>
<tr><td>Resistance to humidity (temperature–humidity cycle)

Resistance to humidity (steady state)</td><td>The insulation resistance shall be larger then the value specified.
<table><tr><th>Minimum gap (mm)</th><th>Insulation resistance Ω</th></tr><tr><td>0,10 ≤ < 0,13</td><td>1×10^{8}</td></tr><tr><td>0,13 ≤</td><td>5×10^{8}</td></tr></table></td><td>Measurement shall be made as is the case of measurement at steady state after leaving the specimen at room temperature for 1 h.</td></tr>
<tr><td>Inter layer</td><td>Steady state</td><td>The insulation resistance shall be larger then the value specified.
<table><tr><th>Minimum insulation thickness (mm)</th><th>Insulation resistance Ω</th></tr><tr><td>0,05 ≤ < 0,20</td><td>1×10^{10}</td></tr><tr><td>0,20 ≤</td><td>5×10^{10}</td></tr></table></td><td>The insulation resistance between inter-layers shall be measured as specified in the Annex C of this standard. The test voltage used for measurement is shown in the following table.
<table><tr><th>Minimum insulation thickness (mm)</th><th>Test voltage</th></tr><tr><td>0,05 ≤ < 0,08</td><td>50</td></tr><tr><td>0,08 ≤ < 0,20</td><td>100</td></tr><tr><td>0,20 ≤</td><td>500</td></tr></table></td></tr>
</table>

Table 29 *(Continued)*

<table>
<tr><th>No.</th><th colspan="3">Item</th><th>Specification</th><th>Test method (JIS C 5012)</th></tr>
<tr><td></td><td></td><td></td><td>Resistance to humidity (temperature–humidity cycle)</td><td>The insulation resistance shall be larger than the value specified.
<table><tr><th>Minimum insulation thickness (mm)</th><th>Insulation resistance Ω</th></tr><tr><td>0,05 ≤ < 0,20</td><td>1×10^8</td></tr><tr><td>0,20 ≤</td><td>5×10^8</td></tr></table></td><td rowspan="2">Measurement shall be made as is the case of measurement at steady state after leaving the specimen at room temperature for 1 h.</td></tr>
<tr><td></td><td></td><td></td><td>Resistance to humidity (steady state)</td><td></td></tr>
</table>