

TECHNICAL REPORT



**Printed board assemblies –
Part 8: Voiding in solder joints of printed board assemblies for use in automotive
electronic control units – Best practices**

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TECHNICAL REPORT



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Part 8: Voiding in solder joints of printed board assemblies for use in automotive electronic control units – Best practices

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

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PRINTED BOARD ASSEMBLIES –

**Part 8: Voiding in solder joints of printed board assemblies
for use in automotive electronic control units – Best practices**

FOREWORD

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IEC TR 61191-8, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this technical report is based on the following documents:

DTR	Report on voting
91/1665/DTR	91/1689/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 61191 series, published under the general title *Printed board assemblies*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

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- replaced by a revised edition, or
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INTRODUCTION

This document applies to electronic and electromechanical automotive printed board assemblies and describes current best-practices for dealing with voiding in solder joints of surface-mount components soldered onto printed boards.

This document is an informative document which serves to illustrate the technically feasible options and to provide a basis for customer and supplier discussions and agreements. It is not intended to be regarded as a specification or standard.

Related standards are gathered in the bibliography.

This document has been prepared based on material provided by the working group DKE AK682.0.7 (Assembly and interconnect technology in automotive electronics).

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PRINTED BOARD ASSEMBLIES –

Part 8: Voiding in solder joints of printed board assemblies for use in automotive electronic control units – Best practices

1 Scope

This part of IEC 61191 gives guidelines for dealing with voiding in surface-mount solder joints of printed board assemblies for use in automotive electronics. This technical report focuses exclusively on voids in solder joints connecting packaged electronic or electromechanical components with printed boards (PBs). Voids in other solder joints (e.g. in a joint between a silicon die and a substrate within an electronic component, solder joints of through-hole components, etc.) are not considered. The technical background for the occurrence of voids in solder joints, the potential impact of voiding on printed board assembly reliability and functionality, the investigation of voiding levels in sample- and series-production by use of X-ray inspection as well as typical voiding levels in different types of solder joints are discussed. Recommendations for the control of voiding in series production are also given.

Annex A collects typical voiding levels of components and recommendations for acceptability.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1

design authority

individual, organization, company, contractually designated authority, or agency responsible for the design of electrical / electronic hardware, having the authority to define variations or restrictions to the requirements of applicable standards, i.e., the originator/custodian of the applicable design standard and the approved or controlled documentation

3.2

manufacturer

individual, organization, or company responsible for the assembly process and verification operations

3.3

preballed component

component delivered with solder balls attached, as ball-grid arrays

3.4

solder coverage

ratio of the overlapping area between parallel and wettable surfaces of printed board and component termination covered with a vertically continuous layer of solder divided by the total overlapping area between parallel and wettable surfaces of printed board and component termination

Note 1 to entry: Voids and empty space are not part of the vertically continuous layer of solder and therefore do not contribute to the solder coverage.

3.5

user

individual, organization, company or agency responsible for the procurement of electrical/electronic hardware, and having the authority to define any variation or restrictions to the requirements of applicable standards, i.e., the originator/custodian of the contract detailing these requirements

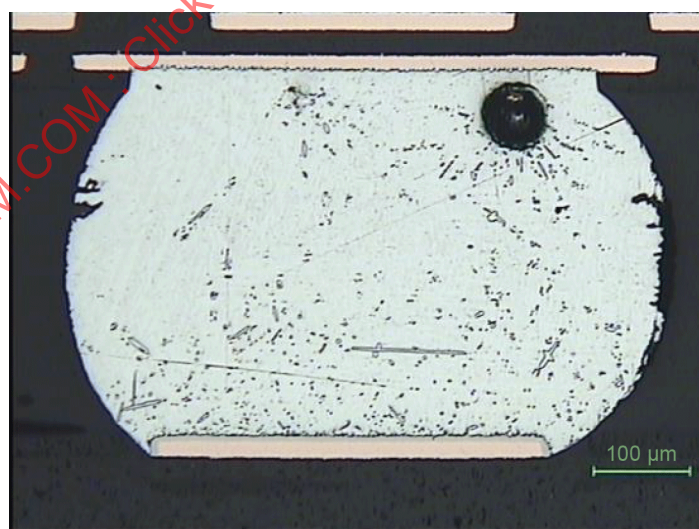
4 Technical background of voiding in solder joints and potential impact on assembly reliability

4.1 Void categories

Different categories of voids exist (see also Annex A). Those are illustrated in Figure 1 to Figure 7:

a) Inclusions / macro voids (type I)

Voids generated by the evolution of volatiles during the reflow process when the solder is molten. The sources of volatiles are fluxes and solder paste, absorbed moisture in laminates or resulting from oxide reduction during the flux reaction. See Figure 1 for an example.



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Figure 1 – Example of inclusion/macro void

b) Design induced voids, (type II)

Voids generated due to the presence of microvia(s) in the land pattern (via in pad design). During reflow, the microvia traps the volatile gases and prevents them from escaping from the solder joint. See Figure 2 for an example.

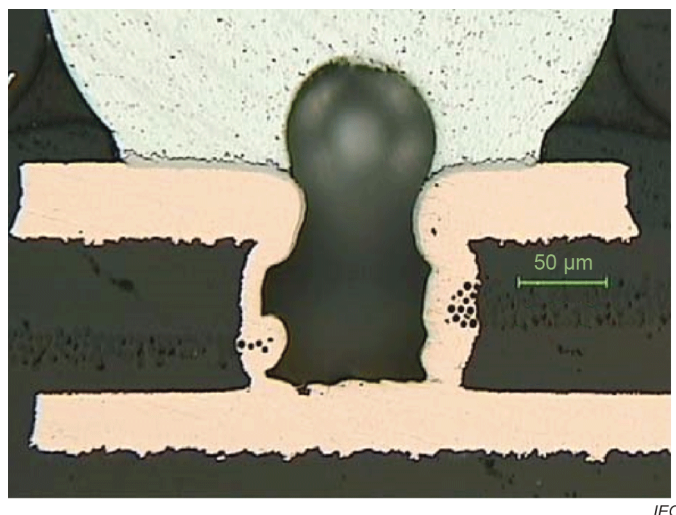


Figure 2 – Example of design induced void

c) Shrinkage voids (type III)

Voids caused by the reduction in solder volume when the solder is in the process of solidification from liquid to solid. See Figure 3 for an example.



Figure 3 – Example of shrinkage void

d) Planar micro voids (type IV)

Small voids (typically < 20 μm in diameter) residing substantially at the interface between PB land or component termination and solder; this type of voiding is sometimes also known as "champagne voids". See Figure 4 for an example.

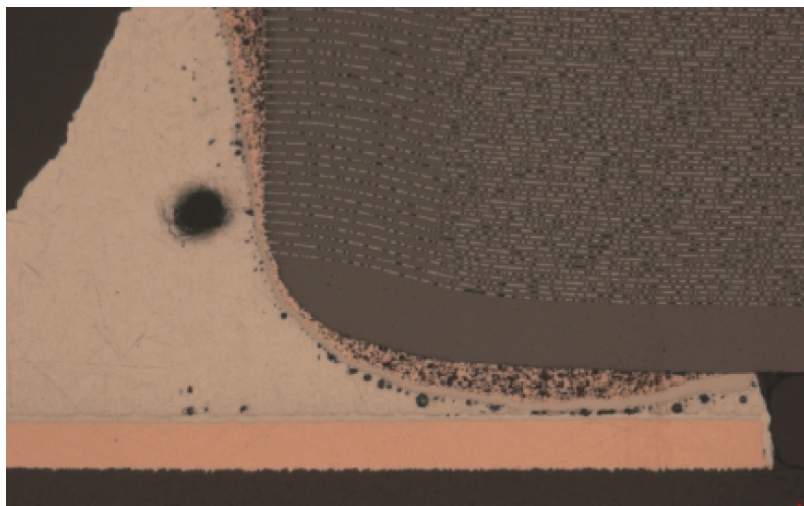


Figure 4 – Example of planar micro voids

e) Intermetallic micro voids (type V)

Voids formed within intermetallic layers, between base metal and component termination, due to organic impurities in the Cu during electroplating. See Figure 5 for an example.

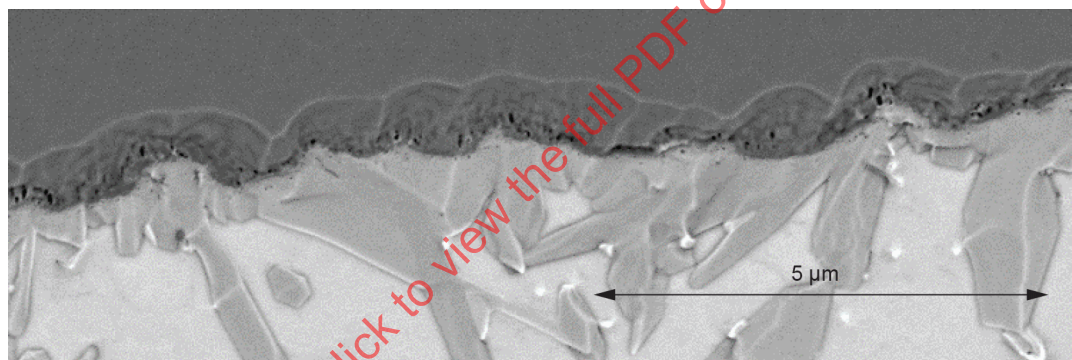


Figure 5 – Example of intermetallic voids

f) Pinhole micro voids (type VI)

Micron-sized voids within the intermetallic compound (IMC), between the IMC and the PB Cu land or (rarely) close to the IMC in the solder; these are due to an unstable plating process, which can lead to chemicals becoming entrapped during the PB fabrication process. See Figure 6 for an example.

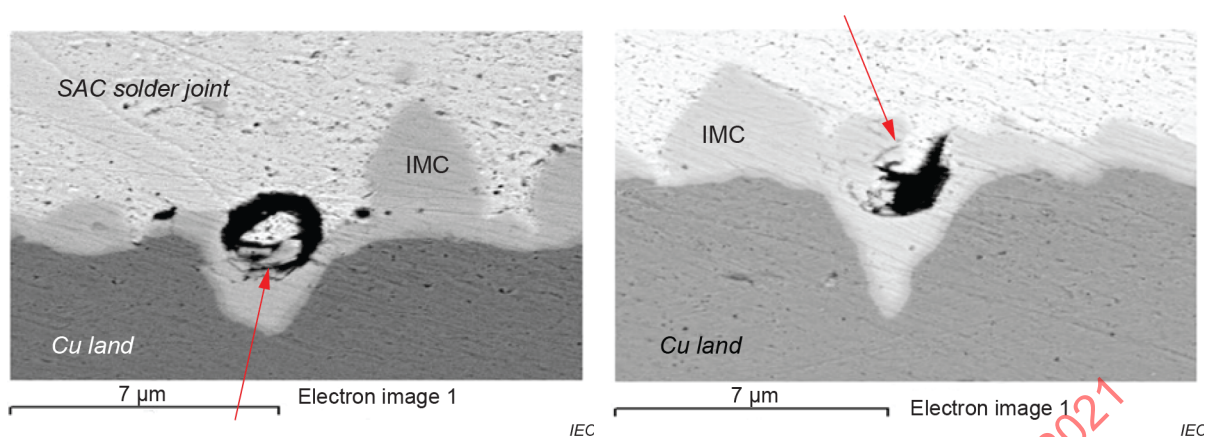


Figure 6 – Example of pinholes¹

g) Blowholes (type VII)

Voids caused by escaping gaseous flux residues, characterized by a hole in the surface of the solder that is connected with a sub-surface cavity. See Figure 7 for an example.

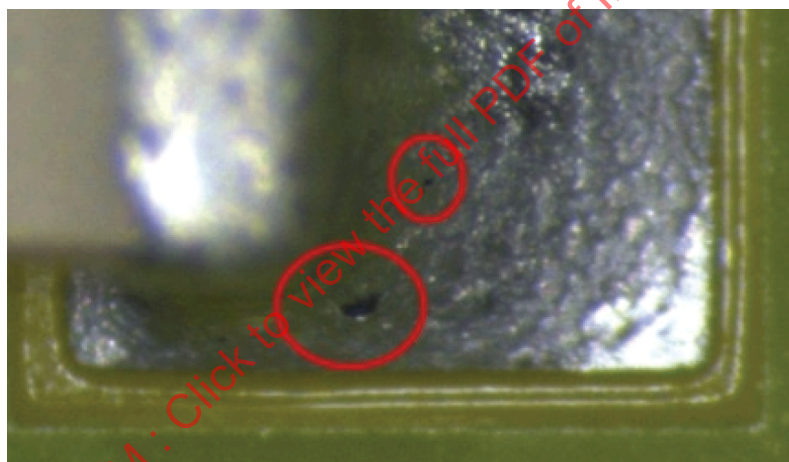


Figure 7 – Example of blowhole voids

4.2 Void occurrence in surface-mount technology solder joints

Voiding in solder joints is primarily caused by outgassing of entrapped flux volatiles in molten solder and the presence of oxides and contaminants on the PB and/or component surfaces that inhibit wetting during the reflow soldering process. Based on the results of most void investigations, it is generally accepted that the most relevant parameters that influence void formation are: solder paste flux chemistry, the cleanliness of PB and component surfaces, the time it takes for the solder powder to coalesce during reflow versus the time it takes for eliminating the metallization oxide(s), paste type (grain size) and, in combination with paste, also the temperature profile of the reflow soldering process. Based on the reflow profile, if the paste coalesces much sooner than the substrate oxide removal at reflow, the flux can adhere to the surface of the substrate oxide (an immobile phase) and become entrapped in the molten solder. Consequently, this entrapped flux will serve as an outgassing source and will constantly release vapour which directly contributes to void formation. The void content also decreases

¹ Reproduced from Aspandiar, R., *Voids in Solder Joints*, Presentation made at the SMTAI 2006 Conference, with the permission of the author.

with increasing solderability. With increasing solderability, the substrate oxide can be cleaned more readily, hence allowing less opportunity for the flux to be entrapped to form voids.

The quality of the surface finish of PBs such as ImSn, OSP, ENIG, ImAg, also plays an important role. Organic residues on surfaces or inclusions from chemical processes can have a significant influence, but if cleanliness and the quality of surface finishes of components and PBs are well controlled, the effect on voiding should be low.

Component surfaces also have a certain impact on voiding behavior, especially if there are surface defects like cracks or holes within component terminations in combination with underlying organic layers. Passing of wettability testing (e.g. IEC 60068-2-58 IEC 60068-2-69, IEC 61189-5-601, J-STD-002, J-STD-003) is mandatory. But good wettability based on these tests is not necessarily a sufficient indicator for obtaining low void levels. Currently there is no sensitive generic test for components which can predict the tendency to voiding with acceptable accuracy.

Note that some of these parameters are not independent of each other, for example, the reflow profile needs to be adapted to the solder paste flux to control outgassing during the melting phase.

An important aspect to be considered to limit void levels is the solder paste volume. For components with different standoff levels, like gullwing components, the solder volume at the standoff (this can be, for example, the exposed thermal pads for quad flat packages – QFPs) must be sufficient to fill the whole gap defined by the standoff level. Otherwise the solder joint will either not cover the whole wettable area or form large voids. In addition to the total solder paste volume, the geometry of the stencil apertures also plays a role. In general, separating a given total volume of solder paste in smaller printed areas tends to reduce voiding levels.

One additional topic to be considered is the non-uniform behaviour of void formation with different types of components, especially preballed components, area-array components with solder balls, versus standard SMT components like chip capacitors and QFPs. For standard solder joints, higher wetting performance of the solder surfaces generally reduces voiding. This can be explained by a lower chance of flux residues remaining on the PB or termination surfaces during the soldering process, acting as potential void sources. Another case is the voiding for area-array components with solder balls. For such components, higher wetting performance generally results in higher voiding levels. This phenomenon can be explained by a simple model, as shown in Figure 8.

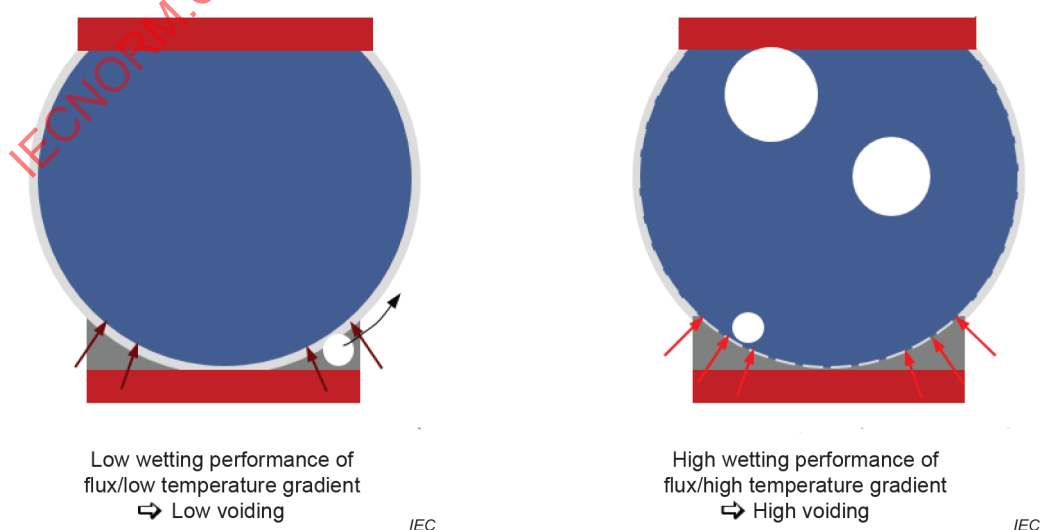


Figure 8 – Theoretical model for voiding behaviour of preballed components

The assumption is that there is some kind of more or less stable “skin” of the BGA ball, which could be an oxidation layer or some phase separation effect at the ball surface. This “skin” is stable during the reflow process until it is penetrated by thermal convection, wetting forces or flux activity. Up to this moment of penetration, all gaseous products forming within the solder paste pass along the ball and will easily leave the solder joint. As soon as the skin is cracked, a significant share of rising gases can enter the ball and voids are captured within. The cracking is accelerated by a higher temperature gradient or higher wetting performance resulting in a higher final void content of the solder joint.

Since this behaviour of preballled components is different from standard SMT components, a general void reduction strategy for panels with mixed component spectrum is limited. In these cases, void reduction for one component can increase void level for others. A reasonable compromise for the whole assembly needs to be sought.

Similarly, a higher peak temperature typically results in higher voiding levels for preballled components, whereas the opposite trend is generally found for other SMT components such as QFPs.

An additional factor for void formation of area-array components is the use of high density interconnect PB technology. In case of microvia in pad designs, so-called design induced voiding can occur.

All these findings show that voiding can be reduced to a certain level, but not reduced to zero with standard convection reflow processes. But if material and process parameters can be kept stable, the variation of average void level can also be kept under control, since the sensitivity of void level to process parameters was found to not be very high.

When voiding levels in solder joints are analyzed, it turns out that typically a rather wider scatter of voiding levels are observed, even for the same joints (i.e. joints at the same layout positions) investigated on a set of printed board assemblies of a certain type. This can be understood as follows: online X-ray analysis during reflow processes has shown that void formation during reflow is a quite dynamic process. Voids are generated, grow and, upon reaching a certain critical size where the voids touch the outer surface of a solder joint, they escape from the solder joint. A few seconds later new voids are forming, often at the same location from flux residues not visible in X-ray inspection. This process can be observed using online X-ray analysis like the images of open solder pads in Figure 9. Thus, the void level in a solder joint during the melting phase of a reflow process can look like an irregular saw-tooth cycle.

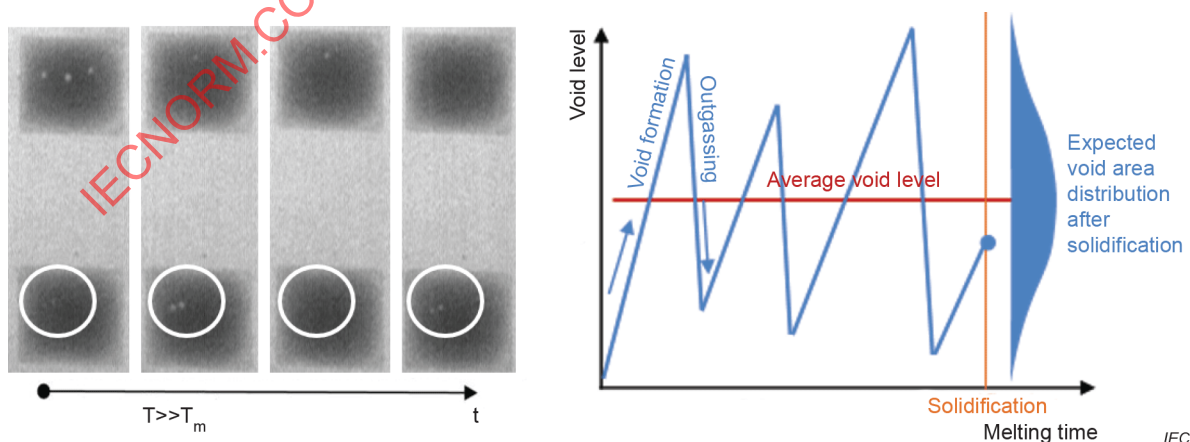


Figure 9 – Online X-ray images and trend of void level during melting phase

For the final state of solder joints, this mechanism implies that the overall average void level can be quite stable, but the void level distribution between different solder joints can exhibit considerable scatter.

4.3 Influence of voiding on solder joint performance

4.3.1 Introductory remarks

Most voiding concerns concentrate on reliability issues related to the thermomechanical, mechanical, thermal and electrical performance of solder joints. The reliability assessment is difficult since solder-joint reliability is a highly complex and multi-faceted topic. Specific types of voids can reduce the lifetime of solder joints under certain loads, thus having a detrimental effect on the reliability of components and therefore products (as shown below). In the context of solder joint reliability, many parameters like materials, surfaces and process parameters, including voiding, influence solder joint formation as well as solder joint reliability. As solder joint reliability is the primary target and void formation is only a problem if it reduces reliability of the assembly, void reduction only makes sense in case it leads to increased reliability.

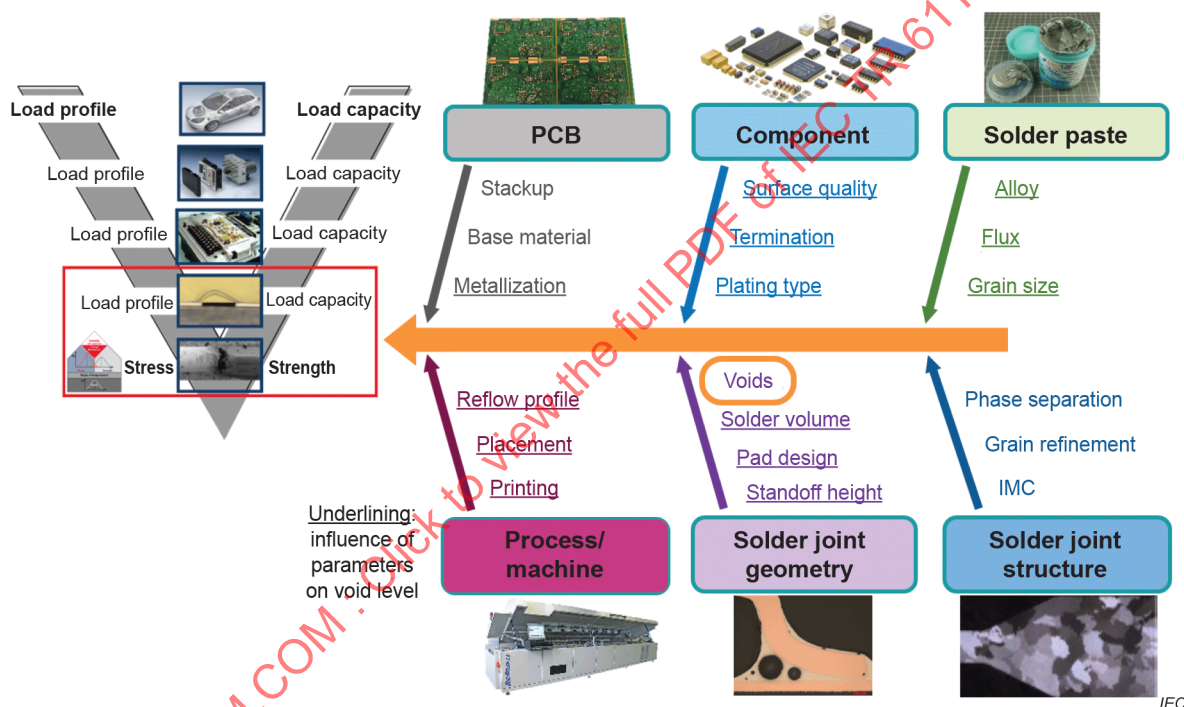


Figure 10 – Principal influencing parameters affecting solder joint reliability

Figure 10 demonstrates the complexity of the subject. On the left side, the principle of reliability is illustrated. Stress profiles and strengths of design elements have to be adjusted to each other, not only on the product level, but likewise also on more detailed levels like the PB, electrical component, solder joint and grain structure. For all practical cases, load levels should be lower than load capacities of design elements, even respecting statistical distributions.

The strength of solder joints on the right side is influenced by many parameters like PB materials and build-up, component materials and quality, solder paste, process and machine parameters, general and individual solder joint geometry and solder joint microstructure. Voiding is only one parameter out of the solder joint geometry parameters. Voiding is influenced by many other parameters like solder paste or component termination, as explained previously. The main parameters influencing void level are underlined in this Figure 10.

It is important to understand that the overall assembly reliability is also a multi-faceted topic: An assembly has to demonstrate satisfactory performance under all relevant internal and environmental loads. As an example, an optimization focusing exclusively on voiding levels in solder joints can result in the use of a solder flux generating residues which are detrimental for the electrochemical reliability of the assembly at elevated temperature and humidity. In such a complex system, a reduction of voiding does not generally enhance the overall assembly reliability. An optimization of voiding levels alone does not necessarily assure the best overall assembly reliability, which should be the main target. Nevertheless, reduction of voiding levels in solder joints is generally aspired to, providing there is no detrimental effect on the reliability of the overall assembly from the actions needed to reduce the voiding.

4.3.2 Thermomechanical reliability

Since voiding affects the solder joint geometry and microstructure, and interacts with crack propagation, it also has an impact on thermomechanical solder joint reliability. For most types of solder joints, preferred crack paths during temperature cycling of boards can be identified. Especially if voids are positioned within these critical paths, the stability against cracking can be reduced as specific types of voids can accelerate the crack propagation and weaken the solder joint stability. This highlights that in addition to its size, the location of a void can have a pronounced effect on its effect on reliability. On the other hand, voids can increase the flexibility of solder joints and improve reliability, at least locally, for certain solder-joint geometries, e.g. for BGA solder joints. The overall effect on solder joint reliability is difficult to assess, especially for components with multiple solder joints like BGAs or QFPs. For these components interactions between the solder joints also have to be taken into account. For example, voids in one solder joint can increase flexibility of that joint but can also partially transfer stress to neighboring solder joints.

The effect of voids on solder joint reliability has been studied by FEM simulation in various investigations, mainly for BGA components. Positive as well as negative effects of voids on solder joint reliability, mainly depending on size and positions of voids within the ball, have been reported. But most of them try to identify a direct correlation between void rate and crack behavior within single balls. Only few examine the interactions between different solder joints. Simulations are mainly facing two limitations:

- a suitable model for crack propagation within solder joints or BGA balls is missing, which would be required to judge the exact influence of voids on this crack propagation process;
- the accuracy of stress level comparison between balls with different geometry (here void content) is very limited with available simulations models.

Since voiding effect on thermomechanical reliability is difficult to assess only by theoretical simulations, some experimental evaluations have been done and reported in literature.

Independent of the limitations discussed above, the two main conclusions that can be obtained from literature (Hillman *et al.* 2011, Holle *et al.* 2018) for BGA voiding are:

- the effect of < 30 % void level is generally rated as insignificant for area-array components;
- the effect of voids on solder joint reliability is strongly depending on the location of the voids, i.e. their relative positions with respect to a potential crack path.

Due to the great amount of effort that is involved in these investigations, they are concentrated on the components that are seen as the most critical concerning both thermomechanical reliability and void level. General experience shows that three groups of components can be selected as the most challenging:

- BGA
- Chip components (resistors or capacitors)
- Bottom-terminated components like QFNs (quad-flat no lead packages), SON (small-outline no lead), etc.

For these groups, some experimental evaluations can be reported in addition to theoretical studies. In one study (Holle *et al.* 2018) the TC lifetime of BGA416 (pitch 1,0) with normal and intentionally increased voiding has been compared. Lifetime in this study is the time until electrical failure during online measurement with temperature cycling between $-40\text{ }^{\circ}\text{C}$ and $+125\text{ }^{\circ}\text{C}$ (see Figure 11).

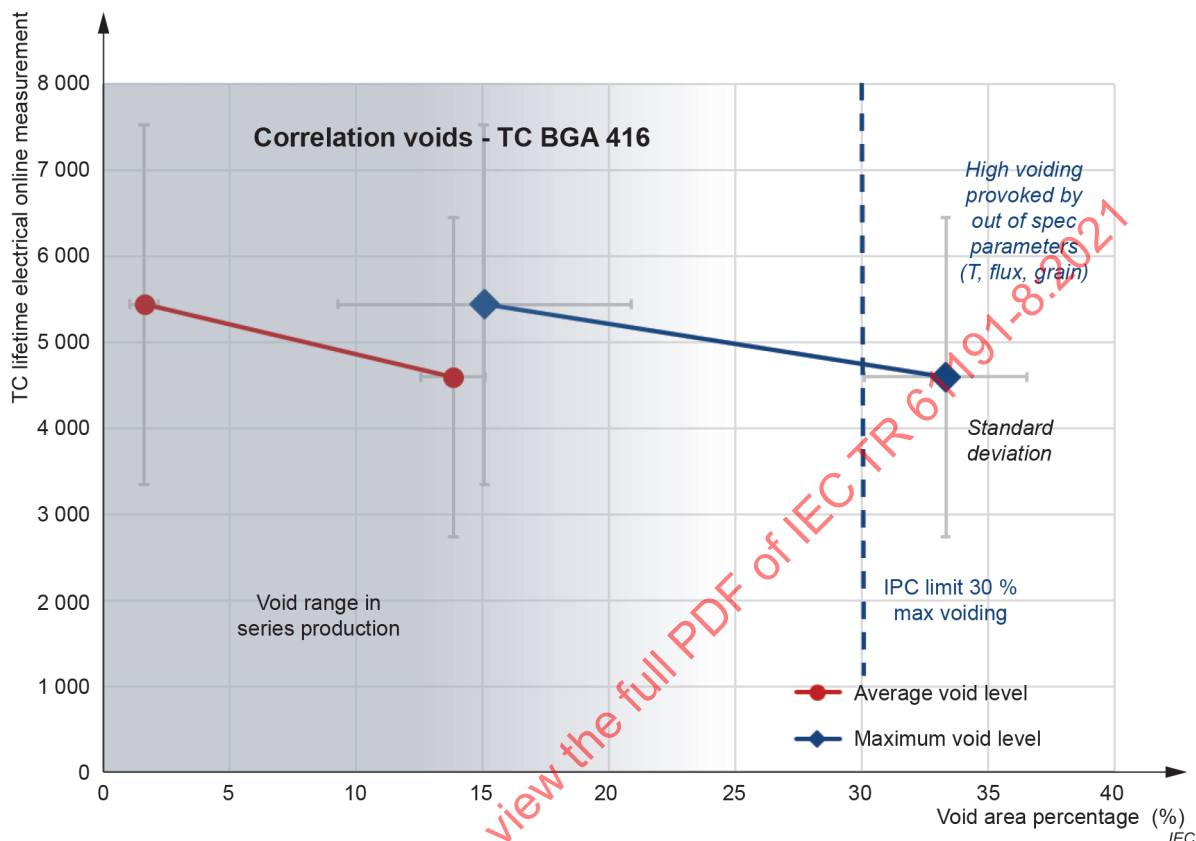


Figure 11 – Correlation of BGA lifetime with average and maximum void levels

These results confirm the conclusion of theoretical studies that maximum voiding, even exceeding 30 %, is not significantly affecting reliability. This result also confirms the current limit for BGA voiding adopted in different standards (see, for example, IPC-A-610, J-STD-001, IEC 61191-2). The second important finding from this investigation is the high variation of lifetime values independent of maximum void level. This effect is confirming the general remark at the beginning of this chapter that voiding is only one effect, maybe only a minor one, on solder joint reliability. To some extent the reason for this variation might also be that detailed void positions are not taken into account with this integral consideration, but this direct correlation between void position and reliability of a component is almost not possible on an experimental level due to the high complexity of interactions.

For the other two component types there are only a few investigations reported in literature. One result from the same study shows the shear force performance of soft terminated 1206 chip resistor solder joints after different levels of temperature cycling $-40\text{ }^{\circ}\text{C}/+125\text{ }^{\circ}\text{C}$ (see Figure 12, Holle *et al.* 2018). For the components in this study, the void level within the standoff area was highly variable due to a component specific termination outgassing issue.

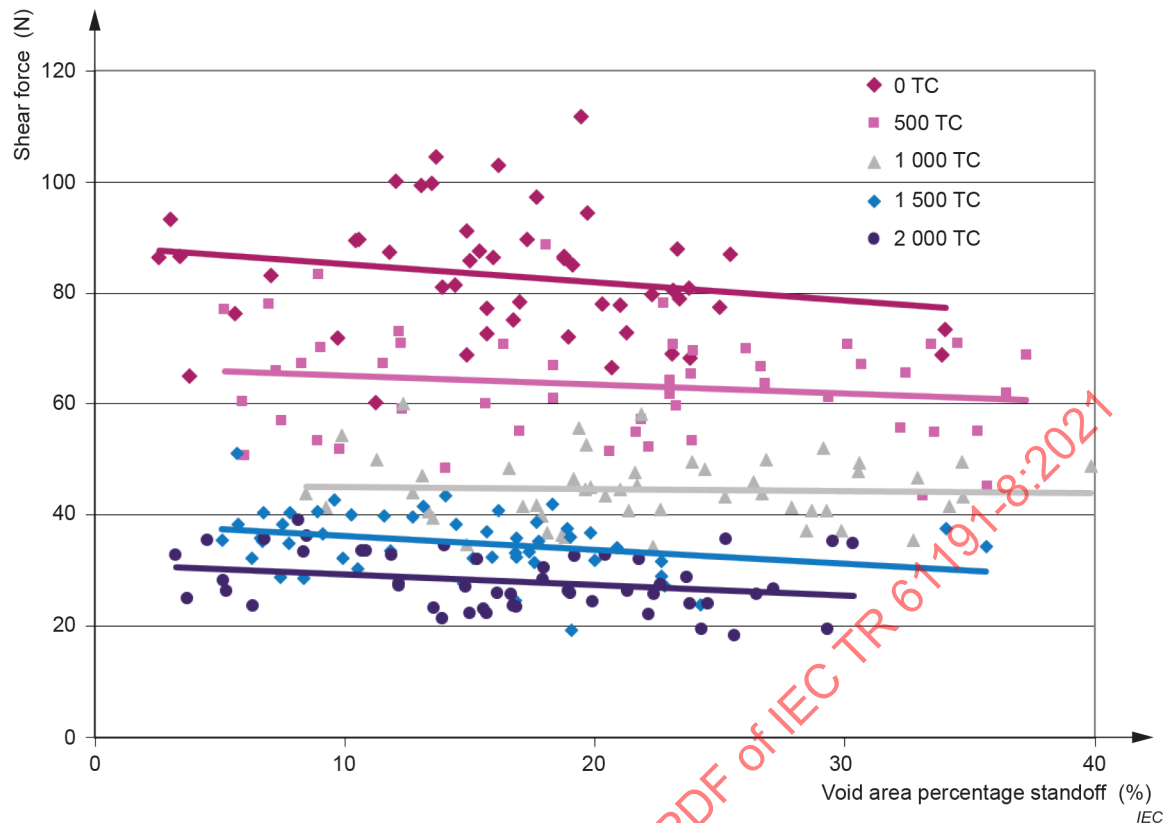


Figure 12 – Correlation void level standoff chip resistor 1206 and shear force after TC

This evaluation shows that independent of TC level, the shear force is almost not affected by void level. The conclusion from this result is that the void level does not affect thermomechanical lifetime performance significantly up to about 35 % void level in the standoff area. This result is primarily valid for voids in the standoff area due to a different cracking behavior of the meniscus. But in most cases, especially for standard SnAgCu solder alloys, the void rate within the meniscus is normally rather low.

For bottom terminated components (BTC) currently only very limited data is available but investigations within different institutions are ongoing. Thus, additional results can be added later. A very rigorous recent study focused on how board design (i.e. vias) affect the formation of voids and whether the presence of voids in the thermal pad impacts the solder joint reliability of the signal interconnect. For the tested components, this study concluded that the magnitude of voiding at the thermal pad does not affect the reliability (Hillman *et al.*, 2019).

As an overall conclusion for the effect of voiding on thermomechanical reliability, voiding can have a negative influence on TC reliability if certain threshold levels are exceeded. Those thresholds are depending on component type. Below such thresholds, the thermomechanical reliability is largely independent of the voiding level.

4.3.3 Mechanical reliability

Influence of voids on mechanical solder joint reliability under vibration, drop, or shock load is not investigated very deeply. Thus, at this place only general assessments based on long term field experience can be reported: Based on field experience, mechanical loads are not generally expected to result in failures related to voiding in solder joints.

For chip components, at least up to 1206 size and also multi-pin components, there is no negative effect of voiding seen, because these components are not critical concerning mechanical load. Some potential risks are seen for 2 groups of components:

- heavy components (electrolytic capacitors, SMD coils, chokes, shunts, etc.) with small pin count (< 4). In these cases, voids could be relevant for shock/drop reliability due to high shear force load during mechanical impact;
- area-array components with low standoff and a high number of solder joints like LGA $> 2 \times 2$ cm and castellated modules. For these cases, bending induced failures could be relevant with voids playing a role.

Due to limited experience and knowledge about void influence on drop, shock, and vibration performance, deeper investigations are recommended, but only in case of exceptionally high requirements concerning mechanical loads.

4.3.4 Thermal functionality

Another concern, in the context of voiding, is a potential heat transfer reduction for large thermal pads, referred to as exposed pads. Within these large area solder joints, void content is normally significantly higher than in small standard I/O solder joints. The voiding in such solder joints reduces the area with a connection between the exposed pad of the components and the PB land (called "soldered area"). A relative percentage of soldered area can be calculated by taking the ratio of the area with a vertically continuous solder connection between exposed pad and PB land with respect to the total wettable area (i.e. area where the exposed pad of the component is overlapping with open Cu on the PB). This ratio is also called solder coverage.

The range that can usually be found with standard production parameters is between 90 % and 50 %, sometimes down to approximately 40 % solder coverage. The influence of the reduction in soldered area on overall thermal resistivity can be calculated.

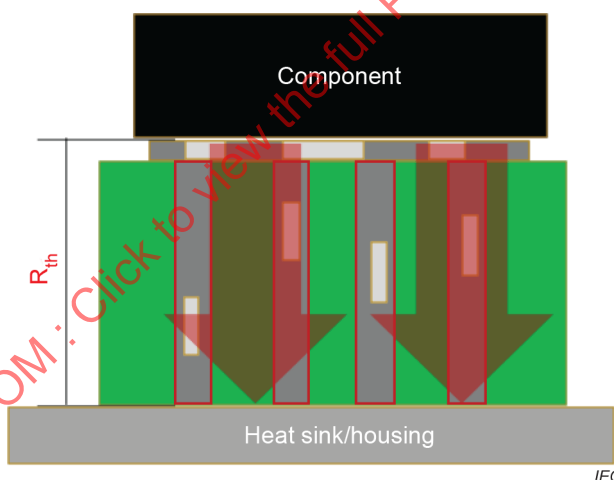


Figure 13 – Sketch of heat transfer with exposed pad solder joints

A sketch of the simplified model behind this calculation is shown in Figure 13. The overall heat resistivity between component surface and heat sink or housing surface on the other PB side is calculated for the whole exposed pad area.

For the model illustrated in Figure 13, the influence of voiding on vertical thermal resistivity of solder joint plus PB is illustrated in Figure 14. Since via filling can reduce the thermal resistance of the PB and enhance the influence of voids, this effect was also considered.

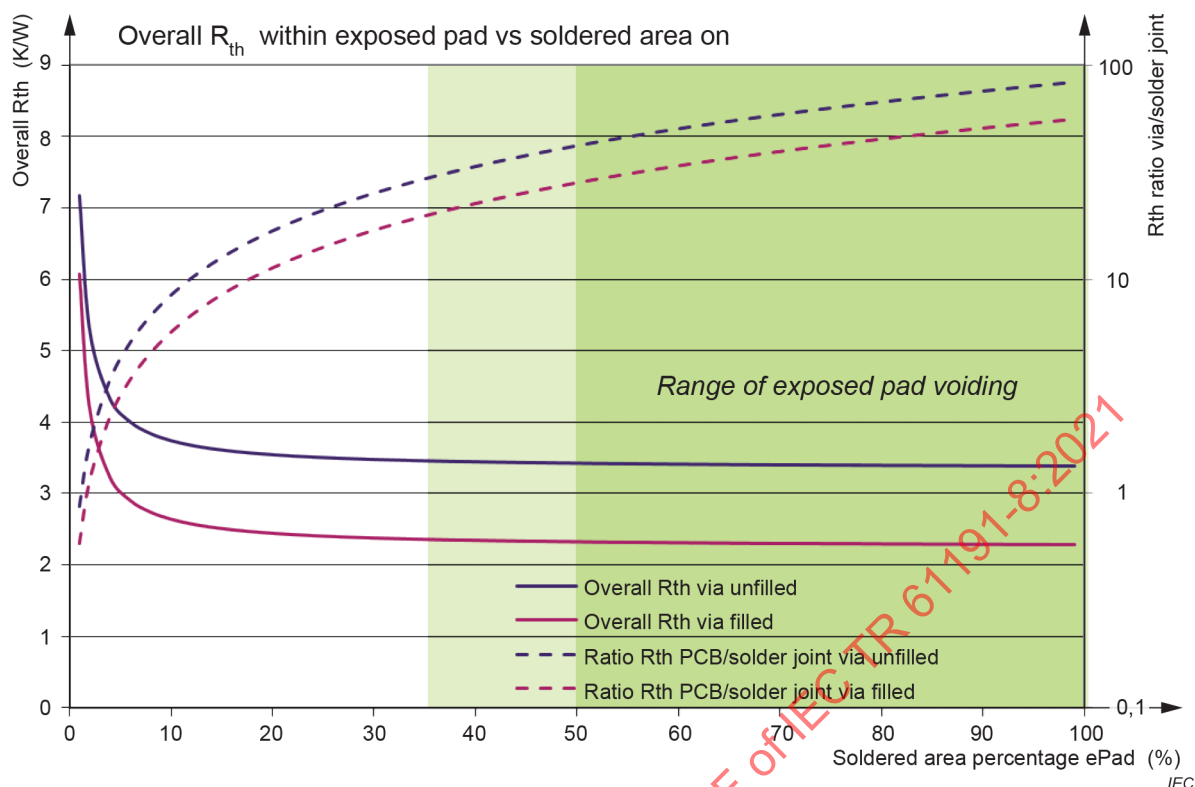


Figure 14 – Calculation of void influence within exposed pads on overall R_{th}

This calculation clearly shows that the solder joints of exposed pads on standard PBs are not sensitive to voiding down to a soldered area of about 20 % or even 10 %. The main bottleneck for heat transfer is the PB with the plated through holes, and not the exposed-pad solder joint, even if a high number of thermal vias is supporting the vertical transfer of heat through the PB. Solder filling of thermal vias also does not change the situation substantially.

The influence of voiding within exposed pads on solder-joint lifetime under thermal cycling was not explicitly investigated, but from field experience, it is known that this kind of solder joint is generally not an issue for reliability providing sufficient thermal transfer is assured.

Thus, at least the normal range of the non-soldered share of the connection area (this includes voiding as well as not completely wetted pads) up to about 65 % does not result in detrimental effects on thermal transfer. This can only be different if the component is soldered directly on to a heat sink (e.g. to a massive copper inlay in the PB). In this case, the PB with the plated through holes is no longer the bottleneck for heat transfer and voids show increased influence on thermal resistivity. For these applications, vacuum soldering is known as an effective method for void reduction.

These considerations are valid for standard conditions and for an overall heat transfer calculation. Special applications with higher heat transfer requirements or dynamic effects, like hot spots within component exposed pad area, can cause additional requirements. Therefore, these results do not claim general validity and a given void level can be acceptable in one application, but not acceptable in another application.

4.3.5 Electrical functionality

Since electrical resistance of solder joints is not critical for most types of components, voiding does not normally affect electrical functionality of components. Exceptions may be high frequency or current applications only. These cases have to be assessed individually.

5 Determination of voiding levels in solder joints

5.1 Instrumentation available for investigation of voiding in solder joints

5.1.1 General

The only non-destructive method for the investigation of voiding in solder joints is X-ray inspection. As some electronic components can be adversely affected by radiation exposure resulting in X-ray doses exceeding component-specific threshold values, component susceptibility should be evaluated and considered prior to X-ray inspection. Suggestions intended to minimize radiation exposure of components are summarized in Appendix D-4 of J-STD-001H.

Two different variants of X-ray inspection equipment (XIE) can be distinguished: 2D XIE and 3D XIE.

5.1.2 X-ray inspection equipment operating in two-dimensional mode

This method involves irradiation of a printed board assembly with an (ideally) point-like X-ray source and recording of the transmitted intensity on an area detector. This can be done under different angles, but for the investigation of voiding the perpendicular (with respect to the plane of the printed board assembly) illumination is usually adopted. Inclined imaging can be employed if solder joints with a principal direction which is normal with respect to the surface of the printed board assembly are investigated (e.g. for through-hole solder joints).

2D XIE has found wide-spread use in electronics manufacturing as a tool to image hidden solder joints. Variants for manual inspection (i.e. an operator inserts printed board assemblies in 2D XIE) and automated inspection (i.e. printed board assemblies are provided for inspection by a conveyor system) exist. The image analysis to determine voiding levels can either be done fully automatically, by using suitable image processing and analysis algorithms, or manually by an operator, by determining areas of voids and solder joints graphically. Semi-automated analysis is also possible, where only certain analysis steps (e.g. contrast enhancement etc.) are done automatically. The automated image analyses still struggle with filtering void geometry out from all other real board information. Repeatable and reproducible results can generally only be achieved with special test boards avoiding disturbing printed board assembly structures or individual adaptation of image evaluation to certain components/positions on a printed board assembly. A general precondition for proper void evaluation is a suitable image magnification that allows for good void recognition. The main challenges are:

- Lack of reference samples for voiding: At present, no reference samples with known void content are commercially available for equipment calibration. Thin metal foils with drilled holes could be taken as a reference, but still this is not the real PB situation since void walls are not vertical in reality and thus detection of the correct void size is much more difficult. As an alternative, a high quality tomography could be chosen as reference if image resolution is significantly higher than for X-ray. The disadvantage of this concept is the high effort and the destructive procedure (high-resolution tomography requires a small sample size, in order to enable a sufficiently high number of projection directions by rotating the sample). Thus, for this issue no satisfying solution has been found.
- Shadowing effects: A projection image of a printed board assembly contains not only contrast variations caused by solder joints and their voids, but all other structure above or below a solder joint, as components on the other PB side, copper structures within the PB (traces on outer and inner layers), buried vias etc. can result in pronounced contrast variations. These contrast variations can affect the results of automated algorithms and can even make a manual voiding assessment difficult. Also, solder joint thickness differences, as the difference in thickness between standoff and meniscus of chip components, disturb the image processing and analysis. This can result in slip, the non-detection of existing voids and pseudo-voiding, i.e. detection of non-existing voids caused by slightly brighter areas within solder joints.

- Influence of equipment settings on voiding results: As every X-ray image taken with a detector has only a limited dynamic range, optimizing illumination and detector sensitivity is crucial for voiding detection. A 'too dark' image tends to underestimate voiding levels, as voids can escape detection and the area of the solder joints are maximized. On the other hand, a 'too bright' image tends to overestimate voiding levels, as areas of voids are maximized, whereas areas of the solder joints can be determined as too small.
- Influence of algorithm settings for void detection on voiding results: Similarly to equipment settings, algorithm settings can have a pronounced effect on the obtained voiding results. In any algorithm, a threshold value will affect the identification of a certain region of a solder joint as a void. As an example, many algorithms rely on binarization of measured images. Such binarization thresholds obviously can have a major influence on the obtained results.
- Definition of reference area: Voiding is usually expressed as a percentage, by taking the area of voids in a given solder joint divided by the area of the solder joint. For many solder joints, the definition of the reference area is not straightforward and generally accepted definitions are lacking. As an example, the area of the solder joint of a chip resistor may or may not include the area of the standoff.

Some of the challenges can be addressed if X-ray inspection systems intended for manual operation are employed. A very thorough procedure is described in IEC 61191-6, which addresses the X-ray investigation of voids in solder joints of ball-grid and land-grid arrays. The method involves recording images of solder joints using two different illuminations, where an image taken with low tube voltage serves to detect the area of the solder joint, whereas an image taken with high tube voltage serves to detect the area of the void.

This approach was found to provide a rather satisfactory result for determining voiding levels, by participants during a round-robin investigation of certain, fixed type, printed board assemblies. However, most image analyses were done manually and variations in shadowing effects were not taken into consideration. The latter can be detrimental for the reproducibility of voiding levels.

5.1.3 X-ray inspection equipment operating in three-dimensional mode

3D XIE aims to obtain three-dimensional absorption-contrast reconstruction based on images or scans of X-ray intensity recorded with different relative orientations of X-ray source, printed board assembly and/or detector. Both so-called tomo-synthesis as well as tomography are employed. Variants for manual inspection (i.e. an operator inserts printed board assemblies in 2D XIE) and automated inspection (i.e. printed board assemblies are provided for inspection by a conveyor system) exist. For the latter, cycle time and equipment costs limited the use of such equipment in mass production. At present, 3D XIE can be used in mass-production assembly lines, but this equipment has not yet found wide-spread use. A major advantage of the three-dimensional reconstruction is that keep-out zones related to the overlapping of all features of printed board assemblies (as bottom- and top-side solder joints, internal component and PB structures) in a 2D image can be largely avoided. The analysis of voiding for 3D XIE is typically algorithm-based, a manual determination of voiding levels is not practical due to the 3D nature of the underlying data. Investigations on the repeatability and reproducibility of 3D XIE-based void inspection are scarce. Of course, difficulties in void analyses related to the lack of reference samples as well as to defining reference areas affect results obtained with 3D XIE as well. Similarly to 2D systems, an influence of algorithm settings for void detection on voiding results will occur.

First results indicate that repeatability and reproducibility for the analysis of voiding is still limited and that these systems are also not totally immune to disturbing effects resulting from shadowing.

5.2 Challenges for the X-ray inspection of voiding: two case studies

5.2.1 Influence of shadowing effects on measuring reproducibility – first results for 3D X-ray inspection equipment

The influence of shadowing effects on measurement reproducibility of voids with real board conditions has been analyzed for a 3D AXI system based on tomographic image reconstruction. Different shadowing situations were realized by adding thin Cu absorber sheets (thickness of 200 μm to 500 μm) to the bottom sides of printed board assemblies with chip components of different case sizes (chip capacitors with case sizes of 0402 and 0805 in inches, chip resistors of case sizes of 0402 and 0805 in inches). In addition, the effects of double-sided assembly and of PB-internal structures were also considered. The results are shown in Figure 15.

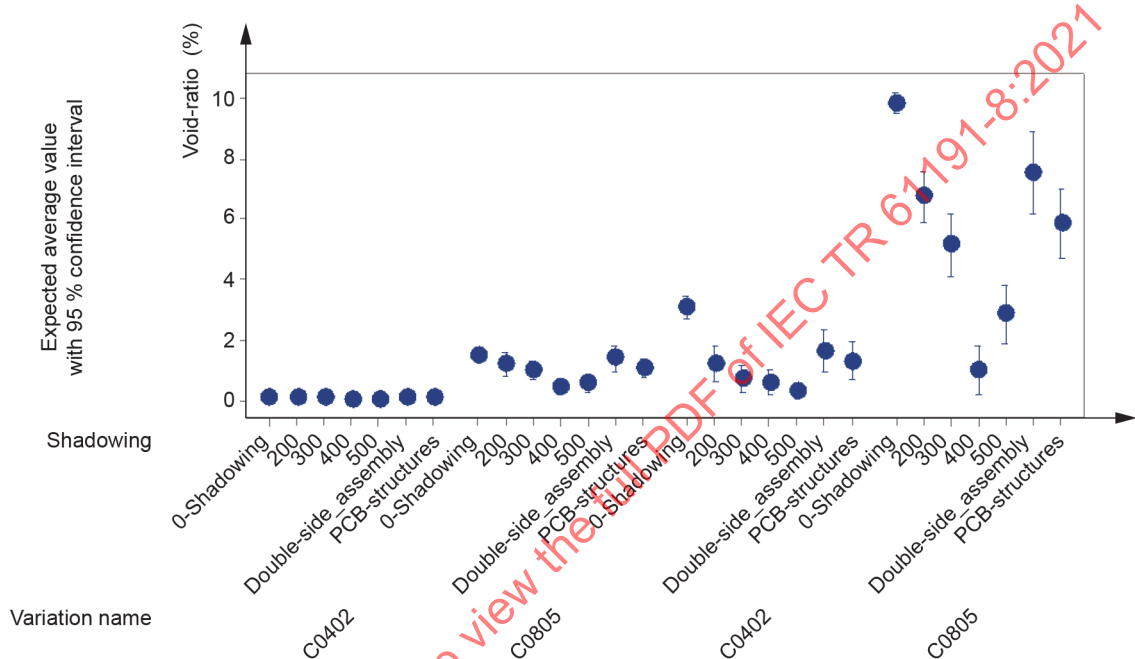


Figure 15 – Average voiding results for different shadowing conditions

NOTE Due to the change of the measurement object by adding additional layers / structures, this analysis is not a standard gauge reproducibility analysis, but it represents the difficulties to reproduce voiding measurements in real mass production under different conditions in a more realistic manner than looking only at exactly the same board. The important point is that not the object itself (i.e. the solder joint) is changed by these realistic modifications, but only the measurability of the object's environment.

The results without shadowing pertain to the repeated investigation of the same solder joints under ideal conditions and represent the intrinsic repeatability of the equipment (see Figure 16). The repeatability is already restricted under ideal shadowing conditions and varies considerably by component type and case size. Already moderate shadowing, as realized by adding absorber sheets of different thickness to the PBs bottom sides, significantly influences the measurement results, i.e. the reproducibility is significantly affected.

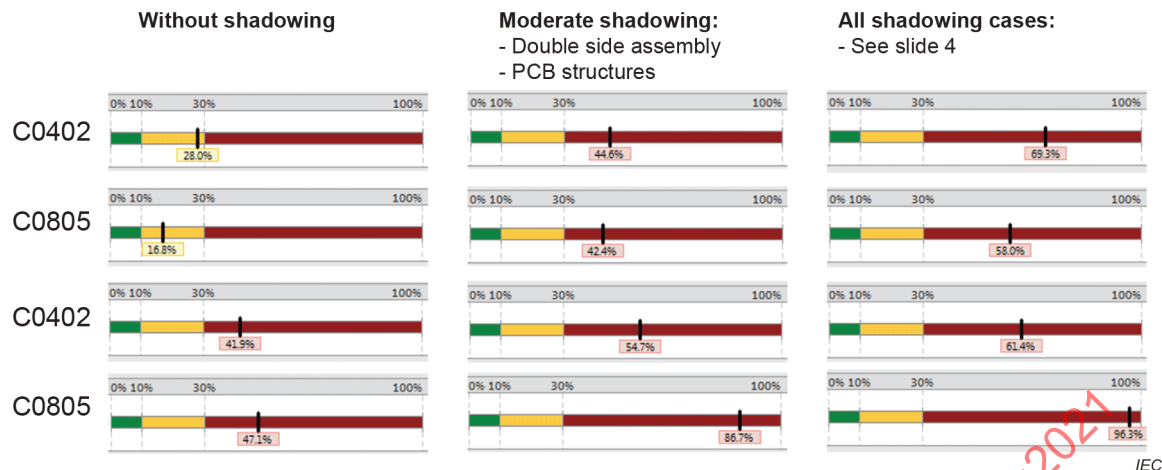


Figure 16 – Gauge reproducibility of void measurement with different shadowing

Especially if all shadowing cases are considered, which represents real product conditions, the gauge R&R (repeatability and reproducibility) value is far beyond an acceptable level. Do note that in this study, only one system has been used. For a full analysis of the reproducibility, different systems would also have to be taken into consideration. These results show that even using 3D XIE, voiding analyses are not sufficiently robust for reliable void measurement.

5.2.2 Influence of X-ray parameters

The second critical aspect is the influence of the X-ray machine settings, especially current and voltage. X-ray settings in mass production are currently not optimized for voiding but more for the detection of general soldering or wetting failures, where the images of solder joints are often too dark for void detection. For acceptable image quality, an optimized image brightness is required. High X-ray voltage or current leads to bright pictures where solder joints are reduced in size compared to reality, but voids are maximized. For low current / voltage, the effect is vice versa. To quantify this effect, an analysis has been made with one BGA region analyzed applying different X-ray parameters. The results are shown as measured void percentage versus $I \times U^2$ (i.e. the product of tube current and the acceleration voltage squared) in Figure 17.

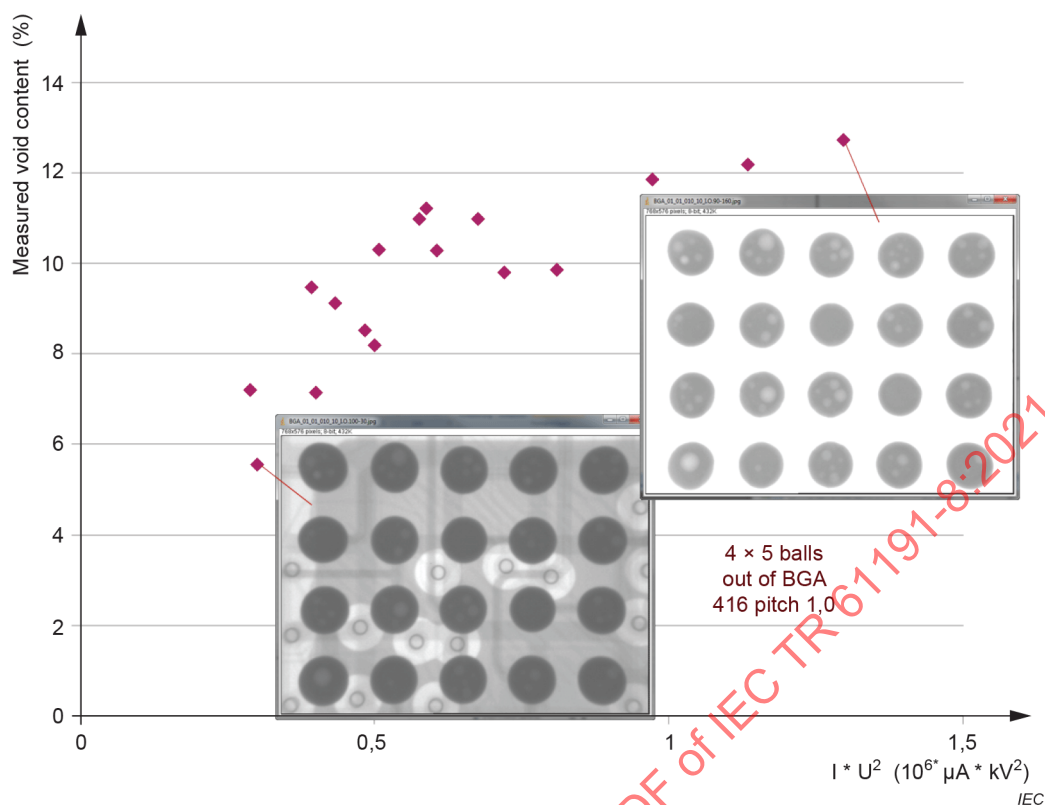


Figure 17 – Void measurement of BGA region with varying X-ray parameters

From this investigation, it can be concluded that there is a high uncertainty in measurement of voids even with identical board conditions, especially if performed on different X-ray machines. There can only be a factor of 2 from X-ray analysis alone without considering the influence of image processing, which can add an uncertainty of similar level. For direct comparison with the same materials, machines, and parameters, the differences are much lower and results can be used for void influence investigations as within this and many other studies. But if X-ray measurement is used for control of void limits in mass production, this low level of measurement capability should be considered, especially since there is currently no reproducible measurement reference available to overcome this drawback. Thus, for further work on void reduction and control, an improvement of X-ray measurement and analysis quality is crucial.

5.2.3 Manual determination of voiding levels in solder joints in sample production

One way to assure high evaluation quality is manual evaluation of void images since humans still can distinguish best between voids and other structures. The lack of reference samples and the missing definition of reference areas is also critical for manual evaluation. Since there is currently no method available with better reproducibility, this procedure is rated as the preferred method for overall confirmation that products show acceptable void levels. This would only be applicable in special cases or with a small number of random samples, as the effort required to conduct this evaluation is very high. The detailed test volume should be defined between user and manufacturer.

To help define suitable methods for void control in series production, a round robin evaluation is currently conducted under DKE (Deutsche Kommission Elektrotechnik – German Electrotechnical Commission) supervision.

6 Recommendations for sample qualification

Since the general influence of material and process parameters on voiding are known, at least qualitatively (see Figure 10), this knowledge should be employed during product and process design to optimize overall assembly reliability with a controlled voiding level. If standard processes are already optimized, stable process conditions and material quality should be strived for.

Voiding levels of samples during different sample stages should be investigated. In particular, initial sample (A- and B-sample) stages enable the early detection of excessive voiding levels and the implementation of measures to reduce voiding to acceptable levels based on Clause A.2. If during this early sample phase, irregularities, i.e. void levels in excess of recommended void levels, are found, the possibilities for void reduction should be evaluated. This can be achieved by implementing measures like adjustments of printing or reflow process and stencil or pad modifications. Only if these measures do not show a significant improvement, a second step could be a proof of sufficient reliability of the particular solder joints with elevated voiding levels through adequate reliability testing covering the potential risks. If this testing can be finalized with a positive result, this increased void level can be established as acceptable for the special product design element under consideration, if agreed between design authority and/or manufacturer and user. The manufacturer and/or the design authority should then provide objective evidence for the acceptability of elevated voiding levels.

Once production-validation samples are built, the voiding levels of selected component types and case sizes should be documented, as a reference for future mass production. To this end, representative component types and case sizes should be selected, so that an overall assessment of the voiding levels for an entire assembly is possible.

Similarity considerations can be applied, to limit the efforts and costs related with voiding analyses. Investigations of voiding levels can also be based on generic test boards, which need to satisfy similarity rules with respect to the product samples under consideration. The manufacturer should provide objective evidence for the validity of any similarity rules applied.

For a statistical assessment of voiding levels, voiding can be treated as an attributive feature. Based on Pearson-Clopper statistics, the ppm-level of solder joints exceeding a given threshold value can be determined based on the number of solder joints investigated and the number of defects (i.e. voiding levels exceeding a given threshold value) detected. In case of zero defects in a given measurement run, this is called a success run.

The required DPMO (defects per million opportunities) level should be as agreed between user and supplier. As a default value, a DPMO level of 10,000 (i.e. 1 %) can be considered acceptable. This DPMO level can be assured with a success run of 300 electronic components (with a confidence level of 95 %). The results should be obtained from different production lots to appropriately cover statistical scatter of the voiding results. Recommended threshold values for acceptability of voiding levels in different types of components are summarized in Clause A.2.

Pearson-Clopper statistics can also be used if no success run occurs. In such cases, the number of components investigated has to be increased to assure compliance with the threshold values (e.g. one failure in about 660 electronic component assures a DPMO level of 10,000 with a confidence level of 95 %).

The required void limit and ppm-level can be confirmed by a lower sample number, if continuous void data and appropriate statistical methods are applied.

7 Recommendations for mass production

7.1 General remarks

A 100 % X-ray control of solder joint voiding is not necessary for product reliability assurance and is technically, as well as economically, not achievable within the near future. Thus, the control of voiding levels in mass production should preferably be assured by establishing robust and stable production processes. The stability of voiding levels can be investigated and controlled by ramp-up quality assurances and, if required, subsequent sample testing. If objective evidence for stable voiding levels and proper process control are available, mass production without X-ray sampling inspection can be pursued, if agreed between user and supplier. In addition, process control of voids can be focused on printed board assemblies for which negative effects on thermomechanical reliability, mechanical reliability, and thermal and/or electrical functionality of a product due to excessive voiding can result.

Typical voiding levels of components and guidelines for acceptability are summarized in Clause A.2.

Similarity considerations can be applied, to limit the efforts and costs related with voiding analyses. The manufacturer should provide objective evidence for any similarity rules applied.

The following 7.2 to 7.4 outline possible scenarios for controlling voiding levels in mass production.

7.2 Ramp-up quality assurance for voiding

A ramp-up quality assurance (RQA) involves tracking of voiding levels over a certain period of time or a certain part count. If particular solder joints are selected for the RQA procedure, some of the difficulties of voiding inspection are avoided: even though it can be impossible to obtain absolute values of voiding, relative changes over time/part count can be tracked with a higher confidence level. An RQA reveals the sensitivity of voiding levels to typical process, materials and component variations occurring in mass production. RQA procedures can involve 100 % inspection of certain solder joints of assemblies (i.e. fixed, selected layout positions) or can be accomplished by sampling with a fixed or flexible frequency. Depending on the results obtained during the RQA phase, it can be decided which procedure is most appropriate during subsequent mass production.

7.3 X-ray sampling inspection

7.3.1 General

When a product has passed product-validation testing with respect to voiding, and if X-ray sampling inspection is required, the manufacturer should implement a documented process control system for characterizing voiding by using X-ray inspection. A documented process control system should define control and corrective action limits and required periodic sample testing.

7.3.2 Control limits

The manufacturer should determine control limits for voiding based on results from product-validation testing and have objective evidence available for review.

7.3.3 Exceeding the control limits

When the control limit, established by the manufacturer, is exceeded:

- 1) X-ray inspection of voiding should be repeated on the sample of the printed board assembly that failed the test.
- 2) If the second test exhibits in-control test results, no manufacturing process action is required, but the X-ray inspection process should be checked.

- 3) If the second test confirms that the control limits have been exceeded, investigation of the root cause of the failure should be performed immediately. The manufacturer should document the disposition process and inform the customer to define the subsequent steps.

7.4 Process control without X-ray sampling inspection

For printed board assemblies featuring well characterized PB surfaces as well as solder materials and components, mass production resulting in stable voiding levels is possible, provided proper process-control measures are in place and objective evidence for compliance with the established thresholds is available. This approach should be adopted based on an agreement between user and manufacturer.

The following process-control measures are mandatory:

- Regular verification of reflow profile: a procedure should be in place to verify periodically that the reflow profile remains within tight limits with respect to the profile that was used for soldering the production-validation samples.
- Documentation and quality controls of relevant parameters for incoming materials and components: relevant parameters (e.g. flux activity) of solder materials should be specified and regularly monitored. This monitoring can be done at sub-suppliers in the framework of a supplier quality management system.

In addition, the following process-control by solder-paste inspection should be considered:

- Solder-paste inspection: solder-paste inspection assures consistent solder-print quality and thus consistent solder volumes. A 100 % 3D inspection of all solder-paste deposits on the assembly should be performed and the results should be within defined control limits and thresholds.

Annex A (informative)

Types of voids and guidelines for acceptability

A.1 Types of voids – Summary

Table A.1 summarizes the different types of voids and provides information on root cause, occurrence in automotive electronic assemblies, detectability, effect on thermomechanical reliability, thermal and electrical function, plus an overall assessment.

Table A.1 – Types of voids with indication of root cause, occurrence in automotive electronic assemblies, detectability, effect on thermomechanical reliability, thermal and electrical function and overall assessment²

Type of voids	Origin / root cause	Occurrence in automotive assemblies	Detectability with in-line automated X-ray inspection	Reliability influence – thermo-mechanical	Influence on thermal / electrical function	Overall assessment
Inclusions / macro voids (type I): typically between 50 µm and 300 µm in diameter, sometimes referred to as 'process' voids	Generated by the evolution of volatiles	Common	Good detectability	No proven reliability impact unless excessive voiding occurs	No impact unless excessive voiding occurs	Common in electronic assemblies, not a concern unless excessive voiding occurs
Design induced voids (type II): typically between 50 µm and a 300 µm in diameter	Generated by gasses entrapped within the microvia, i.e. air, water vapour, flux volatiles	Common for via in pad (microvia) land design	Good detectability	No proven reliability impact unless excessive voiding occurs	No impact unless excessive voiding occurs	Common in electronic assemblies, not a concern unless excessive voiding occurs
Srinkage voids (type III): Elongated, voids with rough, 'dendritic' edges emanating from the surface of the solder joint	Caused by the reduction in solder volume when the solder is in the process of solidification from liquid to solid, related to solidification sequence of lead-free alloys	Common	Poor detectability due to limited size	No impact	No impact	Common in lead-free electronic assemblies, not a concern.

² Adapted from Aspandiar, R., *Voids in Solder Joints*, Presentation made at the SMTAI 2006 Conference.