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High-voltage switchgear and controlgear – Part 306: Guide to IEC 62271-100, IEC 62271-1 and other IEC standards related to alternating current circuit-breakers

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IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

Part 306: Guide to IEC 62271-100, IEC 62271-1 and other IEC standards related to alternating current circuit-breakers

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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DISCLAIMER
This Consolidated version is not an official IEC Standard and has been prepared for user convenience. Only the current versions of the standard and its amendment(s) are to be considered the official documents.

This Consolidated version of IEC TR 62271-306 bears the edition number 1.1. It consists of the first edition (2012-12) [documents 17A/1003A/DTR and 17A/1021/RVC] and its amendment 1 (2018-08) [documents 17A/1161/DTR and 17A/1169/RVDTR]. The technical content is identical to the base edition and its amendment.

In this Redline version, a vertical line in the margin shows where the technical content is modified by amendment 1. Additions are in green text, deletions are in strikethrough red text. A separate Final version with all changes accepted is available in this publication.

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The main task of IEC technical committees is to prepare International Standards. However, a technical committee may propose the publication of a technical report when it has collected data of a different kind from that which is normally published as an International Standard, for example "state of the art".

IEC 62271-306, which is a technical report, has been prepared by subcommittee 17A: High-voltage switchgear and controlgear, of IEC technical committee 17: Switchgear and controlgear.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62271 series, published under the general title *High-voltage switchgear and controlgear*, can be found on the IEC website.

The document follows the structure of IEC 62271-1 and IEC 62271-100. The topics addressed appear in the order they appear in IEC 62271-1 and IEC 62271-100.

The committee has decided that the contents of the base publication and its amendment will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

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INTRODUCTION to the Amendment

At the SC 17A meeting held in Delft (NL) in 2013, the decision was made form a new maintenance team (MT 57) with the task to amend/revise IEC 62271-306. The objective was to update the publication to amendment 2 of IEC 62271-100. Together with MT 34 (IEC 62271-1), MT 36 (IEC 62271-100) and MT 28 (IEC 62271-101) the decision was made to move some of the informative annexes to IEC 62271-306.

This amendment includes the following significant technical changes.

– Annex G of IEC 62271-1:2007 has been included;
– Annexes E, G, H, J, L and Q of IEC 62271-1:2007 have been included;
– I.2 of IEC 62271-100:2008 + A1:2012 has been included;
– Informative parts of Annex O of IEC 62271-100:2008 have been included;
– Former Clause 14 has been added to Clause 13;
– Clause 14 now has heading "Synthetic making and breaking tests". This clause contains annexes A, B, C, D and G of IEC 62271-101;
– Clause 9 has been restructured;
– 16.4 (No-load transformer switching) has been rewritten;
– Annex B has been expanded to include information about fully compensated transmission lines and cables;
– Annex D has been rewritten.

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HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

Part 306: Guide to IEC 62271-100, IEC 62271-1 and other IEC standards related to alternating current circuit-breakers

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1 General

1.1 Scope

This part of IEC 62271 is applicable to a.c. circuit-breakers designed for indoor or outdoor installation and for operation at frequencies of 50 Hz and 60 Hz on systems having voltages above 1 000 V.

NOTE While this technical report mainly addresses circuit-breakers, some clauses (e.g. Clause 5) apply to switchgear and controlgear.

This technical report addresses utility, consultant and industrial engineers who specify and apply high-voltage circuit-breakers, circuit-breaker development engineers, engineers in testing stations, and engineers who participate in standardization. It is intended to provide background information concerning the facts and figures in the standards and provide a basis for specification for high-voltage circuit-breakers. Thus, its scope will cover the explanation, interpretation and application of IEC 62271-100 and IEC 62271-1 as well as related standards and technical reports with respect to high-voltage circuit-breakers.

Rules for circuit-breakers with intentional non-simultaneity between the poles are covered by IEC 62271-302.

This technical report does not cover circuit-breakers intended for use on motive power units of electrical traction equipment; these are covered by the IEC 60077 series.

Generator circuit-breakers installed between generator and step-up transformer are not within the scope of this technical report.

This technical report does not cover self-tripping circuit-breakers with mechanical tripping devices or devices which cannot be made inoperative.

Disconnecting circuit-breakers are covered by IEC 62271-108.

By-pass switches in parallel with line series capacitors and their protective equipment are not within the scope of this technical report. These are covered by IEC 62271-109 and IEC 60143-2.

In addition, special applications (among others parallel switching, delayed current zero crossings) are treated in annexes to this document.

1.2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60060-1:2010, *High-voltage test techniques – Part 1: General definitions and test requirements*

IEC 60071-1:2006, *Insulation co-ordination – Part 1: Definitions, principles and rules*

IEC 60071-2:1996, *Insulation co-ordination – Part 2: Application guide*

IEC 60376, *Specification of technical grade sulfur hexafluoride (SF_6) for use in electrical equipment*

IEC 60480, *Guidelines for the checking and treatment of sulfur hexafluoride (SF_6) taken from electrical equipment and specification for its re-use*

IEC 62146-1, *Grading capacitors for high-voltage alternating current circuit-breakers*[1]

IEC 62271-1:2007, *High-voltage switchgear and controlgear – Part 1: Common specifications*

IEC 62271-4, *High-voltage switchgear and controlgear – Part 4: Handling procedures for sulphur Hexafluoride (SF_6)* [2]

IEC 62271-100:2008, *High-voltage switchgear and controlgear – Part 100: Alternating-current circuit-breakers*
Amendment 1:2012~~3~~
Amendment 2:2017

IEC 62271-101:2012, *High-voltage switchgear and controlgear – Part 101: Synthetic testing*

IEC 62271-102:2001, *High-voltage switchgear and controlgear – Part 102: Alternating current dosconnectors and earthing switches*

IEC 62271-110:2012, *High-voltage switchgear and controlgear – Part 110: Inductive load switching*

IEC 62271-310, *High-voltage switchgear and controlgear – Part 310: Electrical endurance testing for circuit-breakers above a rated voltage of 52 kV*

2 Evolution of IEC standards for high-voltage circuit-breaker

Questions arise frequently concerning the basis and interpretation of standards IEC 62271-100 and IEC 62271-1. In most cases, these questions were due to a lack of background knowledge of the values and requirements laid down in these standards.

A selected number of reference textbooks is listed in the Bibliography. It must be remembered that the technology of high-voltage circuit-breakers is continuously progressing and will continue to do so in the future. Therefore, it is advisable to use such textbooks primarily as a source of information on network behaviour, such as switching conditions, transients, etc., and not for switchgear design.

As the installation of standard equipment in general is more economical than special designs, the application guide will help the utility and industrial engineers in the selection of the appropriate ratings to conform to their needs and specifications. It will enable them to judge which rating is necessary when specifying their circuit-breakers. This should take into account that in future high-voltage networks which will be worked harder and closer to their limits and that high-voltage circuit-breakers of present day technology are designed and procured for a

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1 To be published.

2 To be published.

~~3 To be published.~~

lifetime of several decades. It is recognised that certain conditions may necessitate requirements which are outside the circuit-breaker standards. In such cases, the technical report will help to specify the various ratings or possible additional testing to verify the suitability of the circuit-breaker for a specific application or condition.

Standards should be written fit for purpose, i.e. they should reflect general system requirements to ensure that the installed equipment works properly. Although it is recognised that not 100 % of all conditions occurring in service can be covered, long term experience with high-voltage switchgear standards shows that system conditions are generally covered adequately. Nevertheless, the feedback from service and new developments in equipment and networks must be taken into account in their revision, making standardization an ongoing process. This technical report will be a forum to provide the necessary information concerning the background of changes in the standards.

Technical specification aspects are not generally considered in standards. However, this application guide will address such aspects where appropriate.

As high-voltage transmission and distribution systems and high-voltage circuit-breakers developed it was found necessary to provide standards for circuit-breakers, first on national basis. For example, already in 1923 the first edition of the British Standard B.S.S. No. 116 for circuit-breakers was issued.

In the late 1920s it was recognized that an international agreement should be obtained for a specification for high-voltage circuit-breakers, particularly with respect to their behaviour under short-circuit condition. This lead to the establishment of the "IEC Advisory Committee No. 17" which met for the first time in Stockholm in 1930 and drafted some preliminary recommendations on the international standardization of circuit-breakers.

After a series of specially convened meetings the first IEC Specification No. 56 for Alternating-Current Circuit-Breakers, Chapter I, Rules for Short-Circuit Conditions, was issued in the summer of 1937, with international approval and recognition as a basis upon which to establish national specifications. The first edition of IEC 56 was bilingual and consisted of 55 pages.

Also at that time, already, the need was seen to have Certificates of Ratings issued by approved Testing Authorities to confirm the compliance with Standard Specifications.

The second world war interrupted the further work on the IEC circuit-breaker standards. In 1954 the second edition was published which used and continued the concept of the first edition. It was intended that the IEC Specification No. 56 should ultimately incorporate five chapters which were to be discussed in the following order:

Chapter I	Rules for short-circuit conditions.
	First edition of Publication 56 to be revised and enlarged in a second edition.
Chapter II	Rules for normal-load conditions.
	Part 1 – Rules for temperature-rise.
	Part 2 – Rules for operating conditions.
Chapter III	Rules for strength of Insulation.
Chapter IV	Rules for the selection of circuit-breakers for service.
Chapter V	Rules for the maintenance of circuit-breakers in service.

Actually, the second edition, as the first one, did not progress beyond Chapter I. It was bilingual and had a total of 77 pages. According to its scope it covered a.c. circuit-breakers of 1 000 V and above.

Some major features were:

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– the breaking capacity was expressed in MVA by 2 values, one for a symmetrical and the other for an asymmetrical breaking current;

– the TRV, defined as "restriking voltage", was of single frequency. The amplitude factor or crest value and the TRV frequency or rate-of-rise were not specified but to be evaluated in the tests;

– the first-pole-to-clear factor in general was 1,5. However, in a note allowance was made to use 1,3 for circuit-breakers for earthed systems;

– 50 Hz and 60 Hz were no problem, as for making and breaking tests the tolerance of the frequency was ±25 %;

– the short-circuit current breaking tests consisted of test-duties 1 to 5 with 10 %, 30 %, 60 % and 100 % of the rated symmetrical and the rated asymmetrical breaking current.

Edition 3 was issued in 1971 with a new structure. It applied to high-voltage a.c. circuit-breakers rated above 1 000 V and had six parts which were published as separate booklets:

Publication 56-1:	Part 1: General and definitions.
Publication 56-2:	Part 2: Rating.
Publication 56-3:	Part 3: Design and construction.
Publication 56-4:	Part 4: Type tests and routine tests.
Publication 56-5:	Part 5: Rules for the selection of circuit-breakers for service.
Publication 56-6:	Part 6: Information to be given with enquiries, tenders and orders and rules for transport, erection and maintenance.

IEC 56 consisted of 294 pages when it was issued, but over the years a large number of amendments was added. Out-of-phase was covered by its own publication, IEC 267.

The third edition was the first comprehensive IEC Standard on high-voltage circuit-breakers meeting the originally intended goals. It included, also, the general requirements which are now compiled in IEC 62271-1.

Compared to the second edition a large number of changes were introduced:

– for the first time mechanical tests, tests on insulation properties, tests on auxiliary and control circuits, temperature rise tests, etc., were specified;

– the R 10 series is used for rated normal and breaking currents;

– the TRV (first time to use this term) representation by two or four parameters and the definitions as used up to today are installed;

– for rated voltages up to 100 kV the first-pole to clear factor is 1,5, for 123 kV and above it is alternatively 1,3 or 1,5;

– the supply side rate-of-rise of TRV for 123 kV and above for terminal fault is 1,0 kV/μs for TD 4; 2,0 kV/μs for TD 3 and 5,0 kV/μs for TD 2;

– the short-line fault is introduced. The specified surge impedance is 480 Ω for lines with 1 conductor/phase (52 – 245 kV < 40 kA), 375 Ω for 2 conductors/phase and 330 Ω for 3 or 4 conductors per phase. The line side peak factor is 1,7, 1,6, or 1,5, respectively. The source side rate-of-rise is 0,67 kV/μs;

– test for capacitive current switching (line and cable charging, single capacitors) are prescribed;

– not only type tests, but also routine test procedures are defined.

Edition 4 of IEC 56, published 1987, followed the scheme of the 3rd edition. However, to avoid a duplication of requirements in the various standards for high-voltage switching equipment, IEC 56 was reduced to those requirements that were specific for high-voltage a.c. circuit-breakers. The "common clauses for high-voltage switchgear and controlgear" was published as a separate standard in 1980 with reference number IEC 694.

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Edition 4 of IEC 60056 consisted of one book of 329 pages. To conform with actual service conditions some major changes were incorporated:

– as all systems rated 245 kV and higher are effectively earthed only a first-pole-to-clear factor 1,3 is specified for these voltage levels. For 100 kV to 170 kV alternatives 1,3 and 1,5 are specified;
– based on a large number of network investigations the supply side rate-of-rise of TRV is increased to 2,0 kV/μs for 100 %, 3,0 kV/μs for 60 % and 5,0 kV/μs for 30 % rated breaking current;
– to take into account the clashing of the conductors of a line phase due to the forces of the short-circuit current, which makes it similar to a single conductor, a uniform surge impedance of 450 Ω is specified for all short-line fault tests. The line side peak value is 1,6, the supply side rate-of-rise 2,0 kV/μs;
– the initial Transient Recovery Voltage (ITRV) is introduced for rated voltages of and above 100 kV;
– out-of-phase specifications are included;
– to prove that capacitive current breaking is performed without restrikes the number of tests per duty is increased;
– also, the number of operations during mechanical type tests is increased from 1 000 to 2 000.

And still, IEC 60056 continued to grow. The 4th edition was revised, resulting in the first edition of IEC 62271-100 published in 2001. The first edition of IEC 62271-100 had 575 pages. The structure of the document was retained but its content was revised taking into account service experience and requirements by the utilities:

– classifications of circuit-breaker are introduced with respect to mechanical and (for medium voltage) electrical endurance and restrike behaviour when switching capacitive loads;
– more severe test conditions are prescribed for circuit-breakers to prove a very low probability of restrikes in capacitive current switching;
– for type tests the number of test specimen is limited;
– some test procedures are prescribed in more detail;
– critical current tests and single-phase and double-earth fault tests are treated in particular;
– tolerances are given on practically all test quantities during type tests;
– special cases time constants, longer than 45 ms, are specified for the different levels of rated voltages.

The first edition of IEC 62271-100 was revised and the second edition was published in 2008. The following major changes were made:

– the introduction of harmonised (IEC and IEEE) TRV waveshapes for rated voltages of 100 kV and above (amendment 1 to the first edition);
– the introduction of cable and line systems with their associated TRVs for rated voltages below 100 kV (amendment 2 to the first edition);
– the inclusion of IEC 61633 (Guide for short-circuit and switching tests procedures for metal enclosed and dead tank circuit-breakers) and IEC 62271-308 (Guide for asymmetrical short-circuit breaking test duty T100a).

IEC 60694 covered common matters for equipment falling under the responsibility of subcommittees IEC SC 17A and SC 17C, such as circuit-breakers, disconnectors and earthing switches, switches and their combinations with other equipment, gas-insulated substations, etc. Mainly, these specifications concerned normal and special service conditions, ratings and tests on dielectric withstand, normal and short-circuit current carrying auxiliary and control circuits, and common rules for design and construction. The first edition had 78 pages.

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The experience with this standard on common specifications was very positive. Therefore, when the decision was made to revise IEC 694 this was largely to take into account items which had not been covered by standards, so far. Very little had to be changed or updated in the existing clauses of the first edition. This second edition with title "Common specifications for high-voltage switchgear and controlgear" published in 1996 with reference IEC 60694, has, among others, additional chapters which deal with safety aspects of electrical, mechanical, thermal and operational nature. This had, in particular, consequences for the rules for design and construction as well as tests which now, also, covered topics such as interlocking, position indication, degree of protection by enclosures and tightness. A new and important item that was introduced was electromagnetic compatibility (EMC). Naturally, service and test experiences which had been gathered on the basis of the first edition reflected in the revision. For example, the number of test specimen became limited, the conditions for identification of the test object became more pronounced, and the criteria to pass the test were written in a more exact manner.

The second edition of IEC 60694 was revised and published in 2007 as the first edition of IEC 62271-1.

Manufacturers, users and test laboratories recognize that the reliability of high-voltage switchgear is of crucial importance for the safety and availability of the supply of electric energy. The overall high level of reliability and performance which is common today has its roots in the very good quality of the standards for high-voltage switchgear and controlgear. They are continuously updated to reflect the actual status of the respective technologies.

3 Classification of circuit-breakers

3.1 General

IEC 62271-100 defines the following classes of circuit-breakers:

– Class E1 and E2 of electrical endurance are defined in 3.4.112 and 3.4.113 of IEC 62271-100:2008;
– Class C1 and C2 for capacitive current switching are defined in 3.4.114 and 3.4.115 of IEC 62271-100:2008;
– Class M1 and M2 of mechanical endurance are defined in 3.4.116 and 3.4.117 of IEC 62271-100:2008;
– Class S1 and S2 for specific system application are defined in 3.4.119 and 3.4.120 of IEC 62271-100:2008.

The different classes and their specific applications are discussed in detail in this subclause.

3.2 Electrical endurance class E1 and E2

Two classes are defined for circuit-breakers rated ≤ 52 kV:

– Class E1: basic electrical endurance;
– Class E2: electrical endurance covering the expected operating life of the circuit-breaker.

A circuit-breaker class E1 has a basic electrical endurance, whereas a circuit-breaker of class E2 is designed such as not to require maintenance of the interrupting parts of the main circuit during its expected operating life.

There is no mandatory requirement for electrical endurance for circuit-breakers rated > 52 kV in IEC 62271-100.

Class E2 is defined in IEC 62271-310 for circuit-breakers > 52 kV in the same way as for circuit-breakers ≤ 52 kV. This application is restricted to circuit-breakers used for overhead lines. IEC 62271-310 proposes a unified test procedure for this class E2.

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Class E2 is intended for a low maintenance circuit-breakers used for applications where frequent fault currents are switched.

3.3 Capacitive current switching class C1 and C2

~~Two classes are defined:~~

~~– Class C1: low probability of restrike;~~

~~– Class C2: very low probability of restrike.~~

~~The term "restrike-free" has been deleted from the standard because it did not correspond to a physical reality.~~

~~The standard introduces the term of "restrike probability" during the type tests, corresponding to a certain probability of restrike in service, which, as explained in Annex K of IEC 62271-100:2008, depends on many parameters. For this reason the term cannot be quantified in service.~~

~~The main differences in restrike performances between class C1 and C2 type tests are the number of tests shots and the allowable number of restrikes.~~

~~For class C1 one restrike is permitted on the total number of 48 tests to be performed. If two restrikes occur, the test series has to be repeated permitting only one additional restrike.~~

~~For class C2 the circuit-breaker has to be preconditioned by 3 interruptions at 60 % of the rated short-circuit current. No restrike is permitted on the total number of the required number of tests. If one restrike occurs the test series has to be repeated without any restrike.~~

~~The choice for the user between class C1 and C2 depends on:~~

~~– the service conditions;~~

~~– the operating frequency;~~

~~– the consequences of a restrike to the circuit-breaker or to the system.~~

~~Class C1 is acceptable for medium voltage circuit-breakers and circuit-breakers applied for infrequent switching of transmission lines and cables.~~

~~Class C2 is recommended for capacitor bank circuit-breakers and those used on frequently switched transmission lines and cables.~~

Two classes are defined:

– Class C1: low probability of restrike;
– Class C2: very low probability of restrike.

IEC 60056 contained a definition of the term "restrike-free circuit-breaker". This definition was removed when the capacitive current switching requirements and test procedures were revised. The revised requirements and test procedures were first published in the first edition of IEC 62271-100 (published in 2001). The reason why the term "restrike-free circuit-breaker" was deleted from the standard was because it did not correspond to a physical reality.

The first edition of IEC 62271-100 introduced the term "restrike probability" during the type tests, corresponding to a certain probability of restrike in service, which depends on several parameters (see 9.4.6). For this reason, the term cannot be quantified in service.

The main differences in restrike performance between class C1 and C2 type tests are the number of tests shots and the allowable number of restrikes. Class C2 tests are performed on a pre-conditioned circuit-breaker. Pre-conditioning is done performing 3 breaking operations

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at 60 % of the rated short-circuit current. The pre-conditioning was derived based on CIGRE statistics and is considered to create interrupter wear that is broadly representative of long term service conditions.

The choice for the user between class C1 and C2 depends on:

– the service conditions;
– the operating frequency;
– the consequences of a restrike to the circuit-breaker or to the system.

Class C1 is acceptable for medium-voltage circuit-breakers and circuit-breakers applied for infrequent switching of transmission lines and cables.

Class C2 is recommended for capacitor bank circuit-breakers and those used on frequently switched transmission lines and cables.

The above given conditions are essential when choosing the circuit-breaker for a capacitive switching application, the needed performance class and the voltage factor should be known and demonstrated by the relevant type test. It is important to note that the performance class may vary for different capacitive current switching applications. For example, a circuit-breaker used to switch an overhead line may be tested for class C1 whereas the same circuit-breaker is tested in accordance with class C2 for capacitor bank switching.

3.4 Mechanical endurance class M1 and M2

Two classes are defined:

– Class M1, normal mechanical endurance, a circuit-breaker mechanically type tested for 2 000 operations;
– Class M2, extended mechanical endurance, a circuit-breaker mechanically type tested for 10 000 operations).

As a general rule, the number of operations of high-voltage circuit-breakers switching transmission lines is relatively small, and class M1 is sufficient.

For particular applications, such as frequent switching of reactors, capacitor banks, industrial applications, specification of class M2 is recommended.

It should be noted that it is always possible, in the case of a very special use (pumping station, etc.), to request a larger number of operations than that recommended for class M2.

3.5 Class S1 and S2

3.5.1 General

Two classes are defined:

– Class S1, circuit-breakers intended for use in cable systems;
– Class S2, circuit-breakers intended for use in line systems or in a cable system with direct connection (without cable) to overhead lines.

3.5.2 Cable system

A cable system is a system in which the TRV during breaking of terminal fault at 100 % of short-circuit breaking current does not exceed the two-parameter envelope derived from Table 1 of IEC 62271-100:2008.

NOTE 1 This definition is restricted to systems of rated voltages higher than 1 kV and less than 100 kV.

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NOTE 2 Circuit-breakers of indoor substations with cable connection are generally in cable-systems.

NOTE 3 A circuit-breaker in an outdoor substation is considered to be in a cable-system if the total length of cable (or equivalent length when capacitors are also present) connected on the supply side of the circuit-breaker is at least 100 m. However if in an actual case with an equivalent length of cable shorter than 100 m a calculation can show that the actual TRV is covered by the envelope defined from Table 1 of IEC 62271-100:2008, then this system is considered as a cable system.

NOTE 4 The capacitance of cable-systems on the supply side of circuit-breakers is provided by cables and/or capacitors and/or insulated bus.

3.5.3 Line system

A line system is a system in which the TRV during breaking of terminal fault at 100 % of short-circuit breaking current is covered by the two-parameter envelope derived from Table 2 of IEC 62271-100:2008 and exceeds the two-parameter envelope derived from Table 1 of IEC 62271-100:2008.

NOTE 1 This definition is restricted to systems of rated voltages equal to or higher than 15 kV and less than 100 kV.

NOTE 2 In line-systems, no cable is connected on the supply side of the circuit-breaker, with the possible exception of a total length of cable less than 100 m between the circuit-breaker and the supply transformer(s).

NOTE 3 Systems with overhead lines directly connected to a busbar (without intervening cable connections) are typical examples of line-systems.

3.6 Conclusion

A circuit-breaker is defined by its complete rating, i.e. the basic short-circuit rating and, for example, with or without out-of-phase switching, with or without overhead line capacitive current switching as well as by the endurance classification such as E1, M2, etc.

It is the technical and economic responsibility of the user to select the type of circuit-breaker and its endurance classes according to:

– the technical needs, derived from the point of application and the proposed usage on the user's system;
– the management of the user's circuit-breaker population;
– the user's maintenance policy, which is increasingly linked to the system availability and life cycle costs;
– the cost of the circuit-breakers, with preference for the purchase of standard circuit-breakers.

4 Insulation levels and dielectric tests

4.1 General

Insulation co-ordination is defined as follows (see 3.1 of IEC 60071-1:2006).

insulation co-ordination
selection of the dielectric strength of equipment in relation to the operating voltages and overvoltages which can appear on the system for which the equipment is intended and taking into account the service environment and the characteristics of the available preventing and protective devices

[SOURCE: IEC 60050-604:1987, 604-03-08, modified]

Dealing with insulation co-ordination, it should be kept in mind the difference between "voltage surges" stressing the insulation in service, and "voltage impulses" used in conventional tests.

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TC 28 has classified the different types of overvoltages that can appear in the system and related those to a standardized test voltage. This relationship is given in Table 1 of IEC 60071-1:2006 and is repeated here for convenience (see Table 1).

The current insulating levels for switchgear and controlgear were prepared in 1971 by a joint working group with experts from CIGRE Study Committee A3 and from IEC Subcommittee 17A, when longitudinal and phase-to-phase insulations were not dealt with by the edition of IEC 60071-1 valid at that date. It was considered that the longitudinal insulation might have two very different purposes:

– the working function, that is the separation of two parts of a network;
– the isolating function, to ensure that no voltage is applied on a part of the network where people might be working.

For the isolating function, it was considered that the dielectric withstand of the interrupting gap of a load switch or of a circuit-breaker was not reliable enough, due to its pollution by arc by-products. The isolating function should be provided by a device meeting the requirements of IEC 62271-102 for its expected life.

When an insulation coordination study is made in accordance with the process described in IEC 60071-1, all the electric stresses likely to occur at a given site and with a given probability are taken into account. This is done with respect to the insulation phase-to-earth, phase-to-phase and longitudinal stresses. These are classified according to their front duration whatever their origins. The influence of any voltage protective devices is also considered, see Table 1 of IEC 60071-1:2006. Note that what is called "temporary" overvoltage includes the stresses generated at various frequencies, such as harmonics. The numerous correction factors are applied to each of them to take care of:

– performance criterion: the basis on which the insulation is selected so as to reduce to an economically and operationally acceptable level the probability that the resulting voltage stresses imposed on the equipment will not cause damage to equipment insulation or affect continuity of service;
– statistical distribution: it is normally accepted to disregard those overvoltages which have a probability of occurrence less than 2 %;
– inaccuracy of input;
– effect of the equipment test assembly;
– dispersion in production;
– ageing in service: if not otherwise specified, an ageing factor of 15 % is considered for internal insulation and 5 % for external insulation;
– altitude correction.

To reduce the duration and the costs of the tests, only two types of test voltage shapes are in practical use. These are the power frequency and the standard lightning impulse voltages, for equipment up to and including 245 kV (Range I), and the standard switching and standard lightning impulse voltages, for equipment above 245 kV (Range II). For voltage range I the inherent switching surge strength (in p.u.) is higher than the magnitude of the surges at that voltage. In other words, the amount of insulation that is required to satisfy the lightning impulse and power frequency tests automatically exceed the requirements for the maximum switching surges that can occur on the system. Conversion factors are given in IEC 60071-2 so that "slow-front overvoltages" in range I or short-duration overvoltages of range II be covered by the selected test voltage shapes.

In using this approach, it follows that:

– no overvoltages larger than those used to assess the insulation levels are thought likely to occur on the incoming terminal of a switching device;
– a different probability uncertainty and performance criterion can be applied depending on whether they apply to the working function or to the isolating function. By convention, it

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was decided that the insulation of the "isolating distance" be the closest value to the IEC 60071-1 value but with a 15 % excess over the phase-to-earth insulation;[4]

– although no power frequency tests are required by IEC 60071-1 for range II it can be agreed that product standards may add them when necessary, which is the case with switchgear and controlgear, due to their elaborated design, and because it is a convenient voltage shape for routine tests (IEC 60071-1 deals only with type tests and does not consider the safety aspects).

There are some differences between the insulation levels stated in IEC 60071-1 and those in IEC 62271-1:

– not all of the insulation levels of IEC 60071-1 are taken into IEC 62271-1. This is because the first standard is designed for every type of equipment and some of its values are not used in the latter for switchgear;

– the switching impulse withstand voltage of longitudinal insulating is lower in IEC 62271-1. It should be noted that there are only two cases where longitudinal insulation stress occurs:

  - when a line crosses another line or a busbar;
  - and the case of switchgear and controlgear.

  In the first case, it is easy and economical to use longer clearances; it is more difficult to increase the longitudinal insulation of switchgear and controlgear, and not really necessary, as explained in 4.6. In fact, the insulation levels specified in IEC 62271-1 have been used successfully for more than twenty years (for rated voltages of 800 kV or less), and IEC TC 28, responsible of IEC 60071, agreed that switchgear standards keep their values (see minutes of meeting RM 3606/TC 28).

The splitting into two voltage ranges is done mainly in consideration of neutral earthing systems: in range II, it is considered usual that the neutrals are solidly earthed. Therefore, the voltage stresses are lower. This explains why the same lightning withstand voltage is required for 245 kV and for 300 kV.

Background information on insulation levels and associated testing is provided in 4.6.

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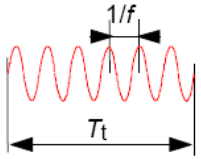
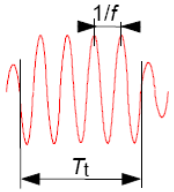
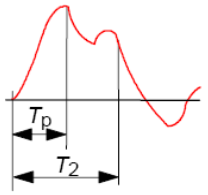
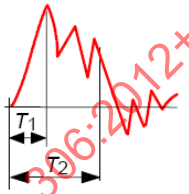
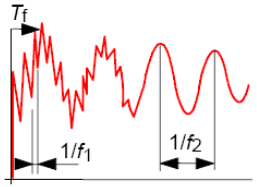
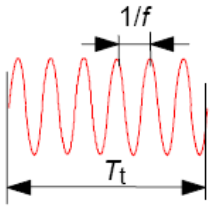
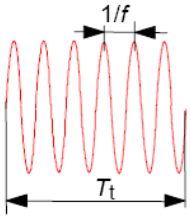
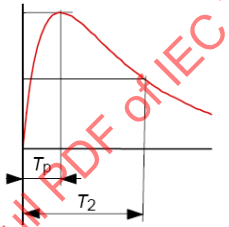
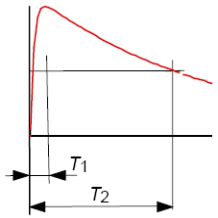
4 Nevertheless, the only safe condition to work on a network is to earth it on each side of the work site.

Table 1 – Classes and shapes of stressing voltages and overvoltages (from IEC 60071-1:2006, Table 1)

Class	Low frequency		Transient		
	Continuous	Temporary	Slow-front	Fast-front	Very-fast front
Voltage or overvoltage shapes					
Range of voltage or overvoltage shapes	f = 50 Hz or 60 Hz $T_t \geq$ 3 600 s	10 Hz < f < 500 Hz 0,02 s ≤ T_t ≤ 3 600 s	20 µs < T_p ≤ 5 000 µs T_2 ≤ 20 ms	0,1 µs < T_1 ≤ 20 µs T_2 ≤ 300 µs	T_f ≤ 100 ns 0,3 MHz < f_1 < 100 MHz 30 kHz < f_2 < 300 kHz
Standard voltage shapes	 f = 50 Hz or 60 Hz T_t [a]	 48 Hz ≤ f ≤ 62 Hz T_t = 60 s	 T_p = 250 µs T_2 = 2 500 µs	 T_1 = 1,2 µs T_2 = 50 µs	[a]
Standard withstand voltage test	[a]	Short-duration power frequency test	Switching impulse test	Lightning impulse test	[a]

[a] To be specified by the relevant apparatus committees.

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4.2 Longitudinal voltage stresses

Normally a circuit-breaker does not have a disconnecting function, this is the duty of the disconnector.

NOTE Circuit-breakers having a disconnecting function are covered by IEC 62271-108.

For its working function, it has firstly to withstand the recovery voltage after having extinguished the arc. In the open position it may be stressed by the power frequency voltage on one terminal with the other stressed by any of the following voltages:

– the D.C voltage resulting from the trapped charge of the overhead line in the case of no-load line or capacitor bank switching;

– power frequency voltage in out-of-phase condition, in the case when busbars or generators are switched;

– a slow-front surge in the case of a switching operation at the remote end;

– a possible fast front surge in the case of a lightning stroke.

The open circuit-breaker is normally isolated by a disconnector and may be stressed only for a short period. That is normally not the case for shunt reactor, capacitor bank, filter and bus tie (busbar) circuit-breakers. For bus tie circuit-breakers the two bus voltages rarely have a large phase shift. Exposed situations where complete out-of-phase voltages will be present for minutes do exist, e.g. in the case of circuit-breakers used for synchronisation purposes, sometimes with a higher component on the generator side.

4.3 High-voltage tests

The standard dealing with high-voltage insulation tests is IEC 60060-1, but the various types and values of dielectric tests are specified in IEC 60071-1, because their statistical meaning is to be taken into account in the process of designing insulation co-ordination. It must be kept in mind that each test voltage shape is a conventional shape to evaluate the behaviour of the insulation when stressed by various voltage stresses, short duration, slow-front or fast front (see Table 1 of IEC 60071-1:2006).

Disruptive discharge voltages are subject to random variations and usually a number of observations must be made in order to obtain a statistically significant value of the withstand voltage. Ideally, the best would be to use a test procedure providing some statistical results. To do that, it is necessary to have an idea of the limit and therefore to have at least one disruptive discharge. But if the test object includes a non-self-restoring part in its insulation system, to reach the limit would mean some destructive effect. In many cases, the insulation is composed of self-restoring parts and of non-self-restoring mixed together. Therefore, several procedures are proposed, supposedly having the same severity, which means that the probability that a "good" specimen is rejected (risk of the manufacturer) is the same as a "bad specimen" being accepted (risk of the user):

– for complete self-restoring insulation (air at atmospheric pressure associated with glass or porcelain), the "up and down" procedure provides the U_{50} value, the critical disruptive level, and an estimate of the standard deviation. It is called "procedure D" in IEC 60060-1:2010;

– for clearly defined non self-restoring insulation, "procedure A" of the same standard assess an assumed withstand voltage (three shots without disruptive discharge);

– for insulation systems composed of mixed self-restoring and non-self-restoring insulation, a compromise was found with procedures B or C, where no disruptive discharges are allowed on the non-self-restoring part of the insulation. Subclause 5.3.4 of IEC 60071-2:1996 shows how procedure B and C give the same probability to pass a test at 90 % of the maximum withstand value. This is with a much better selectivity with procedure B. The question most likely to be raised in the laboratory occurs when the last (or last two) applications of the test voltage leads to disruptive discharges, and whether they are on self-restoring insulation or not. For this reason IEC 62271-1 requires 5 non-

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disruptive discharges to conclude the test. This is aimed at giving confidence that the non-self-restoring insulation is likely to be sound.

Another problem may exist when applying atmospheric correction factors for external insulation in the case that the insulation system of the switchgear and controlgear consists of internal and external insulation in parallel. Subclause 4.3.6 of IEC 60060-1:2010 gives some guidance on how to perform the tests.

The following additional concerns may exist:

– the test voltage across longitudinal insulation or phase-to-phase is higher than the test voltage phase-to-earth. Procedures for those cases are given in 6.2.5.2 of IEC 62271-1:2007;
– three-phase switchgear and controlgear in the same enclosure: test voltages are usually applied between phase and earth, across longitudinal insulation of each pole and phase to phase separately.

4.4 Impulse voltage withstand test procedures

4.4.1 General

The purpose of this subclause is to explain the basis for the several impulse voltage withstand test methods used to verify the insulation integrity of high-voltage switching devices.

In 6.2.5 of IEC 62271-1:2007 the application of the test voltage and test conditions are given. This subclause prescribes several test series, such as testing across the open switching device, to earth, and between phases, as well as tests with power frequency and impulses with positive and negative voltage polarity. Each of these test series has to be considered individually as each of them has to show that the individual insulation under test meets the particular requirements. According to the philosophy of insulation coordination these requirements are based on a flashover probability of 10 %. This should be met by each individual insulation, as well as by the whole switching device. Consequently, adding up all tests performed on the switching device is not justified and does not give any information on the withstand probability of the whole device.

4.4.2 Application to high-voltage switching devices

For impulse tests, the following two procedures are given in 6.2.4 of IEC 62271-1:2007:

– Procedure B of IEC 60060-1:2010: 15 consecutive impulses at the rated lightning or switching impulses at the rated withstand voltage for each test condition and each polarity. The test object is considered to have passed the test if the number of disruptive discharges (flashovers) on the self-restoring part of the insulation does not exceed two for each series of 15 impulses and if no disruptive discharge occurs on non-self-restoring insulation. This method is referred to as the 15/2 method;
– As an alternative, procedure C of IEC 60060-1:2010 may be applied. In this case the test consists of three consecutive impulses for each test condition and each polarity. The test has been passed if no disruptive discharge occurs. If one disruptive discharge (flashover) occurs on the self-restoring part of the insulation, then 9 additional impulses may be applied. If no disruptive discharge occurs during these additional impulses the test object is considered to have passed the test. This test procedure is referred to as the 3/9 method. The 3/9 method is accepted only when all three phases are tested.

The theory on which the test procedures are based is described in 4.4.5.

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4.4.3 Additional criteria to pass the tests

4.4.3.1 Procedure B

Based on the 15/2 method, IEC 62271-100 states additional criteria to pass the tests. If disruptive discharges occur during the application of 15 test impulses it shall be demonstrated that they did not occur on non-self-restoring insulation (SF_6 gas is considered self-restoring). Evidence that damage has not occurred to non-self-restoring insulation can be confirmed by five consecutive impulse withstands following the last disruptive discharge. If permissible disruptive discharges occur within the last five test impulses sufficient additional verification impulses may be applied in order to achieve five consecutive withstands. A disruptive discharge is permissible during the additional verification impulses if only one such discharge occurred during the first 15 test impulses. This procedure leads to a maximum possible number of 25 impulses per series.

4.4.3.2 Procedure C

The original test method required in ANSI/IEEE C37.09 was the so-called 3/3 method. Three test impulses are applied with the following possibilities:

– all three impulses are withstands, then the test is successful and complete;
– if one disruptive discharge occurs, then three further impulses are applied and all must be withstands for the test to be successful;
– if two disruptive discharges occur, the test is a failure.

This method was later modified to the 3/9 method which simply means a disruptive discharge in the application of the first three impulses shall be followed by 9 withstands. The tolerance on the peak voltage is $^{+3}_{0}$ % in accordance with ANSI/IEEE C37.09, whereas it is ±3 % in accordance with IEC 62271-1.

4.4.4 Review and perspective

The statistical sampling plans on which the various test methods discussed above are based are described in 4.4.5.

Subclause 6.2.4 of IEC 62271-1:2007 states that the 15/2 method is the preferred test procedure and further that procedure C of IEC 60060-1:2010 “may be used when all three poles are tested”. Neither of these statements is of the “mandatory” or “advisory” nature that one expects to find in an IEC standard and presents both the manufacturer and user with a choice to be made. The attributes of both test series are shown in Table 2 and will be discussed from two perspectives, namely, insulation coordination and quality assurance.

Table 2 – 15/2 and 3/9 test series attributes

Test series	Probability of passing the test (%)	Risk (%)	
		Manufacturer (α)	User (β)
15/2	76	4,9	29,2
3/9	82	4,6	53,6
NOTE The values in column 2 are based on a flashover probability of 10 %.			

The principles and practices of insulation coordination are described in IEC 60071-1 and IEC 60071-2. In the context of insulation coordination, withstand voltage is defined as the voltage at which there is a 10 % probability of flashover. Figure 1 is derived from the operating characteristics of the two test series shown in Figure 4. The 15/2 test series has a

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76 % probability of passing the test which compares favourably to the 82 % probability for the 3/9 test series. The former test series is thus the more onerous.

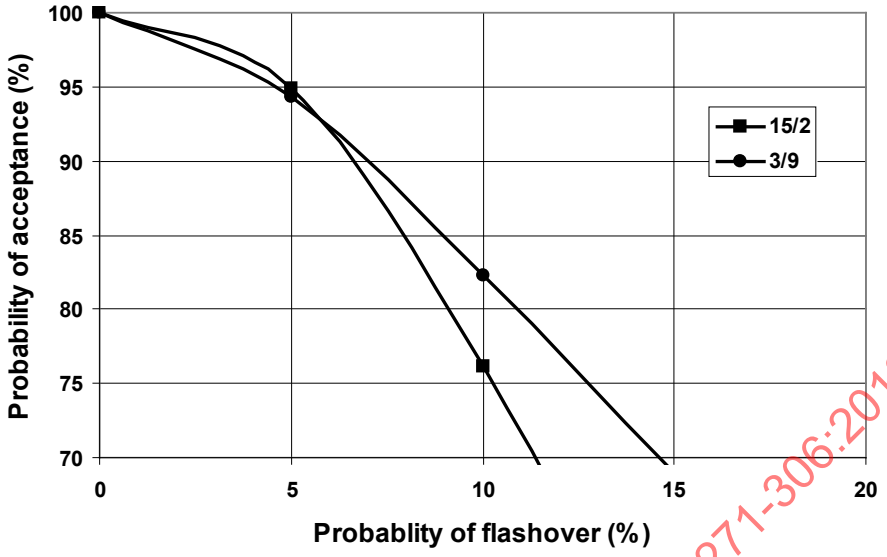

Figure 1 – Probability of acceptance (passing the test) for the 15/2 and 3/9 test series

Taking the quality assurance perspective, it is reasonably argued that a 10 % probability of flashover is too high and that 5 % is a more reasonable and applicable number. Figure 2 shows that the probability of acceptance at 5 % probability of flashover are 94,86 % and 94,7 % for the 15/2 and 3/9 test series, respectively. The corresponding probabilities of rejection are 5,14 % and 5,73 %, respectively, and the argument continues that, on this basis, the two test series are statistically equivalent. However, it is not legitimate to compare two statistical sampling plans at one point only; in fact, equivalent plans would have both similar manufacturer risks at 95 % probability of acceptance (Figure 2) and user risks at 10 % probability of acceptance as shown in Figure 3. With reference to Table 2, the manufacturer risks are near equal but there is a significant difference in the user risks with the 3/9 test series giving the higher risk.

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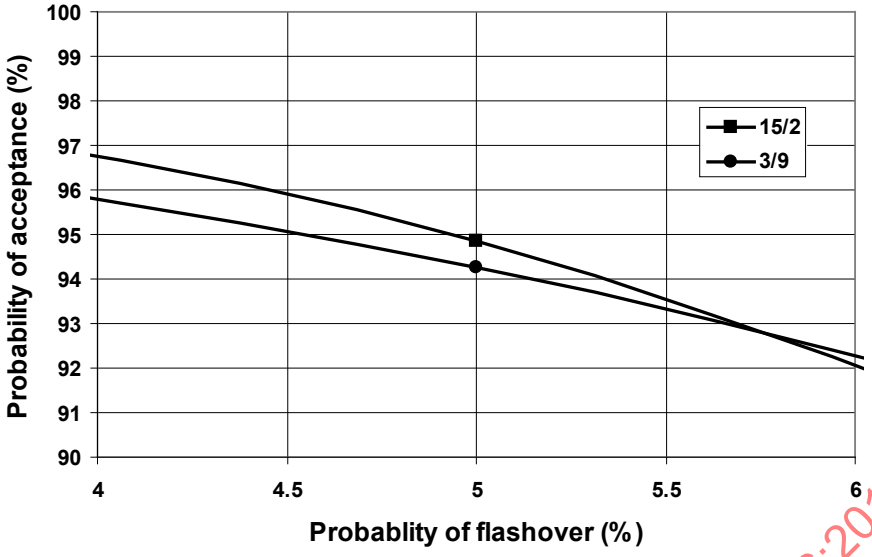

Figure 2 – Probability of acceptance at 5 % probability of flashover for 15/2 and 3/9 test series

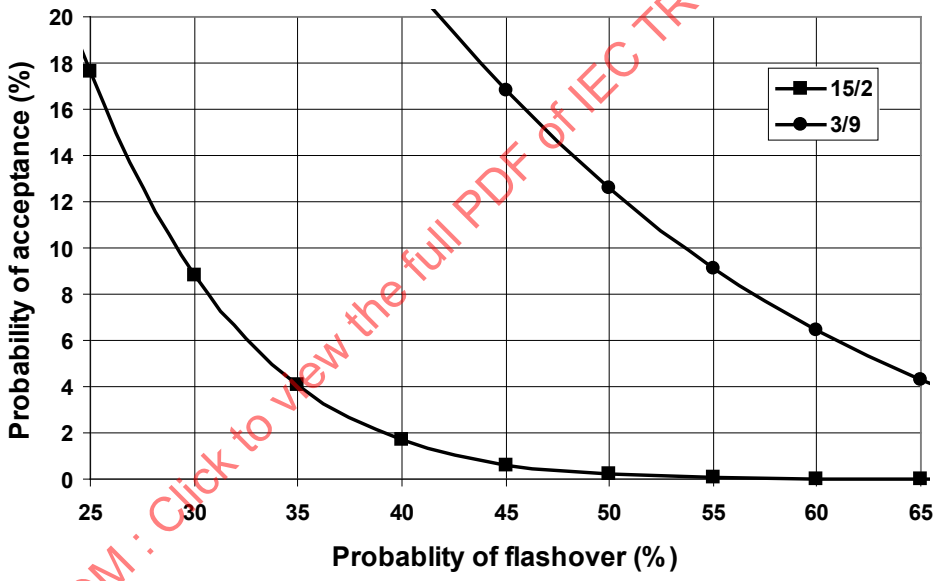

Figure 3 – User risk at 10 % probability of flashover for 15/2 and 3/9 test series

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In reality, the 3/9 test series is used and accepted only in the United States and the 15/2 test series is favoured elsewhere.

The purpose of type testing is to demonstrate that the test object meets the requirements. If it does not pass the test, the reason has to be shown, and exactly what has to be improved or changed in order to justify the repetition of the test. For the new test, a new test object should be submitted which should be an improved device. One should not use the same test object or a second one of the same kind in the expectation of success in a second or third attempt.

4.4.5 Theory

4.4.5.1 General

Originally invented to test insulators, and described in IEC 60060-1, the statistical considerations from which the impulse voltage withstand test procedures were derived actually apply to batches (or lots), i.e. to testing of a relatively large number of samples. Therefore, they are suited in a limited way, only, to prove the quality of individual items, such as switchgear.

Nevertheless, as the procedures have been generally accepted for impulse voltage withstand testing of high-voltage switchgear it may be justified to present their mathematical background.

4.4.5.2 Additive probabilities

According to one axiom of probability the probability function for mutually exclusive events is additive [1] [5]. For example the probability of event A or event B is the sum of their individual respective probabilities providing the two events are mutually exclusive.

4.4.5.3 Special law of multiplication

According to the special law of multiplication the probability that a number of independent events will all occur is the product of their individual respective probabilities [1]. For example the probability of event A and event B is the product of their individual respective probabilities providing the two events are independent.

4.4.5.4 Binomial distribution

The relative merit of the individual plans is analysed by means of the binominal probability distribution and two other relations from probability theory. However, the probability theory has a limited applicability when the number of samples is small or, in the extreme case, when this number is down to one. Yet, this analysis may be useful to understand the background of the test procedures defined in IEC 60060-1 and 6.2.4 of IEC 62271-1:2007 and IEC 62271-100.

Impulse tests are statistically a set of repeated trials. Letting "n" represent the number of trials and "r" the number of test failures, the tests can be analysed using the binominal probability distribution on the basis that the following assumptions apply [1]:

a) There are only two possible outcomes for each trial, "success" or "failure". (Textbooks usually assign the outcome associated with "r" as a success, without inferring that success is necessarily a desirable outcome. In our particular case we are designating the outcome associated with "r" a failure because in the context of dielectric testing a disruptive discharge is a failure.);

b) The probability of failure is constant from trial to trial and is denoted as "p"; the probability of success is thus (1 − p);

c) There are "n" trials, where "n" is a given constant;

d) The "n" trials are independent.

The probability of r failures in n trials for a probability of failure p is given by:

$$b(r, n, p) = \binom{n}{r} p^r (1-p)^{n-r}$$

5 Numbers between square brackets refer to the references in the bibliography.

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where $\binom{n}{r} = \frac{n!}{r!(n-r)!}$

It follows from the axiom described above that the cumulative probability of r or fewer failures in n trials is:

$$B(r, n, p) = \sum_{r=0}^{r} \binom{n}{r} p^r (1-p)^{n-r}$$

$B(r,n,p)$ is the probability of acceptance of the test based on a single sampling plan where a maximum of "r" failures are allowed.

In the case of sampling schemes consisting of more than one sampling plan, the cumulative probability distributions for the respective plans are combined in accordance with the axiom and law described above to yield the probability of acceptance for various values of "p" using that scheme.

P_a will be denoted as the probability of acceptance using a particular sampling scheme.

To illustrate the application of the theory, the 3/9 method is considered. The acceptable outcomes are 3/0 or (3/1 and 9/0):

$$P_a = \binom{3}{0} p^0 (1-p)^{3-0} + \left[\binom{3}{1} p^1 (1-p)^{3-1} \times \binom{9}{0} p^0 (1-p)^{9-0} \right]$$

$$= \frac{3!}{0!(3-0)!}(1-p)^3 + \left[\frac{3!}{1!(3-1)!} p(1-p)^2 \times \frac{9!}{0!(9-0)!}(1-p)^9 \right] = (1-p)^3 + 3p(1-p)^{11}$$

The plot of P_a as a function of "p" is usually called an operating characteristic curve.

An equation and associated operating characteristic curve can be similarly developed for the 15/2 test series [2].

The operating characteristic curves for the 15/2 and 3/9 test series are plotted in Figure 4.

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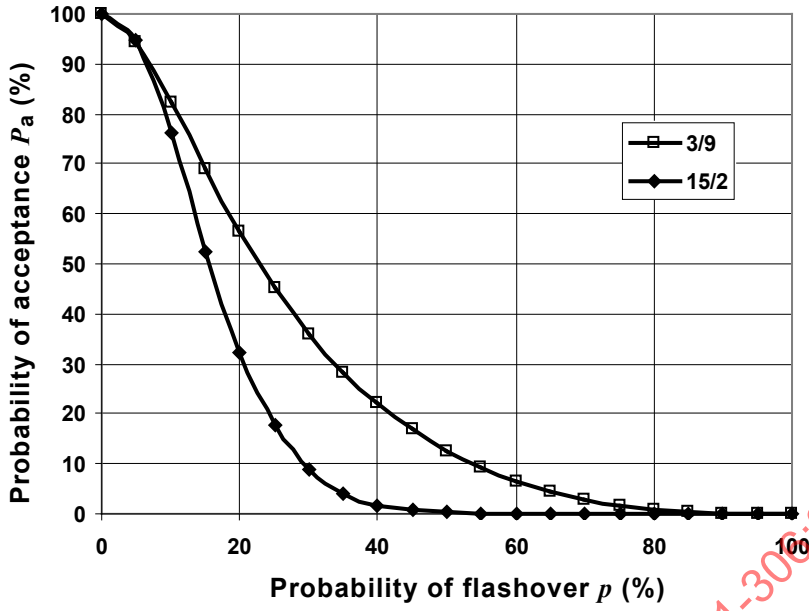

Figure 4 – Operating characteristic curves for 15/2 and 3/9 test series

4.4.5.5 Comparison of the different test methods

4.4.5.5.1 General

The various test methods are actually statistical sampling plans developed to distinguish between "good" and "bad" products out of a larger number of samples, the 15/2 method being a single sampling plan and the 3/9 method being a double sampling plan. The notion of sampling implies risk: the manufacturer's risk is that a "good" product will be rejected (fails the test) and the risk of the user is that a "bad" product will be accepted (passes the test). In reality both risks are mitigated by design safety margins and the ultimate question is which plan gives the best product quality.

To make a comparison between the different methods, two quantities need to be defined (again, it must be remembered that these considerations apply to a large number of samples and not to testing of an individual test object).

4.4.5.5.2 Manufacturer's risk (α risk)

The manufacturer's risk is the probability that a "good" lot will be rejected by the sampling plan. This risk is usually set at 5 % (corresponds to 95 % acceptance) and is stated in conjunction with a numerical definition of "good" quality such as an Acceptable Quality Level (AQL). Ideally the AQL is the value of "p" corresponding to a value of P_a equal to 95 %. The AQL is thus the maximum percent defective that, for the purpose of sampling inspection (testing in this case), can be considered satisfactory as a process average.

4.4.5.5.3 User's risk (β risk)

The user's risk is the probability that a "bad" lot will be accepted by the sampling plan and is stated in conjunction with a numerical definition of "bad" quality such as a Lot Tolerance Percent Defective (LTPD). In quality assurance procedures, when checking and selecting the acceptable samples out of a lot, a user's risk of 10 % is common and LTPD is the lot quality (i.e. value of "p") for which there is a 10 % probability of acceptance, i.e. 10 % of such lots will be accepted.

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The α and β risks for the operating characteristic curves of Figure 4 are shown in Figure 5 and Figure 6 and summarized in 4.4.6.

Another measure for comparison of sampling plans is to consider how well the plans discriminate between "good" and "bad" lots. An ideal plan would discriminate absolutely between the "good" and "bad" lots as is shown in Figure 7 for an AQL of 10 %; all lots to the left of the vertical acceptance line will be accepted and those to the right will be rejected. The closer the actual sampling plan comes to the ideal plan, the better its discrimination.

Readers interested in a more detailed description of statistical sampling are referred to the referenced textbooks on quality control [3, 4, 5].

4.4.6 Summary of 15/2 and 3/9 test methods

The theoretical analysis is summarized in Table 3 and in Figure 5, Figure 6 and Figure 7.

Table 3 – Summary of theoretical analysis

Method	Description	Number of acceptable outcomes	AQL (%)	LTPD (%)	Comments
15/2	As for 15/2M except that one (1) disruptive discharge permissible in the verification impulses if only one such discharge occurred in the basic 15 impulses	38	5	29,2	Addresses the disadvantages of the 15/2 and 15/2M while retaining the principle of maximum two (2) disruptive discharges permissible
3/9	Basic 3 impulses, one (1) disruptive discharge permissible in which event nine (9) further impulses applied with no disruptive discharges permissible	3	4,6	53,5	Used only in the United States

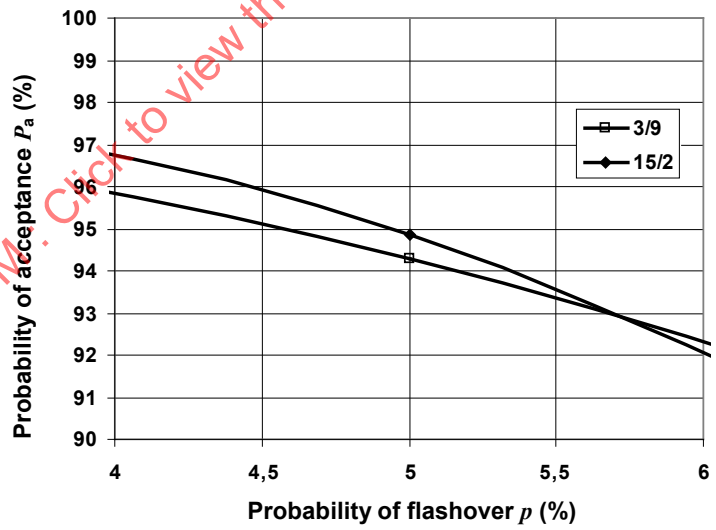

Figure 5 – α risks for 15/2 and 3/9 test methods

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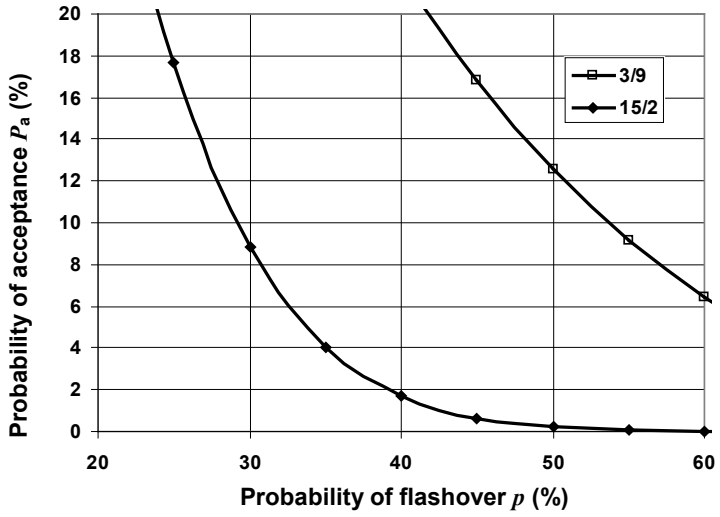

Figure 6 – β risks for 15/2 and 3/9 test methods

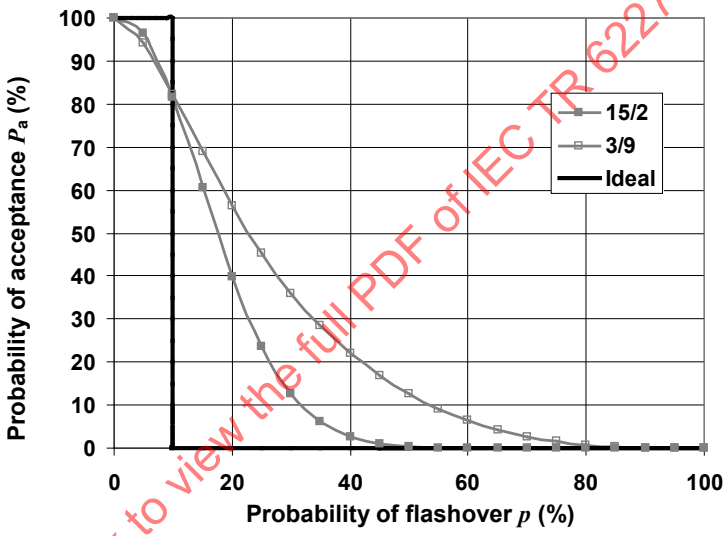

Figure 7 – Ideal sampling plan for AQL of 10 %

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4.4.7 Routine tests

It should be noted that routine tests are detailed in the relevant standards. The power frequency test is used because it is most suitable for factory conditions.

4.5 Correction factors

4.5.1 Altitude correction factor

4.5.1.1 General

In the determination of the required withstand voltages, a number of factors have to be taken into account: the atmospheric correction factor k_{at} and a safety factor k_s. These factors are multipliers to be applied to the insulation level (see 4.5.1.2).

An effect of altitude is the reduction of the atmospheric pressure. A reduced atmospheric pressure reduces the disruptive voltage of a given gap in air. Subclause 4.2.2 of IEC 60071-2:1996 provides equations for derating insulation levels according to the voltage

shape and to the electrode configurations based on measurements made in HV laboratories. The difficulty occurs when it comes to switching surges. So, in IEC 62271-1, it was proposed and accepted to simplify the altitude correction factor as shown in Figure 1 of this standard. In addition, these equations are general for any altitude above sea level. But in the process of assessing insulation level in IEC 60071-1, a correction is already included to cover use up to 1 000 m. As a consequence, the insulation levels stated in IEC 62271-1 are valid up to 1 000 m and, for higher altitudes, the equation for the correction factor is modified accordingly.

The altitude correction is applicable to external insulation only and is incorporated into the atmospheric correction factor, since the air density is a function of the altitude. The dielectric strength is dependent on the air density. The altitude dependence on the atmospheric pressure is given in IEC 60721-2-3 in tabular form. IEC TC 28 (Insulation coordination) has transferred the information given in IEC 60721-2-3 into Equation (1) that deviates by no more than 1 % from the information given in IEC 60721-2-3:

$$\frac{b_0}{b} = e^{H/8150} \tag{1}$$

where

b_0 is the standard barometric pressure, 101,3 kPa (or 1 013 mbar);

b is the pressure at altitude H above sea level (Pa);

H is the altitude above sea level (m).

The air density correction factor is given as (IEC 60060-1):

$$k_d = \delta^m \tag{2}$$

with $\delta = \frac{b}{b_0} \times \frac{273 + t_0}{273 + t}$

where,

k_d is the air density correction factor;

δ is the air density;

t_0 is the standard reference temperature, 20 °C;

t is the actual ambient temperature;

m is an exponent dependent on the minimum discharge path and other attributes. Values of m can be derived from Figure 4 of IEC 60060-1:2010. These values are based on measurements performed at altitudes up to 2 000 m.

The fixed (and conservative) values for m are given for convenience, more detailed values are given in IEC 60071-2. The values are reproduced here from IEC 62271-1 (see Table 4):

Table 4 – Values for *m* for the different voltage waveshapes

m	Power frequency	Switching impulse	Lightning impulse
Phase-to-earth	1	0,75	1
Phase-to-phase	1	1	1
Longitudinal	1	0,9	1

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Combining Equations (1) and (2) and assuming standard reference temperature applies, the following equation is obtained for the altitude correction factor:

$$k_{alt} = e^{m\left(\frac{H}{8\,150}\right)} \quad (3)$$

Subclause 2.2.1 of IEC 62271-1:2007 specifies the following altitude correction factor:

a) altitudes up to and including 1 000 m: $k_{alt} = 1$

b) altitudes higher than 1 000 m: $k_{alt} = e^{m(\frac{H-1\,000}{8\,150})}$ (4)

where

k_{alt} is the altitude correction factor;

H is the altitude in m above sea level;

m is an exponent.

The specification of the altitude correction factor as given in IEC 62271-1 has been based on the following considerations.

The safety factors used are k_s = 1,05 for external insulation and k_s = 1,15 for internal insulation.

Considering the overall correction k_{total} = ($k_{alt} \times k_s$) as a function of the altitude at constant humidity and temperature, assuming m = 1, the following can be determined:

External insulation: at 0 m k_{total} = 1,05 and at 1 000 m k_{total} = 1,19

Internal insulation: k_{total} = 1,15 (independent of altitude)

For a circuit-breaker having internal and external insulation in parallel (which is frequently the case), the overall correction factors are nearly equal at 1 000 m. This means that the safety factor of 1,15 covers the requirements for both internal and external insulation up to an altitude of 1 000 m.

As the safety factor is included in the required withstand voltages, these voltages are valid up to and including 1 000 m.

4.5.1.2 Examples of application of the altitude correction factor

Example 1: A 245 kV circuit-breaker is going to be installed in a substation at an altitude of 1 800 m above sea level. The user specification for the insulation level is 1 050 kV at site level. Which circuit-breaker will fulfil these requirements?

The required insulation level at standard atmospheric conditions (sea level) will be obtained applying the altitude correction factor (Equation (4)) and the following considerations:

– For lightning impulse and power frequency m = 1, hence k_{alt} = 1,103. This means that the circuit-breaker needs to be tested at sea level with a voltage of 1 050 × k_{alt} = 1 158 kV.

– The nearest standardized impulse voltage is 1 175 kV, which belongs to a system voltage of 362 kV.

– The requirement for the power frequency withstand at sea level is 507 kV (dry and wet). Regarding the test to earth this is not fully covered by the requirements for a 362 kV circuit-breaker. However, a 362 kV circuit-breaker has been tested with switching impulse (dry and wet), which gives higher stresses on the external insulation compared to the

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power frequency test, hence one can safely assume that a 362 kV circuit-breaker fulfils the requirements of a 245 kV circuit-breaker used at 1 800 m above sea level.

Conclusion: The 245 kV circuit-breaker fulfilling the requirements for an altitude of 1 800 m will be a circuit-breaker having an insulation level belonging to a system voltage of 362 kV. Application of surge arresters with the intent to lower the insulation level of the substation may result in a more advantageous choice of equipment.

Example 2: A 245 kV circuit-breaker is tested in a testing station that is located at an altitude of 800 m above sea level. What are the correct test values?

Test values and conditions for testing of switchgear and controlgear is referring to standard atmospheric conditions. As the testing station is located at 800 m above sea level, the test values for external insulation need to be corrected to the standard atmospheric conditions. Applying Equation (3) using H = 800 and m = 1 gives k_{alt} = 1,103.

The test values for external insulation in the testing station may be reduced to 1 050/k_{alt} = 952 kV_{peak} for the lightning impulse withstand test and 417 kV r.m.s. for the power frequency test, providing the circuit-breaker has external insulation only. When the circuit-breaker has both internal and external insulation, k_{alt} = 1.

Example 3: The circuit-breaker of Example 2 is tested in the same testing station at an altitude of 800 m for application at an altitude of 1 800 m. What is the correct test voltage?

The testing values at sea level have been derived in Example 1 and are 1 158 kV for the lightning impulse withstand test and 507 kV r.m.s. for the power frequency withstand test.

Application of Equation (3) (calculated in Example 2) to these values give the following result:

– lightning impulse withstand test: 1 050 kV_{peak};
– power frequency withstand test: 460 kV.

Again, this is only valid for the external insulation of the circuit-breaker.

4.5.2 Humidity correction factor

IEC 62271-1 deviates from IEC 60060-1 with respect to the humidity correction factor h to be applied during dry tests of switchgear and controlgear having a rated voltage above 1 kV and up to and including 52 kV.

In fact, the correction factors as defined in IEC 60060-1 do not fully apply to switchgear and controlgear having a rated voltage above 1 kV and up to and including 52 kV in which dielectric stress implies short distances and highly stressed insulating surfaces, and where the location and length of the disruptive discharge are practically impossible to define. The disruptive discharge depends on temperature and humidity as shown in Figure 8:

- in area 3 and 4, the external insulation behaves as an air gap;
- in area 2, due to high absolute moisture content, it is observed that disruptive discharges generally occur along the insulating surface and cannot be considered as if in air. In case of high moisture content with condensation, the weakest point may become the surface instead of the air gap;
- the cases corresponding to area 1 practically do not exist except for the zone near the standard conditions.

In order to avoid varying interpretations and have a practical approach for laboratories, a simplified method to determine w values is preferred to the calculation as given in IEC 60060-1. It was based on the experience of IEC 60694:1981 in which the factor w value equal to 1 had been used for long time by laboratories with satisfactory results especially in

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area 3 of Figure 8 ($h \leq 11$ g/m^3), and on recent results in area 2 ($h > 11$ g/m^3) showing that taking $w = 0$ gives good correlation with experimental data.

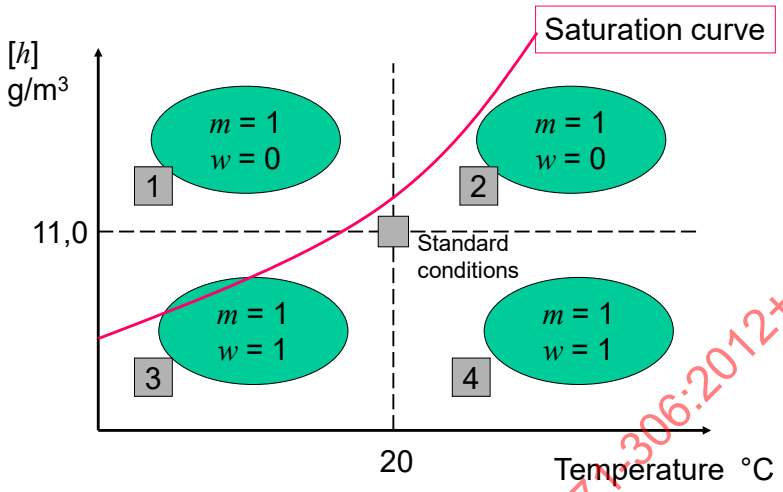

Figure 8 – Disruptive discharge mode of external insulation of switchgear and controlgear having a rated voltage above 1 kV up to and including 52 kV

4.6 Background information about insulation levels and tests

4.6.1 Specification

4.6.1.1 General

The rated insulation levels are mainly based on the requirements of IEC 60071-1. The application guide IEC 60071-2 explains the relationship between the nominal system voltage and the standardized insulation levels. However, these standards are intended to be applied to all types of equipment: insulators, cables, power transformers, etc. Therefore, some related considerations need to be addressed in applying them to high-voltage switchgear and controlgear.

4.6.1.2 Phase-to-earth

The insulation levels have been selected taking into account the values most commonly used for switchgear and controlgear.

In addition to IEC 60071-1, a rated short-duration power-frequency withstand voltage is required for rated voltages higher than 245 kV, in order to verify internal insulation voltage withstand capability with respect to temporary overvoltages.

4.6.1.3 Phase-to-phase

No changes are made to the specifications of IEC 60071-1 for the insulation between poles.

4.6.1.4 Longitudinal insulation

Since no other IEC product standards specify requirements for longitudinal insulation, SC 17A has developed its own set of rated withstand values.

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4.6.1.5 Isolating distance

In addition to the requirements of insulation coordination, the standard specifies insulation of the “isolating distance”. This is to cover special conditions which are to be met by disconnectors to provide an additional safety factor (1,15) (see 5.102 of IEC 62271-102:2001).

The intent of the isolating distance is not to provide fundamental-coordination but to require that any disruptive discharge occurs phase-to-earth on the switching device rather than between its open contacts. Exceptions may occur, for example when high creepage distances to earth are required. However, it is generally recognized that when work has to be carried out on a high-voltage conductor, safety is assured only when the conductor is directly connected to earth. Local safety rules should apply.

4.6.1.6 Combined voltage tests

A combined voltage test is one in which two separate sources, generating voltages against earth, are connected to two terminals of the test object (see Clause 9 of IEC 60060-1:2010 and Tables 2a and 2b of IEC 62271-1:2007).

Such tests are required for switchgear and controlgear of 300 kV and above to demonstrate longitudinal voltage withstand capability. They may also be useful for testing where the test voltage between two live parts is specified to be higher than the phase-to-earth value.

The components of the combined voltage tests have been specified based on the following considerations:

a) Short-duration power-frequency withstand voltage

The specified power-frequency withstand voltage values correspond to the most severe situation of full load rejection after disconnection of a generator at full load. The overvoltage on the generator side of the switching device may reach up to 1,5 times the system voltage and may last up to 3 s with a possible phase shift. At the same time, the network side of the switching device is energized at the normal operating voltage. The sum of the two voltages in out-of-phase condition is 2,5 times the system voltage, extended here to 2,5 the rated voltage.

b) Switching impulse withstand voltage

The switching impulse voltage value specified phase to earth in Column 4 of Table 2 of IEC 62271-1:2007 is designed to cover the highest slow-front overvoltage likely to occur at the switching device terminal. This occurs at the remote end of a line after fast reclosing from the other end on a trapped charge. This highest overvoltage is of the same polarity as the power-frequency voltage of the network at this instant and therefore is not to be used when the maximum stress across a switching device is the consideration. The maximum longitudinal stress takes place when an overvoltage occurs on the polarity opposite to the power-frequency voltage of the system. The maximum value for this case occurs on closing from the remote end and is lower than the value occurring on reclosing. Therefore, the values of switching impulse specified in Column 6 of Table 2 of IEC 62271-1:2007 are lower than those of Column 4 of Table 2 of IEC 62271-1:2007.

c) Lightning impulse

In the process of designing insulation coordination, IEC 60071-1 takes into account the probability of occurrence of a particular event in order to determine the performance criteria. The likelihood that the maximum fast-front overvoltage occurs on the terminal of a switching device at the instant when its opposite terminal is energized with the maximum system voltage at opposite polarity is small. Therefore, the specified lightning impulse to be considered in this particular case need not be as high as for the general case. The reduction of about 5 % of the power frequency voltage that appear in IEC 60694 has been changed in IEC 62271-1 to a tolerance on the total test voltage of $^{+3}_{-0}$ %.

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4.6.2 Testing

4.6.2.1 Test of the longitudinal insulation with the alternative method

To be strictly in compliance with the preferred method, the voltage between the energized terminal and the base frame U_f should be equal to the rated withstand voltage phase to earth. But it is difficult to control this voltage during the test of the longitudinal insulation. The value of U_f has been fixed considering the following facts:

– the test voltage between any terminal and the base frame cannot exceed the rated phase to earth withstand voltage without risk;

– the electric field stress across open contacts is mainly dependent on the voltage across them, and to a lesser extent on the voltage to earth;

– the determination of the rated withstand voltage of the isolating distance is not that accurate;

– a safety factor is included in the process of insulation coordination (see IEC 60071-1) to account for such testing difficulties.

4.6.2.2 Test between phases for rated voltages above 245 kV

4.6.2.2.1 Voltage sharing between the two switching impulse components of the phase-to-phase test

The actual ratio of the two components may have any value in the network. In order to simplify the tests, IEC 60071-1 decided to specify balanced components (same amplitude with opposite polarities). Since this leads to a less severe condition, the total test voltage was increased to cover any realistic case (see Annex A of IEC 60071-2:1996). Therefore, if the same total test voltage is applied by an unbalanced sharing of the components, the test is more difficult than required.

In reality few laboratories have two impulse generators and the peak of a power-frequency voltage may replace one component. However, this leads to power-frequency voltages higher than specified phase-to-earth and for a rather long duration. Therefore, some compromise is necessary depending on the actual phase-to-earth withstand voltage of the switching device and on the facilities of the laboratory.

4.6.2.2.2 Wet tests

No wet switching impulse tests are normally necessary between phases for the following reasons:

– enclosed insulation does not need wet tests;

– insulation between phases exposed to precipitation is atmospheric air only and is not sensitive to this influence for switchgear and controlgear of rated voltage above 245 kV.

4.6.3 Combined voltage tests of longitudinal insulation

4.6.3.1 Tolerance on the power-frequency voltage component

According to IEC 60060-1, the tolerance of the power-frequency component voltage for a test with a duration longer than 1 min should be maintained within ±3 % of the specified level. This allows for some variations from the main voltage without permanent adjustment. During a combined voltage test, however, the laboratory has also to monitor many other parameters from the impulse voltage source. Therefore a higher tolerance is acceptable for the power frequency component with the understanding that the test voltage to be considered is the actual total voltage across the open contacts or the isolating distance. The tolerance on the total voltage is $^{+3}_{-0}$ %.

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4.6.3.2 Atmospheric correction factor

For atmospheric corrections the parameter g (4.3.4.3 of IEC 60060-1:2010) shall be calculated considering combined or composite test voltage value. The parameter $k1$ and k_2 (4.3.4.1 and 4.3.4.2 of IEC 60060-1:2010) shall be calculated for the higher of the two test voltages and be applied to both.

4.7 Lightning impulse withstand considerations of vacuum interrupters

4.7.1 General

The lightning impulse withstand voltage performance of vacuum interrupters has some characteristics that must be considered when testing. The breakdown voltage between the open contacts of a switching device in general depends on two things.

– the gaseous material between the contacts, and
– the contact surfaces.

In cases with high pressure gases at or above the normal atmospheric pressure, the gas exerts a major influence on breakdown in comparison to the contacts. In cases with vacuum gaps the contact surfaces exert the major influence.

Electrical breakdown between the contacts in a gas gap is called avalanche breakdown. The electrons that are accelerated by the electric field between the contacts collide with neutral atoms or molecules and knock off an increasing number of new electrons until a complete breakdown of the gap occurs. A *key* parameter influencing these collisions is the mean free path. The mean free path is the distance between collisions of electrons with neutral atoms or molecules as the electrons are accelerated by the electric field between the contacts. In a gas gap, the mean free path is a very small fraction of a millimetre and hence an even smaller fraction of the contact gap. Hence breakdown between the open contacts of a gas interrupter depends largely on the type of gas and the gas pressure.

In a vacuum gap, the gas pressure is 8 to 10 orders of magnitude less than the normal atmospheric pressure. In contrast, the mean free path in a vacuum gap is 10 or more times greater than the distance between the contacts. Hence breakdown between the open contacts of a vacuum interrupter is determined largely by the condition of the contact surfaces.

4.7.2 Conditioning during vacuum interrupter manufacturing

The procedure used to increase the breakdown voltage of a vacuum gap is called "*conditioning*" or "*seasoning*". Conditioning is of great practical importance to improve the withstand voltage capability and achieve the required lightning impulse withstand voltage performance of vacuum interrupters. At the end of the manufacturing process all vacuum interrupter will go through a conditioning process. The common procedure used by all leading vacuum interrupter manufacturers to condition vacuum interrupters is voltage conditioning where the contacts are blocked in the open position and an a.c.-voltage is applied across the open contact gap. The conditioning voltage level is chosen such that the vacuum interrupter can subsequently be able to pass its rated lightning impulse withstand voltage and can therefore be safely applied at the required voltage rating in circuit-breakers that comply with standards like, e.g., IEC, IEEE.

If the lightning impulse withstand voltage test is done immediately after the seasoning operation when the contacts are still in the blocked open position, the impulse voltage withstand performance is at its best. However, after the contacts are allowed to touch, some microscopic roughness occurs that reduces to a small degree the lightning impulse withstand voltage performance of the interrupter. In addition, mechanical cycling of a switching device once the interrupter is installed can also result in some small reduction of the lightning impulse withstand voltage performance of the interrupter.

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4.7.3 De-conditioning in service

Most common causes for de-conditioning in service are:

- high inrush currents during contact closure, for example during the making of an capacitive current with a high peak inrush current;
- interruption of high short-circuit currents (≥ 10 kA);
- passage of high currents (≥ 10 kA) through closed contacts.

The interruption of many high short-circuit currents often reduces the lightning impulse withstand voltage capability. So over time, the impulse withstand voltage capability of the vacuum interrupter may be reduced below the rated value.

4.7.4 Re-conditioning in service

In contrast, various phenomena can improve the lightning impulse voltage withstand performance, such as one or more breakdowns during impulse voltage testing or arcing between the contacts when breaking current. The interruption of load currents or lower fault currents (< 5 kA) can often re-condition the contacts from the effects of inrush currents or high currents passed through the vacuum interrupter contacts.

4.7.5 Performing lightning impulse withstand voltage tests

NOTE 3 of 6.2.4 of IEC 62271-1:2007 may be applied for the preliminary impulse voltage tests. This note does not specify how many preliminary tests nor how many breakdowns are acceptable.

After the completion of the preliminary impulse voltage tests, the official certification tests at the rated withstand voltage are performed in accordance with 6.2.4 of IEC 62271-100:2008.

5 Rated normal current and temperature rise

5.1 General

This section of the guide also applies to other switchgear and controlgear components of similar basic construction to circuit-breakers and hence it is written making reference to switchgear and controlgear rather than circuit-breakers alone.

5.2 Load current carrying requirements

5.2.1 Rated normal current

The switchgear and controlgear is designed for applications where the load current does not exceed the rated normal current under specific conditions. These conditions are:

– the altitude above sea level for the application is 1 000 m or less;
– the ambient temperature does not exceed 40 °C and the average value, measured over a period of 24 h, does not exceed 35 °C.

NOTE 1 No correction factor is applied for altitudes up to 2 000 m. For altitudes higher than 2 000 m refer to 5.2.2.4.

When choosing the switchgear and controlgear for an application the following parameters should be taken into account:

– the expected maximum load current. The rated normal current of the switchgear should be selected from the R10 series, specified in IEC 60059.

NOTE 2 The R10 series is based on the work of a French army engineer (Col. Charles Renard), who proposed in the 1870s a set of preferred numbers for use with the metric system. His system was adopted in 1952 as

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international standard ISO 3. Renard's system of preferred numbers divides the interval from 1 to 10 into 5, 10, 20, or 40 steps. The factor between two consecutive numbers in a Renard series is constant (before rounding), namely the 5th, 10th, 20th, or 40th root of 10 (1,58; 1,26; 1,12 and 1,06, respectively), which leads to a geometric sequence. This way, the maximum relative error is minimized if an arbitrary number is replaced by the nearest Renard number multiplied by the appropriate power of 10.

The R10 series is based on the following equation: $R(i) = 10^{\frac{i}{10}}$, where i is the i^{th} element of the series.

– the expected maximum ambient temperature around the switchgear. For ambient temperatures up to 40 °C no special requirements are given.

5.2.2 Load current carrying capability under various conditions of ambient temperature and load

5.2.2.1 General

The rated normal current is based on the maximum permissible total temperature limitations of various parts of the switchgear and controlgear when it is carrying its rated normal current at an ambient temperature of 40 °C. The total temperature of these parts under service conditions depends both on the actual load current and the actual ambient temperature. It is therefore possible to operate at a current higher than the rated normal current when the ambient temperature is less than 40 °C, provided that the allowable temperature limit is not exceeded. Similarly, when the ambient temperature is higher than 40 °C, the current must be reduced to less than the rated normal current to keep the total temperature within the allowable limits.

The methods of calculating the allowable current under various conditions of ambient temperature and load are given in 5.2.2.2 through 5.2.2.4. For some high ambient temperature conditions, it may not be practical to reduce the current sufficiently to keep the total temperatures within their allowable limits. Forced air cooling will help in many cases. Temperature limits of associated equipment such as cables and current transformers must be considered as this heat transfer is not taken into account during type testing. However no advice can be given for these cases or the similar effects of solar radiation which also must be considered.

5.2.2.2 Continuous load current capability based on actual ambient temperature

If the ambient temperature is above 40 °C, parts of the switchgear and controlgear may exceed the specific limits given in Table 3 of IEC 62271-1:2007, when carrying its rated normal current. In this case a higher rated normal current range for the switchgear and controlgear has to be selected. For load currents which are lower than the rated normal current of the circuit-breaker, a permissible maximum ambient temperature for that load current can be calculated with the help of Equation (5):

$$\theta_a = \theta_{max} - \left(\frac{I_a}{I_r}\right)^{1,8} \times (\theta_r) \quad (5)$$

where

I_a is the allowable continuous load current, in A, at actual ambient temperature θ_a (I_a is not to exceed two times I_r);

I_r is the rated normal current, in A;

θ_{max} is the allowable hottest spot total temperature (θ_{max} = θ_r + 40), in °C;

θ_r is the allowable hottest spot temperature rise at rated normal current, in K;

θ_a is the allowable or actual ambient temperature, in °C.

NOTE The exponent would normally be 2, since the heat development in the switchgear and controlgear is proportional to the square of the current. Due to radiation and convection, the exponent may vary. Experience has

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shown that the exponent, depending on switchgear and controlgear design and components within the switchgear and controlgear, generally is in the range of 1,6 to 2,0. A value of 1,8 represents a compromise that covers most cases and is used in this application guide.

If Equation (5) is solved for the current I_a the allowable continuous load current at an actual ambient temperature θ_a can be calculated as given in Equation (6).

$$I_a = I_r \left(\frac{\theta_{max} - \theta_a}{\theta_r} \right)^{1/1,8} \quad (6)$$

The design features of switchgear and controlgear dictate the appropriate values of θ_{max} and θ_r to be used in the calculation. The major components of a circuit-breaker have several different temperature limitations which are specified in Table 3 of IEC 62271-1:2007. The values for θ_{max} and θ_r should be determined as follows:

a) if the actual ambient temperature is less than 40 °C, the component with the highest specified values of allowable temperature limitations should be used for θ_{max} and θ_r;

b) if the actual ambient temperature is greater than 40 °C, the component with the lowest specified values of allowable temperature limitations should be used for θ_{max} and θ_r.

The use of these values in the calculation will result in an allowable continuous current which will not cause the temperature of any part of the switchgear to exceed the permissible limits.

Example: A circuit-breaker that has been tested for 3 150 A rated normal current at an ambient temperature of 40 °C will carry a maximum load current of 2 500 A. What is the highest permissible ambient temperature?

As the estimated load current is less than rated current a higher ambient temperature is permissible. For the calculation θ_{max} and θ_r should be chosen as described under b).

In this case the lowest specified value in Table 3 of IEC 62271-1:2007 is θ_{max} = 90 °C and θ_r = 50 K for the bare bolted connection in air. With Equation (5) the maximum permissible ambient temperature in this example is

$$\theta_a = \theta_{max} - \left(\frac{I_a}{I_r} \right)^{1,8} \times (\theta_{max} - 40) = 57\ °C$$

5.2.2.3 Short-time load current capability

When switchgear and controlgear has been operating at a current level below its allowable continuous load current I_a, it is possible to increase the load current for a short time to a value greater than the allowable current without exceeding the permissible temperature limitations. There are different factors which influence the length of time period t_s of the overcurrent I_s. These are:

– the magnitude of the current I_s itself;
– the magnitude of the initial current I_i carried prior to the application of I_s;
– the thermal time characteristic (thermal time constant) of the switchgear and controlgear;
– the ambient temperature prior to and during application of overcurrent I_s.

The allowable duration of current I_s can be calculated directly by use of the Equation (7) and Equation (8):

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$$t_s = \tau\left[-\ln\left\{1-\frac{\theta_{max}-Y-\theta_a}{Y\left\langle(I_s/I_i)^{1,8}-1\right\rangle}\right\}\right] \quad (7)$$

$$Y = (\theta_{max}-40)\times\left(\frac{I_i}{I_r}\right)^{1,8} \quad (8)$$

where

θ_{max} is the allowable hottest spot total temperature (see Table 3, IEC 62271-1:2007), in °C;

θ_a is the actual ambient temperature in °C;

I_i is the initial current carried prior to application of I_s, in A (maximum current carried by the circuit-breaker during the 4 hour period immediately preceding the application of current I_s);

I_s is the short-time load current, in A;

I_r is the rated normal current, in A;

τ is the thermal time constant of circuit-breaker, derived from temperature rise test in h;

t_s is the permissible time for carrying current I_s at ambient θ_a after initial current I_i, time is given in the same unit as τ, h;

Y is the a coefficient used for convenience, in K.

The time duration of the current I_s determined in this way will not cause the total temperature limits of the switchgear and controlgear to be exceeded, provided that the following requirements are fulfilled:

a) the switchgear, and in particular the main contacts, shall have been well maintained and in essentially new condition;

b) the value used for current I_i is the maximum current carried by the switchgear during the 4 hour period immediately preceding the application of current I_s. To achieve the current value it is necessary to have a record of the current flow over the last 4 hours;

c) at the end of the period, the current I_s is reduced to a value which is not greater than the current I_a;

d) the value of current I_s is limited to a maximum value of two times rated normal current I_r. Otherwise actual overheating may occur as the heat from hot spots cannot be distributed fast enough to colder regions.

NOTE If the temperature rise due to the short-time load current I_s does not exceed θ_{max}, I_s is in an acceptable steady state. Thus the allowable time t_s is indefinite. Use of Equation (5) gives the information regarding the need, or otherwise, to apply Equation (7) and Equation (8).

Example: An SF_6 gas-insulated metal-enclosed switchgear with rated normal current carrying capability of I_r = 3 150 A (having a temperature rise of 65 K at 3 150 A) will carry a short-time load current I_s of 3 600 A. Before application of the short-time load current the initial current I_i was 2 500 A, the ambient temperature θ_a is 30 °C.

The highest total temperature θ_{max} = 115 °C is taken for bolted silver-coated connections in SF_6.The thermal time constant, derived from the type test, is 1,5 h. Generally, the time constant can be considered independent of the load and the temperature of the equipment.

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With Equation (7) and Equation (8) the allowable time t_s is calculated to

$$t_s = 1{,}5\left[-\ln\left\{1-\frac{115-Y-30}{Y\left\langle\left(\frac{3600}{2500}\right)^{1{,}8}-1\right\rangle}\right\}\right] = 2{,}22\,\text{h}$$

from Equation (8):

$$Y = (115-40)(2500/3150)^{1{,}8} = 49{,}5\,\text{K}$$

After 2 h and 13 min the current has to be reduced to the maximum allowable current I_a which can be calculated with the help of Equation (6).

5.2.2.4 Influence of the altitude of switchgear and controlgear location

If the switchgear and controlgear relies on natural circulation of the ambient air and is located at an altitude between 2 000 m and 4 000 m, correction is unnecessary. The reason for this is that the increase of temperature rise at higher altitude due to the reduced cooling effect of the air is compensated for by the reduced maximum ambient temperature at that altitude (see Table 5). Consequently the final temperature is relatively unchanged at a given current.

Table 5 – Maximum ambient temperature versus altitude (IEC 60943)

Altitude m	Maximum ambient air temperature °C
0 – 2 000	40
2 000 – 3 000	30
3 000 – 4 000	25

5.3 Temperature rise testing

5.3.1 Influence of power frequency on temperature rise and temperature rise tests

A test performed at a specific frequency is considered to be valid for the same current rating at a lower rated frequency.

In the case of open type switchgear and controlgear without ferrous parts adjacent to the current path a test performed at 50 Hz is also valid for 60 Hz provided that the temperature rise values recorded during the 50 Hz test do not exceed 95 % of maximum permissible values.

Caution is needed when tests performed at 50 Hz on switchgear and controlgear with ferrous parts are to be used to prove the performance of the switchgear and controlgear when rated for 60 Hz. The reason is that the ferrous parts adjacent to the current-carrying parts will have a frequency dependant heating effect due to the magnetic and eddy current losses. This will influence the temperature rise of the switchgear and controlgear.

5.3.2 Test procedure

The test procedure, the test arrangement and the tolerances for current, frequency and ambient temperature are given and described in 6.5 of IEC 62271-1:2007. The temperature

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rise is defined as the difference between the temperature of the part under consideration and the ambient temperature.

The duration of the test is determined by the time constant of the test object and the requirement to reach a stable value for the temperature rise. This condition is assumed to be satisfied when the increase of temperature rise does not exceed 1 K/h. This case will normally be met after a test duration of five times the thermal time constant of the test object. Care should be taken that this requirement is checked at the temperature rise values for each measurement point in relation to the ambient temperature (see Table 6). The change of the ambient temperature during the last quarter of the test period shall not exceed 1 K/h.

Table 6 – Some examples of the application of acceptance criteria for steady state conditions

Value	Example 1	Example 2	Example 3	Example 4
Change of absolute temperature during the last 1 h on the measurement point in K	1,8	0,5	1,1	0,8
Change of ambient temperature during the last 1 h in K	0,1	1,2	0,1	-0,6
Change of temperature rise of the measurement point during last 1 h in K	1,7	-0,7	1,0	1,4
Result	Steady state not reached. Change of temperature rise exceeds 1 K/h.	Steady state not reached Change of ambient temperature exceeds 1 K/h.	Steady state reached. All criteria fulfilled.	Steady state not reached. Change of temperature rise exceeds 1 K/h.

In Figure 9 the values are shown which have to be taken into account to check the steady state condition. At steady state the following conditions need to be fulfilled

– the increase of temperature rise ($\Delta\theta_c$) does not exceed 1 K in 1 h;

– the change in ambient temperature ($\Delta\theta_a$) during the last quarter of the test duration does not exceed 1 K in 1 h.

The values $\Delta\theta_c$ and $\Delta\theta_a$ are shown in Figure 10 which is an expansion of the relevant section of Figure 9. As mentioned above this condition will normally be reached after a test time of five times the time constant of the test object (see Figure 9).

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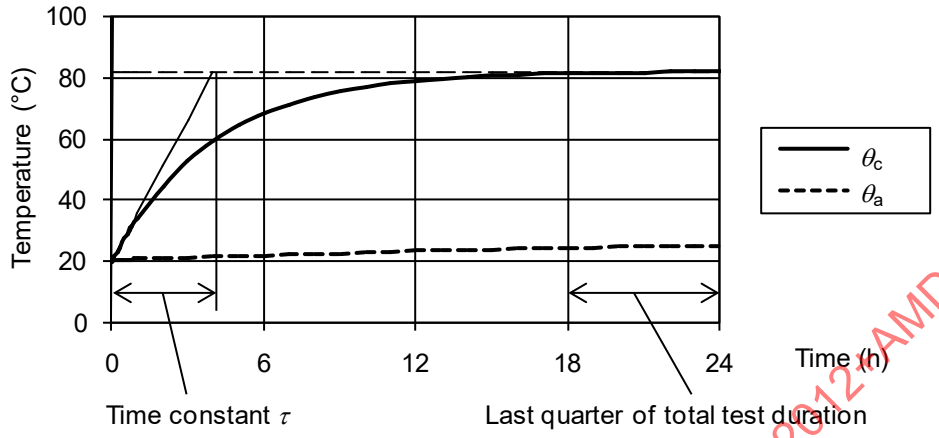

Figure 9 – Temperature curve and definitions

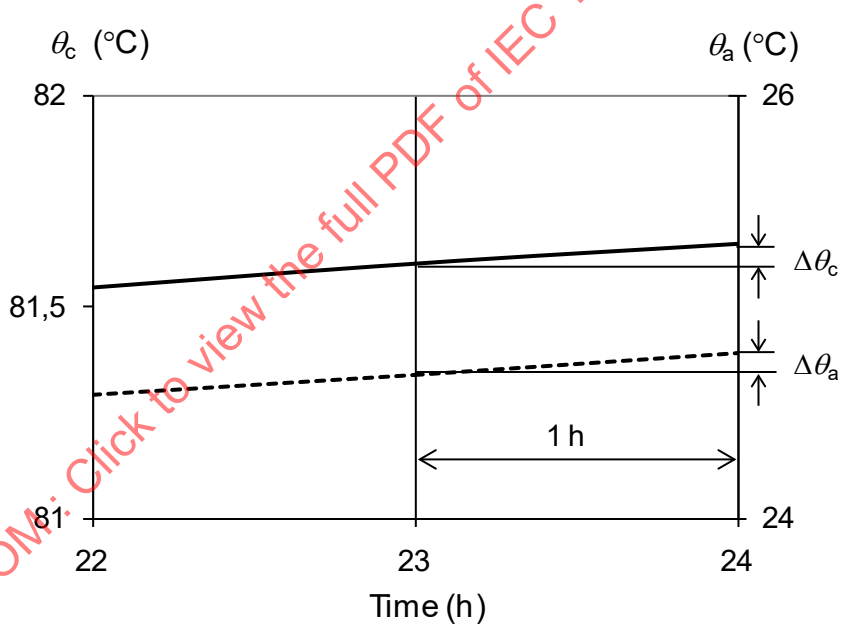

Figure 10 – Evaluation of the steady state condition for the last quarter of the test duration shown in Figure 9

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5.3.3 Temperature rise test on vacuum circuit-breakers

The temperature rise tests on vacuum circuit-breakers are performed in the same manner as for other types of circuit-breakers and switchgear and controlgear. However, it is not possible to connect a thermometer or thermocouple to the main contacts of the interrupter unit. As stated in IEC 62271-1 the temperature at the terminals or connection parts of the vacuum bottle is taken as the qualifying measurement. The temperature rise of these parts shall not exceed the limits given in Table 3 of IEC 62271-1:2007.

5.3.4 Resistance measurement

The procedure for measurement of the resistance of circuits is described in 6.4 of IEC 62271-1:2007.

The recommended minimum value of the injected current is 50 A d.c. to ensure that any surface contamination (sulfides or oxides) is broken down and that there is a sufficient voltage drop such that it can be measured accurately.

5.4 Additional information

5.4.1 Table with ratios I_a/I_r

In Table 7 the following variables are used:

– I_a is the allowable continuous load current, in A, at actual ambient temperature θ_a;
– I_r is the rated normal current, in A;
– θ_{max} is the allowable hottest spot total temperature ($\theta_{max} = \theta_r + 40$), in °C;
– θ_r is the allowable hottest spot temperature rise at rated normal current, in K.

Table 7 – Ratios of I_a/I_r for various ambient temperatures based on Table 3 of IEC 62271-1:2007

Maximum ambient temperature °C	Limiting temperature of different switchgear components °C									
	θ_{max}	70	80	90	100	105	115	120	130	155
	θ_r	30	40	50	60	65	75	80	90	115
		Ratios of I_a/I_r								
60	a	0,54	0,68	0,75	0,79	0,81	0,84	0,85	0,86	0,89
50	a	0,79	0,85	0,88	0,90	0,91	0,92	0,92	0,93	0,95
40		1,00	1,00	1,00	1,00	1,00	1,00	1,00	1,00	1,00
30	b	1,17	1,13	1,10	1,08	1,08	1,07	1,06	1,06	1,04
20	b	1,32	1,25	1,20	1,17	1,16	1,14	1,13	1,11	1,09
10	b	1,47	1,36	1,29	1,25	1,23	1,20	1,19	1,17	1,13
0	b	1,60	1,46	1,38	1,32	1,30	1,26	1,25	1,22	1,18
-10	b	1,72	1,56	1,46	1,40	1,37	1,32	1,30	1,27	1,22
-20	b	1,84	1,66	1,54	1,46	1,43	1,38	1,36	1,32	1,26
-30	b	1,95	1,75	1,62	1,53	1,50	1,44	1,41	1,37	1,30

a for limiting current at this ambient temperatures, use lowest θ_{max} and θ_r.

b for limiting current at this ambient temperatures, use highest θ_{max} and θ_r.

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5.4.2 Derivation of temperature rise equations

The temperature rise equations used for calculation of allowable time of a overload current are derived in the following manner:

Let

θ_s is the total temperature, in °C, that would be reached if the overload current I_s were applied continuously at ambient θ_a;

θ_i is the total temperature, in °C, due to continuous current I_i at ambient θ_a;

θ_t is the total temperature, in °C, at some time t after current is raised from I_i to I_s.

I_i is the initial current carried prior to application of I_s, in A (maximum current carried by the circuit-breaker during the 4 hour period immediately preceding the application of current I_s);

I_s is the overload current, in A;

I_r is the rated normal current, in A;

Then

$$\theta_t = (\theta_s - \theta_i) \times \left(1 - e^{-t/\tau}\right) + \theta_i \tag{9}$$

Let $\theta_t = \theta_{max}$; solve for t.

Then

$$t_s = -\tau \ln\left[1 - \frac{\theta_{max} - \theta_i}{\theta_s - \theta_i}\right] \tag{10}$$

where

$$\theta_i = (\theta_{max} - 40\ °C) \times \left(\frac{I_i}{I_r}\right)^{1,8} + \theta_a \tag{11}$$

and

$$\theta_s = (\theta_{max} - 40\ °C) \times \left(\frac{I_s}{I_r}\right)^{1,8} + \theta_a \tag{12}$$

For the special case where the initial current is zero, the equations in this form are useful. By substitution and further manipulation, the equations given in 5.2.2.3 in terms of Y are obtained; these are convenient to use in the more usual case where the initial current is not zero.

6 Transient recovery voltage

6.1 Harmonization of IEC and IEEE transient recovery voltages

6.1.1 General

The Transient Recovery Voltage (TRV) is defined by a waveform of voltage versus time and is the voltage impressed by the circuit across the opening contact gap in the circuit-breaker. The TRV peak is generally higher than the power frequency recovery voltage peak. However, as the TRV is damped out, the voltage across the opening contact gap in the circuit-breaker becomes the power frequency recovery voltage within a couple of milliseconds and that recovery voltage is then the system voltage of the circuit being interrupted. TRV waveform requirements were first specified in IEC and IEEE circuit-breaker standards in 1971. At that

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time, the two standards organizations each chose different waveforms to describe the same basic electrical transient. The TRV waveforms have been harmonized through a common work done by IEC SC 17A and the IEEE Switchgear Committee between 1997 and 2009. Since the approval of the relevant IEEE standards concluded in November 2009, TRV envelopes and parameters are (with few exceptions) harmonized for rated voltages higher than 1 kV and up to and including 800 kV. On the IEC side, the revisions were implemented first in amendments 1 and 2 to the first edition of IEC 62271-100 and additional changes were introduced in edition 2.0.

The first changes made to IEC 62271-100 and the relevant C37 series of IEEE standards on high-voltage circuit-breakers focused on TRVs for rated voltages of 100 kV and above. These TRV changes were adopted by IEC in May 2002.

The second set of changes was focused on voltages above 1 kV and less than 100 kV, where the waveforms used by IEC and IEEE were basically the same in that they both described a 1-cosine waveform. The main differences were that the IEC values for the TRV peak were lower and the Rate of Rise of Recovery Voltage (RRRV) was slower, which is a characteristic of cable connected systems. The IEEE values for the TRV peak were higher and the RRRV was faster, which is a characteristic of line connected systems. The harmonization process resulted in a compromise such that each standard adopted the other's set of values and that the less severe set of values was intended for application in cable connected systems and the more severe set of values for application in line connected systems. In summary, manufacturers and users will have two sets of TRV requirements to choose from that are distinguished by the application as in primarily cable connected distribution circuits or overhead line connected distribution circuits. The TRV changes to IEC for voltages above 1 kV and less than 100 kV were adopted in October 2006. These same TRV changes were later adopted by IEEE.

6.1.2 A summary of the TRV changes

6.1.2.1 The TRV harmonization plan

Working Group 23 of IEC SC 17A was formed in 1995 to prepare and execute a plan to harmonize power test procedures used in short-circuit testing of high-voltage circuit-breakers. The working group initially addressed differences in the table of tests to be performed. Upon completion of changes to the test procedures, the differences in TRV were then the *key* remaining differences that required harmonization. The following summarizes the harmonization approach developed.

6.1.2.2 Affected standards

The affected documents at the time the harmonization project began were the following.

– IEC 60056 (all parts), *High-voltage alternating current circuit-breakers*;[6]

– IEEE C37.04:1979, *IEEE standard rating structure for ac high-voltage circuit-breakers rated on a symmetrical current basis*;

– ANSI C37.06:1979, *AC high-voltage circuit-breakers rated on a symmetrical current basis – Preferred ratings and related required capabilities*;

– IEEE C37.09:1979, *IEEE standard test procedure for ac high-voltage circuit-breakers rated on a symmetrical current basis*;

– IEEE C37.011:1979, *IEEE application guide for transient recovery voltage for ac high-voltage circuit-breakers rated on a symmetrical current basis*.

These documents cover the rating, testing and application of high-voltage circuit-breakers. They were revised during the harmonization process.

[6] This series of standards was withdrawn.

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6.1.2.3 Similarities between the standards

The **Key** similarities between IEC and IEEE TRVs at the beginning of the harmonization activity were as follows:

a) RRRV at 100 % of rated I_{sc} (short-circuit current);
   - both standards used 2 kV/μs as the RRRV;
   - both standards used a time delay of 2 μs.

b) Peak TRV;
   - both standards used a first-pole-to-clear factor (k_{pp}) of 1,3 for effectively grounded systems at 245 kV and above;
   - both standards had maximum peaks of the TRV wave that are nearly the same and which are reached at about the same time.

c) Short-Line fault (SLF)
   - both standards used the same surge impedance of 450 Ω and the same time delays of either 0,2 μs at rated voltages less than 245 kV or 0,5 μs at rated voltages of 245 kV and above;
   - both standards used a peak factor of 1,6;

d) Initial TRV (ITRV)
   - both standards had the same requirements.

6.1.2.4 Differences between the standards

The *key* remaining differences between IEC and IEEE TRVs at the time the harmonization project began were the following.

a) IEEE used an exponential/1-cosine wave (Ex-Cos) description which defines all points as a curved function of time. The Ex-Cos wave shape can be explained with an analytical approach to TRV calculation. The initial exponential part of the TRV is the response of a parallel $L - Z$ circuit consisting of the inductance L of the local sources in parallel with the surge impedance Z of the lines connected to the bus. The later 1-cosine part of the TRV is an approximation to the TRV wave later in time when the exponential TRV that travelled as a wave out on the transmission system returns as a positive reflection from the first open circuit discontinuity. This analytical approach allows the TRV to be calculated for a given application condition and provides a similarly derived rated envelope for comparison.

b) IEC used a 4-parameter straight line description which allowed a TRV wave to be described in terms of simple straight lines. The 4-parameter TRV did not correspond to the response of a circuit that can be analysed. However, the 4-parameter TRV did allow the results of a measured or a calculated TRV wave to be described as simple straight lines for comparison to a similar set of straight lines as the rated envelope.

c) The Ex-Cos and the 4-parameter TRVs were comparable initially and at their peaks, but they diverged in the middle as shown in Figure 11, which shows both TRV envelopes for 100 % of rated short-circuit current at 145 kV.

d) Other differences existed between the TRVs at fractional ratings. For example, at 30 % of the rated short-circuit current; IEC used a 4-parameter envelope while IEEE used a 1-cosine (2-parameter) TRV. In addition, the peak voltages and times to peak were close, but not the same at both 30 % and 10 % of the rated short-circuit current for TRV peaks at rated voltage less than 245 kV.

e) Finally, in 1999 IEEE set the first-pole-to-clear factor to be 1,3 for voltages under 245 kV while IEC had values listed for both 1,3 and 1,5.

Overall, the differences in TRV requirements between the two standards were judged to be small.

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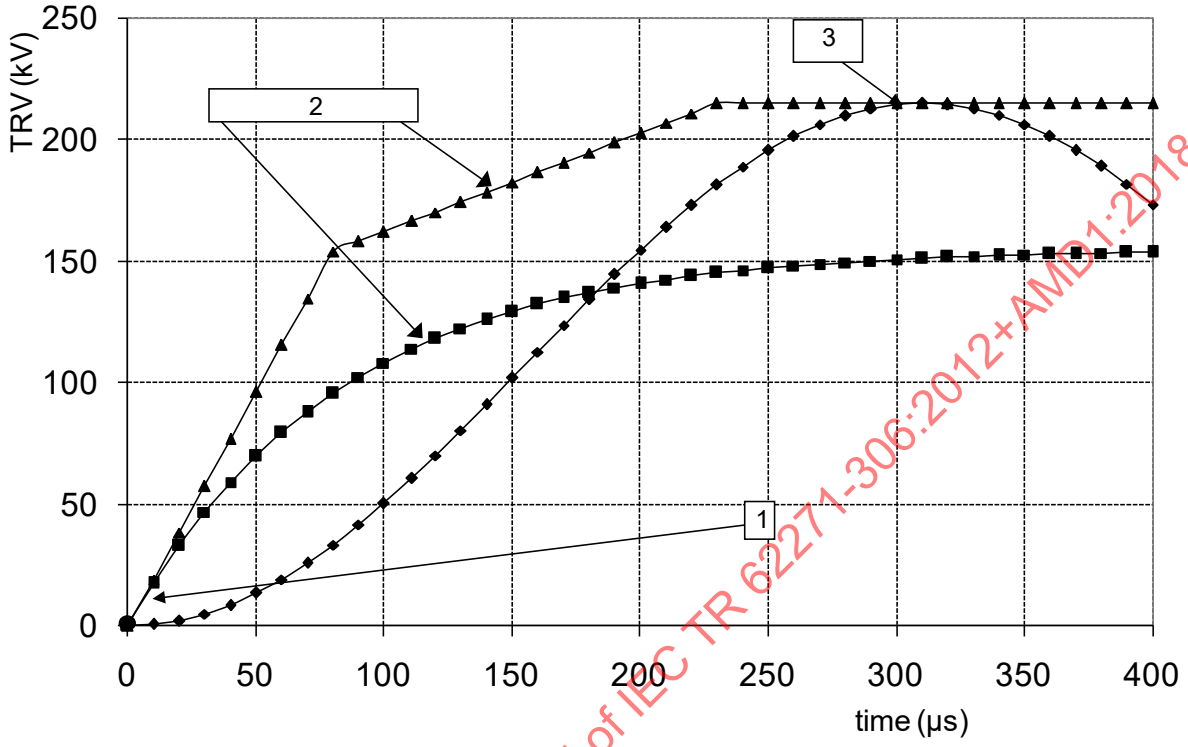

Key

▲	Four parameter TRV	1	Both standards have the same rate-of-rise of recovery voltage and time delay
■	Exponential TRV	2	The two standards differ in the middle region
◆	1-cos TRV	3	Both standards have approximately the same peak

Figure 11 – Comparison of IEEE, IEC and harmonized TRVs, example for 145 kV at 100 % I_{sc} with k_{pp} = 1,3

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6.1.2.5 The importance of harmonization of TRV standards

Both methods of describing TRV and of specifying ratings have served the industry very well. This is supported by the fact that very few failures of circuit-breakers in service have been attributed to an excessive TRV stress, regardless of which of the two standards was used to design, test and apply the circuit-breakers.

WG 23 of IEC SC17A studied the TRV descriptions in the standards and also reviewed some of the literature describing the origins of these standards. The harmonizing changes recommended to the TRV descriptions in both standards were then considered equitable by WG 23 whose members represent both the IEEE Switchgear Committee and IEC SC 17A.

The recommended changes are summarized in Table 8 and explained in detail in 6.1.3.1.

Table 8 – Summary of recommended changes to harmonize IEC and IEEE TRV requirements

Item	Changes to IEEE
A1	Adopt the 4-parameter TRV as the rated TRV description at 100 % and 60 % I_{sc}, and Adopt the 2-parameter TRV as the rated TRV description at 30 % and 10 % I_{sc}
A2	Adopt the same RRRVs, time delays and delay line descriptions as IEC at 100 % and 60 % I_{sc}
A3	Adopt the peak voltage values of u_c (E_2 in IEEE) and times to peak of t_2 presently in IEC standards at 100 % and 60 % of rated I_{sc}
Item	**Changes to IEC**
B1	Adopt the 2-parameter TRV as the rated TRV description at 30 % I_{sc}
Item	**Changes to IEEE and IEC**
C1	Adopt new harmonized values for u_1 and t_1 as a compromise between IEEE and IEC to harmonize the 2 standards around the middle of the TRV wavefront where the major differences presently exists: Present IEC: u_1 = 1,0 per unit, with (t_2/ t_1) = 3; Present ANSI: u_1 = 0,5 per unit, with (t_2/t_1) = 5,5 approximately Harmonized: u_1 = 0,75 per unit, with (t_2/t_1) = 4
C2	Adopt the new compromise peak TRV voltage values of u_c (E_2) and times to peak of t_3 (T_2) at 30 % and 10 % of rated I_{sc}
C3	Use these new harmonized TRV values for the source side TRV under short-line fault conditions
C4	Use these new harmonized TRV values for the source side TRV under out-of-phase switching conditions
C5	Develop new common 2-parameter TRV values for special purpose fast rate of rise TRV conditions such as transformer fed faults based on the new trial use standard IEEE C37.06.1-1997

6.1.3 Revision of TRVs for rated voltages of 100 kV and above

6.1.3.1 TRVs for terminal faults

WG 23 recommended that IEC and IEEE adopt a common compromise value for u_1, the first TRV voltage parameter that occurs at time t_1. The recommended values are given in Table 9.

Table 9 – Recommended u_1 values

I % I_{sc}	u_1 p.u.
100	0,75
60	0,75

Where 1 p.u. for u_1 is defined as:

$1\,\text{p.u.} = k_{pp} \times \frac{U_r\sqrt{2}}{\sqrt{3}}$ and the first-pole-to-clear factor k_{pp} = 1,3 for the standard case of effectively grounded systems and k_{pp} = 1,5 for the special case of non-effectively earthed systems.

These values represented a compromise and, moreover, were also consistent with reported system data.

– IEC used a single value of u_1 = 1,0 p.u. for all currents. This was a simple compromise choice made in the original IEC or CIGRE working group. However, the system data reported in Figure 7 of report 13-10 presented at CIGRE session 1968 [6], shows that for

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currents of 25 kA and above, a u_1 value of 0,75 p.u. is adequate and 1,0 is too high. Therefore, the recommended change in IEC standards to 0,75 p.u. at 100 % and 60 % was made to bring things into better compliance with reported system data.

– IEEE did not specify a u_1 value. However, applying the 4-parameter method to the Ex-Cos envelope as shown in Figure 11 suggests an apparent u_1 of approximately 0,5 p.u. at 100 % and 60 % I_{sc}. At such values, there was a large perceived difference between ANSI and IEC.

Therefore, the recommended changes in both IEC and ANSI/IEEE standards of u_1 = 0,75 p.u. at 100 % I_{sc} and 60 % I_{sc} brought IEEE and IEC into harmonization and brought the standard TRV into better compliance with reported system data as well.

Moreover, a value of 0,75 preserves a simple relationship between u_1, t_1 and u_c, t_2 as follows:

At 100 % of rated I_{sc}:

– present IEC standard, with u_1 = 1,0 p.u. and RRRV = 2 kV/µs;

  $t_2 = 3 \times t_1$;

– proposed harmonized standard, with u_1 = 0,75 p.u. and RRRV = 2 kV/µs;

  $t_2 = 4 \times t_1$ results in the same t_2 values as presently used in IEC standards.

At 60 % of rated I_{sc}:

– present IEC standard, with u_1 = 1,0 per unit and RRRV = 3 kV/µs;

  $t_2 = 4{,}5 \times t_1$;

– proposed harmonized standard, with u_1 = 0,75 per unit and RRRV = 3 kV/µs;

  $t_2 = 6 \times t_1$ results in the same t_2 values as presently used in IEC standards.

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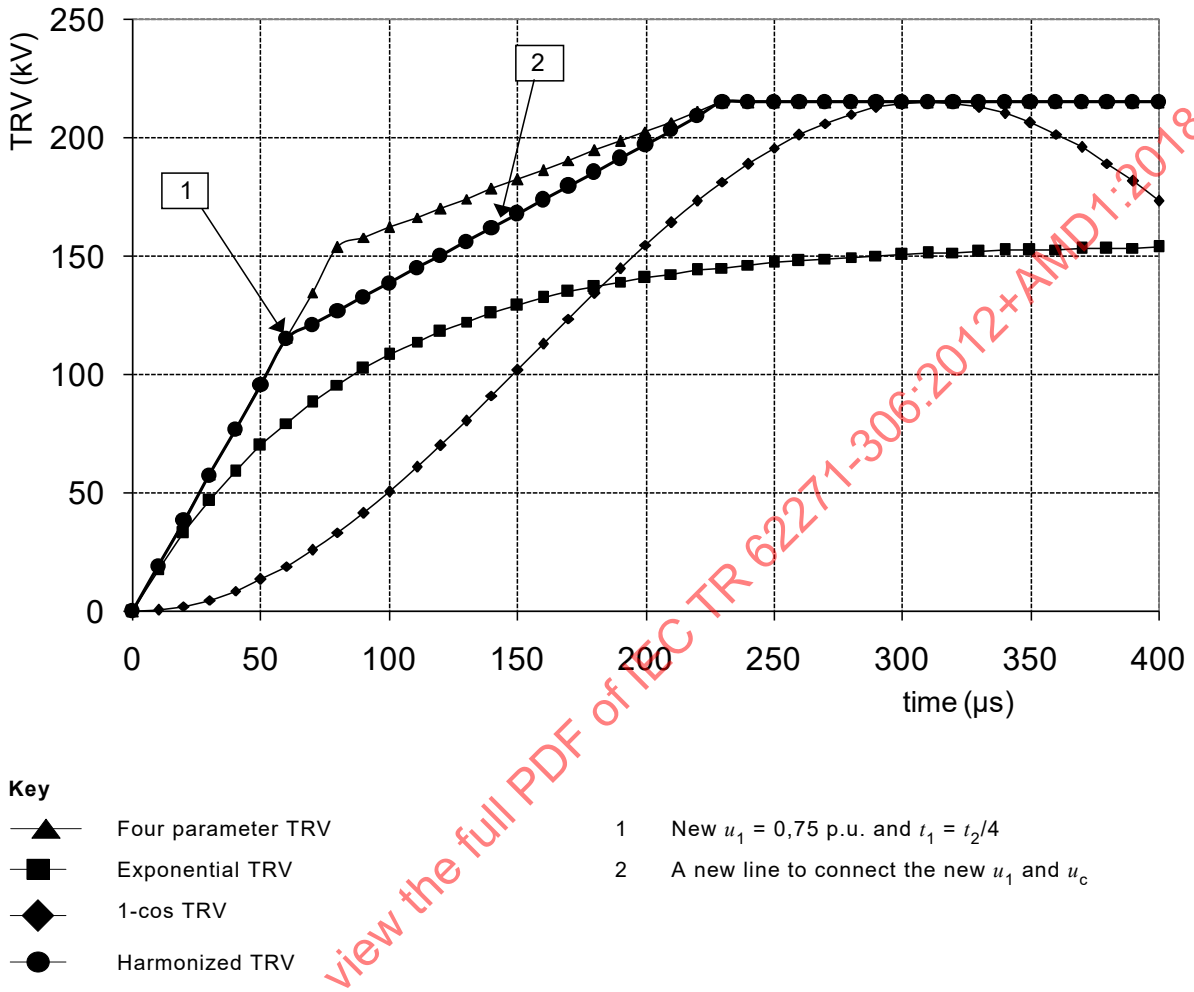

Figure 12 – Comparison of IEEE, IEC and harmonized TRVs with compromise values of u_1 and t_1, example for 145 kV at 100 % I_{sc} with k_{pp} = 1,3

After introduction of these first recommended changes, the two standards were further harmonized with the same values of RRRV for all terminal fault and short-line fault test duties.

In the past ANSI/IEEE used a first-pole-to-clear factor of 1,5 for all rated voltages. However, a change was adopted in 1999 to reduce the first-pole-to-clear factor to 1,3. This change was motivated by the following:

– a recognition that most power systems are effectively earthed at these voltages;

– a recognition that this change would move in the direction of harmonization with IEC, at least at the upper end of the spectrum of rated voltages.

~~After extensive discussions within the IEEE TRV Working Group, a decision was made for rated voltages equal or higher than 245 kV to use the value of k_{pp} = 1,3 as the preferred value and to retain the value of k_{pp} = 1,5 to allow users to specify this traditional value in case of three-phase ungrounded faults.~~

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~~IEC uses a first-pole-to-clear factor of 1,3 for effectively earthed neutral systems and first-pole-to-clear factor of 1,5 for non-effectively earthed neutral systems. An exception is made for terminal fault test duty T10 where k_{pp} is 1,5 for all rated voltages. This deviation was introduced in edition 2.0 of IEC 62271-100 in order to cover transformer-limited fault conditions with X_0/X_1 higher than 3,2 (e.g. non-effectively earthed transformers in effectively earthed neutral systems, or cases of transformers having one side effectively earthed and the other connected to non-effectively earthed neutral systems). The TRV specified covers also cases of 3-phase line faults with effectively earthed neutral systems (k_{pp} = 1,3) where coupling between phases can lead to an amplitude factor of 1,76.~~

The amplitude factor in IEC is 1,76; 1,54; 1,5 and 1,4 for T10, T30, T60 and T100, respectively for effectively earthed and non-effectively earthed neutral systems. These values have been adopted by IEEE in all cases for T60 and T100, and also for T10 and T30 in case of effectively earthed neutral systems and grounded faults. IEEE has kept the amplitude factors of ANSI C37.06 – 1979 for T10 and T30 in case of non-effectively earthed systems or ungrounded faults in effectively-earthed systems i.e. 1,64 for T10 and 1,58 for T30.

6.1.3.2 TRVs on the supply side for short-line fault interruption

For the supply side in short-line fault conditions, IEC and IEEE adopted TRVs as defined already in IEC but with a lower u_1 value set in the same manner as described for T60 and T100.

6.1.3.3 TRVs for out-of-phase switching

For use in out-of-phase switching conditions, IEC and IEEE adopted TRVs as defined already in IEC but with a lower u_1 value set in the same manner as described for T60 and T100.

The first-pole-to-clear factor is 2,0 in both standards in case of effectively-earthed neutral systems, in IEEE it follows that this value is used for rated voltages 170 kV and above.

The first-pole-to-clear factor is 2,5 in both standards in case of non-effectively-earthed neutral systems.

6.1.4 Revision of TRVs for rated voltages less than 100 kV

6.1.4.1 General

Following extensive studies done by several CIGRE working groups from 1983 to 1998, IEC started in 2001 the revision of TRVs for circuit-breakers with rated voltages higher than 1 kV and less than 100 kV. This revision lead to TRVs defined in amendment 2 to edition 1.0 of IEC 62271-100.

At the same time the IEEE Switchgear Committee started revising the TRVs for high-voltage circuit-breakers in standards ANSI/IEEE C37.04, C37.06, C37.09 and C37.011. In the range of rated voltages less than 100 kV, the IEEE working groups in charge of the revision of their respective standards decide to adopt the revised IEC values. As a consequence, the TRVs proposed were expected to be fully harmonized between IEC and ANSI/IEEE standards in this rated voltage range.

6.1.4.2 Revision of IEC 62271-100

In IEC the input coming from former Working Groups (WGs) of CIGRE Study Committee (SC) A3 (High-voltage Equipment) was used. These working groups studied the necessity to adapt the TRV requirements for circuit-breakers rated less than 100 kV. In 1983, a CIGRE SC A3 Task Force reported on Transient Recovery Voltages in Medium Voltage Networks, the results of the study have been published in Electra 88 [7]. Another working group, WG 13.05, studied the TRVs associated with clearing transformer fed faults and transformer secondary faults. The results of the work of WG 13.05 were presented in Electra 102 [8]. In 1992 together with

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CIRED (Congrès International des Réseaux Electriques de Distribution), CIGRE SC A3 created WG CC-03 to investigate again the definition of TRVs for medium voltage switching devices. The results of these investigations were published in CIGRE Technical Brochure 134 [9], they are in line with earlier studies.

The IEC work lead to amendment 2 to the first edition of IEC 62271-100. The main feature is the distinction between two types of systems that can be met in the range considered of rated voltages higher than 1 kV and less than 100 kV:

– Cable-systems have a TRV during breaking of terminal fault at 100 % of short-circuit breaking current that does not exceed the two-parameter envelope shown in 3. Standard values of TRVs for cable-systems are as in the first edition of IEC 62271-100.

  In practice, a circuit-breaker in an outdoor substation with cable connection to overhead lines is considered to be in a cable system if the total length of cable connected on the supply side of the circuit-breaker is at least 100 m. It has to be noted also that the capacitance of cable systems on the supply side of circuit-breakers can be provided by cables and/or capacitors and/or insulated bus.

– Line systems have a TRV during breaking of terminal fault at 100 % of short-circuit breaking current higher than the envelope defined for cable systems but not exceeding the two-parameter envelope shown in Figure 13. For the purpose of harmonization, standard values of TRVs for line-systems are those defined in ANSI/IEEE C37.06 for outdoor circuit-breakers.

  In line-systems, no cable is connected on the supply side of the circuit-breaker, with the possible exception of a short length of cable between the circuit-breaker and the line(s) or the supply transformer. Systems with transmission lines directly connected to a busbar, without intervening cable connections, are typical examples of line systems.

Figure 13 shows the comparison of TRVs for cable-systems and line-systems. The RRRV for line systems is approximately twice the value for cable-systems.

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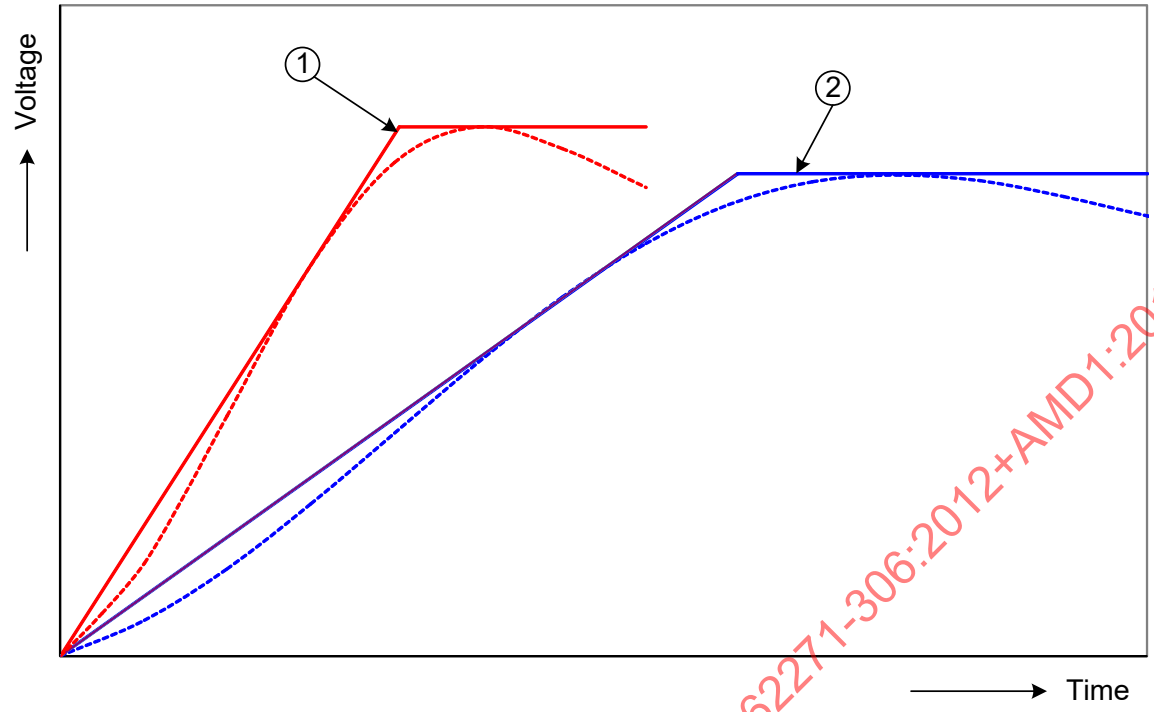

Key

1 Envelope of a line system TRV

2 Envelope of a cable system TRV

Figure 13 – Comparison of TRV's for cable-systems and line-systems

Explanatory notes on the revision of TRVs for circuit-breakers of rated voltages less than 100 kV are given in Annex G.

6.1.4.3 Revision of ANSI/IEEE C37.04 and 06

In the process of harmonization of IEC and IEEE standards for high-voltage circuit-breakers, the IEEE Switchgear Committee has adopted the corresponding revision of TRVs. As illustrated by Figure 14, the aim is to have fully harmonized requirements with IEC in the voltage range between 1 kV and 100 kV.

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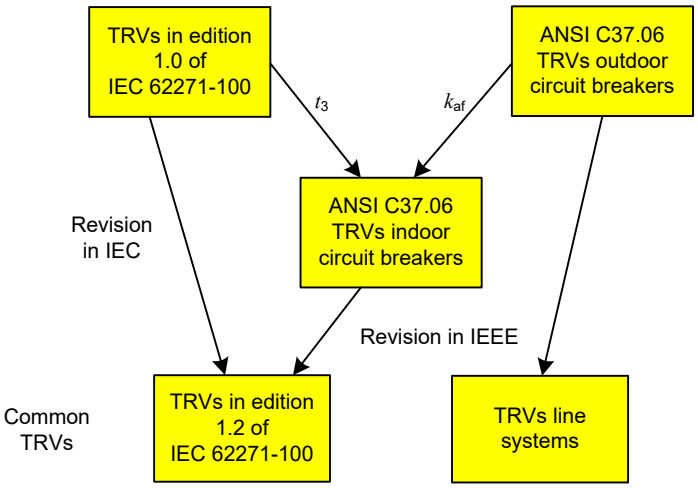

Figure 14 – Harmonization of TRVs for circuit-breakers < 100 kV

Following the approved revision of IEEE C37.04 [10] and IEEE C37.06 [11], the harmonization of TRVs in IEC and IEEE standards for high-voltage circuit-breaker was completed in 2009.

6.2 Initial Transient Recovery Voltage (ITRV)

6.2.1 Basis for specification

Due to travelling waves on the busbar and reflections from the first major discontinuity along the busbar, a high-frequency oscillation occurs which is similar to the one observed on a faulted line under short-line fault conditions. As the busbar is usually on the network side of the circuit-breaker this oscillation, which is called “Initial Transient Recovery Voltage (ITRV)” is superimposed to the very beginning of the terminal fault TRV.

The ITRV is mainly determined by the busbar and line bay configuration of the substation. Compared with the short-line fault the first voltage peak is rather low, but the time to the first peak is extremely short, that is, within the first 1,5 μs after current zero. Therefore the thermal mode of interruption may be influenced.

CIGRE WG 13-01 studied nearly all the basic network configurations and established the basic considerations with representative figures which served as the basis for ITRV specification [12] [13]:

– the initial part of ITRV depends only on the surge impedance of the connection and on the current;
– based on the dimensions of the busbar and the connections to them a surge impedance of 260 Ω is considered as a good estimate for practical applications with rated voltages up to 550 kV;
– the time to the first peak of ITRV is twice the travelling time of the wave to the main discontinuity. It depends on the dimensions of the substation, which is related to the rated voltage (see Table 10) and thus on the arrangement of the busbar;
– in practice, the main discontinuity is either a division in two branches of the busbar or the presence of a capacitance of more than 1 000 pF;
– the velocity of the wave propagation along the busbar was found to be about 260 m/μs.

6.2.2 Applicability

As the ITRV is proportional to the busbar surge impedance and to the current, the ITRV requirements can then be neglected in the following cases:

– for all circuit-breakers with a rated short-circuit breaking current of less than 25 kA;

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– for circuit-breakers installed in metal enclosed gas insulated switchgear (GIS) because of the low surge impedance;

– for circuit-breakers with a rated voltage below 100 kV because of the small dimensions of the busbars.

– for circuit-breakers directly connected to a busbar with a connection having a capacitance higher than 800 pF. The value of 800 pF was chosen such that the corresponding time constant is higher than the arc time constant for high current interruption in SF_6. The arc time constant is approximately 0,3 µs.

If a circuit-breaker with a rated voltage equal or less than 800 kV has a short-line fault rating, the ITRV requirements are covered if the short-line fault tests are carried out using a line with insignificant time delay (see 6.104.5.2 and 6.109.3 of IEC 62271-100:2008) unless both terminals are not identical from an electrical point of view (for instance when an additional capacitance is used as mentioned in the note). When terminals are not identical from an electrical point of view, test circuits which produce an equivalent TRV stress across the circuit-breaker may be used.

For circuit-breakers with a rated voltage higher than 800 kV, the ITRV requirements are considered to be covered if the short-line fault tests are carried out using a line with insignificant time delay and a surge impedance of 450 Ω unless both terminals are not identical from an electrical point of view (for instance when an additional capacitance is used as mentioned in the NOTE). When terminals are not identical from an electrical point of view, test circuits which produce an equivalent TRV stress across the circuit-breaker may be used.

NOTE Where the breaking capability of the circuit-breaker is not sufficient to interrupt a short-line fault, additional capacitance at the line side of the circuit-breaker or parallel to the breaking unit(s) can be used, both during the test and in service. The value and the location of this additional capacitance used during the tests should be stated in the test report.

Depending on the size of the additional capacitance (in pF) in relation to the circuit of interest (i.e. test circuit or service conditions), the line side time delay increases while the surge impedance of the line may be reduced. The latter will result in a lower rate-of-rise of the line side TRV.

During type testing the prospective TRV (given in Table 8 of IEC 62271-100:2008) is evaluated without the circuit-breaker or its additional capacitance present. It should be observed that the TRV values measured during the test will be different as a result of the influence of the circuit-breaker and its additional capacitance.

6.2.3 Test duties where ITRV is required

As interruption is influenced by ITRV mainly for high values of the short-circuit current, testing under ITRV conditions is required for T100a, T100s and L_{90}.

If the circuit-breaker has a short-line fault rating, the ITRV requirements are considered to be covered if the short-line fault tests are carried out using a line with insignificant time delay, unless both terminals are not identical from an electrical point of view (for instance when an additional capacitance is used).

6.2.4 ITRV waveshape

The ITRV is defined by the voltage u_i and the time t_i. As shown on Figure 12b of IEC 62271-100:2008, reproduced hereafter as Figure 15.

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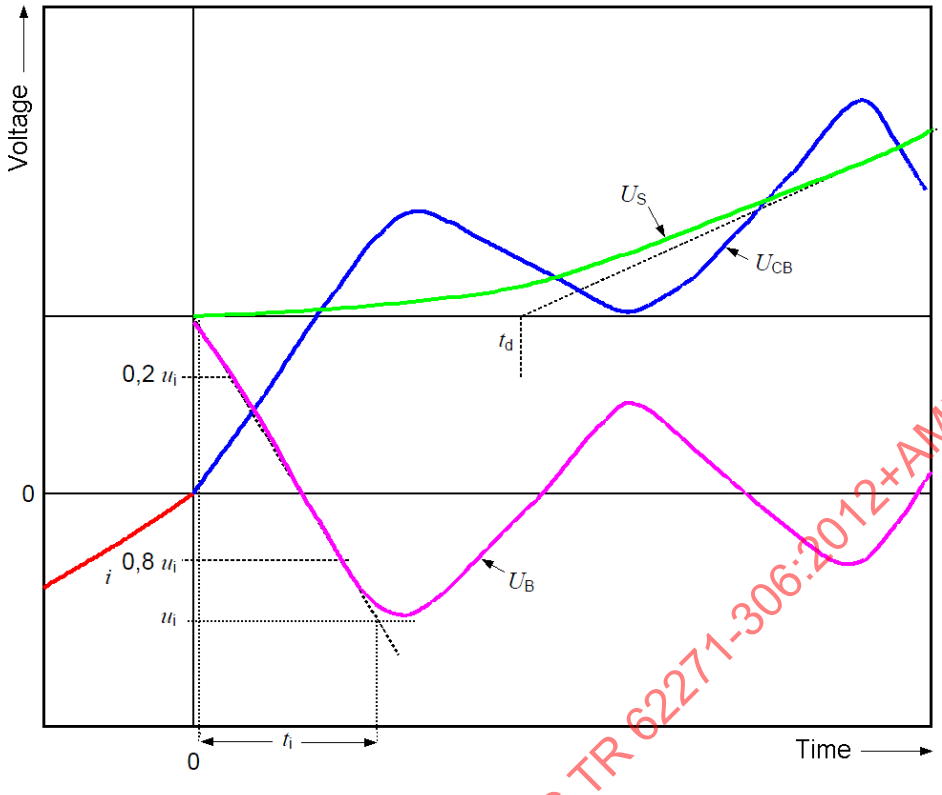

Key

i	Short-circuit current	U_{CB}	TRV across the circuit-breaker
u_i	Peak voltage of ITRV	U_B	Inherent busbar TRV
t_i	Time co-ordinate of ITRV	U_S	Inherent source side voltage TRV
t_d	Source side time delay		

Figure 15 – Representation of ITRV and terminal fault TRV

The rate of rise of the ITRV is dependent on the interrupted short-circuit current and its amplitude depends upon the distance to the first discontinuity along the busbar.

The inherent waveshape shall follow a straight line drawn using the 20 % and the 80 % point of the ITRV peak voltage u_i and the required rate of rise of the ITRV.

6.2.5 Standard values of ITRV

A multiplying factor f_i is used to determine the amplitude of the first peak u_i as function of the r.m.s value of the short-circuit breaking current.

Values of time to peak t_i are given in Table 7 of IEC 62271-100:2008 (reproduced here for convenience of reading as Table 10). These values were developed from the average distances from the breaker to the first discontinuity for the various system voltages [12].

The standard values cover both three-phase and single-phase faults. They are based on the assumption that the busbar, including the elements connected to it (supports, current and voltage transformers, disconnectors, etc.), can be roughly represented by a resulting surge impedance Z_i of about 260 Ω in the case of a rated voltage lower than 800 kV and by a resulting surge impedance Z_i of about 325 Ω in the case of a rated voltage of 800 kV. The relation between f_i and t_i is then:

$$f_i = t_i \times Z_i \times \omega \times \sqrt{2}$$

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where

$\omega = 2\pi f_r$ is the angular frequency corresponding to the rated frequency of the circuit-breaker.

Table 10 – Standard values of initial transient recovery voltage – Rated voltages 100 kV and above

Rated voltage U_r kV	Multiplying factor to determine u_i as function of the r.m.s. value of the short-circuit breaking current I_{sc} [a] f_i kV/kA		Time t_i µs
	50 Hz	60 Hz	
100	0,046	0,056	0,4
123	0,046	0,056	0,4
145	0,046	0,056	0,4
170	0,058	0,070	0,5
245	0,069	0,084	0,6
300	0,081	0,098	0,7
362	0,092	0,112	0,8
420	0,092	0,112	0,8
550	0,116	0,139	1,0
800	0,159	0,191	1,1
1 100	0,173	0,208	1,5
1 200	0,173	0,208	1,5

[a] The actual initial peak voltages are obtained by multiplying the values in these columns by the r.m.s. value of the short-circuit breaking current.

6.3 Testing

6.3.1 ITRV measurement

The ITRV should be handled as for the short-line fault TRV. Consequently it is necessary to measure the inherent ITRV circuit value.

As connections between the ITRV circuit and the supply circuit can also contribute to the initial part of the TRV, the inherent ITRV is that of the complete circuit from the circuit-breaker terminal to the first discontinuity i.e. the delay capacitor. Other contributions from the supply circuit, apart from ITRV and the normal two or four parameters TRV, must be damped by appropriate RC circuits.

As ITRV is characterized by a very high frequency in the MHz range, caution is recommended when measuring its inherent value. Diodes used in current injection methods must have short characteristic times (duration during which it differs notably from an ideal circuit-breaker), otherwise measurement could show a falsely damped ITRV with reduced RRRV [14].

The inherent waveshape shall mostly follow a straight reference line drawn from the beginning of the ITRV to the point defined by u_i and t_i. The inherent ITRV waveshape shall follow this reference line from 20 % to 80 % of the required ITRV peak value (see Figure 15). Deviations from the reference line are permitted for an ITRV amplitude below 20 % and above 80 % of the specified ITRV peak value.

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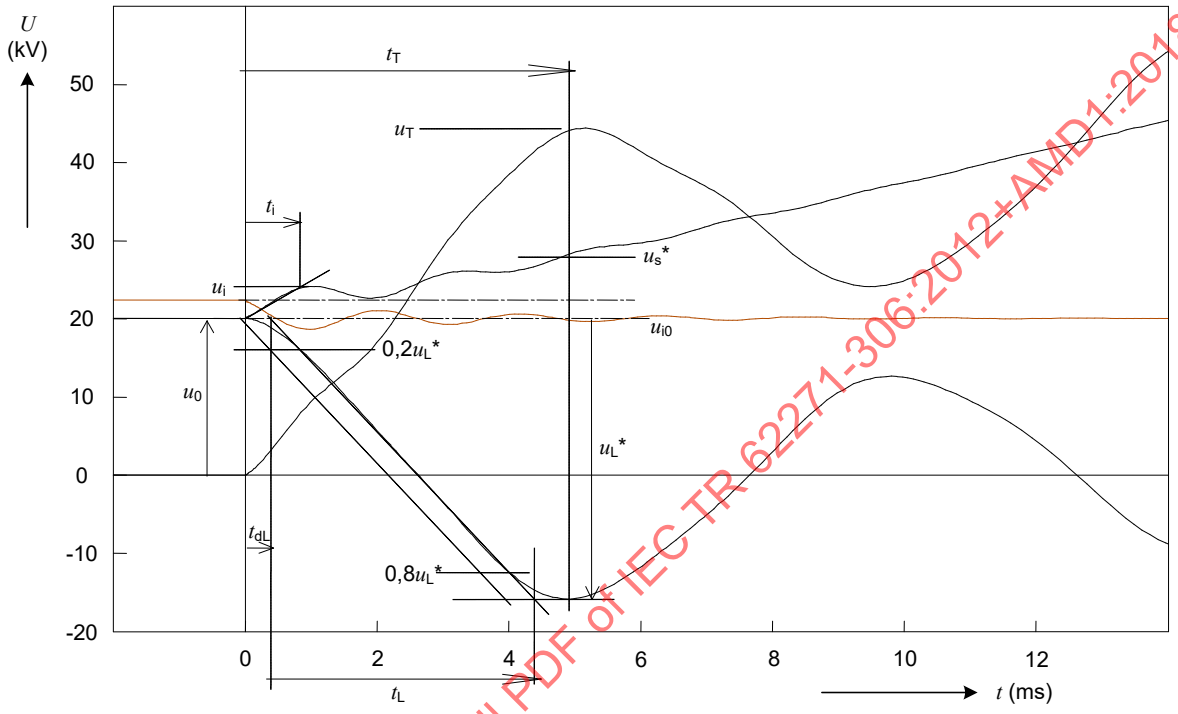
6.3.2 SLF with ITRV

Where short-line fault duties are to be performed, it may be convenient to combine the ITRV and SLF requirements in the line side circuit.

Figure 16 shows a typical graph of line and source side TRV in the case of line side TRV with time delay and source side with ITRV.



Key

t_{dL}	Line side time delay	u_{i0}	Busbar voltage drop
t_i	Time to peak of ITRV	u_L^*	Line side TRV
u_0	Induced voltage drop across the line inductance	u_s^*	Source side TRV
u_i	First peak of the ITRV	u_T	First peak of TRV across the circuit-breaker

Figure 16 – Typical graph of line side TRV with time delay and source side with ITRV

The first peak voltage across the circuit-breaker (u_T) is equal to sum of the line side TRV (u_L^*) and the source side TRV (u_S^*). Annex A of IEC 62271-100:2008 gives the calculation of these TRVs.

When the ITRV is combined with the transient voltage of a short line having a time delay t_{dL} as specified in Table 4 of IEC 62271-100:2008, the total stress is, for practical considerations, considered to be equal to the stress of a short line with insignificant time delay.

Further justification of the equivalence can be found in [15].

Subclause 6.109.3 of Amendment 1 to IEC 62271-100:2008 states the following.

Where applicable, a circuit-breaker with rated voltage higher than 800 kV can be tested with a line having an insignificant time delay and a surge impedance of 450 Ω (see 6.104.5.1 of IEC 62271-100:2008). If the circuit-breaker fails during this test procedure after a time corresponding to the first peak of ITRV, the test can be repeated with the required test circuit

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having the specified ITRV and a line having a surge impedance of 330 Ω and the specified time delay (t_{dL}). For both cases it is not required to perform T100s and T100a with circuits reproducing the rated ITRV.

6.3.3 Unit testing

As for SLF, ITRV circuit inductance must be divided by the number of breaks in series while time t_i is unchanged.

If the circuit-breaker has distribution capacitors, one capacitor shall be put in parallel to the unit under test.

6.4 General considerations regarding TRV

6.4.1 General

The purpose of 6.4 is to provide a background framework for some of the TRV requirements.

6.4.2 TRV waveshapes

In some cases, particularly in systems with a voltage 100 kV and above, and where the short-circuit currents are relatively large in relation to the maximum short-circuit current at the point under consideration, the transient recovery voltage contains first a period of high rate of rise, followed by a later period of lower rate of rise. This waveshape is generally adequately represented by an envelope consisting of three line segments defined by means of four parameters (see Figure 96).

The TRVs for terminal fault test-duties T100 and T60 represent cases where the major contribution of fault current is over transmission lines from multiple sources. The TRVs consist of the initial component at the fault bus and the additional component due to later arriving multiple reflected waves at the fault bus. The TRVs are overdamped (exponential) owing to the effect of the surge impedances of the lines and represented by four parameters to cover both of the above components. For terminal fault test duties T30 and T10 TRV cases, the fault current is from a single source and damping is determined by the involved circuit elements. The TRVs are underdamped (oscillatory) and thus represented by two parameters.

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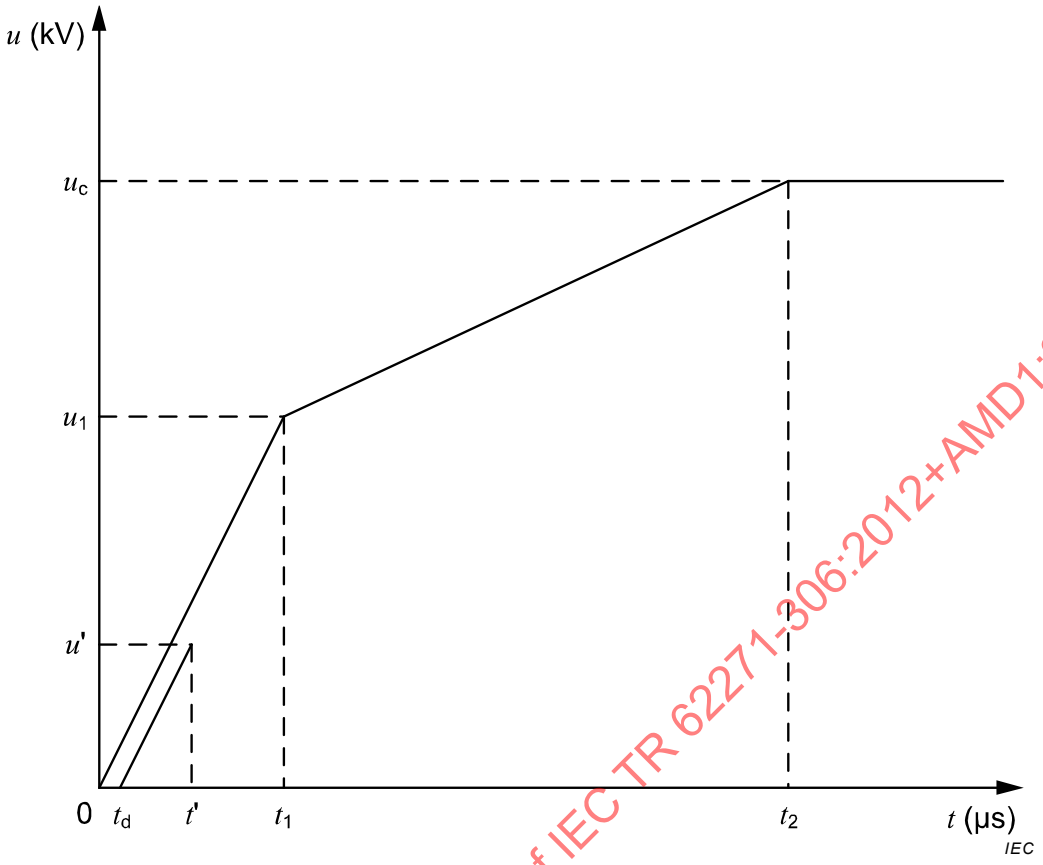

Figure 96 – Representation of a four-parameter TRV and a delay line

In other cases, particularly in systems with a voltage less than 100 kV, or in systems with a voltage greater than 100 kV in conditions where the short-circuit currents are relatively small in relation to the maximum short-circuit currents limited by transformers, the transient recovery voltage approximates to a damped single frequency oscillation. This waveshape is adequately represented by an envelope consisting of two line segments defined by means of two parameters (see Figure 97).

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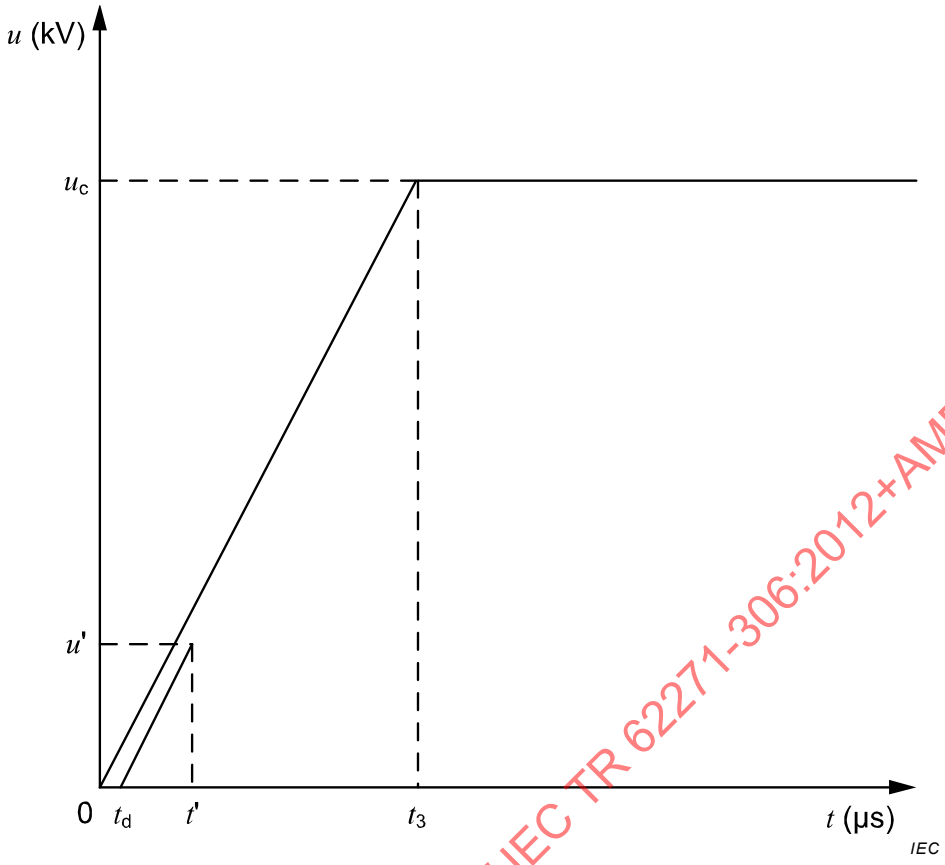

Figure 97 – Representation of a specified TRV by a two-parameter reference line and a delay line

Such a representation in terms of two parameters is a special case of representation in terms of four parameters.

The influence of local capacitance on the source side of the circuit-breaker produces a slower rate of rise of the voltage during the first few microseconds of the TRV. This is taken into account by introducing a time delay.

6.4.3 Earthing of the system

The system may be earthed in different ways depending on system voltage and application. The following definitions are used (Clause 3 of IEC 62271-100:2008 and as noted below):

solidly earthed (neutral) system (3.1.106 of IEC 62271-100:2008)
a system whose neutral point(s) is (are) directly earthed

[SOURCE: IEC 60050-601:1985, 601-02-25]

effectively earthed neutral system (3.1.128 of IEC 62271-100:2008)
system earthed through a sufficiently low impedance such that for all system conditions the ratio of the zero-sequence reactance to the positive-sequence reactance (X_0/X_1) is positive and less than three, and the ratio of the zero-sequence resistance to the positive-sequence reactance (R_0/X_1) is positive and less than one. Normally such systems are solidly earthed (neutral) systems or low impedance earthed (neutral) systems.

Note 1 to entry: For the correct assessment of the earthing conditions not only the physical earthing conditions around the relevant location but the total system is to be considered.

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non-effectively earthed neutral system (3.1.129 of IEC 62271-100:2008)
system other than effectively earthed neutral system, not meeting the conditions given in 3.1.128 of IEC 62271-100:2008. Normally such systems are isolated neutral systems, high impedance earthed (neutral) systems or resonant earthed (neutral) systems

Note 1 to entry: For the correct assessment of the earthing conditions not only the physical earthing conditions around the relevant location but the total system is to be considered.

6.4.4 Power frequency recovery voltage and first-pole-to-clear factor

6.4.4.1 General

The first-pole-to-clear factor (k_{pp}) is a function of the earthing arrangements of the system. As defined in 3.7.152 of IEC 62271-100:2008, it is the ratio of the power frequency voltage across the interrupting pole before current interruption in the other poles, to the power frequency voltage occurring across the pole or poles after interruption in all three poles. For non-effectively earthed neutral systems, this ratio is or tends towards 1,5. For rated voltages less than 170 kV, such systems are quite common, particular within Europe and Japan.

For effectively earthed neutral systems, the realistic and practical value is dependent upon the sequence impedances of the actual earth paths from the location of the fault to the various system neutral points (the ratio X_0/X_1). The value used in IEC 62271-100 is taken to be ≤ 3 (see Equation (144)). The X_0/X_1 value is a standard value confirmed by system studies of various networks. Hence, for rating purposes, IEC 62271-100 considers two values for the three-phase short-circuit condition. These are adequate for the many, different, system earthing arrangements:

a) the non-effectively earthed, to cover all unearthed systems and those with some deliberate additional impedance in the neutral system. A standardised value for k_{pp} of 1,5 is used for all such systems;

b) all effectively earthed systems where it is accepted that some impedance exists. For standardization purposes for power systems operating at 800 kV and below the value for k_{pp} used is 1,3. For ultra-high-voltage (UHV) power systems operating above 800 kV, k_{pp} is 1,2 based on an X_0/X_1 ratio of 2.

For single-phase-to-earth faults in solidly or effectively earthed neutral systems, the pole factor k_{pp} is 1,0.

At transmission voltages, there has been an increase in interconnection and transformation, particularly in major urban systems. The high number of transformer neutrals connected effectively to earth causes the value of 1,3 to be questioned. Although this has been considered, the text of IEC 62271-100 does not take these developments into account. It is important for users with such systems to note that as k_{pp} decreases towards unity the value of the second-pole-to-clear factor will fall. In addition, the value of the phase currents will change. The three phases become three independent single-phases each with k_{pp} approaching 1,0. In general the users of such systems are aware of this possibility and of the need to consider the actual system conditions when assessing the suitability of their specified requirements and the test evidence they are offered against these.

For rated voltages higher than 800 kV, systems are characterized by long transmission lines and large transformers that contribute a relatively large part of the total short-circuit current. The first-pole-to-clear factor is function of the X_0/X_1 ratio that is in this case equal to or lower than 2,0, as a consequence k_{pp} is equal to or less than 1,2 and has been standardized to 1,2.

Where the ratio of three-phase to single-phase earth fault current is 1,0, k_{pp} is also 1,0. However, although this is normally assumed to be adequately covered by the use of the three-phase requirements and the associated k_{pp} of 1,2 or 1,3, it is important that evidence is provided to demonstrate the extended arc condition of the single-phase fault. In accordance with IEC 62271-100, a full extinguishing window shall be demonstrated.

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It should be noted that in accordance with 6.108 of IEC 62271-100:2008, specific recovery voltage conditions are required to demonstrate the ability of a circuit-breaker to clear double earth faults.

Regarding earthing of the test circuit, reference is made to 6.103.3 of IEC 62271-100:2008.

6.4.4.2 Equations for the first, second and third-pole-to-clear factors

The equation for the first-pole-to-clear factor is:

$$k_{pp} = \frac{3X_0}{X_1 + 2X_0} \quad (144)$$

where X_0 is the zero sequence, and X_1 the positive sequence reactance of the system. Table 39 gives the k_{pp} values for various earthing arrangements based on the definitions given in 6.4.1.

Table 39 – First-pole-to-clear factors k_{pp}

Earthing arrangement	X_0/X_1	k_{pp}	System voltage
Solidly earthed	1	1	All
Effectively earthed	2	1,2	> 800 kV
Effectively earthed	3	1,3	≤ 800 kV
Non-effectively earthed	∞	1,5	≤ 170 kV
NOTE Calculation of k_{pp} for the effectively earthed case (X_0/X_1 = 3) gives k_{pp} = 1,286 which is then rounded to 1,3.			

Following interruption of the first pole, the remaining two phases continue to conduct fault current.

In systems with non-effectively earthed neutrals the second and third poles interrupt in series under the phase-to-phase voltage so that for the second and third pole,

$$k_p = \frac{\sqrt{3}}{2},$$

where k_p is the pole-to-clear factor of the individual poles.

In systems with effectively earthed neutrals the second pole clears with a pole-to-clear factor of,

$$k_p = \frac{\sqrt{3(X_0^2 + X_0X_1 + X_1^2)}}{X_0 + 2X_1} \quad (145)$$

NOTE In Equations (144) and (145) the resistances are neglected.

Equation (145) can be expressed as a function of the ratio $\alpha = X_0/X_1$:

$$k_p = \frac{\sqrt{3}\sqrt{\alpha^2 + \alpha + 1}}{2 + \alpha}$$

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For the third-pole-to-clear in an effectively earthed system k_p = 1. Table 40 gives k_p for each clearing pole as a function of X_0/X_1 as appropriate.

Table 40 – Pole-to-clear factors for each clearing pole

X_0/X_1	Pole-to-clear factor		
Ratio	First	Second	Third
1	1,0	1,00	1,0
2	1,2	1,15	1,0
3	1,3	1,26*	1,0
∞	1,5	0,866	0,866
* Equation (145) assumes that system impedances are inductances only.			

The respective multiplying factors for the peak value of the TRV (u_c) are given in Table 6 of IEC 62271-100:2008. It is important to note that the amplitude factor is the same for each pole. The multiplying factors are as applied to the power frequency voltages.

6.4.4.3 Standardised values for the second- and third- pole-to-clear factors

As discussed above, IEC 62271-100 has standardised values for the second and third-pole to clear factors for three-phase testing. Subclause 13.3 deals with this topic in relation to demonstration of arcing times for these poles and the appropriate pole factors relevant to each opening pole. It is important to note that on systems where the neutral earthing is solid, both the first-pole-to-clear factor of 1,3 and the values provided above for second pole-to-clear factors are lower. This is likely to be a rare occurrence, generally associated with urban systems where there are numerous effectively earthed transformers in close proximity. Where such differences are significant, the user is generally aware that it may be necessary to specify system-specific requirements and tests (e.g. extinguishing window and single-phase short-circuit current).

Circuit-breakers are rated on the basis of their ability to interrupt a three-phase to earth fault in either an effectively or non-effectively earthed neutral systems. Taking the former case, the three poles clear in sequence:

- The first pole clears with k_{pp} given by Equation (144) leaving a two-phase to earth fault.
- The second pole clears with k_p given by Equation (145) leaving a single-phase to earth fault. For the case of a two-phase to earth, the k_{pp} for the first clearing pole is also given by Equation (145).
- Third pole with k_p = 1 which is also applicable to the single-phase to earth fault case.

Similar logic can be applied to faults in non-effectively earthed neutral systems. A summary of the pole-to-clear factors for the different fault cases is given in Table 41.

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Table 41 – Pole-to-clear factors for other types of faults in non-effectively earthed neutral systems

Type of fault	First-pole-to-clear	Second-pole-to-clear	Third-pole-to-clear
Phase-to-earth	1	-	-
Two-phase not involving earth	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	-
Two-phase-to-earth	$k_p = \frac{\sqrt{3}\sqrt{\alpha^2+\alpha+1}}{2+\alpha}$	1	-
Three-phase not involving earth	1,5	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$

6.4.5 TRV characteristics

6.4.5.1 Terminal fault TRVs for rated voltages higher than 1 kV and less than 100 kV

6.4.5.1.1 General

Following the decision taken at the SC17A meeting in Beijing (CN) in October, 2002, IEC SC 17A/WG35 has prepared a proposal for the revision of TRVs for circuit-breakers rated above 1 kV and less than 100 kV.

This proposal used the input coming from former Working groups of CIGRE Study Committee A3 (Switching Equipment) that have studied the necessity to adapt the TRV requirements for circuit-breakers rated less than 100 kV. In 1983, a CIGRE SC A3 Task Force reported on Transient Recovery Voltages in Medium Voltage Networks. The results of the study have been published in Electra 88. Another CIGRE working group, WG 13.05, studied the TRVs generated by clearing transformer-fed faults and transformer secondary faults. The results have been presented in Electra 102 (1985). In 1992, together with CIRED, CIGRE SC A3 created working group CC-03 to investigate again the definition of TRVs for medium voltage switchgear. The outcome of these investigations has been published in CIGRE Technical Brochure 134 (1998) and is in line with earlier studies.

The first edition of IEC 62271-100 (IEC 62271-100:2001) was amended in 2006 (Amendment 2) to include the new TRV values. The modifications can be summarized as follows:

a) In order to cover applications in all types of networks (distribution, industrial and sub-transmission) for rated voltages higher than 1 kV and less than 100 kV, and for standardization purposes, two types of systems and two classes of circuit-breakers are defined:
   - cable systems:

     cable-systems are defined in 3.1.132 of IEC 62271-100:2008;
   - line systems:

     line systems are defined in 3.1.133 of IEC 62271-100:2008;
   - Circuit-breaker class S1: circuit-breaker to be used in a cable system;
   - Circuit-breaker class S2: circuit-breaker to be used in a line system.

b) A particular test duty T30 is specified for the special case of circuit-breakers intended to be connected to a transformer with a connection of small capacitance (cable length less than 20 m), in order to verify their capability to interrupt transformer-limited faults. This is covered in Annex M of IEC 62271-100:2008.

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In the general case where the capacitance of the connection is high enough, the normal test duty T30 demonstrates the capability to interrupt transformer-limited faults.

6.4.5.1.2 Terminal fault TRV for circuit-breakers in line systems

6.4.5.1.2.1 General

In North America, line systems are prevalent at 72,5 kV and below. Therefore, the TRV ratings as listed in Table 2 of ANSI C37.06-2000 were the basis to define the new Table 25 of IEC 62271-100:2008. The values for t_3 are 0,88 times the T_2 values specified in ANSI.

NOTE 1 The factor 0,88 is derived from a pure "1-cos"-waveshape multiplied with ½ amplitude factor. The standard TRV wave-shape "1-cos" in ANSI C37-06-2000 for rated voltages less than 100 kV did not coincide with the precise mathematical equation for parallel or series damped circuits, for which another ratio t_3/T_2 is applicable.

NOTE 2 TRV parameters are defined in the standard for rated voltages of 15 kV to 72,5 kV, for rated voltages less than 15 kV the TRV parameters can be derived using k_{pp} = 1,5, the values of amplitude factor, time t_3 and time delay given in 6.4.1.2.2.2, 6.4.1.2.2.3 and 6.4.1.2.2.4.

6.4.5.1.2.2 Amplitude factor

For T100, T60, T30 and T10 the following values were taken from ANSI C37.06-2000:

– 1,54 for T100;
– 1,65 for T60;
– 1,74 for T30;
– 1,8 for T10.

6.4.5.1.2.3 Time t_3

The rate-of-rise of recovery voltage (RRRV) is calculated using Equation (146),

$$\text{RRRV} = 0{,}4 U_r^{0{,}305} \tag{146}$$

Time t_3 for terminal fault is equal to $4{,}65 \times U_r^{0{,}7}$, with t_3 in µs and U_r in kV. Equation (146) was derived from the values given in Table 2 of ANSI C37.06-2000 for rated voltages 15,5 kV, 25,8 kV, 48,3 kV and 72,5 kV. The same equation is used for other rated voltages.

6.4.5.1.2.4 Time delay

The time delay in Table 25 of IEC 62271-100:2008 is derived using the following equation, $t_d = 0{,}05 \times t_3$, as in the first edition of IEC 62271-100:2001 for rated voltages 48,3 kV – 52 kV and 72,5 kV. The equation has been extended to the lower rated voltages as no change in the initial part of the TRV wave-shape is expected (the initial part is exponential, even with the short line lengths that can be met in distribution and sub-transmission systems). This requirement is not judged excessive, as in the worst case (U_r = 15 kV), the time delay value of 2 µs is as specified for circuit-breakers with rated voltages higher than 72,5 kV.

It recognizes the fact that this time delay can be critical during short-line fault testing and test duty T100 with ITRV and has therefore to be taken into account. However, as shown in Tables 13 and 14 of the first edition of IEC 62271-100 published in 2001, such verification can be made when performing short-line fault tests. Therefore, as it is already the case for rated voltages higher than 38 kV, it is allowed to have a longer time delay during testing of T100, up to $0{,}15 \times t_3$, provided that short-line fault tests are performed. This possibility is indicated in Table 25 of IEC 62271-100:2008.

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6.4.5.1.3 Terminal fault TRV for circuit-breakers in cable systems

6.4.5.1.3.1 Amplitude factor

For T60, the value of 1,5 in the first edition of IEC 62271-100:2001 is kept, due to the positive experience obtained.

For T30 and T10, the amplitude factor has been raised from 1,5 to respectively 1,6 and 1,7, as the contribution to TRV comes mainly from the voltage variation across transformer(s), which has low damping; this combined with source voltage results in a TRV with a relatively high amplitude factor.

For T100, the value of 1,4 in the first edition of IEC 62271-100 published in 2001 is retained owing to the positive experience with past editions of this standard.

6.4.5.1.3.2 Time delay

The time delay t_d is as given in the first edition of IEC 62271-100 published in 2001 for rated voltages less than 52 kV, t_d = 0,15 × t_3. The equation is generalized to all cable systems (rated voltage less than 100 kV).

6.4.5.1.4 Terminal fault TRV for rated voltages equal to or higher than 100 kV

6.4.5.1.4.1 Amplitude factor

The values of the amplitude factors are given in IEC 62271-100. These values were adopted into IEC 62271-100 as a result of system studies and generally remain acceptable.

6.4.5.1.4.2 Rate-of-rise of recovery voltage and time delay

The values for the rate-of-rise-of-recovery-voltage (RRRV) for the first-pole-to-clear, and the associated time delay values, were derived from system studies, supported by system tests performed in and before the mid-1970s. The values adopted (2 kV/µs etc.) have been shown by this work to be adequate for all developed systems, and are generally acceptable for others. IEC 62271-100 gives multipliers for the RRRV for the second and third poles-to-clear. These values were derived by calculation.

6.4.5.1.5 Basis for the current TRV values of test-duty T10

Test-duty T10 is detailed in IEC 62271-100 and represents the following cases:

– a transformer limited fault condition with the circuit-breaker under consideration clearing a fault on the remote side of the transformer.

  In such circumstances, the fault current is limited by the impedance of the transformer to a value, chosen for standardization purposes, of approximately 10 %. The value of 10 % is historic, having been established from system studies and modelling using the typical impedance values of transformers of standardised ratings.

  For this duty, the fault-current is limited by the value of the impedance of the transformer. The TRV is also dominated by the transformer characteristics which give it a (1-cos) wave-shape form. The values given in IEC 62271-100 for amplitude factor, time coordinates and delay line have been established from system studies and modelling during the 1960s and before. The present values are accepted as being adequate for the vast majority of systems;

– a long line fault for circuit-breakers having a rated voltage of 245 kV and above

  For rated voltages below 245 kV, k_{pp} = 1,5 in view of the fact that the contribution of transformers to the short-circuit current is relatively larger at smaller values of the short-circuit current. Additionally, a comparatively large number of transformers having an unearthed neutral are in service in earthed neutral systems. As the damping of the TRV oscillation on a high-voltage transformer is less than in a network, an amplitude factor of

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1,7 has been standardised except for line systems, with a voltage reduction across the transformer of 10 % for voltages of 100 kV and above.

Thus, the TRV peak u_c for test-duty T10 is $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ with the following parameters:

a) for rated voltages below 100 kV:
   1) for circuit-breakers in cable systems
      k_{pp} = 1,5 and k_{af} = 1,7.
   2) for circuit-breakers in line systems
      k_{pp} = 1,5 and k_{af} = 1,8.
b) for rated voltages of 100 kV up to and including 170 kV:
   k_{pp} = 1,5 and k_{af} = 0,9 × 1,7 = 1,53.
c) for rated voltages of 245 kV up to and including 800 kV:
   k_{pp} = 1,3 and k_{af} = 1,76.
d) for rated voltages above 800 kV:
   k_{pp} = 1,2 and k_{af} =1,76.

6.4.6 Short-line fault TRV

6.4.6.1 General

Short-line fault (SLF) is a mandatory duty for circuit-breakers with rated voltages 15 kV and above that are directly connected to overhead lines. As specified already in IEC 62271-100:2001 for circuit-breakers rated 48,3 kV and above, the rated short-circuit current shall be higher than 12,5 kA (i.e. $I_{sc} \geq$ 16 kA).

As it is considered that there are only few line systems below 15 kV, no short-line fault breaking capability is required for rated voltages below 15 kV. In the rare cases where a circuit-breaker with a voltage rating below 15 kV is directly connected to an overhead line, no short-line fault requirement is necessary as the line contribution to the TRV would be too low to produce a significant stress.

NOTE For class S2 circuit-breakers, short-line fault test-duty L90 is not required as it would lead to an unrealistic short length of faulted line.

The short-line fault test specified is regarded as covering three-phase short-line faults as well as two-phase and single-phase faults for the following reasons:

– the representative surge impedance, seen from the terminals of the clearing pole, is such that for all cases the RRRV for all three poles to clear is covered by the specified characteristics listed in Table 8 of IEC 62271-100:2008;
– the single-phase short-line fault test, with an interrupting window of (180°−dα), covers the requirement for the multi-phase fault cases for effectively-earthed and non-effectively earthed systems;
– the withstand of the peak value of TRV during three-phase fault interruption is demonstrated by terminal fault test duty T100.

6.4.6.2 Rated voltage less than 100 kV

6.4.6.2.1 General

In IEC 62271-100:2001, short-line fault requirements have been specified for circuit-breakers with a rated voltage of 52 kV and 72,5 kV, in the range of rated voltages considered in this edition, and directly connected to overhead-lines.

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In IEC 62271-100:2008, short-line fault requirements are specified for class S2 circuit-breakers with a rated voltage of 15 kV and above and directly connected (with busbars) to overhead-lines, irrespective of the type of network on the source side.

As the network and substation topology and layout for 48,3 kV is identical to those of 52 kV and 72,5 kV systems, the short-line test duty for 48,3 kV is specified in a way similar to 52 kV and 72,5 kV.

For rated voltages of 15 kV to 38 kV, the characteristics and procedure are slightly different. As normally no equipment is connected to the line side of the circuit-breaker, the line characteristics are adapted to virtually no delay capacitance: $t_{dL} < 0,1$ µs. As the line length to the fault location should correspond to realistic distances, the test duty L_{90} has been dropped and the tolerances on the line length for L_{75} have been adapted.

Time t_3 and the amplitude factor of the supply circuit is the same as for terminal fault test-duty T100.

6.4.6.2.2 Rated voltage equal to or higher than 100 kV

The amplitude factor and the inherent value of the RRRV of the supply circuit are as specified for terminal fault test duty T100. During a SLF interruption the RRRV on the supply side is equal to the inherent value of RRRV for the supply circuit multiplied by the ratio of the SLF current divided by the rated short-circuit breaking current.

6.4.7 Out-of-phase TRV

Not enough system information is available to revise TRV parameters for breaking in the out-of-phase condition. CIGRE SC A3 has been asked to investigate the system and service conditions leading to out-of-phase current clearing. Therefore, the TRVs for out-of-phase breaking are basically unchanged.

The values of t_3 for out-of-phase are in all cases two times the value for terminal fault T100.

6.4.8 TRV for series reactor fault

Due to the very small inherent capacitance of a number of current-limiting reactors, the natural frequency of transients involving these reactors can be very high. A circuit-breaker installed immediately in series with such type of reactor will face a high-frequency TRV when clearing a terminal fault (reactor at supply side of circuit-breaker) or clearing a fault behind the reactor (reactor at load side of circuit-breaker). The resulting TRV frequency generally exceeds by far the standardized TRV values.

In these cases, it is necessary to take mitigation measures, such as the application of capacitors in parallel to the reactors or connected to earth. The available mitigation measures are very effective and cost efficient [125]. It is strongly recommended to use them, unless it can be demonstrated by tests that a circuit-breaker can successfully clear faults with the required high-frequency TRV.

Considering the economical aspect as well as service experience with TRV mitigation measures, there is no need for special requirements in IEC 62271-100 for circuit-breakers for this type of application.

More information is given in IEEE Std. C37.011 [126].

6.4.9 TRV for last clearing poles / tests circuit topology

In Table 2 of IEC 62271-100:2001, multipliers for transient recovery voltage values for second and third clearing poles are given for circuit-breakers with rated voltages higher than 72,5 kV.

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Under NOTE 1, it is stated that for voltages equal to or lower than 72,5 kV, the values are under consideration.

For circuit-breakers with rated voltages equal to or lower than 72,5 kV, as not enough information is available to define values other than those specified for higher rated voltages, IEC SC17A has decided during its meeting in Montreal (CA), October 2003, to extend the validity of Table 2 to all rated voltages higher than 1 kV.

6.5 Calculation of TRVs

6.5.1 General

TRV parameters are defined as a function of the rated voltage (U_r), the rated first-pole-to-clear factor (k_{pp}) and the amplitude factor (k_{af}). k_{pp} is a function of the earthing of the system neutral. The rated values of k_{pp} are:

– 1,2 for terminal fault breaking by circuit-breakers with rated voltages higher than 800 kV in effectively earthed neutral systems;

– 1,3 for terminal fault breaking by circuit-breakers for rated voltages up to and including 800 kV in effectively earthed neutral systems;

– 1,5 for terminal fault breaking by circuit-breakers for rated voltages less than 245 kV in non-effectively earthed neutral systems.

6.5.2 Rated voltages less than 100 kV

A representation by two parameters of the prospective TRV is used for all test-duties.

– For circuit-breakers in cable systems.

  The TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ where k_{af} is equal to 1,4 for test-duty T100, 1,5 for test-duty T60, 1,6 for test duty T30 and 1,7 for test duty T10, 1,25 for out-of-phase breaking.

  Time t_3 for test-duty T100 is taken from Tables 24 and 43 of IEC 62271-100:2008 with IEC 62271-100:2008/AMD1:2012 and IEC 62271-100:2008/AMD2:2017. Time t_3 for test-duties T60, T30 and T10 is obtained by multiplying the time t_3 for test-duty T100 by 0,44 (for T60), 0,22 (for T30) and 0,22 (for T10).

– For circuit-breakers in line systems.

  TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ where k_{af} is equal to 1,54 for test-duty T100 and the supply side circuit for short-line fault, 1,65 for test-duty T60, 1,74 for test duty T30 and 1,8 for test duty T10, 1,25 for out-of-phase breaking.

  Time t_3 for test-duty T100 is taken from Tables 25 and 44 of IEC 62271-100:2008 with IEC 62271-100:2008/AMD1:2012 and IEC 62271-100:2008/AMD2:2017. Time t_3 for test-duties T60, T30 and T10 is obtained by multiplying the time t_3 for test-duty T100 by 0,67 (for T60), 0,40 (for T30) and 0,40 (for T10).

– Time delay t_d for test-duty T100 is $0{,}15\,t_3$ for cable systems, $0{,}05\,t_3$ for line systems, $0{,}05\,t_3$ for the supply side circuit for short-line fault.

– Time delay t_d is $0{,}15\,t_3$ for test-duties T60, T30 and T10 and for out-of-phase breaking.

– Voltage $u' = u_c/3$.

– Time t' is derived from u', t_3 and t_d according to Figure 97, $t' = t_d + t_3/3$.

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6.5.3 Rated voltages from 100 kV to 800 kV

A representation by four parameters of the prospective TRV is used for test-duties T100 and T60, and the supply circuit of SLF for test duties L_{90} and L_{75} and for out-of-phase test duties OP1 and OP2 and by two parameters for test-duties T30 and T10.

– First reference voltage $u_1 = 0{,}75 \times k_{pp} \times U_r \times \sqrt{2/3}$

– Time t_1 for terminal fault test duties is derived from u_1 and the specified value of the rate of rise u_1/t_1. For test duties OP1 and OP2, t_1 is two times t_1 for test duty T100 and the rate of rise is derived from u_1 and t_1.

– TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \times \sqrt{2/3}$

where k_{af} is equal to 1,4 for test-duty T100 and for the supply side circuit for SLF, 1,5 for test-duty T60, 1,54 for test-duty T30, 0,9 × 1,7 for test-duty T10, and 1,25 for out-of-phase breaking.

– Time t_2 is equal to $4t_1$ for test-duty T100 and for the supply side circuit for short-line fault and between t_2 (for T100) and $2t_2$ (for T100) for out-of-phase breaking. Time t_2 is equal to $6t_1$ for T60.

– For test-duties T30 and T10, time t_3 is derived from u_c and the specified value of the rate of Figure 96. Time delay t_d is 2 µs for test-duty T100, between 2 µs and $0{,}3t_1$ for test-duty T60, between 2 µs and $0{,}1t_1$ for test duties OP1 and OP2. Time delay is 0,15 t_3 for test-duties T30 and T10. For the supply side circuit for short-line fault the time delay is equal to 2 µs. When short-line fault tests are performed, the time delay t_d for test-duty T100 can be extended up to 0,28 t_1. The relevant value of t_d to be used for testing is given in 6.104.5.2 to 6.104.5.5 of IEC 62271-100:2008.

– Voltage u' = $u_1/2$ for test-duties T100 and T60 and the supply side for SLF and out-of-phase breaking, and $u_c/3$ for test-duties T30 and T10.

– Time t' is derived from u', u_1/t_1 and t_d for test-duties T100, T60 and the supply circuit for SLF and out-of-phase breaking, and in accordance with Figure 96; and from u', u_c/t_3 and t_d for test-duties T30 and T10 in accordance with Figure 97.

6.5.4 Rated voltages higher than 800 kV

A representation by four parameters of the prospective TRV is used for test-duties T100 and T60, and the supply circuit of SLF for test duties L_{90} and L_{75} and by two parameters for test-duties T30, T10 and for out-of-phase test duties OP1 and OP2.

– First reference voltage $u_1 = 0{,}75 \times k_{pp} \times U_r \times \sqrt{2/3}$

– Time t_1 for terminal fault test duties is derived from u_1 and the specified value of the rate of rise u_1/t_1.

– Time t_3 for out-of-phase test duties OP1 and OP2 is derived from u_c and the specified value of the rate of rise.

– TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \times \sqrt{2/3}$

where k_{af} is equal to 1,5 for test-duty T100 and for the supply side circuit for SLF, 1,5 for test-duty T60, 1,54 for test-duty T30, 1,76 for test-duty T10, and 1,25 for out-of-phase breaking.

– Time t_2 is equal to 3 t_1 for test-duty T100 and for the supply side circuit for short-line fault. Time t_2 is equal to 4,5 t_1 for T60.

– For test-duties T30 and T10, time t_3 is derived from u_c and the specified value of the rate of rise u_c/t_3.

– Time delay t_d is 2 µs for test-duty T100, between 2 µs and 0,3 t_1 for test-duty T60. Time delay is 0,15 t_3 for test duties T30 and T10, 0,05 t_3 for test duties OP1 and OP2. For the supply side circuit for short-line fault the time delay is equal to 2 µs. When short-line fault

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tests are performed, the time delay t_d for test-duty T100 can be extended up to 0,28 t_1. The relevant value of t_d to be used for testing is given in 6.104.5.2 to 6.104.5.5.

– Voltage u' = $u_1/2$ for test-duties T100 and T60 and the supply side for SLF, and $u_c/3$ for test-duties T30, T10 and out-of-phase test duties.

– Time t' is derived from u', u_1/t_1 and t_d for test-duties T100, T60 and the supply circuit for SLF, and in accordance with Figure 96; and from u', u_c/t_3 and t_d for test-duties T30, T10 and out-of-phase test duties in accordance with Figure 97.

7 Short-line faults

7.1 Short-line fault requirements

7.1.1 Basis for specification

Short-line fault (SLF) tests are made to prove the capability of a line circuit-breaker to break faults which occur from a few hundred meters up to several km down the line. They are due to numerous causes such as lightning, tree interfering with a line, etc.

These faults are characterised by a high short-circuit current and a rate of rise of the transient recovery voltage (RRRV) which is generally much higher than the values specified for other tests duties. The transient recovery voltage (TRV) applied to the circuit-breaker is a combination of a source side component, with a RRRV comparable to the value required for terminal fault tests, and a high frequency line side component.

The latter is caused by a travelling wave. This is initiated at the moment of current interruption and sent into the line to be reflected at the fault. The reflected wave is of triangular wave-shape and has a high RRRV which is imposed on the circuit-breaker open contacts on the line side.

The RRRV and the amplitude of the line side TRV as well as the magnitude of the short-circuit current depend on the distance of the fault location from the circuit-breaker, as well as the rated voltage and the source-side conditions.

In standardization it has been found advantageous to define the stress on the circuit-breaker in case of SLF by the relation between the corresponding short-circuit current I_L and the terminal fault current I_{sc} of T100 for the same source-side conditions: For example, in case of the 90 % short-line fault test duty L_{90}: $I_L = 0{,}9 \times I_{sc}$.

L_{90} corresponds to a fault distance of a few hundred meters to less than 2 km, the 75 % short-line fault test duty L_{75} to 1 km to 5 km.

An SLF interrupting capability is required for circuit-breakers designed for direct connection to overhead lines in systems having a rated voltage of 52 kV and above and a rated short-circuit current higher than 12,5 kA. This is explained below in the technical comment.

When required, SLF test duties are applicable to all types of circuit-breakers, regardless of their interrupting medium or technology. They must break short-line faults occurring at any practical value of line length. As explained in SLF testing (7.2.3.1) the range of currents specified is such that critical values for all kinds of interrupting medium and circuit-breaker technologies are likely to be covered.

The procedure to calculate the line side and source side transient recovery voltages under conditions of a short-line fault is described in detail in Annex A of IEC 62271-100:2008.

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7.1.2 Technical comment

For rated short-circuit currents lower than or equal to 12,5 kA the requirements in terms of RRRV and current (or di/dt) are considered to be covered by the basic terminal fault test duties.

For example, during SLF test duty L_{90} a circuit-breaker rated 100 kV, 12,5 kA – 50 Hz would have to withstand a RRRV of 2,25 kV/µs while interrupting 11,25 kA (di/dt = 5 A/µs). Under terminal fault test duty T100 at 100 % of 12,5kA (di/dt = 5,5 A/µs) it is tested to withstand a RRRV of 2 kV/µs.

As stated in 7.1.1, short-line faults tests apply to circuit-breakers directly connected to overhead lines. Direct connection is defined as a connection between the circuit-breaker and overhead line having a capacitance less than 5 nF. A time delay of more than 2 µs is obtained when a capacitance of 5 nF is added between the circuit-breaker and a line having a surge impedance of 450 Ω ($t_d = C \times Z = 5 \times 10^{-9} \times 450 = 2{,}25$ µs). It follows that the initial part of TRV is covered by terminal fault test duty T100s and the SLF test duty is not required in this case. For voltages lower than 52 kV the situation is discussed in CIGRE Technical Brochure 134 [~~9~~ 128] where it is recognised that the majority of connections to line circuits is made via cables, and in these systems SLF tests are generally not necessary. In the case of systems with overhead lines connected directly to the circuit-breaker without any length of cable, it is recommended to verify the SLF interrupting capability of the circuit-breaker.

7.1.3 Single-phase faults

SLF testing of circuit-breakers is based on single-phase faults because these faults are by far the most frequent. In addition, in effectively earthed systems, it corresponds to the condition of the last pole-to-clear which is the more severe condition for a three-phase fault.

This test condition covers also the case of the first-pole-to-clear of a three-phase fault in non-effectively earthed systems.

7.1.4 Surge impedance of the line

7.1.4.1 Surge impedance selection

For standardization purposes a surge impedance of 450 Ω adequately covers overhead line configurations up to and including 800 kV (see [16]).

For rated voltages of 1 100 kV and 1 200 kV, the surge impedance is 330 Ω.

7.1.4.2 Technical comment

The surge impedance is a function of many characteristics of a line (diameter, number, spacing, height of conductors), circuit configuration (single or double), earth resistivity and presence/type of earth wire.

For a symmetrical transmission line, the surge impedance for a single-phase fault (or the surge impedance for the last pole to clear a three-phase fault) is related to the positive and zero sequence surge impedances in the following way:

$$Z = \frac{2Z_1 + Z_0}{3} \tag{13}$$

where

Z_1 is the positive sequence surge impedance;

Z_0 is the zero sequence surge impedance.

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Typical values are given in 7.4.

Subclause 7.4 shows that for single circuit arrangements, the surge impedance is maximum when a pole clears when the others are already opened. This is also the case for double circuit constructions.

On transmission lines of system rated voltages up to and including 800 kV using bundled sub-conductor phase construction, the sub-conductors of a faulted phase are attracted together to constrict the effective diameter of the bundle during fault conditions. This changes the line impedance for that phase during the duration of the fault. This fact has been taken into account when evaluating and standardising the value of surge impedance. For rated voltages of 1 100 and 1 200 kV the value of 330 Ω is based on the fact that the individual conductors in the bundle do not make contact under the influence of a short-circuit.

Calculations performed on 420 kV lines have shown that the surge impedance is between 434 Ω and 456 Ω when bundle contraction during fault is considered [16].

Therefore, in the 4th edition of IEC 60056 a single value of 450 Ω was standardised irrespective of the number of conductors per phase as short-circuit conditions were similar to those of a single conductor line.

Even though values for single conductor lines could be found to be slightly higher, a surge impedance of 450 Ω adequately covers all practical cases for rated voltages up to and including 800 kV and 330 Ω for 1 100 kV and 1 200 kV, because when evaluating SLF parameters only the worst conditions are considered [17]:

– three-phase short-line fault at a critical distance;
– it is assumed that the supply has a single-phase short-circuit current equal to 100 % of the rated (3-phase) short-circuit current. In practice this is unlikely to happen as 100 % generation is generally not available and the single-phase short-circuit current is in many cases lower than the three-phase short-circuit current (see 7.2.6);
– in addition it is assumed that the impedance of earth return is negligible, whereas in practice this impedance effectively reduces the short-circuit current and the rate-of-rise of recovery voltage.

7.1.5 Peak voltage factor

7.1.5.1 Definition and selection of value

The peak factor (k) is the ratio of amplitudes of the first peak of the TRV on the line side (u_L*) to the peak voltage at the circuit-breaker terminals prior to interruption (u_0) (see Figure 16 of IEC 62271-100:2008).

As shown in 7.1.5.2 and 7.4, the standardised value of 1,6 adequately covers all practical values.

7.1.5.2 Technical comment

The peak factor (k) is given by:

$$k = \frac{u_L^*}{u_0} \tag{14}$$

The rate of rise of recovery voltage on the line side is equal to the product $Z \times \frac{di}{dt}$,

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where

Z is the surge impedance;

$\frac{\mathrm{d}i}{\mathrm{d}t} = \omega \times I_{\mathrm{L}} \times \sqrt{2}$ is the current derivative before interruption.

The time to the first peak u_{L}* is equal to two times the reflection time from the circuit-breaker to the fault point (time necessary for the travelling wave to reach the fault and be reflected back to the circuit-breaker):

$$\frac{2\lambda}{v} = t_{\mathrm{L}}$$

where

λ is the distance from the opening circuit-breaker to the fault;

v is the velocity of light.

The rate-of-rise of recovery voltage is then given by:

$$\frac{u_{\mathrm{L}}^{*}}{t_{\mathrm{L}}} = Z\frac{\mathrm{d}i}{\mathrm{d}t}$$

It follows that the first peak of the line side TRV is given by:

$$u_{\mathrm{L}}^{*} = Z\frac{\mathrm{d}i}{\mathrm{d}t} \times \frac{2\lambda}{v} \tag{15}$$

$$u_0 = X_{\mathrm{L}} \times \lambda \times I_{\mathrm{L}}\sqrt{2} \tag{16}$$

where

X_{L} is the line reactance per unit length.

From Equations (14), (15) and (16):

$$k = \frac{2\omega Z}{X_{\mathrm{L}} \times v} \tag{17}$$

$$X_{\mathrm{L}} = \frac{(2L_{1\mathrm{w}} + L_{0\mathrm{w}})\omega}{3} \tag{18}$$

where

$L_{1\mathrm{w}}$ is the positive sequence power frequency line inductance per unit length;

$L_{0\mathrm{w}}$ is the zero sequence power frequency line inductance per unit length.

$$Z_1 = \sqrt{\frac{L_1}{C_1}} \tag{19}$$

$$v = \frac{1}{\sqrt{L_1 C_1}} \tag{20}$$

where

L_1 is the high-frequency positive sequence line inductance per unit length;

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C_1 is the high-frequency positive sequence line capacitance per unit length.

From Equations (19) and (20):

$$\frac{Z_1}{v} = L_1 \tag{21}$$

Combining Equation (17) with Equation (13), (18) and (21) gives:

$$k = \frac{2L_1(2 + \frac{Z_0}{Z_1})}{2L_{1w} + L_{0w}} \tag{22}$$

If the high-frequency inductance L_1 is equal to the power frequency inductance of the line L_{1w}, Equation (22) simplifies to:

$$k = \frac{2(2 + \frac{Z_0}{Z_1})}{2 + \frac{L_{0w}}{L_{1w}}} \tag{23}$$

if $\frac{L_{0w}}{L_{1w}} = 3$ is assumed for high-voltage networks,

$$k = 0{,}4(2 + \frac{Z_0}{Z_1}) \tag{24}$$

In practice the high frequency inductance L_1 is lower than the power frequency value L_{1w}, and losses which are always present have been neglected in the calculation. For these reasons the peak factor obtained by Equation (23) is a conservative value.

Subclause 7.4 gives values of peak factors calculated for HV networks 72,5 kV to 550 kV. All the values obtained are equal or lower than 1,55. The specified value of 1,6 is therefore conservative.

7.1.6 Rate-of-Rise of Recovery Voltage (RRRV) factor "*s*"

7.1.6.1 General

The RRRV on the line side is given by $Z\frac{\mathrm{d}i}{\mathrm{d}t}$ or $Z \times \omega \times I_L\sqrt{2}$. For practical applications it is sometimes useful to express the RRRV as follows:

$$\text{RRRV} = s \times I_L, \text{ with } s = Z \times \omega\sqrt{2} \text{ and } \omega = 2\pi f_r$$

For rated frequencies (f_r) of 50 Hz and 60 Hz, and with Z= 450 Ω, the RRRV factor s is then equal to:

f_r = 50 Hz s = 0,20 kV/μskA

f_r = 60 Hz s = 0,24 kV/μskA

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7.2 SLF testing

7.2.1 Test voltage

As SLF tests are based on single-phase faults, the test voltage is equal to the phase to earth voltage i.e. the rated voltage divided by √3, with a first-pole-to-clear factor k_{pp} = 1,0.

7.2.2 Operating sequence

SLF is mainly a single-phase fault on a line. During network operation the fault is cleared by a circuit-breaker performing its rated operating duty: an auto-reclosing duty as usual for overhead line networks.

In order to reproduce service conditions, IEC 62271-100 requires circuit-breakers to perform their rated operating duty during testing.

7.2.3 Test duties

7.2.3.1 General

The severity of SLF tests depends on the position of the fault along the line length as it determines the magnitude of the current (and di/dt) and the transient recovery voltage characteristics: RRRV (proportional to di/dt) and first peak value (proportional to the reflection time from the circuit-breaker to the fault). Circuit-breakers must break short-line faults with any practical values of line length corresponding to fault currents ranging from tens of percent to about 90 % of the rated short-circuit current.

For example for a 145 kV, 40 kA, 60 Hz circuit-breaker, a short-line-fault test at 90 % of the rated short-circuit current corresponds in practice to a fault on the line occurring 330 m away from the circuit-breaker.

The critical percentage of short-circuit current is dependent on the interrupting medium of the circuit-breaker.

An arc in SF_6 has a very short time constant (less than 0,5 µs) i.e. its resistance or conductance changes rapidly during the transient recovery period. Therefore interruption is affected by the very high frequencies of TRV met in L_{90} test duty and the associated high values of the short-circuit current [18].

An arc in high pressure air has a longer time constant (typically 10 times the value in SF_6), so interruption is mostly affected by the lower frequencies and higher amplitudes met in L_{75}.

Other technologies such as oil or vacuum circuit-breakers have proved to be insensitive to short-line fault conditions, as long as they have the corresponding terminal fault breaking capability.

In order to cover the possible critical values of short-circuit current, two ranges of currents are specified for short-line fault tests, in percentage of the rated short-circuit current:

– test duty L_{90} with 90 % (-0 %, +2 %) of I_{sc};
– test duty L_{75} with 75 % (-4 %, +4 %) of I_{sc}.

If there is a significant increase of arcing time when the current is reduced from 90 % I_{sc} to 75 % I_{sc}, an additional series of tests with 60 % (± 5 %) I_{sc} (L_{60}) is required to confirm that there is no critical current in the 60 % to 75 % region.

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7.2.3.2 Technical comment

Compared to terminal fault conditions and assuming the same source side impedance as in the case of a 100 % terminal fault (T100) the short-circuit current in a short-line fault is lower as the line between circuit-breaker and fault introduces an additional impedance into the total circuit.

Standard values of the current I_L related to line length are specified corresponding to a reduction of the a.c. component of the rated short-circuit current to 90 % (L_{90}) and 75 % (L_{75}).

In IEC 62271-100 the line length has been standardised.

As the line length represented in a test may differ from the standardised value within a tolerance given in Annex B of IEC 62271-100:2008, the short-circuit current during tests may vary in the following ranges for circuit-breakers having rated voltages of 48,3 kV and above:

L_{90}:	I_L = 90 % of I_{sc}	(line length = standardised value)
	I_L = 92 % of I_{sc}	(line length = standardised value – 20%)
L_{75}:	I_L = 71 % of I_{sc}	(line length = standardised value + 20%)
	I_L = 79 % of I_{sc}	(line length = standardised value – 20%)

In cases (see c) of 6.109.4 of IEC 62271-100:2008) where a test duty L_{60} is required:

L_{60}:	I_L = 55 % of I_{sc}	(line length = standardised value + 20%)
	I_L = 65 % of I_{sc}	(line length = standardised value – 20%)

These values are derived from calculations given in 7.5.

NOTE Since the network topology and layout for 48,3 kV is identical to those of 52 kV and 72,5 kV, the value of 48,3 kV has been chosen as the lower value.

For circuit-breakers with voltage ratings equal to or higher than 15 kV and lower than 48,3 kV only test duty L_{75} has to be performed with a line length equal to the standardized value with a tolerance of +0 % and -20 %.

7.2.4 Test current asymmetry

7.2.4.1 General

The test current is symmetrical at contact separation (with a d.c. component less than 20 %) because the most severe condition is obtained in the thermal phase of interruption when the current derivative ($\frac{di}{dt}$) and the RRRV ($Z\frac{di}{dt}$) are maximum.

7.2.4.2 Technical comment

It is recognised that lightning strikes are the most likely events leading to a short-line fault. As these are random events in relation to the point on the voltage cycle they will generally lead to asymmetrical currents. However the d.c. component of this current decreases more rapidly for a line fault than for other faults due to the high value of resistance in the earth return circuit. Therefore for the most likely system condition giving SLF, although asymmetrical at initiation, will approach the symmetrical condition or at least a low degree of asymmetry, by the time of current interruption by the circuit-breaker.

Based on the above SLF breaking tests need not be asymmetrical. As a result the simpler test regime of symmetrical testing has been standardised on for this duty.

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SLF breaking tests with asymmetrical currents are also not required because when compared with symmetrical conditions, the $\frac{di}{dt}$ at current zero and RRRV ($Z\frac{di}{dt}$) applied on circuit-breakers are reduced.

7.2.5 Line side time delay

The local capacitance always present in a substation between the circuit-breaker and the line introduce a time delay t_{dL} in the initial part of the line side TRV. This capacitance represents the typical capacitance that can be met in actual networks. It is for example introduced by supports and stray capacitance of the connection between the circuit-breaker and the faulted line.

For rated voltages equal and lower than 170 kV, the time delay t_{dL} is standardised to 0,2 μs.

For rated voltages equal to and higher than 245 kV, it is standardised to 0,5 μs.

These values correspond to a line side phase to earth capacitance C_{dL} equal to 445 pF and 1 110 pF, respectively.

NOTE In order to cover the ITRV requirement, where it is specified on the supply side (see 6.104.5.2 and 6.109.3 of IEC 62271-100:2008), the SLF tests are generally performed with an insignificant time delay (less than 0,1 μs) on the line side. ITRV specification is not applicable to circuit-breakers in Gas Insulated Substations.

7.2.6 Supply side circuit

7.2.6.1 Supply side circuit definition

The short-circuit impedance of the supply side circuit is such that the rated short-circuit current is obtained in terminal fault conditions. This is due to the fact that the single-phase short-circuit current is assumed to be equal to the three-phase short-circuit current.

For rated voltages equal to or higher than 15 kV and less than 100 kV, it is assumed that the TRV frequency and the amplitude factor of the supply circuit are the same as for a three-phase terminal fault. It follows that the RRRV of the supply side circuit is equal to the RRRV of the circuit for terminal fault test duty T100s divided by 1,5, and the amplitude factor is 1,54.

For rated voltages equal to 100 kV and above, the supply side RRRV is equal to the RRRV specified for three-phase faults.

The supply side TRV is adjusted to obtain the crest value according to the first-pole-to-clear factor 1,0 and amplitude factor 1,4. The RRRV of 2,0 kV/μs is retained. The time parameters (t_3 or t_1 and t_2) are adjusted accordingly.

7.2.6.2 Technical comment

System studies have shown that the supply side RRRV is, as a first approximation, equal to the RRRV defined for three-phase faults [19]. Such an approximation is justified as the RRRV is equal to the product $Z\frac{di}{dt}$, with the supply side surge impedance Z and the current derivative ($\frac{di}{dt}$) having similar values for single-phase and three-phase conditions.

Generally speaking the supply side RRRV for single-phase faults is slightly lower than for three-phase faults. This has been supported by TRV studies in 420 kV networks [19]. However, as there is a large scatter of values, the RRRV for a single phase terminal fault, corresponding to the supply side TRV in the case of a short-line fault, has been standardised

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to be the same value 2 kV/μs for rated voltages equal or higher than 100 kV as defined for three-phase faults.

During a SLF breaking operation, the voltage at the circuit-breaker terminals at current zero is equal to the voltage drop on the faulted line and is not zero as would be the case under terminal fault conditions. It follows that the TRV voltages on the supply side during SLF interruption are accordingly lower than the inherent values defined previously.

During test duties L_{90} and L_{75}, and neglecting the influence of the circuit-breaker, the source side TRV peak is reduced by a factor 1,36/1,4 and 1,30/1,4, respectively. The derivation of TRV peak values is explained in Annex A of IEC 62271-100:2008.

7.3 Additional explanations on SLF

7.3.1 Surge impedance evaluation

7.3.1.1 General

The surge impedance is the ratio of the TRV slope ($\frac{\mathrm{d}u}{\mathrm{d}t}$ or RRRV) divided by the current derivative $\frac{\mathrm{d}i}{\mathrm{d}t}$. The RRRV is defined as the slope between the points corresponding to 20 % and 80 % of the line side TRV peak of the inherent test circuit response.

7.3.1.2 Technical comment

In the case of very short lines between the opening circuit-breaker and the fault, with $t_L < 5\ t_{dL}$, the wave shape of the line side TRV is deformed and cannot be compared to a triangular shape with an initial time delay.

The curves presented in 7.6 show that for a correct evaluation of the surge impedance it is necessary to define the rate of rise of the line side recovery voltage as the slope between the points corresponding to 20 % and 80 % of the peak voltage, as in this region the shape is not influenced by the time delaying capacitance.

Although the previous 10 % to 90 % method leads also to correct values where $t_L \geq 5t_{dL}$, this 20 % to 80 % method is generalised for the evaluation of inherent line side TRVs in the 1st edition of IEC 62271-100.

7.3.2 Influence of additional capacitors on SLF interruption

7.3.2.1 General

Additional capacitance connected between the circuit-breaker terminals (grading capacitor or capacitor used to assist the interruption) or line-to-earth, has two effects:

– it decreases the oscillation frequency and the RRRV of the line side TRV;
– it increases the time delay of the line side TRV.

Both effects tend to ease the interruption, and capacitors are sometimes used to increase the short-line fault breaking capability of circuit-breakers.

Historically resistors where used in air-blast circuit-breakers resistors to reduce the RRRV and facilitate the interruption. RRRV is reduced by a factor $\frac{R}{R+Z}$ where R is the resistor value and Z the surge impedance of the line.

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7.3.2.2 Reduction of the line side RRRV by a phase to earth capacitor

As SF_6 circuit-breakers are more sensitive to the initial part of the TRV (first μs) the use of additional capacitors has proved to be more efficient.

When capacitors mounted across the circuit-breaker terminals are used to meet a SLF breaking capability, caution is recommended as high values of capacitance could lead to ferro-resonance with electromagnetic instrument transformers connected between the circuit-breaker and a de-energized line or connected to a supposedly de-energized bus.

If the capacitor is connected phase to earth on the line side, the reduction of the line side RRRV can be estimated by a simple calculation:

Definitions:

C_{add} is the additional line-to-earth capacitance;

L is the line inductance;

Z is the line surge impedance;

C_L is the total line capacitance = $\frac{L}{Z^2}$;

C_e is the equivalent line capacitance.

The equivalent line capacitance C_e is defined as the capacitance which, together with the inductance L, gives the line frequency of oscillation:

$$f_L = \frac{1}{2\pi\sqrt{LC_e}} \tag{25}$$

The period of oscillation is equal to $\frac{2u_L^*}{\left(\frac{du}{dt}\right)_L}$ with:

$$u_L^* = 2X_L \times I_L\sqrt{2} \quad \text{and} \quad \left(\frac{du}{dt}\right)_L = Z \times \omega \times I_L\sqrt{2}$$

It follows that:

$$f_L = \frac{Z \times \omega}{4X_L} \tag{26}$$

From Equations (25) and (26):

$$C_e = \frac{4L}{\pi^2 \times Z^2} = \frac{4C_L}{\pi^2} = 0{,}4C_L \tag{27}$$

If an additional capacitance is added at the line entrance, the RRRV on the line side is reduced in the same manner as the line frequency of oscillation:

$$\frac{du}{dt} = Z \times \omega \times I_L\sqrt{2}\,\frac{2\pi\sqrt{LC_e}}{2\pi\sqrt{L(C_e + C_{add})}}$$

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Using Equation (27) gives:

$$\frac{\mathrm{d}u}{\mathrm{d}t} = Z \times \omega \times I_{\mathrm{L}} \sqrt{2}\, \frac{\sqrt{C_{\mathrm{L}}}}{\sqrt{C_{\mathrm{L}} + 2{,}5 C_{\mathrm{add}}}}, \text{ or } \frac{\mathrm{d}u}{\mathrm{d}t} = Z \times \omega \times I_{\mathrm{L}} \sqrt{2} \sqrt{\frac{C_{\mathrm{L}}}{C_{\mathrm{L}} + 2{,}5 C_{\mathrm{add}}}} \quad (28)$$

with $C_{\mathrm{L}} = \frac{L}{Z^2}$

Equation (28) can be used in practice to estimate the effect of a phase-to-earth capacitance C_{add} on the line side rate of rise of recovery voltage.

The method presented in 7.6 can also be used to evaluate the effect of a capacitance on the line side TRV in more detail. The time delay t_{dL} is calculated by taking into account the total capacitance on the line side, i.e. line capacitance plus additional capacitance from the circuit-breaker (see Figure 17).

The reduction of the line side RRRV by a phase to earth capacitor is especially important to be reproduced in synthetic testing where the capacitor must be installed in parallel to the line. If, for practical reasons the capacitor is connected in parallel to the circuit-breaker, then its value shall be calculated (by Electromagnetic Transient Program or equivalent) to produce an equivalent TRV.

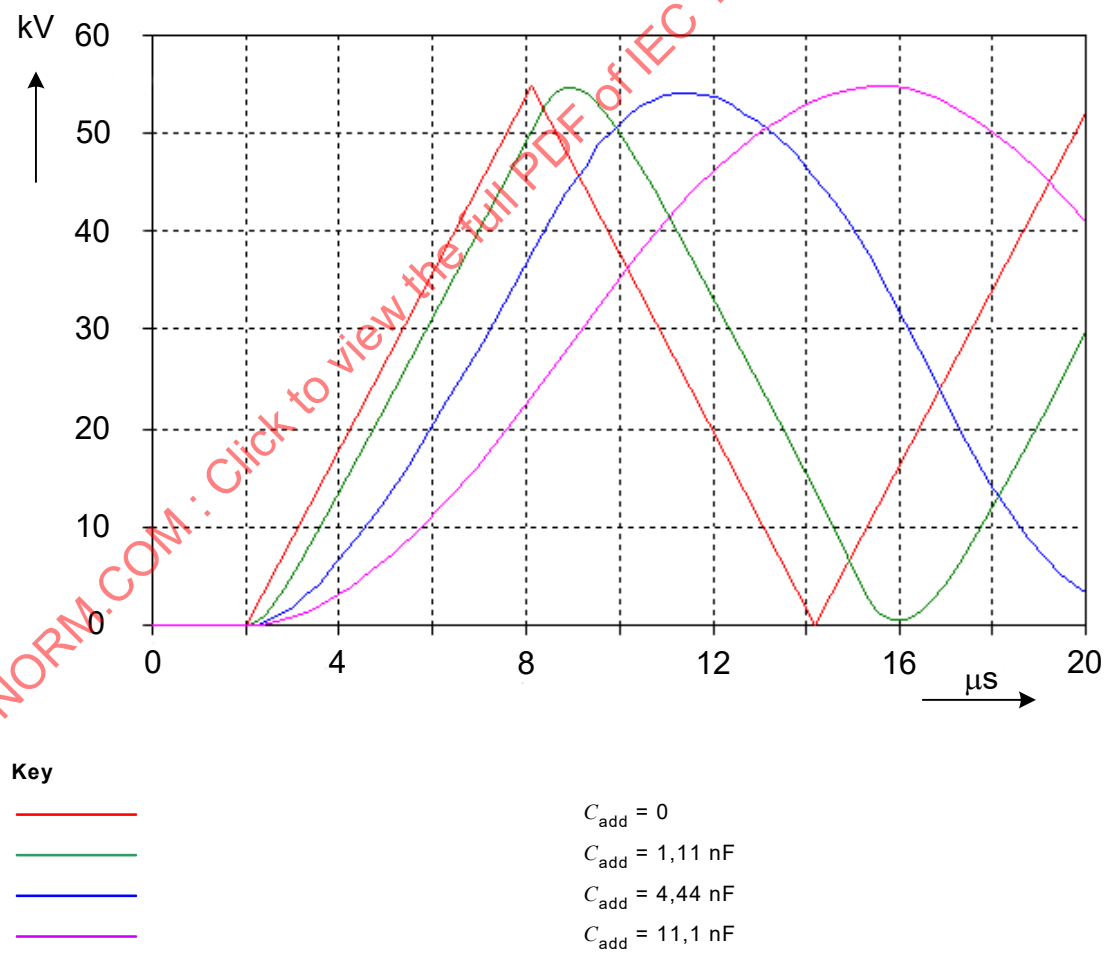

Figure 17 – Effects of capacitor size on the short-line fault component of recovery voltage with a fault 915 m from circuit-breaker

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7.3.2.3 Influence of the location of phase-to-earth capacitors

In a substation it can be advantageous to take into account the existing phase-to-earth capacitances between the circuit-breaker and the line (such as cables, GIS bus, CVTs) in order to define the necessary additional value of the phase-to-earth capacitor which has to be delivered with the circuit-breaker. However caution is recommended if the circuit-breaker is to be moved to a different location.

For maximum effectiveness the capacitor should be close to the circuit-breaker terminal.

CVTs due to their inherent capacitance have an influence on the TRV, but as shown in Figure 18, taken from [20], caution is necessary because to be of benefit they shall be close enough to the circuit-breaker to influence current interruption. Figure 18 shows that if the capacitor is located too far from the circuit-breaker, the time delay of the recovery voltage is decreased and the amplitude of the first voltage jump is increased, both effects resulting in a lowering of the benefit of the capacitance to the circuit-breaker interruption capability.

Based on these considerations if a smaller value of the phase-to-earth capacitor is used compared to that applied for type testing to take the existing phase-to-ground capacitance in the substation into account, it is recommended to calculate its final value by Electromagnetic Transient Program or equivalent to produce an equivalent TRV of the lumped capacitor used for testing.

This calculation has to be repeated if the location of the circuit-breaker or the substation configuration changes (a CVT is substituted by another one having a different capacitance, a cable is substituted by a bus bar connection).

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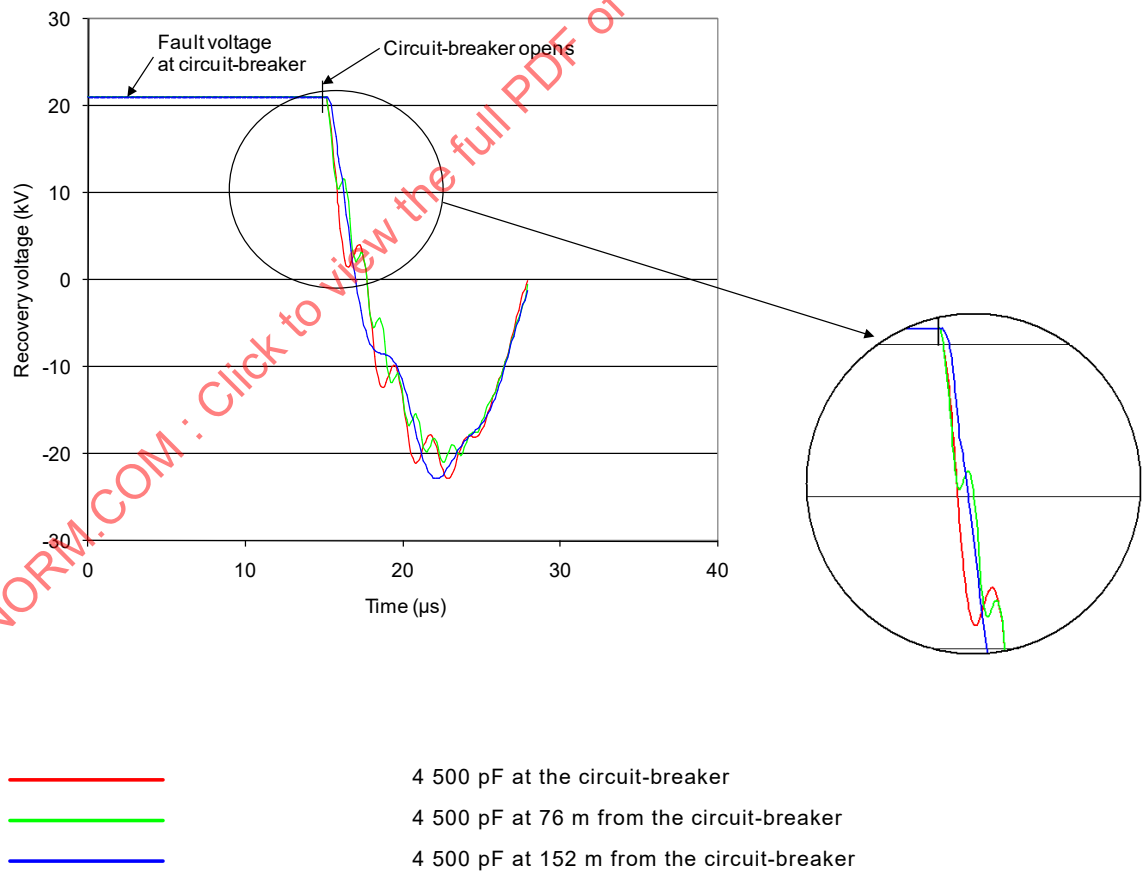


Figure 18 – Effect of capacitor location on short-line fault component of transient recovery voltage with a fault 760 m from circuit-breaker

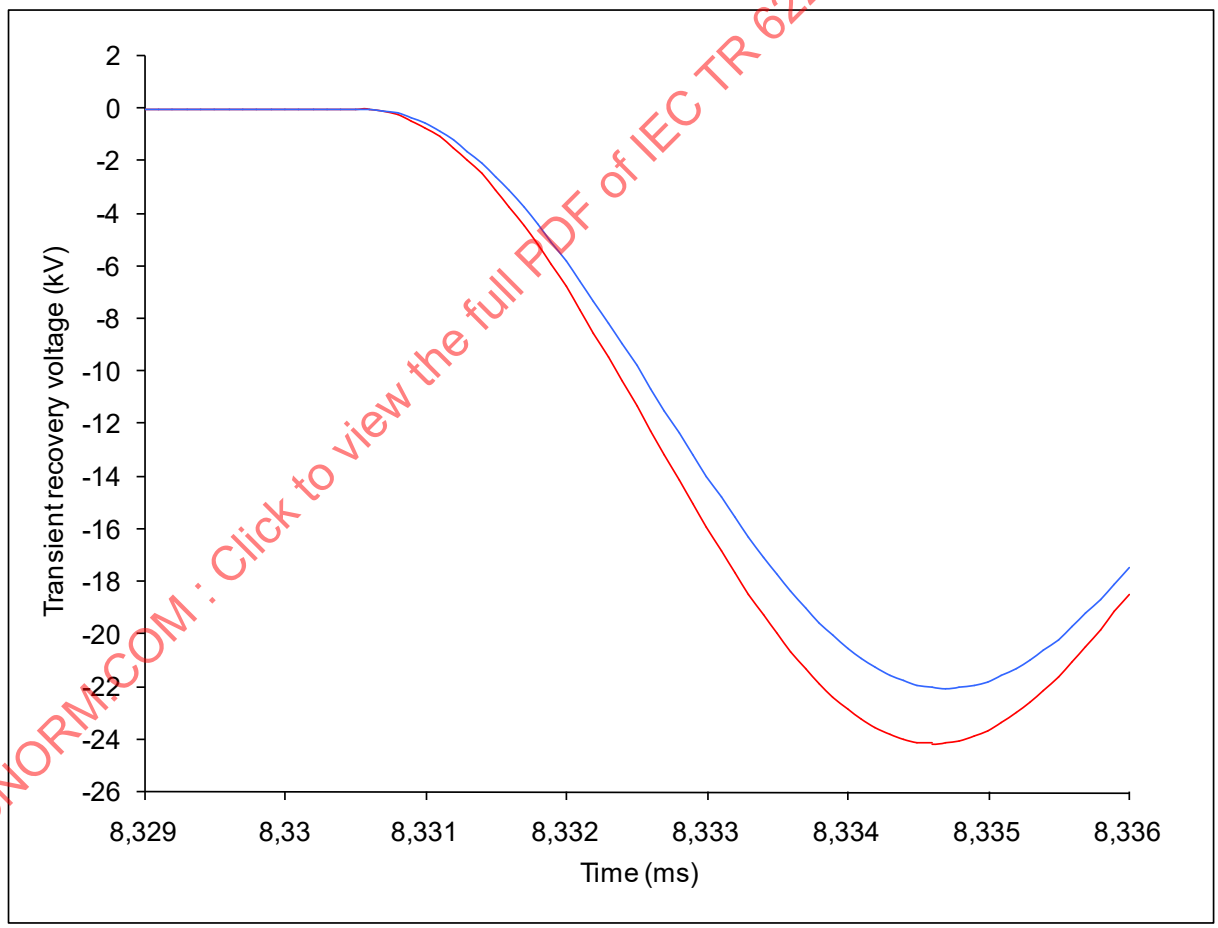
7.3.2.4 Relative influence of phase to earth and parallel capacitors

When circuit-breakers are fitted with capacitors between terminals (grading capacitors for example) the frequency of the line side oscillation is reduced in a similar way as with a phase to earth capacitor, but the effect of a given value of capacitance is different as the TRV is affected on both sides of the circuit-breaker. A lower value of capacitor is needed to obtain a given reduction of the TRV if it is connected between the terminals instead of phase-to-earth.

Figure 19 shows the TRV calculated obtained during a L_{90} test duty on a 145 kV, 50 kA, 60 Hz circuit-breaker with an additional capacitor of 3 nF connected phase-to-earth (curve 1: maximum slope from the instant of interruption = 6,91 kV/μs) or between terminals (curve 2: maximum slope from the instant of interruption = 6,18 kV/μs).

As the effects of parallel (between terminals) or phase-to-earth capacitors are not the same, it is important to indicate in the type test report the position of any additional capacitor. The relevant capacitance is the one measured at the circuit-breaker line side terminal. The capacitance used for measurements is already taken into account in the adjustment of the line side TRV.

It should be noted that the parallel capacitor is part of the circuit-breaker and that the TRV modified by the capacitor does not need to be compensated.



Key

Red trace	Additional capacitor of 3 nF connected phase-to-earth
Blue trace	Additional capacitor of 3 nF connected between terminals

Figure 19 – TRV obtained during a L_{90} test duty on a 145 kV, 50 kA, 60 Hz circuit-breaker

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7.4 Comparison of surge impedances

Table 11 shows a comparison of the typical values of the surge impedances for single-phase fault (or the third pole to clear a three-phase fault) and the first pole to clear a three-phase fault.

Table 11 – Comparison of typical values of surge impedances for a single-phase fault (or third pole to clear a three-phase fault) and the first pole to clear a three-phase fault

U_r (kV)	123		245		420	
Z_1 (Ω)	375	350	365	300	240	235
Z_0 (Ω)	680	655	585	465	450	445
peak factor k (p.u.)	1,55	1,55	1,52	1,43	1,41	1,34
Z single-phase fault (Ω)	476	452	438	355	310	305
Z 1st pole to clear a three-phase fault (Ω)	440	414	416	340	284	279
Z is the surge impedance. Z_1 is the positive sequence surge impedance. Z_0 is the zero sequence surge impedance.						

7.5 ~~Calculation of actual percentage of SLF breaking currents~~ Test current and line length tolerances for short-line fault testing

~~The line reactance corresponding to the standardised line length can be calculated with~~

$$X_{L,stand} = \frac{1 - \frac{I_{L,stand}}{I_{sc}}}{\frac{I_{L,stand}}{I_{sc}}} \times X_{source}$$

~~where~~

~~$I_{L,stand}$ is the short-line fault breaking current corresponding to the standardised line length;~~

~~$X_{L,stand}$ is the line reactance corresponding to the standardised line length;~~

~~X_{source} is the reactance corresponding to the rated short-circuit breaking current.~~

~~If the reactance of the actual line differs from the reactance corresponding to the standardised line length within the tolerances of -20 % for L_{90} and ±20 % for L_{75} and L_{60}, as stated in 6.109.2 of IEC 62271-100:2008, the related current values can be calculated as follows:~~

$$I_{L,act} = \frac{U_r}{\sqrt{3}\,(X_{L,act} + X_{source})}$$

~~where~~

~~$I_{L,act}$ is the short-line fault breaking current corresponding to the actual line length;~~

~~$X_{L,act}$ is the line reactance corresponding to the actual line length.~~

~~The actual line length is calculated considering the standardised line length and the percentage deviation of the actual line length from the standardised one:~~

$$l_{act} = l_{stand}\left(1 + \frac{d}{100}\right)$$

~~where~~

~~l_{stand} is the standardised line length;~~

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~~l_{act} is the actual line length;~~

~~d is the deviation of the actual line length from the standardised one in percent.~~

~~The actual line reactance is calculated using the following equation:~~

$$X_{L,act} = X_{L,stand} \times \frac{l_{act}}{l_{stand}} = X_{L,stand}\left(1 + \frac{d}{100}\right)$$

~~The actual percentage short-line fault breaking current $I_{perc,act}$ is determined by the following equation:~~

$$I_{perc,act} = \frac{I_{L,act}}{I_{sc}} \times 100 = \frac{I_{perc,stand}}{1 + \frac{d}{100} \times \left(1 - \frac{I_{perc,stand}}{100}\right)}$$

~~In Table 12 the actual percentage short-line fault breaking currents are stated for each standardised short-line fault breaking current $I_{perc,stand}$ taking the maximum tolerances for the line length into account.~~

~~Table 12 – Actual percentage short-line fault breaking currents~~

~~Standardised short-line fault breaking current $I_{perc,stand}$ (%)~~	~~Deviation d (%)~~	~~Actual short-line fault breaking current $I_{perc,act}$ (%)~~
~~90~~	~~–20~~	~~91,8~~
~~90~~	~~0~~	~~90~~
~~75~~	~~–20~~	~~78,9~~
~~75~~	~~±20~~	~~71,4~~
~~60~~	~~–20~~	~~65,2~~
~~60~~	~~±20~~	~~55,5~~

The line reactance corresponding to the standardised line length can be calculated as follows:

$$X_{L,\,stand} = \frac{1 - \frac{I_{L,\,stand}}{I_{sc}}}{\frac{I_{L,\,stand}}{I_{sc}}} X_{source}$$

where

$I_{L,stand}$ is the short-line fault breaking current corresponding to the standardised line length;

I_{sc} is the rated short-circuit current;

$X_{L,stand}$ is the line reactance corresponding to the standardised line length;

X_{source} is the reactance corresponding to the rated short-circuit breaking current.

If the reactance of the line applied in practice differs from the reactance corresponding to the standardised line length within the tolerances of –20 % for L_{90} and ±20 % for L_{75} and L_{60}, as stated in 6.109.2 of IEC 62271-100:2008, the related current values can be calculated as follows:

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$$I_{\mathrm{L,\,act}} = \frac{U_{\mathrm{r}}}{\sqrt{3}\left(X_{\mathrm{L,\,act}} + X_{\mathrm{source}}\right)}$$

where

$I_{\mathrm{L,act}}$ is the short-line fault breaking current corresponding to the actual line length;

$X_{\mathrm{L,act}}$ is the line reactance corresponding to the actual line length.

The actual line length is calculated considering the standardised line length and the percentage deviation of the actual line length from the standardised one:

$$I_{\mathrm{act}} = I_{\mathrm{stand}}\left(1 + \frac{d}{100}\right)$$

where

l_{stand} is the standardised line length;

l_{act} is the actual line length;

d is the deviation of the actual line length from the standardised line length in percent.

The actual line reactance is calculated using the following equation:

$$X_{\mathrm{L,\,act}} = X_{\mathrm{L,\,stand}} \times \frac{I_{\mathrm{act}}}{I_{\mathrm{stand}}} = X_{\mathrm{L,\,stand}}\left(1 + \frac{d}{100}\right)$$

The actual percentage short-line fault breaking current $I_{\mathrm{perc,act}}$ is determined by the following equation:

$$I_{\mathrm{perc,\,act}} = \frac{I_{\mathrm{L,\,act}}}{I_{\mathrm{sc}}} \times 100 = \frac{I_{\mathrm{perc,\,stand}}}{1 + \frac{d}{100}\left(1 - \frac{I_{\mathrm{perc,\,stand}}}{100}\right)}$$

In Table 42 the actual percentage short-line fault breaking currents are stated for each standardised short-line fault breaking current $I_{\mathrm{perc,stand}}$ taking the maximum tolerances for the line length into account.

Table 42 – Actual percentage short-line fault breaking currents

Standardised short-line fault breaking current $I_{\mathrm{perc,stand}}$ %	Deviation of the line length d %	Actual short-line fault breaking current $I_{\mathrm{perc,act}}$ %
90	–20	91,8
90	0	90
75	–20	78,9
75	+20	71,4
60	–20	65,2
60	+20	55,5

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7.6 TRV with parallel capacitance

The short-line fault TRV from an idealised distributed parameter line is known as a triangular wave shape. In the Laplace domain, this can be written as follows:

$$\mathrm{TRV}(s) = \frac{\omega IZ}{s^2}(1 - 2\mathrm{e}^{-t_{\mathrm{L}}s}) \tag{29}$$

where

t_{L} is the time to peak without capacitance;

ω is the angular frequency of the breaking current;

I is the breaking current peak;

Z is the surge impedance;

s is the Laplace operator.

Equation (29) is valid for $0 \le t \le 2t_{\mathrm{L}}$. If the TRV for $t > 2t_{\mathrm{L}}$ is required, Equation (29) should be replaced by the following:

$$\mathrm{TRV}(s) = \frac{\omega IZ}{s^2}(1 - 2\mathrm{e}^{-t_{\mathrm{L}}s} + 2\mathrm{e}^{-2t_{\mathrm{L}}s} + \ldots\ldots) \tag{30}$$

In order to introduce damping of the wave, the term $2\mathrm{e}^{-t_{\mathrm{L}}s}$ in Equation (29) should be replaced by $2k\mathrm{e}^{-t_{\mathrm{L}}s}$, where $k < 1{,}0$.

The TRV can be represented by the product of the breaking (= injection) current and the impedance, also in the Laplace domain. The injection current in the Laplace domain can be approximated such as:

$$\frac{\omega I^2}{s^2} \quad \text{(corresponding to } \omega It \text{ in the time domain)}$$

Then the impedance of the distributed parameter line in Laplace domain is:

$$Z(1 - 2\mathrm{e}^{-t_{\mathrm{L}}s}) \tag{31}$$

The lumped capacitance impedance in the Laplace domain is represented by:

$\frac{1}{Cs}$, where C = capacitance

The capacitance value includes both the lumped capacitance at the circuit-breaker terminal side producing the inherent t_{dL} of the line and the additional capacitance, if any.

Connecting the two impedances represented by Equations (30) and (31) in parallel, the following equation is obtained for the total impedance in the Laplace domain:

$$\frac{Z(1 - 2\mathrm{e}^{-t_{\mathrm{L}}s})}{Cs\left(\frac{1}{Cs} + Z - 2Z\mathrm{e}^{-t_{\mathrm{L}}s}\right)} = \frac{Z(1 - 2\mathrm{e}^{-t_{\mathrm{L}}s})}{(1 + t_{\mathrm{dL}}s) - 2t_{\mathrm{dL}}s\mathrm{e}^{-t_{\mathrm{L}}s}} \tag{32}$$

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where $t_{dL} = ZC$.

t_{dL} is applicable also for conditions with parallel additional capacitances.

The product of the injection current ($\omega I/s^2$) and the impedance Equation (32) is the TRV with parallel capacitance in the Laplace domain:

$$\omega IZ \times \frac{1}{s^2} \times \frac{(1-2e^{-t_L s})}{(1+t_{dL}s)-2t_{dL}se^{-t_L s}}$$

$$= \omega IZ\left[\frac{1}{s^2} \times \frac{1}{1+t_{dL}s} - \frac{1}{s^2} \cdot \frac{2e^{-t_L s}}{(1+t_{dL}s)^2} + \ldots\ldots\ldots\right]$$

$$= \omega IZ\left[\frac{1}{s^2} - \frac{t_{dL}}{s} + \frac{t_{dL}^2}{1+t_{dL}s} - 2e^{-t_L s}\left(\frac{1}{s^2} - \frac{2t_{dL}}{s} + \frac{2t_{dL}^2}{1+t_{dL}s} - \frac{t_{dL}^2}{(1+t_{dL}s)^2}\right)\right] \quad (33)$$

The second line of Equation (33) is valid for $t_L \le t \le 2t_L$ only.

By inverse Laplace transformation, SLF TRV with parallel capacitance in time domain is calculated as follows:

$0 \le t \le t_L$:

$$TRV_1(t) = \omega IZ\left[t + t_{dL}\left(e^{-\frac{t}{t_{dL}}} - 1\right)\right] \quad (34)$$

$t_L \le t \le 2t_L$

$$TRV_2(t) = TRV_1(t) - 2\omega IZ\left[t'\left(e^{-\frac{t'}{t_{dL}}} + 1\right) + 2t_{dL}\left(e^{-\frac{t'}{t_{dL}}} - 1\right)\right] \quad (35)$$

with $t' = t - t_L$.

Using equations (34) and (35), the correct waveshapes of SLF TRVs with line inherent t_{dL} and for conditions with additional parallel capacitance can be calculated.

For cases $t > 2t_L$, Equation (30) instead of Equation (29) should be applied. When damping is introduced, $2ke^{-t_L s}$ should be used instead of $2e^{-t_L s}$ in Equation (29) as mentioned before. The total calculation process is then slightly modified.

For every case, with or without parallel capacitance, the peak value of the TRV is quasi equal to ωIZt_L. Dividing Equations (34) and (35) by ωIZt_L, gives the following equations.

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$$\mathrm{TRV}(10) = \frac{t_{\mathrm{dL}}}{t_{\mathrm{L}}}\left[\frac{t}{t_{\mathrm{dL}}} + \left(\mathrm{e}^{-\frac{t}{t_{\mathrm{dL}}}} - 1\right)\right] \tag{36}$$

$$\mathrm{TRV}(20) = \mathrm{TRV}(10) - \frac{2t_{\mathrm{dL}}}{t_{\mathrm{L}}}\left[\frac{t'}{t_{\mathrm{dL}}}\left(\mathrm{e}^{\frac{-t'}{t_{\mathrm{dL}}}} + 1\right) + 2\left(\mathrm{e}^{\frac{-t'}{t_{\mathrm{dL}}}} - 1\right)\right] \tag{37}$$

The TRV wave shape given by Equations (36) and (37) can be normalised such that the peak value is unity and time unit is in t_{dL}. The parameter is $t_{\mathrm{L}}/t_{\mathrm{dL}}$.

Figure 20 shows the results of a calculation for $t_{\mathrm{L}}/t_{\mathrm{dL}}$ = 4,0. Multiplying the Y-axis value by ωIZt_{L} and X-axis value by t_{dL}, the actual wave shape is obtained.

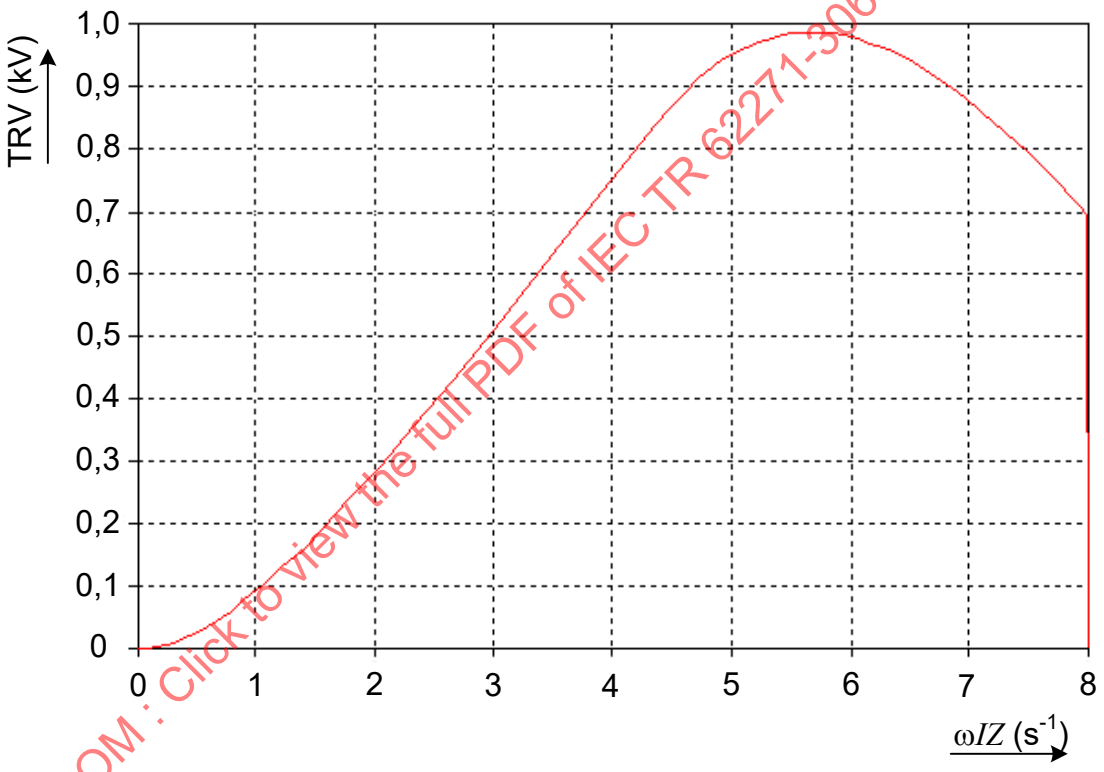

Figure 20 – TRV vs. ωIZ as function of t/t_{dL} when $t_{\mathrm{L}}/t_{\mathrm{dL}}$ = 4,0

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8 Out-of-phase switching

8.1 Reference system conditions

8.1.1 General

Although the out-of-phase switching condition is a rare occurrence, two cases are considered to illustrate the background to the standard requirements of IEC 62271-100.

Case A Instability of a system in service, due to overloading, load rejection, or other major disturbance such as that caused during a severe storm, etc.;

Case B Erroneous switching operation during synchronizing.

8.1.2 Case A

The system conditions illustrated above are often considered in power system stability studies. In such events, as the parts of the system separate the out-of-phase occurs across an impedance in a system, where it can be assumed a heavy load current exists. Out-of-phase breaking is initiated by a protective system detecting the voltage phase angle difference across the impedance and sending a tripping signal to the associated circuit-breakers. The first to open of these will experience the out-of-phase condition. Studies indicate that during such disturbances, the phase angles of the individual generators scatter so that it is unlikely that the two sections will have a simple, uniform phase angle between them. Also, a densely connected part of a system can rarely be separated to be out-of-phase with the rest of the system.

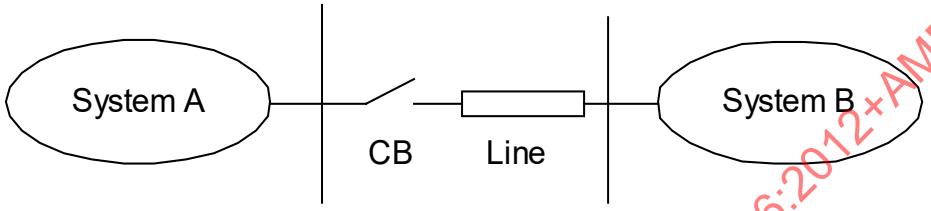

Figure 21 – Typical system configuration for out-of-phase breaking for case A

Figure 21 is a representation of a separating system where a line is the link between the two separate parts, i.e. system A and system B. The connecting line (or impedance such as a transformer) exists in between. Each of system A and B is considered to be corresponding to a system operating at its T30 to T60 short-circuit level.

Cases where the short-circuit power of both systems A and B correspond to T100 can be considered exceptional.

Cases with a weak sub-system on one side can be considered covered by case B with regard to TRV parameters.

8.1.3 Case B

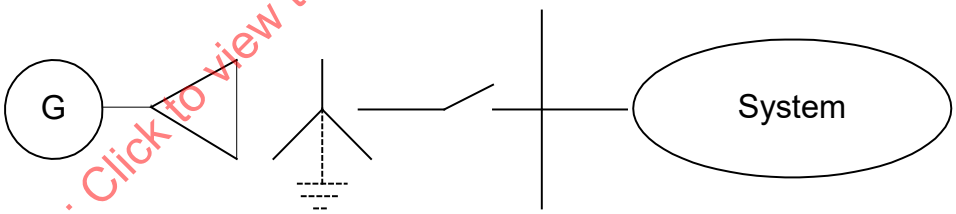

Figure 22 – Typical system configuration for out-of-phase breaking for Case B

Synchronizing between relatively strong systems can be considered a rare case and is covered by case A with regard to TRVs.

A more typical system layout for synchronizing is shown in Figure 22, where a generator interfaces with a system via a step up transformer. The right-hand side system short-circuit power can be considered to be corresponding to a T60 level. In such systems, a synchronizing operation is mostly performed at the high-voltage side of the step-up transformer. Typical characteristics are:

– generator sub-transient reactance is 0,3 p.u.;
– step-up transformer reactance is 0,1 p.u.

Present day maximum ratings of generator units are in the order of 600 MVA and 1 300 MVA for 245 kV and 550 kV, respectively. Introducing, also, the short-circuit reactance of the

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system, the out-of-phase breaking current (generator-side short-circuit current on the high-voltage side) is 0,5 kA up to 8 kA for most common applications.

The following points are also to be considered:

– due to the connection of the transformer windings, i.e., Δ on the LV side and Y on the HV side, for solidly earthed systems, the zero sequence reactance of the generator side is far lower than that of positive sequence, i.e. ca. 25 %. Therefore the pole-to-clear factor is maximum for the 3rd pole, and is 1,0;
– the recovery voltage of the generator after the fault current has been cleared is heavily damped, giving a damping factor in the order of 0,8;
– statistically a 180 degree out-of-phase condition very rarely occurs in practice and an additional factor of 0,8 can be introduced.

8.2 TRV parameters introduced into Tables 1b and 1c of the first edition of IEC 62271-100

8.2.1 General

As rated TRV parameters in tables 1b, 1c and 1d of the first edition of IEC 62271-100 published in 2001, system requirements and experiences based on circuit-breaker characteristics and other duties, i.e. terminal faults, etc., are to be considered.

8.2.2 Case A

8.2.2.1 Breaking current

The breaking current listed is 25 % of the rated short-circuit breaking current.

As shown before, actual out-of-phase occurs between the portions of a system via a certain impedance. As already noted, it is unlikely that a perfect 180 degree of out-of-phase will ever occur. The value 25 % is taken to cover the majority of cases.

8.2.2.2 First-pole-to-clear factor

A first-pole-to-clear factor of 2,0/2,5 is specified by IEC 62271-100 for effectively/non-effectively earthed systems, respectively.

The theoretical maximum values are 2,6/3,0, but stability studies have shown that the phase angles of the individual generators are scattered. This fact has been taken into account by introducing a factor of 0,8. Furthermore, the majority of today's effectively earthed systems have a first-pole-to-clear factor of 1,15 at the most. Therefore, the values of 2,0/2,5 are considered to be conservative.

8.2.2.3 Amplitude factor

An amplitude factor of 1,25 is specified by IEC 62271-100.

The theoretical maximum value can be 1,4. However, due to the statistical displacement between the timings of the TRV peaks of the two parts of the system, a factor of 0,7 is introduced to cover the effect of the two randomly over-swinging parts, i.e.:

$$(2 + 2 \times 0{,}4 \times 0{,}7)/2 = 1{,}28$$

Considering the higher value of the first-pole-to-clear factor, the value 1,25 is appropriate.

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8.2.2.4 RRRV

The rate-of-rise of recovery voltage is specified by IEC 62271-100 as 1,54 kV/μs or 1,67 kV/μs depending on the earthing conditions.

$u_1 = 0{,}75 \times (\sqrt{2}/\sqrt{3}) \times U_r \times k_{pp}$

– The value depends on the system layout and is common to other breaking duties, i.e. T100, T60, etc.

– The factor 0,75 was agreed between IEC SC 17A and the IEEE PES Switchgear Committee as a harmonised value.

$t_1 = u_1/\text{RRRV}$;

$u_c = (\sqrt{2}/\sqrt{3}) \times U_r \times$(first-pole-to-clear factor)×(amplitude factor);

The t_2 value mainly depends on the system scale and is to be common to the other duties, i.e. T100, T60, etc. The value specified for T100 is satisfactory as system requirement. Laboratory experience shows that the t_2 value introduces no significant influence on circuit-breaker performance.

Like the RRRV condition above, the case of direct connection to a line can be excluded for t_d values. The value of t_d also depends on the system layout and, based on experience, the T60 time delay can be applied as rated value with no detriment.

8.2.3 Case B

Simulation calculations have been performed and the results are shown in, Figure 23, Figure 24 and Figure 25. In this study a 1 500 MVA synchronous generator (at present the highest capacity available) is connected to a 550 kV system through a step-up transformer. The 550 kV system has a short-circuit current of 30 kA. The generator parameters used here are the actual parameters as supplied by the manufacturer:

– sub-transient reactance ca. 0,3 p.u.

– transformer short-circuit reactance ca. 0,1 p.u.

The following conditions apply:

– two parameter TRV waveshape;

– generator/transformer side contribution is predominant for the TRV across the circuit-breaker terminals due to higher voltage drop in these reactances;

– due to the step-up transformer winding connections (Δ/Y on the generator side/HV side, respectively), the positive sequence reactance is four times the zero sequence reactance. Hence the third-pole-to-clear sees a maximum TRV of 1,0 p.u. (as for a solidly earthed system);

– the generator side recovery voltage just after current interruption shows significant damping (in the order of 0,7 – 0,8) and then gradually recovers to the original value;

– due to the statistically rare occurrence of a full 180 degrees out-of-phase condition a factor of 0,8 is applied to the first-pole-to-clear factor, which, corresponds to an out-of-phase condition of up to 115 degrees depending on the neutral earthing conditions.

Based on these assumptions, for effectively earthed neutral systems, TRV parameters are well covered by those of T10. Specifying TRVs for case B is not necessary.

For non-effectively earthed neutral systems, u_c is higher than that of T10, but not higher than for case A. In actual systems of the voltage class applying non-solidly earthed neutral, it is necessary to consider the multi-frequency TRV wave shapes, and the voltage drop portion in the generator/transformer reactance, etc. Hence lower u_c and/or RRRV are probable. Based on that TRV ratings for case B are not considered necessary.

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8.2.4 TRV parameters for out-of-phase testing

As mentioned before and from laboratory experience, t_2, t_d and t' values are viewed as less dominant on out-of-phase breaking phenomena provided the other test duties (T10 to T100, SLF, etc.) are performed. For rating purposes, the t_2 value is that of T100s as specified in Tables 1a, 1b, 1c and 1d of the first edition of IEC 62271-100. However, for convenience of testing and since the influence of t_2 is not considered critical, the testing values given in Tables 14a and 14b of the first edition of IEC 62271-100 extend this value up to two times that for T100s.

System requirement basis is considered appropriate.

t_d, t' Lowest side values as used for T60

Again the system basis is used.

Figure 23, Figure 24 and Figure 25 represent a typical simulation result for a case B study.

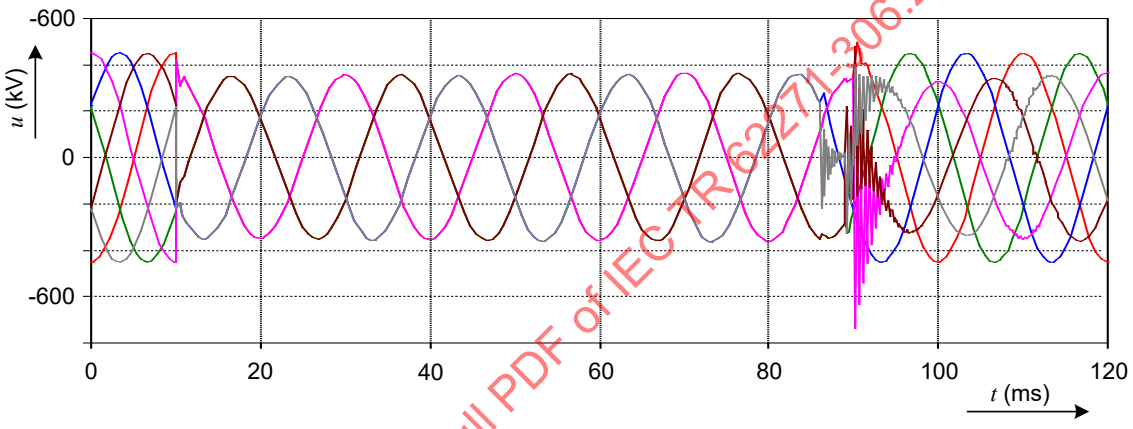

Figure 23 – Voltage on both sides during CO under out-of-phase conditions

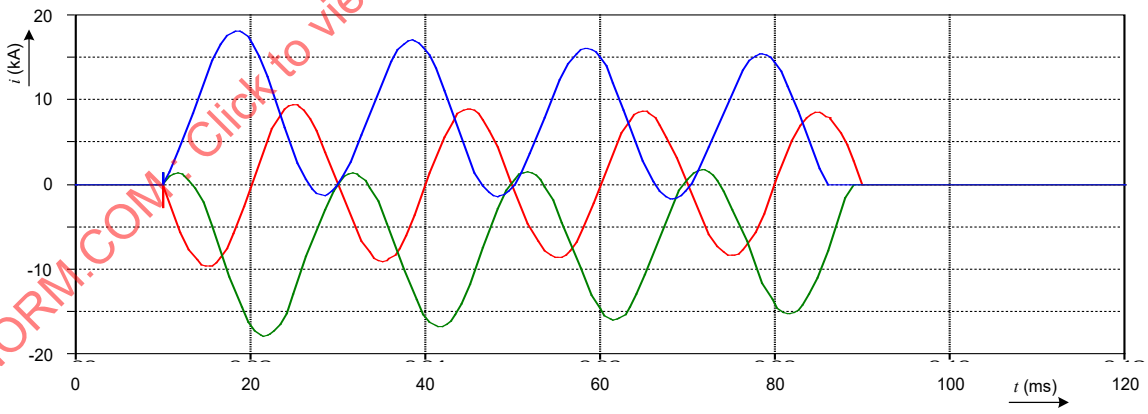

Figure 24 – Fault currents during CO under out-of-phase

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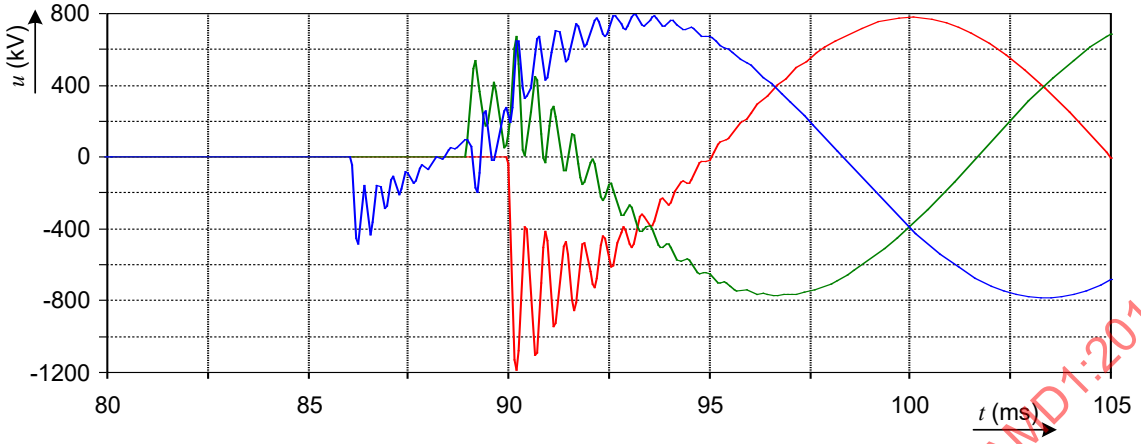

Figure 25 – TRVs for out-of-phase clearing (enlarged)

9 Switching of capacitive currents

9.1 General

Capacitive currents are encountered in the following cases:

- switching of no-load overhead lines;
- switching of no-load cables;
- switching of capacitor banks;
- switching of filter banks.

Interruption of capacitive currents is generally a light duty for a circuit-breaker, because the currents are normally a few hundred amperes. There is however a risk that restrikes will occur, which may lead to undesirable overvoltages or high frequency transients affecting the power quality in the network. Restrikes may also cause damage to the breaking unit.

Energisation of capacitive loads may lead to overvoltages or high currents. Two such cases are the switching of parallel capacitor banks and the switching of no-load lines.

Type testing is designed to be representative of the service conditions up to the point of either clearing, reigniting or restriking. Because the actual value of overvoltage and transient response is totally system dependent, tests cannot replicate these effects. By providing a means of assessing the likelihood of restrike occurrence the user can determine what best suits their application. It is assumed that since capacitor switching is not the only source of overvoltage, other protection systems are employed and in the case of unacceptable power quality for sensitive electronic equipment a sufficiently low number of likely events are selected. A separate study of actions relative to power quality on energisation must also be made.

In the selection of the rating for the circuit-breaker for capacitive current switching the following needs to be considered:

a) application, i.e. overhead line, cable, capacitor bank or filter bank;

b) power frequency of the network;

c) earthing situation of the network;

d) presence of single or two phase-to-earth faults.

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From the application the restrike performance class of the circuit-breaker can be determined (C1 or C2) as well the mechanical endurance class (M1 or M2). The earthing situation of the network, presence of single and two phase-to-earth faults are important factors that determine the recovery voltage across the circuit-breaker which, in its turn, determines the test voltage of the circuit-breaker.

In the following clauses the general theory of capacitive current switching is given as well as the application and testing considerations.

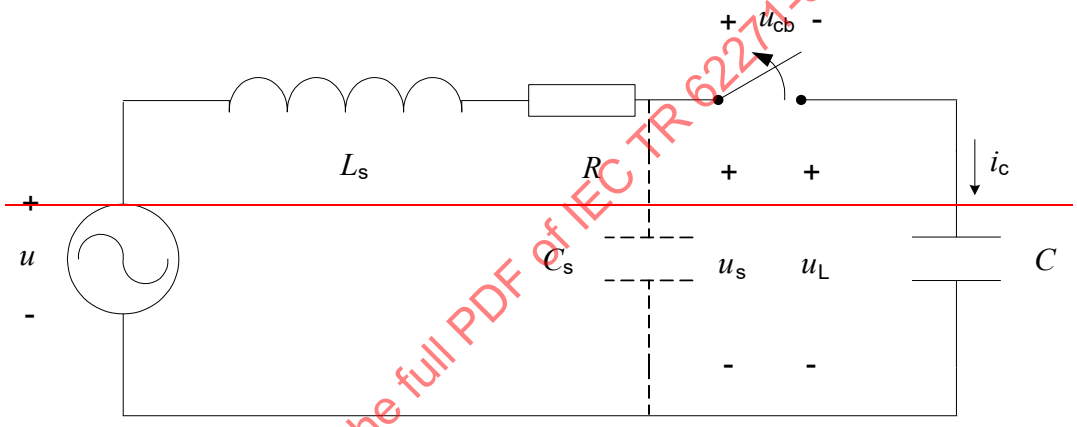
9.2 General theory of capacitive current switching

9.2.1 De-energisation of capacitive loads

9.2.1.1 Capacitor banks

9.2.1.1.1 General

The single-phase equivalent circuit shown in Figure 26 may be used to illustrate the conditions when de-energising a capacitor bank.



Key

u	Source voltage (r.m.s.)	u_{cb}	Voltage across the circuit-breaker (r.m.s.)
L_s	Source side inductance	u_L	Voltage across the capacitor bank (r.m.s.)
R	Resistor representing the losses in the circuit	i_c	Capacitive current (r.m.s.)
C_s	Source side capacitance (stray capacitance)	C	Capacitive load (capacitor bank)
u_s	Source side voltage (r.m.s.)		

Figure 26 – Single-phase equivalent circuit for capacitive current interruption

9.2.1.1.2 Capacitive current

The capacitive current i_c flowing in the circuit is given by the following equation:

$$i_c = \frac{\omega_s C \times u}{1-\omega^2 L_s C} = \frac{\omega_s C \times u}{1-\frac{\omega_s^2}{\omega_l^2}} \quad (38)$$

with

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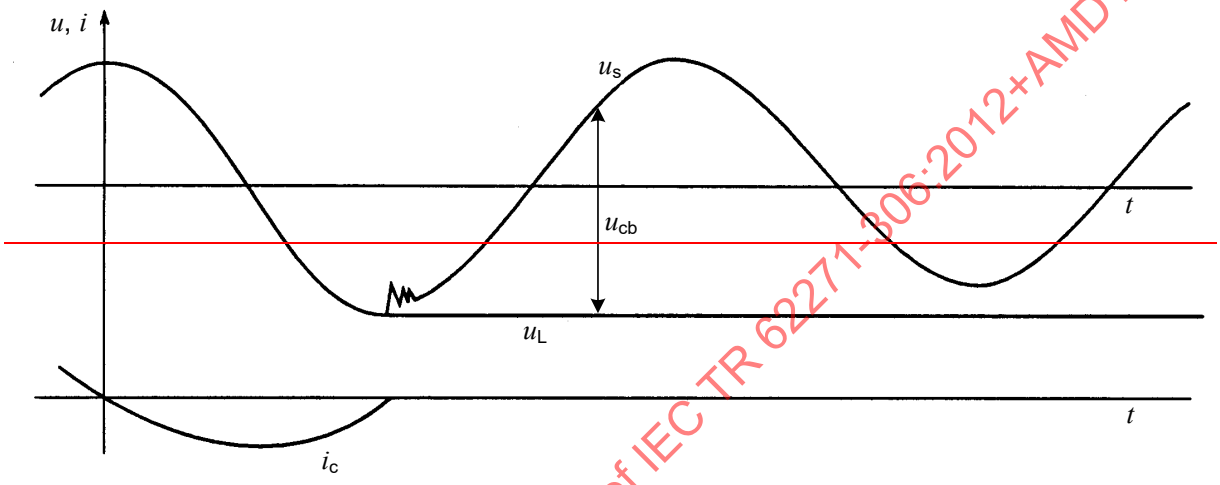
~~$\omega_s = 2\pi f_s$, where f_s is the system frequency in Hz~~

~~$\omega_i = \frac{1}{\sqrt{L_s C}} = 2\pi f_i$, where f_i is the inrush current frequency in Hz (see also 9.2.2.2)~~

~~With $\omega_i >> \omega_s$, Equation (38) transforms to $i_c = \omega_s C \times u$~~

~~9.2.1.1.3 Recovery voltage~~

~~Figure 27 shows the current and voltage shapes at interruption.~~



~~Key~~

~~i_c~~	~~Capacitive current~~
~~u_L~~	~~Voltage on the load side of the circuit-breaker~~
~~u_{cb}~~	~~Voltage across the circuit-breaker~~
~~u_s~~	~~Voltage on the source side of the circuit-breaker~~

~~Figure 27 – Voltage and current shapes at capacitive current interruption~~

~~After interruption of the current, the supply side voltage u_s will be more or less unaffected. There is only a minor decrease in amplitude, associated with the disappearance of the capacitive load. The transition to the new amplitude value is associated with a slight oscillation, the frequency of which is determined by L_s and C_s.~~

~~From the moment the current is interrupted, the charge of the capacitor bank C is trapped. The voltage u_L will therefore remain constant at the value it had at current zero (namely the peak value of the supply voltage).~~

~~Together with the low current amplitude to be interrupted, the low initial rate-of-rise of the recovery voltage makes it relatively easy for the circuit-breaker to interrupt. Some circuit-breakers may interrupt even if the current zero would occur immediately after contact separation. Half a cycle after current zero, the recovery voltage has risen to an amplitude of twice the peak value of the supply voltage. Consequently, a rated frequency of 60 Hz is more severe than 50 Hz. The circuit-breaker may then not be able to withstand the high value of the recovery voltage across a relatively small contact gap. Dielectric breakdown may occur between the contacts and current would start to flow again.~~

~~Figure 28 shows current and voltage wave shapes in a case where voltage breakdown occurs relatively close to the recovery voltage peak. The load side voltage will swing up to a voltage~~

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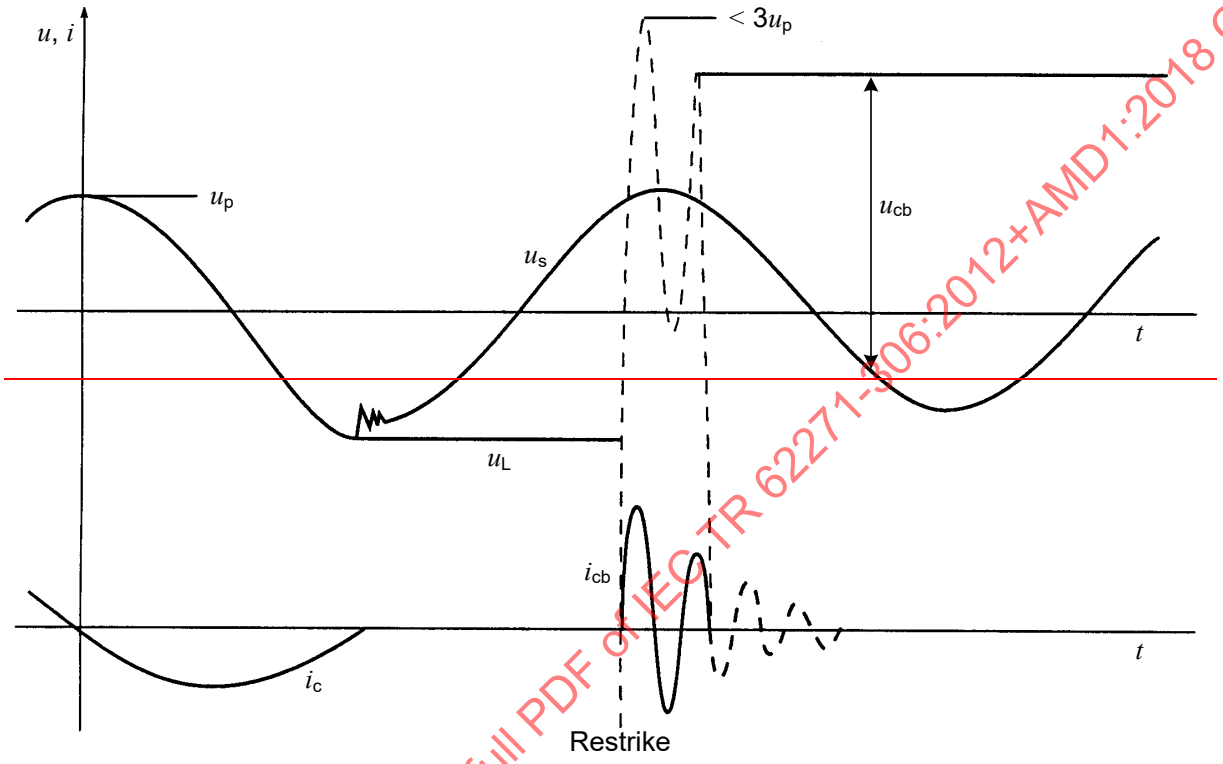
~~that ideally (without damping present) reaches three times the supply voltage peak u_p. The oscillation frequency of the current and voltage after the breakdown is determined by L_s and C (assuming $C \approx C_s$). The circuit-breaker may easily interrupt the current again at one of its current zeros, with the result that the voltage across the capacitor may attain a new constant value, perhaps higher than before. Further breakdowns associated with even higher overvoltages across the load may then occur (see also Figure 29).~~



~~Key~~

~~up~~	~~Peak of the source voltage~~
~~ic~~	~~Capacitive current~~
~~icb~~	~~Current through the circuit-breaker~~
~~uL~~	~~Voltage on the load side of the circuit-breaker~~
~~ucb~~	~~Voltage across the circuit-breaker~~
~~us~~	~~Voltage on the source side of the circuit-breaker~~

~~Figure 28 – Voltage and current wave shapes in the case of a restrike~~

~~Voltage breakdowns at capacitive current interruption are divided into two categories:~~

~~1. Re-ignitions.~~
~~Voltage breakdown during the first 1/4 cycle following current interruption.~~

~~2. Restrikes.~~
~~Voltage breakdown 1/4 of a cycle or more following current interruption.~~

~~Another phenomenon, which has been observed predominantly on vacuum circuit-breakers, may occur during capacitive current and short-circuit breaking current tests, but also at lower currents and voltages. This phenomenon is known as a Non Sustained Disruptive Discharge, or NSDD. For further details regarding NSDDs refer to 9.3.~~

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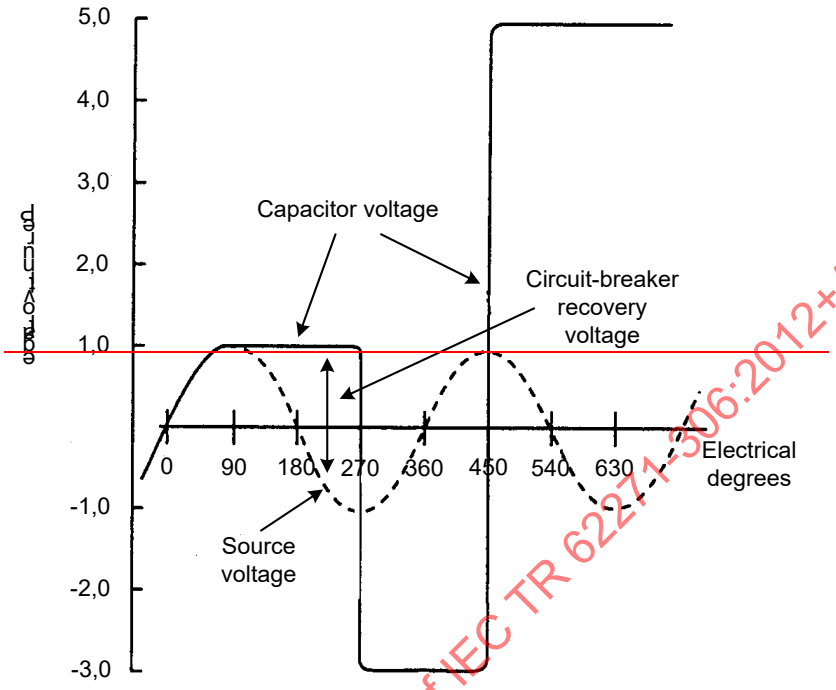
Restrikes will lead to overvoltages across the capacitive load (maximum 3 p.u. for a single restrike, where 1 p.u. is the peak value of the phase-to-earth voltage) while re-ignitions will not produce any overvoltages (theoretically max. 1 p.u.). Re-ignitions are acceptable, but they may cause power quality problems.



Key

1 per unit is the peak value of the phase-to-earth voltage

Figure 29 – Voltage build-up by successive restrikes

In reality there are no restrike-free circuit-breakers. It would take an infinite number of test shots to verify this. For this reason the concept of restrike performance was introduced IEC 62271-100.

When interrupting small capacitive currents, some circuit-breaker types may exhibit current chopping. Current chopping is a distortion of the current prior to current zero and is usually caused by the high arc voltage. Different types of circuit-breakers have varying degrees of current chopping.

Current chopping will cause an interruption prior to the current zero of the power frequency current. This also means that the trapped charge on the capacitive load will not be at its peak, which results in a lower recovery voltage peak and a lower stress on the contact gap of the circuit-breaker.

The recovery voltages in three-phase circuits are more complicated than in the single-phase case. Figure 30 shows as an example the recovery voltage of the first-pole-to-clear in a case with a non-effectively earthed capacitive load. The recovery voltage initially has a shape that would lead to a peak value equal to three times the supply voltage peak (dotted line). When the two last poles interrupt 90 electrical degrees after the first, there is however, a discontinuity in the slope and the final peak value for the first-pole-to-clear is 2,5 times the supply voltage peak (see also 9.2.1.4).

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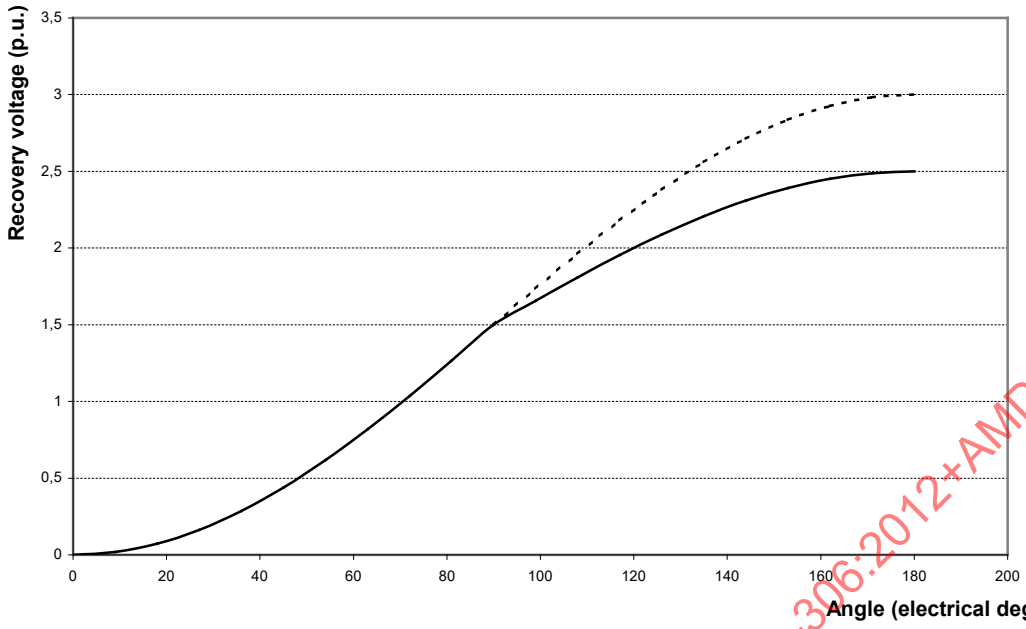

Figure 30 – Recovery voltage of the first-pole-to-clear at interruption of a three-phase non-effectively earthed capacitive load

9.2.1.2 No-load cables

9.2.1.2.1 Cable charging current

The cable charging current is a function of the following characteristics:

a) system voltage;

b) cable geometry;

c) insulation dielectric constant;

d) cable length.

The shunt capacitive reactance can be obtained from the cable manufacturer, or if the physical constants of the cable are known, the shunt capacitive reactance can be calculated. For single-conductor and three-conductor shielded cables (for the different three-conductor cable configurations see Figure 32 and Figure 33) the shunt capacitive reactance can be written as:

$$X_c = \frac{0{,}349\ 5}{f_s \varepsilon_r} \ln \frac{r_i}{r_c} \text{ (MΩ per phase per km, see NOTE)} \qquad (39)$$

where

f_s is the system frequency, in Hz;

ε_r is the dielectric constant of cable dielectric material, in F/m;

r_i is the inside radius of shield, in mm;

r_c is the conductor radius, in mm.

NOTE When using the quantity MΩ per phase per km, the shunt capacitive reactance in MΩ for more than 1 km decreases because the capacitance increases. For more than 1 km of cable, therefore, the value of shunt capacitive reactance as given above is divided by the number of km of cable.

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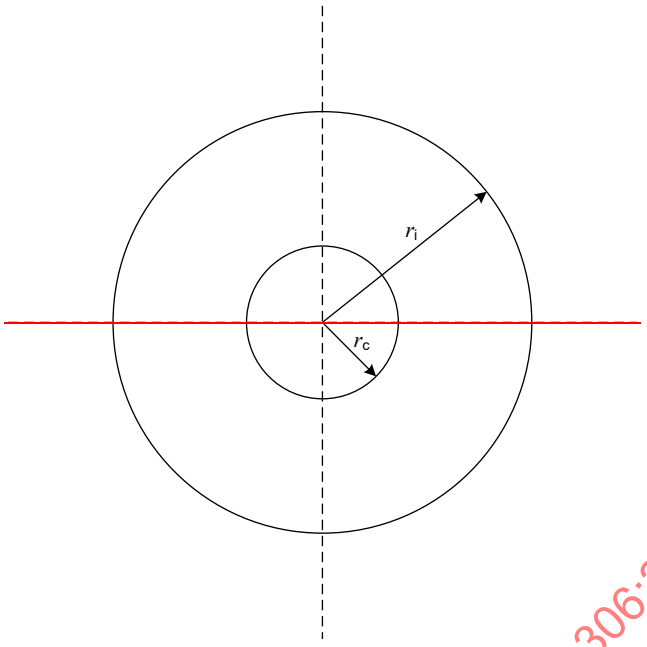
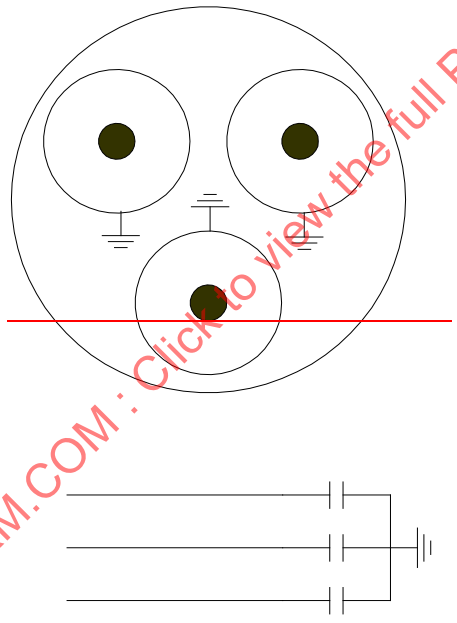
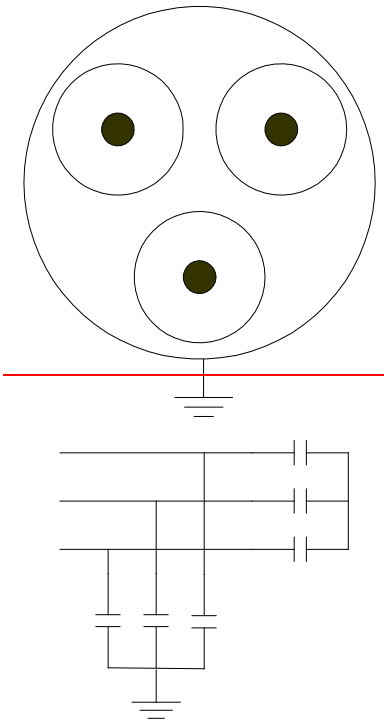


~~Figure 31 – Cross-section of a high-voltage cable~~

~~Using the capacitive reactance, the cable charging current can be calculated and compared with the rated cable charging current of the circuit-breaker given in IEC 62271-100. If the calculation exceeds the rating, the manufacturer should be consulted. Before an application can be made, the inrush current rating should also be checked (see 9.2.2.6).~~



~~Figure 32 – Screened cable with equivalent circuit~~



~~Figure 33 – Belted cable with equivalent circuit~~

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9.2.1.2.2 Recovery voltage

In the case of a screened cable, the recovery voltage is similar to that of a capacitor bank with earthed neutral (see 9.2.1.1.3). In the case of a belted cable, the recovery voltage is similar to that of uncompensated overhead lines (see 9.2.1.3.1.2).

9.2.1.3 No-load overhead lines

9.2.1.3.1 Uncompensated overhead lines

9.2.1.3.1.1 Line charging current

A no-load overhead line can generally be represented by a capacitance. In the case of short lines (< 200 km) this capacitance can be considered concentrated, but in the case of long lines it must be considered distributed. Typical capacitance values vary from 9,1 nF/km per phase for single conductor overhead lines to 14 nF/km per phase for four-conductor bundle overhead lines (see also [21]).

9.2.1.3.1.2 Recovery voltage

Overhead lines have capacitance both between phases and to earth. Figure 34 shows the peak value of the recovery voltage in the first-pole-to-clear as a function of the capacitance ratio C_1/C_0 (positive to zero sequence capacitance). It has been assumed that the amplitude approaches 3 p.u. This is the case without capacitance to earth and delayed interruption of the second phase. An example of the voltages in such a case is given in Figure 30. The other extreme, $C_1 = C_0$, is the case where each phase has capacitance to earth only. The recovery voltage peak is then 2 p.u. as in a single-phase case.

Overhead lines in transmission systems typically have C_1/C_0 ratios in the order of 2,0. In this case Figure 34 shows that the recovery voltage peak is approximately 2,4 p.u. The recovery voltage peak is the differential voltage of the source and line sides, including the effects of coupled voltage on the first cleared pole. It follows that the voltage factor for single-phase testing to cover three-phase interruption is equal to 1,2. Figure 30 and Figure 34 assume that the second and third poles interrupt 90° after the first.

When the characteristics of the voltage in service (shape and peak value) are deviating from those of the test voltage, the restrike probability may increase. For example, if the line is compensated, the line side component is not a trapped voltage resulting from the trapped charge, but a voltage oscillating with a frequency determined by the compensating reactors and the line side capacitance (see 9.2.1.3.2).

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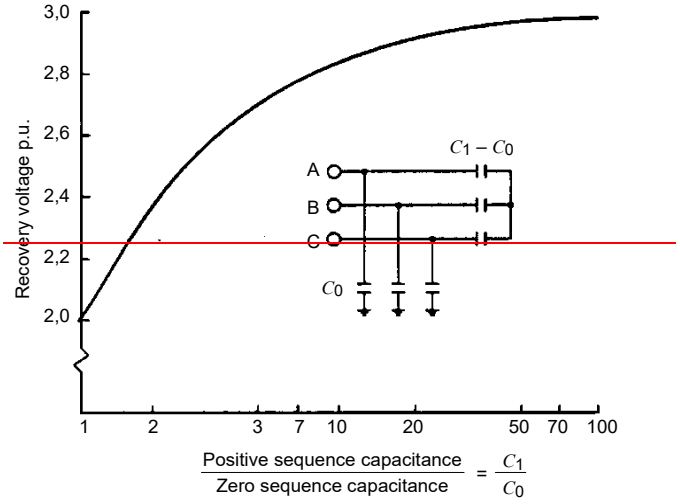

Figure 34 – Recovery voltage peak in the first-pole-to-clear as a function of C_1/C_0, delayed interruption of the second phase

If the C_1/C_0 ratio is greater than 2, higher voltages may be coupled to the first-pole-to-clear, resulting in increased probability of restrike. In this case the manufacturer should also be consulted since circuit-breaker designs are sensitive to both current magnitude and recovery voltage waveshapes.

9.2.1.3.2 Compensated overhead lines

9.2.1.3.2.1 General

Long overhead lines are often compensated with shunt reactors to reduce the charging current of the line. The compensation factor (k_L) of an overhead line is given by the ratio of the capacitive reactance ($X_{C,line}$) to the inductive reactance ($X_{L,\ reactor}$) of the compensating reactor, in equation:

$$k_L = \frac{X_{C,line}}{X_{L,reactor}} \quad (40)$$

If $X_{L,\ reactor} > X_{C,\ line}$, the line is undercompensated, a line with $X_{L,\ reactor} < X_{C,\ line}$ is called overcompensated.

9.2.1.3.2.2 Line charging current

The compensated line charging current is given by $I_{Lc} = I_c'(1-k_L)$

where

I_{Lc} is the line charging current of the compensated line;

I_c' is the line charging current of uncompensated line;

k_L is the compensation factor.

Assuming a line compensated at 60 % (i.e. k_L = 0,60), the line charging current is

$I_{Lc} = I_c'$ (1-0,6) = 0,4I_c', or 40 % of the uncompensated value.

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~~9.2.1.3.2.3 Recovery voltage~~

~~If the line is compensated, the line side component of the recovery voltage is no longer a d.c. voltage, but an oscillation of which the frequency is determined by the compensating reactor and the line capacitance.~~

~~The resonant frequency is approximated by:~~

$$f_L \approx \frac{1}{2\pi\sqrt{LC}} = f_s \sqrt{\frac{X_{C,line}}{X_{L,reactor}}} = f_s \sqrt{k_L} \quad (41)$$

~~where~~

~~f_L is the resonance frequency of the compensated line (Hz);~~

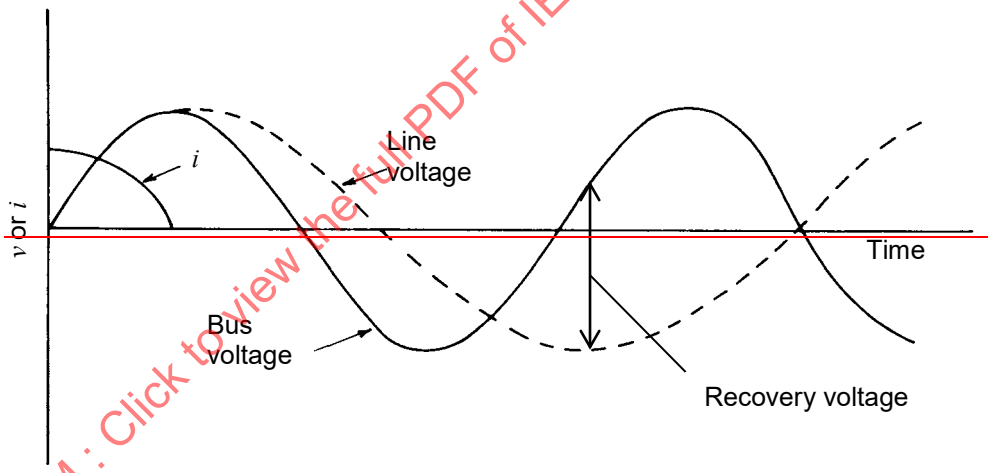
~~L is the inductance of the reactor (H);~~

~~C is the total capacitance of the line (F);~~

~~f_s is the system frequency (Hz);~~

~~k_L is the compensation factor.~~

~~In other words: the resonance frequency of a compensated line is dependent on the degree of compensation. Since the compensation usually is less than 1, this resonance frequency is less than the system frequency, resulting in a reduction of the recovery voltage. Typical current and voltage waveshapes are given in Figure 35.~~



~~**Figure 35 – Typical current and voltage relations for a compensated line**~~

~~The first half-cycle of recovery voltage is, for this example, as shown in Figure 36. Compensation thus results in a decrease of the probability of restrike at a particular current. Under these conditions improved performance may result, the circuit-breaker becoming restrike-free or possibly able to interrupt higher values of charging current. The manufacturer should be consulted on applications which markedly alter the recovery voltage.~~

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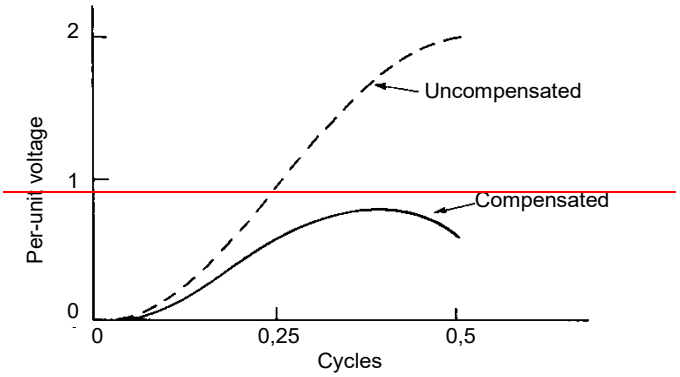

Figure 36 – Half cycle of recovery voltage

9.2.1.3.3 Switching the charging currents of long overhead lines

Very long overhead lines in excess of 300 km, even those of simple construction type, present a special case not covered by the requirements of 6.111.7 of IEC 62271-100:2008 or its notes. Where such long lines are to be switched, consideration should be given to the higher value of peak recovery voltage present on interruption. Some idea of the ability of a particular circuit-breaker for making and breaking of this requirement can be gained by considering any out-of-phase switching evidence which may exist. Such evidence will usually provide adequate demonstration of the elevated recovery voltage. For full compliance, evidence will be required to satisfy the capacitive current switching requirements of 6.111 of IEC 62271-100:2008, but to the elevated values required by the specific application.

Some users may be concerned about rare or occasional switching operations from one end on a series of long lines. This can occur during the early development stages of a system when intermediate substations may not be fully equipped or may even be by-passed. In such cases it may be appropriate to consider the out-of-phase capability in relation to the combined load presented by the series of lines. If satisfactory for the current and voltage conditions then specific testing for the severe capacitive current switching duty of IEC 62271-100 would not be necessary at the enhanced levels of the extended line. They would be required for the switching duty of the individual lines of the series, as normal.

9.2.1.4 Voltage factors for capacitive current switching tests

Depending on the capacity of a high-power laboratory, capacitive current switching tests may be performed as three-phase tests or single-phase tests. For the higher voltages (362 kV, 420 kV, 550 kV and 800 kV) unit tests are sometimes made.

When single-phase tests are made to cover three-phase application, the test voltage shall reflect the application of the circuit-breaker in the field. One of the factors influencing this is the earthing situation of the network. The other is the presence of single or two-phase faults.

Subclause 6.111.7 of IEC 62271-100:2008 gives the following voltage factors for single-phase test voltage (see Table 13). The test voltage measured at the circuit-breaker location prior to interruption shall not be less than the rated voltage $U_r/\sqrt{3}$ and the voltage factors given in Table 13.

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Table 13 – Voltage factors for single-phase capacitive current switching tests

Voltage factor k_e	Application
1,0	Tests corresponding to normal service in solidly earthed neutral systems without significant mutual influence of adjacent phases of the capacitive circuit, typically capacitor banks with solidly earthed neutral and screened cables.
1,2	Test on belted cables and line-charging current switching [a] corresponding to normal service conditions in solidly earthed neutral systems with mutual influence of adjacent phases of the capacitive circuit for rated voltages 52 kV and above.
1,4	1. breaking during normal service conditions in systems having a non-effectively earthed neutral including screened cables [a]; 2. breaking of capacitor banks non-effectively earthed neutral; 3. test on belted cables and line-charging current switching [b] corresponding to normal service conditions in effectively earthed systems for rated voltages less than 52 kV; 4 breaking in the presence of single or two-phase to earth faults in systems having a solidly earthed neutral.
1,7	Tests corresponding to breaking in non-effectively earthed systems in the presence of single or two-phase to earth faults [c].

a) When a significant capacitance to earth on the source side is present, the factor will be reduced.

b) Under the condition that the line can be replaced partly or fully by a concentrated capacitor bank.

c) The factor 1,7 is derived from the fact that the healthy phase sees the phase-to-phase voltage.

Notes to Table 13:

- The voltage factors for line-charging current switching tests of 1,2 and 1,4 are applicable to single-circuit line construction. Requirements for multiple overhead line constructions may be greater than these factors.
- The 1,4 factor is a compromise and is valid for breaking of capacitive currents in non-effectively earthed systems, where the second and third-pole-to-clear interrupt 90° after the first.
- When the non-simultaneity of contact separation in the different poles of the circuit-breaker exceeds 1/6th of a cycle of rated frequency, it is recommended to raise the voltage factor or to make only three-phase tests.

The voltage factor 1,4 is explained as follows (see Figure 37):

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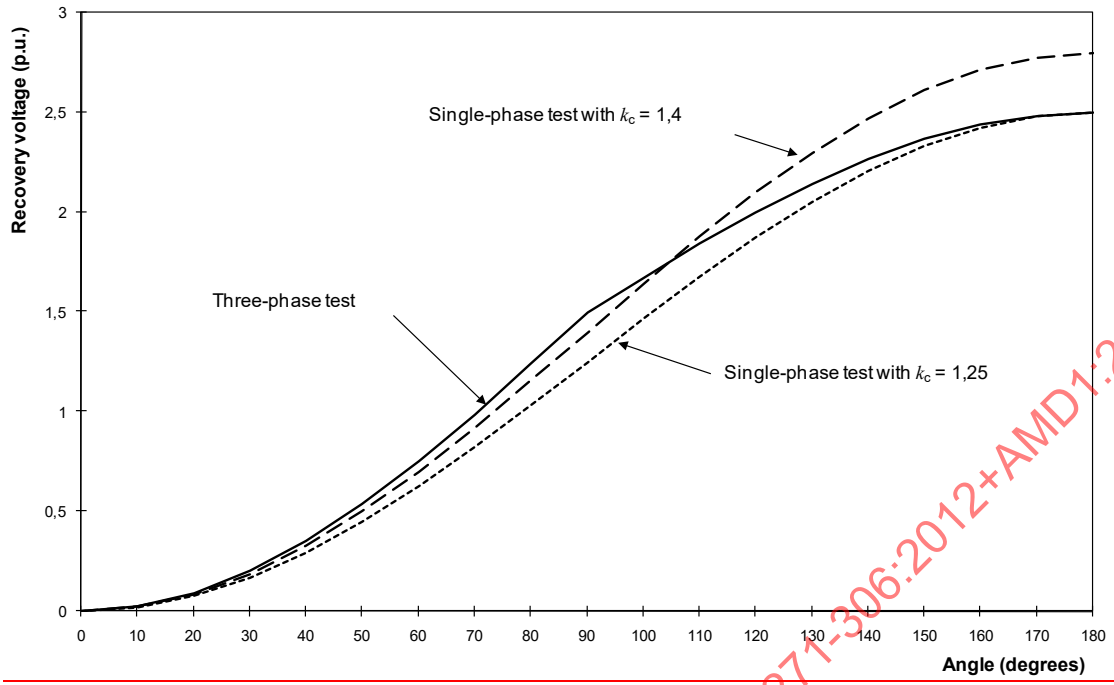

Figure 37 – Recovery voltage on first-pole-to-clear for three-phase interruption: capacitor bank with isolated neutral

When the current in the first pole is interrupted, the voltage across the circuit-breaker will rise as if the voltage factor would have been 1,5. When the second and third poles interrupt 90° later, there is a discontinuity and the resulting recovery voltage peak across the first-pole-to-clear will have a voltage factor of 1,25. The recovery voltage is indicated by the solid line in Figure 37. By using a voltage factor of 1,25 (dotted line in Figure 37), the initial portion of the recovery voltage across the first pole is not adequately covered. Using a voltage factor of 1,5 will result in a too high stress. A voltage factor of 1,4 as indicated by the dashed curve in Figure 37 is a compromise that adequately covers the actual recovery voltage.

Careful consideration should be given to these voltage factors when circuit-breakers are relocated to other parts of the system where the application is different from that of the original location.

The voltage factors specified in Table 13 are associated with single circuit line constructions and are chosen to accommodate all known physical arrangements of the conductors of such circuits. Note a) to Table 13 indicates that switching in the case of multiple overhead line constructions which have parallel circuits may require a voltage factor greater than 1,2 and 1,4. This is because such circuits are likely to have an enhancement to the line side residual voltage following interruption. This is associated with the coupling (pick-up) from the parallel circuit and may add a power frequency peak voltage of up to 0,2 p.u. This is dependent upon the geometry of the conductor systems of the two circuits.

In addition, the effect of these changes on the line side voltage, following interruption by the first-pole-to-clear, does affect the shape of the TRV across that opening pole. Consideration of this may require additional testing if the existing factor does not adequately cover the combined effects. Alternatively, the higher of the given values, e.g. 1,4 for 1,2, can be selected to encompass the specific waveshape.

On occasion utilities have specified a voltage factor of 1,3 instead of 1,2 for their double circuit lines.

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~~**9.2.2 Energisation of capacitive loads**~~

~~**9.2.2.1 General**~~

~~Energisation of capacitive loads by closing a circuit-breakers results in voltage and current transients. Those transients are the following:~~

~~a) inrush currents;~~

~~b) overvoltages caused by the system response to the voltage dip when energising capacitor banks (see 9.2.2.2);~~

~~c) overvoltages caused by travelling waves on transmission lines and cables.~~

~~In this section the phenomena associated with energisation of capacitor banks, lines and cables is treated.~~

~~**9.2.2.2 Capacitor banks**~~

~~**9.2.2.2.1 General**~~

~~Since the use of capacitor banks for compensation purposes is increasing, it is common that more than one capacitor bank is connected to the same bus. This has no influence on the conditions at interruption. The current at closing, however, is affected to a high degree. Two different situations may occur:~~

~~a) The capacitor bank is energized from a bus that does not have other capacitor banks energized. This is called single (isolated) capacitor bank switching.~~

~~b) The capacitor bank is energized from a bus that has other capacitor banks energized. This is called back-to-back capacitor bank switching.~~

~~The conditions for isolated and back-to-back capacitor bank switching are given in 9.2.2.2.2 and 9.2.2.2.3. Even energized capacitor banks in nearby substations may contribute to the inrush current such that a back-to-back situation occurs.~~

~~In particular, the second case may give rise to an inrush current of very high amplitude and frequency which sometimes has to be limited in order not to be harmful to the circuit-breaker, the capacitor banks and/or the network. The magnitude and frequency of this inrush current is a function of the following:~~

~~c) applied voltage (point on the voltage wave at closing);~~

~~d) capacitance of the circuit;~~

~~e) inductance in the circuit (amount and location);~~

~~f) any charge on the capacitor bank at the instant of closing;~~

~~g) any damping of the circuit due to closing resistors or other resistances in the circuit.~~

~~It is assumed that the capacitor bank is discharged prior to energisation. This is a reasonable assumption, as capacitor units are fitted with discharging resistors that will discharge the capacitor bank. Typical discharge times are in the order of 5 min.~~

~~The transient inrush current to a single (isolated) bank is less than the available short-circuit current at the capacitor bank terminals. It rarely exceeds 20 times the rated current of the capacitor bank at a frequency that approaches 1 kHz. Since a circuit-breaker must meet the making current requirements of the system, transient inrush current is not a limiting factor in single (isolated) capacitor bank applications. For this reason making tests with inrush current are not required for single (isolated) capacitor bank switching.~~

~~When capacitor banks are switched back-to-back, that is, when one bank is switched while another bank is connected to the same bus, transient currents of prospective high magnitude and with a high natural frequency may flow between the banks on closing of the circuit-~~

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breaker. The effects are similar to that of a restrike on opening. This oscillatory current is limited only by the impedance of the capacitor bank and the circuit between the energized bank or banks and the switched bank. This transient current usually decays to zero in a fraction of a cycle of the system frequency. In the case of back-to-back switching, the component supplied by the source is at a lower frequency and so small it may be neglected.

9.2.2.2.2 Single (or isolated) capacitor bank

A bank of shunt capacitors is considered single (isolated) when the inrush current on energisation is limited by the inductance of the source and the capacitance of the bank being energized. A capacitor bank is also considered single (isolated) if the maximum rate of change, with respect to time, of transient inrush current on energising an uncharged bank does not exceed the maximum rate of change of the symmetrical short-circuit current at the voltage at which the current is applied. The limiting value is equal to

$$\left(\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}\right)_\mathrm{max} = \omega_\mathrm{s} I_\mathrm{sc} \sqrt{2} \qquad (42)$$

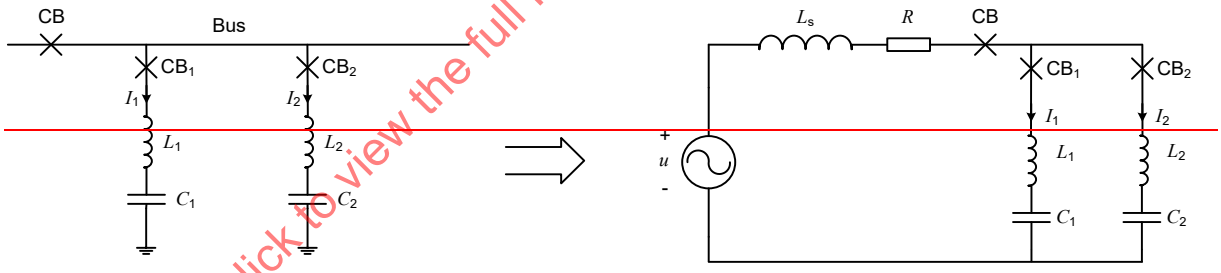
where

$\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}$ is the rate of change of inrush current, A/s;

I_sc is the rated short-circuit current, in A r.m.s.;

$\omega_\mathrm{s} = 2\pi f_\mathrm{s}$ is the system frequency, in rad/s and f_s is the power frequency, in Hz.

The single-phase equivalent of a circuit where two capacitor banks (C_1 and C_2) are connected to a busbar is shown in Figure 38. L_1 and L_2 represent the stray inductance (or stray inductance plus additional damping inductance). The inductance L_s of the supply network will be several orders of magnitude higher than L_1 and L_2.



Key

CB	Busbar circuit breaker
CB_1, CB_2	Capacitor bank circuit breakers
I_1, I_2	Capacitor bank current
L_1, L_2	Stray inductance plus additional damping inductance
C_1, C_2	Capacitor bank

Figure 38 – Parallel capacitor banks

The case of energising a single (isolated) capacitor bank is equal to energisation of C_1 when C_2 is not connected in the circuit described in Figure 38. The circuit consists then of the source inductance L_s in series with the capacitor bank C_1. L_1 can be disregarded here, since $L_\mathrm{s} >> L_1$. In this case, the peak of the inrush current ($i_\mathrm{i\ peak}$) and inrush current frequency (f_i) are limited by the source impedance L_s.

NOTE Busbar circuit breaker CB will not be exposed to back-to-back capacitor bank switching.

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Assuming that bank C_1 is to be connected to the busbar and bank C_2 is not connected, the following equations apply:

$$i_{\mathrm{i}} = \hat{u}\sqrt{\frac{C_1}{L_{\mathrm{s}}}}\sin\omega_{\mathrm{i}}t \tag{43}$$

and

$$f_{\mathrm{i}} = \frac{1}{2\pi\sqrt{(L_{\mathrm{s}} + L_1)C_1}} \tag{44}$$

where

i_{i} is the inrush current, in A;

$\hat{u}$ is the peak of the source voltage, in V;

$\omega_{\mathrm{i}} = 2\pi f_{\mathrm{i}}$ is the angular inrush frequency in rad/s, where f_{i} is the inrush current frequency, in Hz.

with $L_{\mathrm{s}} >> L_1$, the frequency of the inrush current is:

$$f_{\mathrm{i}} = \frac{1}{2\pi\sqrt{L_{\mathrm{s}}C_1}} \tag{45}$$

The highest inrush current peak is obtained when switching the capacitor bank at the peak of the supply voltage.

$$i_{\mathrm{ipeak}} = u\sqrt{2}\sqrt{\frac{C_1}{L_{\mathrm{s}}}} \tag{46}$$

With $I_{\mathrm{sc}} = \frac{u}{\omega_{\mathrm{s}}L_{\mathrm{s}}}$ and $I_1 = \omega_{\mathrm{s}}uC_1$, Equations (45) and (46) transform to

$$f_{\mathrm{i}} = f_{\mathrm{s}}\sqrt{\frac{I_{\mathrm{sc}}}{I_1}} \tag{47}$$

and

$$i_{\mathrm{imax}} = \sqrt{2}\sqrt{I_{\mathrm{sc}}I_1} \tag{48}$$

where

f_{s} is the power frequency, in Hz;

I_{sc} is the short-circuit current of the source, in A (r.m.s.);

I_1 is the current through capacitor bank 1, in A (r.m.s.);

i_{imax} is the maximum peak of the inrush current.

In the three-phase case the same equations may be applied. The voltage u is then the phase-to-earth voltage.

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9.2.2.2.3 Back-to-back capacitor bank

The inrush current of a single (isolated) bank will be increased when other capacitor banks are connected to the same bus.

If in Figure 38 bank C_1 is connected to the busbar and bank C_2 is to be connected, the inrush current associated with the charging of bank C_2 is supplied by bank C_1 (back-to-back switching). As stated in 9.2.2.2, capacitor bank C_2 is discharged prior to energisation. The peak and frequency of the inrush current are now limited by L_1 and L_2, in equation:

$$i_{\text{i peak}} = u\sqrt{2}\sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}} \tag{49}$$

with

$$C_{\text{eq}} = \frac{C_1 C_2}{C_1 + C_2} \tag{50}$$

and

$$L_{\text{eq}} = L_1 + L_2 \tag{51}$$

This can reach extreme values since the magnitude of L_{eq} can be arbitrarily small.

The frequency of the inrush current is now:

$$f_{\text{i}} = \frac{1}{2\pi\sqrt{L_{\text{eq}} C_{\text{eq}}}} \tag{52}$$

Inserting Equations (50) and (51) in Equations (49) and (52) gives the following equation for the inrush current peak and frequency:

$$i_{\text{i peak}} = u\sqrt{2}\sqrt{\frac{I_1 I_2}{u\omega_{\text{s}} L_{\text{eq}}(I_1 + I_2)}} = \sqrt{2}\sqrt{\frac{uI_1 I_2}{\omega_{\text{s}} L_{\text{eq}}(I_1 + I_2)}} = \sqrt{\frac{uI_1 I_2}{\pi f_{\text{s}} L_{\text{eq}}(I_1 + I_2)}} \tag{53}$$

$$f_{\text{i}} = \frac{1}{2\pi}\sqrt{\frac{\omega_{\text{s}} u(I_1 + I_2)}{L_{\text{eq}} I_1 I_2}} = \frac{1}{2\pi}\sqrt{\frac{2\pi f_{\text{s}} u(I_1 + I_2)}{L_{\text{eq}} I_1 I_2}} = 2\pi\sqrt{\frac{f_{\text{s}} u(I_1 + I_2)}{L_{\text{eq}} I_1 I_2}} \tag{54}$$

In Equations (53) and (54) it is assumed that $I_1 = \omega_{\text{s}} C_1 u$ and $I_2 = \omega_{\text{s}} C_2 u$ (see also 9.2.1.1.2)

Connecting bank C_{n+1} with n banks in parallel that are already connected:

$$L' = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + \ldots\ldots \frac{1}{L_n}} \tag{55}$$

and

$$C' = C_1 + C_2 + \ldots\ldots + C_n \tag{56}$$

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To obtain the inrush current peak and frequency can be done by using Equation (49) and substituting C_1 by C' and C_2 by C_{n+1} in Equation (51). L_{eq} can be obtained by substituting L_1 by L' and L_2 by L_{n+1} in Equation (54).

$$C_{eq} = \frac{C' \times C_{n+1}}{C' + C_{n+1}} \text{ and } L_{eq} = L' + L_{n+1}$$

With $L_1 = L_2 = \ldots\ldots = L_{n+1} = L$ and $C_1 = C_2 = \ldots\ldots = C_{n+1} = C$, $L' = L/n$ and $C' = nC$,

$$i_{ipeak} = u\sqrt{2}\,\frac{n}{n+1}\sqrt{\frac{C}{L}} \quad (57)$$

and

$$f_i = \frac{1}{2\pi\sqrt{LC}} \quad (58)$$

In a three-phase case the same equations may be applied. The voltage u is then the rated phase-to-earth voltage $U_r/\sqrt{3}$.

In this case Equations (53) and (54) transform to:

$$i_{ipeak} = \sqrt{\frac{10^3 U_r I_1 I_2}{\pi f_s \sqrt{3} \times 10^{-6} L_{eq}(I_1 + I_2)}} = 13\,556\sqrt{\frac{U_r I_1 I_2}{f_s L_{eq}(I_1 + I_2)}} \approx 13\,500\sqrt{\frac{U_r I_1 I_2}{f_s L_{eq}(I_1 + I_2)}} \quad (59)$$

and

$$f_i = \frac{1}{2\pi} \times 10^3 \sqrt{\frac{2\pi f_s 10^3 U_r (I_1 + I_2)}{\sqrt{3} \times 10^{-6} L_{eq} I_1 I_2}} \approx 9{,}5\sqrt{\frac{f_s U_r (I_1 + I_2)}{L_{eq} I_1 I_2}} \quad (60)$$

where

f_i is the inrush current frequency (kHz);
f_s is the system frequency (Hz);
I_1, I_2 is the capacitor bank currents (A, r.m.s.);
i_{ipeak} is the inrush current peak (A);
U_r is the rated voltage (kV);
L_{eq} is the equivalent inductance (μH).

Typical amplitudes of the inrush currents for back-to-back energisation of capacitor banks are several kA with frequencies of 2 kHz to 5 kHz. Typical values are given in Table 9 of IEC 62271-100:2008. Capacitors can normally withstand amplitudes up to 100 times their charging current.

If the inrush current amplitude and frequency exceed those stated in Table 9 of IEC 62271-100:2008, it may be necessary to limit them. This can be done by insertion of additional series inductance in the circuit, or by using pre-insertion resistors (see 9.2.2.7). Another possibility is to use controlled switching.

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9.2.2.3 Cables

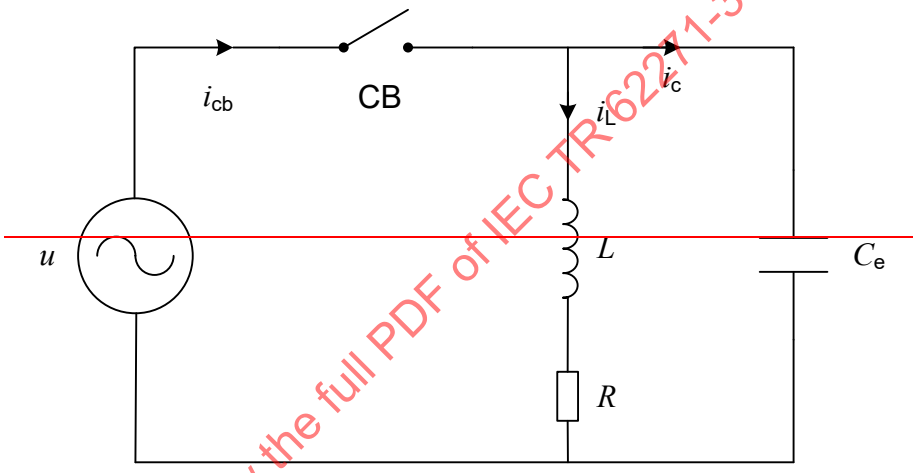
9.2.2.3.1 General

A circuit-breaker may be required to energize a no-load cable during its normal operating duties. Prior to energisation the cable is usually at earth potential, but can have a trapped charge from a previous switching operation. A cable may be switched from a bus that does not have other cables energized (single or isolated cable) or against a bus that has one or more cables energized (back-to-back).

Besides these widely known effects also other phenomena may occur during cable energisation at rated voltages of 420 kV and above.

When operating the cable nearly fully compensated the phenomenon of delayed current zero crossings may occur. This phenomenon is similar to the one described at faults close to generators (see Annex B).

The simplified single-phase equivalent circuit is shown in Figure 39.



Key

u	Phase-to-earth voltage	R	Resistance to earth of compensating reactor
CB	Circuit-breaker	i_{cb}	Current through the circuit-breaker
C_e	Cable capacitance to earth	i_L	Current through the compensating reactor
L	Inductance to earth of compensating reactor	i_c	Current through the cable

Figure 39 – Equivalent circuit of a compensated cable

When energising the compensated cable by closing the circuit-breaker the current starts flowing in the cable (i_c, momentary value of the current is not continuous and may change suddenly) and in the reactor (i_L, momentary value of the current is continuous due to the fact that di/dt at a inductance is zero at the instant of closing the circuit-breaker). The sum of both currents flows through the circuit-breaker (i_{cb}).

Due to the fact that the instantaneous current value in the reactor before energising and the current value directly after energising must be identical ($di/dt = 0$), a d.c. equalizing current flows depending on the making angle and the instantaneous value of the making voltage, respectively. The change of the current through the inductance when closing the circuit-breaker causes a magnetic field. Due to the continuity requirement this magnetic field is compensated. The equalizing magnetic field causes the d.c. equalizing current.

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If the circuit-breaker is closed at voltage maximum, the equalizing current is zero and when closing at voltage zero the equalizing current is at its maximum due to the 90° phase shift between voltage and current for an inductance.

This d.c. equalizing is superimposed on the inductive a.c. current of the reactor to the total reactor current i_L. Due to the resistance of the reactor the d.c. current decays over time.

The following two different cases are distinguished:

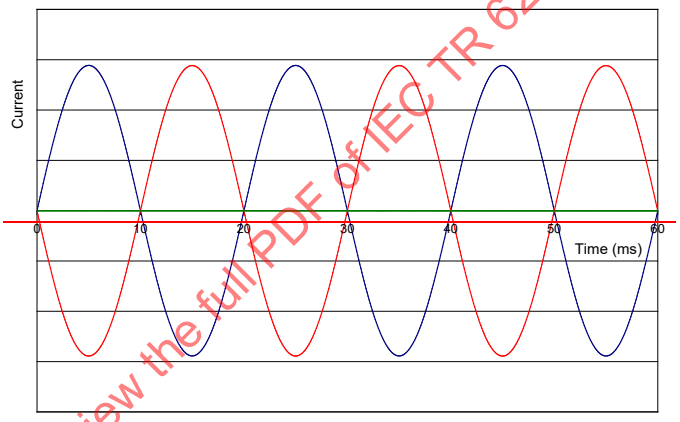
– a fully compensated cable;

– a partly compensated cable.

9.2.2.3.2 Fully compensated cable

When operating a fully compensated cable the inductive a.c. current and the capacitive a.c. current will be of the same amount. Hereby the capacitive current i_e has the opposite sign of the inductive current i_L.

The idealized graphs of the inductive current i_L, the capacitive current i_e and the total current through the circuit-breaker i_{cb} are shown in Figure 40 for making at voltage maximum and full compensation.



Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_e
Green trace	Total current through the circuit-breaker i_{cb}

Figure 40 – Currents when making at voltage maximum and full compensation

The idealized graphs of the inductive current i_L, the capacitive current i_e and the total current through the circuit-breaker i_{cb} are shown in Figure 41 for making at voltage zero and full compensation. The transient effects of the suddenly changing capacitive current when closing the circuit-breaker are not considered.

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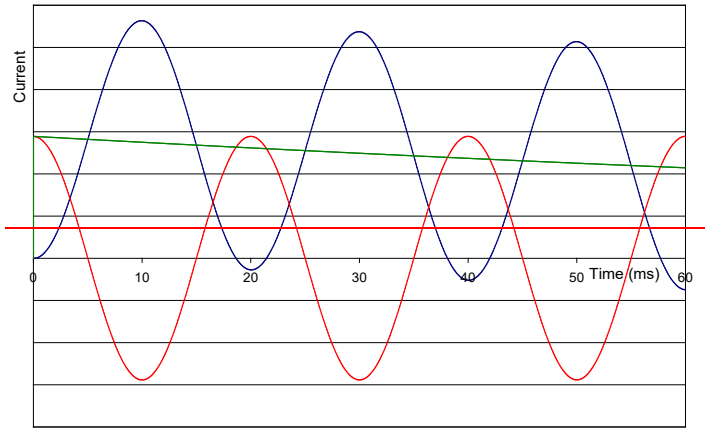

~~Key~~

~~Blue trace~~	~~Inductive current i_L~~
~~Red trace~~	~~Capacitive current i_c~~
~~Green trace~~	~~Total current through the circuit-breaker i_{cb}~~

~~Figure 41 – Currents when making at voltage zero and full compensation~~

~~It can be seen that the inductive current i_L and the capacitive current i_c in both cases always show zero crossings.~~

~~In case of making at voltage maximum, the current through the circuit-breaker for a fully compensated cable is zero due to the fact that the inductive current i_L and the capacitive current i_c have the same magnitude and opposite polarity.~~

~~In case of making at voltage zero the current through the circuit-breaker does not show zero crossings for several periods. If within this time period the circuit-breaker is tripped it may have severe difficulties to interrupt the current. This will be described in detail further in this clause.~~

~~9.2.2.3.3 Partly compensated cable~~

~~If the cable is partly compensated (undercompensated) the inductive a.c. current is smaller than the capacitive a.c. current. The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 42 for making at voltage maximum and partial compensation (e.g. 80 %).~~

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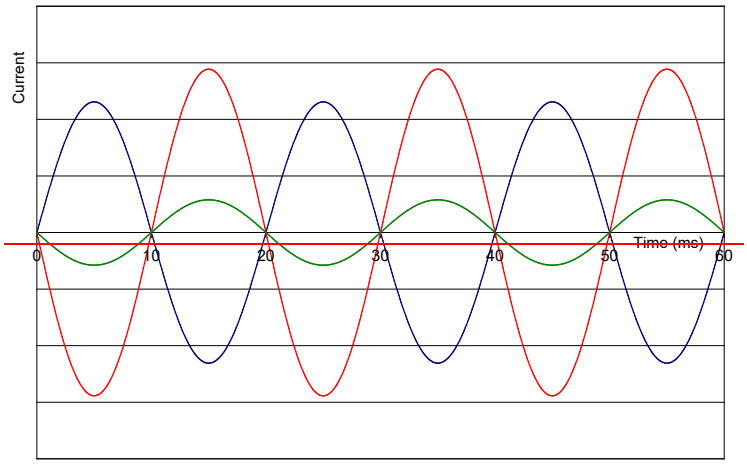


~~Key~~

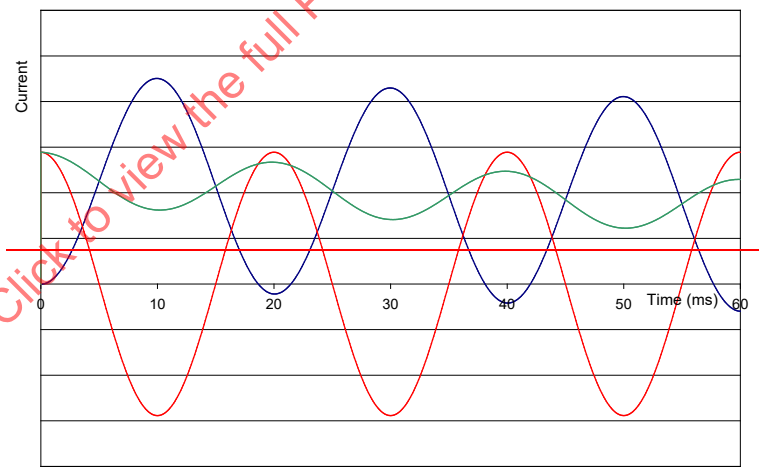
~~Blue trace~~ ~~Inductive current i_L~~

~~Red trace~~ ~~Capacitive current i_c~~

~~Green trace~~ ~~Total current through the circuit-breaker i_{cb}~~

~~Figure 42 – Currents when making at voltage maximum and partial compensation~~

~~The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 43 for making at voltage zero and partial compensation (e.g. 80 %). The transient effects of the suddenly changing capacitive current when closing the circuit-breaker are not considered.~~



~~Key~~

~~Blue trace~~ ~~Inductive current i_L~~

~~Red trace~~ ~~Capacitive current i_c~~

~~Green trace~~ ~~Total current through the circuit-breaker i_{cb}~~

~~Figure 43 – Currents when making at voltage zero and partial compensation~~

~~Also in case of undercompensated operated cables it can be seen that the inductive current i_L and the capacitive current i_c in all cases always show zero crossings.~~

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In case of making at voltage zero the current through the circuit-breaker also does not show zero crossings for several periods even if the amplitude of the d.c. equalizing current is smaller due to the lower inductive current at partial compensation.

9.2.2.3.4 Summary

The amplitude of the d.c. equalizing current depends on the degree of compensation and the instant of making. The duration of the time period of missing current zero crossings depends on the X/R ratio, the damping of the compensation reactor and the degree of compensation.

In the past the resistance of the compensation reactors was comparably high. Therefore the X/R ratio (equivalent to the d.c. time constant τ) was low and the d.c. equalizing current was damped fast enough to create current zeros. Nowadays the resistance of the compensation reactors is reduced further in order to minimize the ohmic losses.

The phenomenon of delayed current zero crossings may become problematic if the circuit-breaker is tripped during the time period of missing zero crossings. To solve this problem two basic approaches are possible:

– prevention of the occurrence of currents with delayed zero crossings;

– choice of a circuit-breaker suitable for the application.

To prevent currents with delayed zero crossings the making must always occur around the voltage maximum in each phase. This can be done using controlled closing (point-on-wave closing). Controlled closing ensures that the making occurs in all phases at or near voltage maximum. The disadvantage of this method is the occurrence of switching overvoltages.

If the making at voltage zero cannot be prevented, the decay of the d.c. equalizing currents can be increased by using circuit-breaker types equipped with pre-insertion resistors. Due to the additional resistance the X/R ratio is decreased and hence the first zero crossing of the current i_{cb} occurs significantly earlier. The resistance value of the pre-insertion resistor should be dimensioned in a way that the first zero crossing occurs about 10 ms after making. In this case a successful opening operation can also be ensured for the worst-case (e.g. opening command is already given during closing of the circuit-breaker). For each application an individual calculation must be performed due to the different parameters of reactor and network parameters as well as a different degree of compensation.

If no suitable resistance value can be determined or controlled switching is not possible, the current shows delayed zero crossings. Hence a suitable circuit-breaker type must be chosen to ensure a successful current interruption at all cases. The arc in the circuit-breaker during the breaking operation represents a non-linear resistance which also leads to a decreased X/R ratio and therefore to an earlier occurrence of zero crossings. With special tests the parameters for an arc model can be determined for each circuit-breaker type. Using this arc model the influence on the current i_{cb} can be determined. Depending on the amplitude and time constant of the d.c. equalizing current circuit-breaker types with high arc voltages may be necessary. Also with this method for each application an individual calculation must be performed due to the different parameters of reactor and network parameters, different parameters of the circuit-breaker arc as well as a different degree of compensation.

9.2.2.4 Single (isolated) cable

A cable is defined as single (isolated) if the maximum rate of change, with respect to time, of transient inrush current on energising an uncharged cable does not exceed the rate of change of current associated with the maximum symmetrical interrupting current. This limiting value is numerically equal to

$$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max} = \omega_{\mathrm{s}}\sqrt{2}I_{\mathrm{sc}} = 2\pi f_{\mathrm{s}}\sqrt{2}I_{\mathrm{sc}} \qquad (61)$$

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where

$\left(\frac{di_i}{dt}\right)_{max}$ is the maximum rate of change of inrush current in A/s;

I_{sc} is the rated r.m.s. short-circuit current, in A;

$\omega_s = 2\pi f_s$ is the system frequency in rad/s, where f_s is the power frequency in Hz.

By this definition it is possible to have cable circuits which are physically back-to-back, but are considered single (isolated) for application purposes provided a large inductance is located between the two cable circuits. The inductance must be large enough so that by itself it would limit fault current to a value less than or equal to the circuit-breaker rating.

9.2.2.5 Back-to-back cables

Cables are considered switched back-to-back if the maximum rate of change of transient inrush current on energising an uncharged cable exceeds that specified for a single (isolated) cable.

9.2.2.6 Cable inrush current

9.2.2.6.1 General

The energisation of a cable by the closing of a circuit-breaker will result in a transient inrush current. The magnitude and rate of change of this inrush current is a function of the following:

– applied voltage (including the point on the voltage wave at closing);

– cable surge impedance;

– cable capacitive reactance;

– inductance in the circuit (amount and location);

– any charges on the cable at the instant of closing;

– any damping of the circuit because of closing resistors or other resistance in the circuit.

The transient inrush current to a single (isolated) cable is less than the available short-circuit current at the circuit-breaker terminals. Since a circuit-breaker must meet the making current requirements of the system, transient inrush current is not a limiting factor in isolated cable applications.

When cables are switched back-to-back (that is, when one cable is switched while other cables are connected to the same bus), transient currents of high magnitude and initial high rate of change may flow between cables when the switching circuit-breaker is closed or restrikes on opening. This surge current is limited by the cable surge impedances and any inductance connected between the energized cable(s) and the switched cable. This transient current usually decays to zero in a fraction of a cycle of the system frequency. During back-to-back cable switching, the component of current supplied by the source is at a lower rate of change and so small that it may be neglected. Due to the very high damping of the inrush current, the switching of parallel cables usually does not represent a problem for modern circuit-breakers. Therefore no problems are expected for back-to-back cable configurations. The case of back-to-back cable switching is not addressed in IEC 62271-100.

A typical circuit for back-to-back cable switching is shown in Figure 44.

The inductances L_1, L_2, and L_b between the cables are often very small with respect to the inductance L_s of the source. In many cases they will be less than 1 % of the source inductance. They consist of the inductances from the cables to the circuit-breakers, the circuit-breaker inductances, and the bus inductance of the current path. Values of inductance depend upon the physical configuration and are hence site specific and unable to be standardised. However, a representative range is 0,66 µH to 1,0 µH per phase per m.

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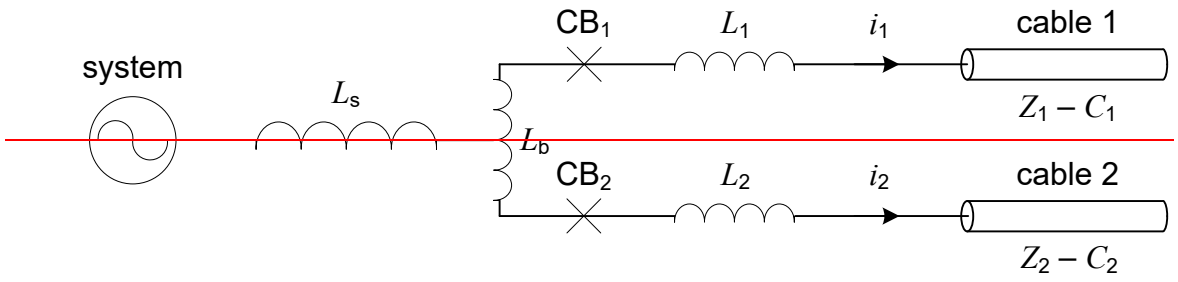

~~Key~~

~~CB_1~~	~~Circuit-breaker~~
~~CB_2~~	~~Circuit-breaker, open for single (isolated) cable switching, closed for back-to-back switching~~
~~L_S~~	~~Source inductance~~
~~L_1, L_2~~	~~Inductance between cables 1 and 2 and bus~~
~~Z_1, Z_2~~	~~Surge impedance of cables 1 and 2~~
~~C_1, C_2~~	~~Capacitance of cables 1 and 2~~
~~L_b~~	~~Inductance of bus connecting the cables~~

~~Figure 44 – Typical circuit for back-to-back cable switching~~

~~9.2.2.6.2 Single (isolated) cable~~

~~In switching a single (isolated) cable, if the source inductance is greater than 10 times the cable inductance, the cable can be represented as a capacitor. Otherwise, under transient conditions the cable can be represented by its surge impedance. An expression for surge impedance [22] is given for single-conductor and three-conductor shielded cables by~~

$$Z = \sqrt{\frac{L}{C}} = \frac{138}{\sqrt{\varepsilon}} \log_{10}\left(\frac{r_2}{r_1}\right) \quad (62)$$

~~where~~

~~Z is the surge impedance, in Ω;~~

~~L is the distributed inductance of cable, in H/m;~~

~~C is the distributed capacitance of cable, in F/m;~~

~~ε is the dielectric constant of cable dielectric material;~~

~~r_2 is the inside radius of sheath, in mm;~~

~~r_1 is the outside radius of conductor, in mm.~~

~~Typical values of ε range from 2,3 (polyethylene) to 4 (fluid impregnated paper); a typical value for Z is 50 Ω.~~

~~To calculate the inrush current for a single cable, Figure 44 may be used, with $Z_2 = 0$.~~

$$i_1(t) = \frac{U_m - U_t}{Z_1}\left[1 - \exp\left(\frac{Z_1}{L}t\right)\right] \quad (63)$$

~~with $i_{1peak} = \frac{U_m - U_t}{Z_1}$~~

~~where~~

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U_m is the crest of applied voltage;

U_t is the trapped voltage on cable being switched;

f_s is the source frequency (power frequency);

i_i is the inrush current;

$i_{i\,peak}$ is the peak of the inrush current;

Z_1 is the cable surge impedance;

L is the source inductance.

The initial rate-of-rise (di/dt at $t = 0$) of the inrush current is $\frac{U_m - U_t}{L}$. For application purposes i_{peak} should be compared to the value given in Table 9 of IEC 62271-100:2008.

The cable inrush current is not oscillatory in the usual frequency-related sense, but the initial slope can be used to determine an equivalent frequency which can be compared with the rated inrush frequency. In general,

$$\left(\frac{di_i}{dt}\right)_r = 2\pi f_{ir} I_{ir} \qquad (64)$$

where

$\left(\frac{di_i}{dt}\right)_r$ is the rate-of-change of rated inrush current in A/s;

f_{ir} is the rated inrush current frequency;

I_{ir} is the rated peak inrush current.

The equivalent frequency f_{eq} for a cable inrush current is then obtained as follows:

$2\pi f_{eq} I_{ir} = \frac{U_m - U_t}{L}$ which gives $f_{eq} = \frac{U_m - U_t}{2\pi L I_{ir}}$ and for proper circuit-breaker application, f_{eq} should be less than the rated inrush current frequency.

9.2.2.6.3 Back-to-back cable inrush current

Neglecting the source contribution, back-to-back cables can be represented as shown in Figure 45.

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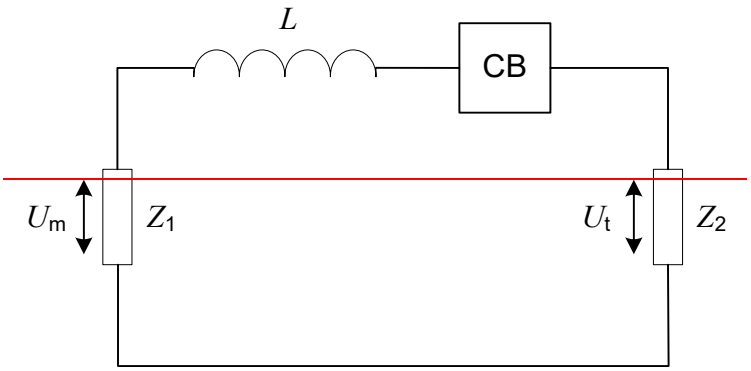

Key

U_m	Crest of applied voltage
U_t	Trapped voltage on cable being switched
Z_1, Z_2	Cable surge impedance
L	Total inductance between cable terminals
CB	Circuit breaker

Figure 45 – Equivalent circuit for back-to-back cable switching

The initial pulse of current has a front expressed as

$$i(t) = \frac{U_m - U_t}{Z_1 + Z_2}\left[1 - \exp\left(-\frac{Z_1 + Z_2}{L}t\right)\right] \quad (65)$$

Assuming that the $L/(Z_1 + Z_2)$ time constant is less than 1/5 of the travel time of the cable out and back, the initial crest of the inrush current is then $(U_m - U_t)/(Z_1 + Z_2)$, which for application should be less than the rated peak inrush current.

The inrush current when energising a cable with another already connected to the bus is given by

$$i_{ipeak} = \frac{U_m - U_t}{Z_1 + Z_2} \quad (66)$$

and

$$f_{eq} = f_s\left[\frac{U_m - U_t}{\omega(L_1 + L_2)I_{ir}}\right] \quad (67)$$

The inrush current when energising a cable with an equal cable already connected to the bus is given by

$$i_{ipeak} = \frac{U_m - U_t}{2Z}\,(\mathrm{A/s}) \quad (68)$$

and

$$f_{eq} = f_s\left[\frac{U_m - U_t}{\omega(L_1 + L_2)I_{ir}}\right]\,(\mathrm{Hz}) \quad (69)$$

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Differentiating the expression for the current at $t = 0$, will give the maximum initial rate of change of the inrush current, in equation

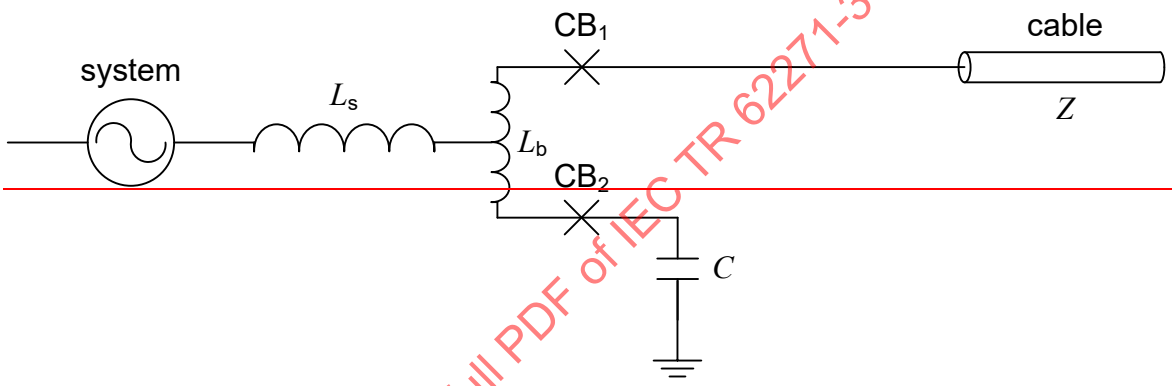
$$\left(\frac{\mathrm{d}i}{\mathrm{d}t}\right)_0 = \frac{U_\mathrm{m} - U_\mathrm{t}}{L}\ (\mathrm{A/s}) \qquad (70)$$

This can reach extreme values since the magnitude of L can be arbitrarily small.

Additional inductance may be added in series with the inductances making up L to meet the rated inrush frequency requirement.

9.2.2.6.4 Alternate configurations

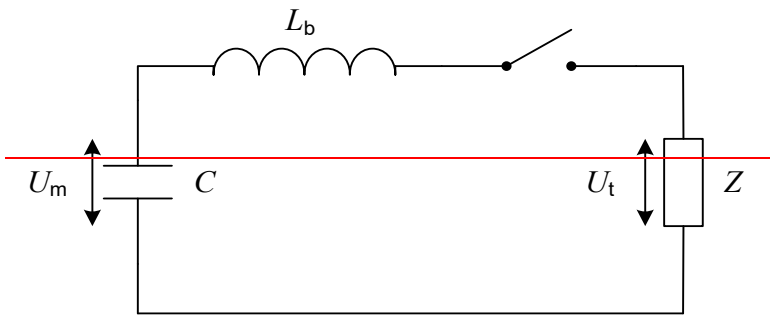
Other combinations of circuit elements can produce inrush currents associated with cable switching. For example, a cable can be switched from a bus which has a capacitor bank connected as shown in Figure 46. The inrush current can be calculated using the equivalent circuit of Figure 47.



Key

CB_1	Cable circuit breaker
CB_2	Capacitor bank circuit breaker
L_S	Source inductance
L_b	Total inductanced between bank and cable
Z	Cable surge impedance
C	Capacitance of bank

Figure 46 – Bank-to-cable switching circuit



Key

U_m	Crest of applied voltage
U_t	Trapped voltage on cable being switched

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~~Z Cable surge impedance~~

~~L_b Circuit inductance between bank and cable~~

~~C Capacitance of capacitor bank~~

~~Figure 47 – Equivalent bank-to-cable switching circuit~~

~~The maximum initial rate of change of current is given by the expression~~

$$\left(\frac{di}{dt}\right)_0 = \frac{U_m - U_t}{L_b} \text{ (A/s)} \quad (71)$$

~~and, as before, is limited by the loop inductance L_b. The equivalent frequency is determined as in 9.2.2.6.2, and required adjustments can be made by increasing the value of L_b (e.g. insertion of a reactor).~~

~~The form of the inrush current is a function of the circuit parameters which, in the equivalent circuit, form a series RLC circuit. Using standard methods of analysis, the maximum peak inrush currents are~~

~~Critically damped circuit: $\frac{Z^2}{4} = \frac{L_b}{C}$ $i_{ipeak} = 0{,}736 \frac{U_m - U_t}{Z}$ (72)~~

~~Underdamped circuit: $\frac{Z^2}{4} < \frac{L_b}{C}$ $i_{ipeak} = \frac{U_m - U_t}{\sqrt{L_b/C - Z^2/4}} \left[\exp\left(-\frac{Z\pi}{4} \frac{1}{\sqrt{L_b/C - Z^2/4}}\right)\right]$ (73)~~

$$\frac{Z^2}{4} > \frac{L_b}{C} \quad i_{ipeak} = \frac{U_m - U_t}{2\sqrt{Z^2/4 - L_b/C}} \left[e^{r_1 t_m} - e^{r_2 t_m}\right] \quad (74)$$

~~where~~

$$t_m = \frac{\ln r_1/r_2}{r_1 - r_2} \quad (75)$$

$$r_1 = -\frac{Z}{2L_b} + \sqrt{\left(\frac{Z}{2L_b}\right)^2 - \frac{1}{L_b}} \quad (76)$$

$$r_2 = -\frac{Z}{2L_b} - \sqrt{\left(\frac{Z}{2L_b}\right)^2 - \frac{1}{L_b}} \quad (77)$$

~~For application, the peak inrush current should be checked against the capability of the circuit-breaker in question.~~

~~Many other combinations of banks, cables, and lines will occur in practice. For example, a cable may be used to exit from a substation and then connect to an overhead line after a short distance. One possible approach when considering circuits of this type is to compare the relative contributions of the cable and the line. For short cable runs this circuit could be considered the equivalent of a line with a capacitor to earth replacing the cable. Similar simplifications can be used for other configurations.~~

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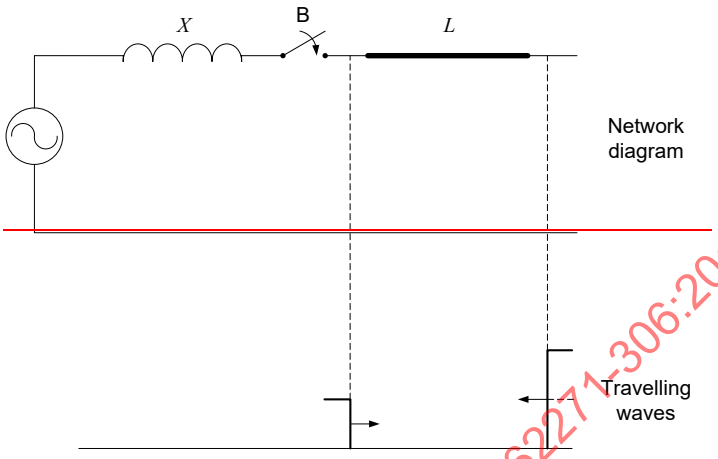
9.2.2.7 Energisation and re-energisation of overhead lines

When an overhead line is switched onto an energized network, a voltage wave is imposed on the line. The resulting phenomena are similar to those of energising a cable. The imposed wave will be reflected at the far end of the line and when the line is open at the far end (or terminated by a high impedance load for high frequencies), the reflected wave results in doubling of the amplitude as shown in Figure 48.



Key

X	Source inductance
B	Circuit-breaker
L	Overhead line

Figure 48 – Energisation of no-load lines: basic phenomena

An even higher voltage is obtained when the line has a trapped charge before being energized and the circuit-breaker happens to close at an instant when the polarity of the network voltage is opposite to that of the voltage that was present on the line. The voltage on the line can, after reflection of the wave, theoretically be up to three times the network voltage. This situation can occur in conjunction with auto-reclosing of a line.

Even higher voltages can develop on a three-phase line, when the three circuit-breaker poles are not closing simultaneously. A wave on one phase will then generate induced waves on the other phases and under unfavourable circumstances this can lead to a further rise in voltage on another phase.

An efficient way of reducing the overvoltages during energisation and re-energisation of no-load lines is to equip the circuit-breaker with pre-insertion resistors to ensure that the closing takes place in two stages. A pre-insertion resistor is a device that connects a resistor in series with the overhead line at a predetermined time before the closing of the main contacts of the circuit-breaker (see Figure 49).

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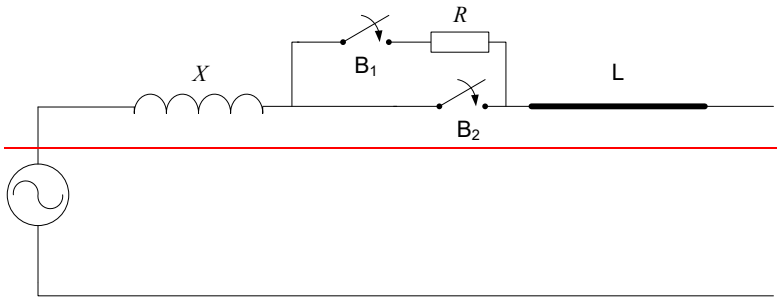

Figure 49 – Pre-insertion resistors and their function

In the first stage of closing, a resistor (R) is switched in series with the line (L) by the resistor contacts (B_1) and a voltage division is obtained. This reduces the amplitude of the imposed wave on the line.

In the second stage, the main contacts (B_2) close and at the same time the resistor is short-circuited. This gives rise to a new wave on the line, but the amplitude of this wave is also reduced. The resistor contacts are reset (opened) before the main contacts are opened.

The optimum value of the resistance of the pre-insertion resistor is usually of the same order of magnitude as that of the surge impedance of the line. The insertion time should be 6 ms to 8 ms in order to be effective.

Surge arresters have also been successfully used to control voltage transients when energising transmission lines. See IEEE C62.22 [23].

Another way of reducing overvoltages is using controlled closing see also 9.4.8.3.

9.3 Non-sustained disruptive discharge (NSDD)

NSDDs (Non-Sustained Disruptive Discharges) have been discussed, up to now, in a rather controversial manner. This phenomenon, which has been observed predominantly on vacuum circuit-breakers, may occur during capacitive current and short-circuit breaking current tests, but also at lower currents and voltages. NSDDs have not been identified in actual service.

An NSDD is defined as follows:

non-sustained disruptive discharge
NSDD
disruptive discharge associated with current interruption, which does not result in the resumption of power frequency current or, in the case of capacitive current interruption does not result in current in the main load circuit

NOTE Oscillations following NSDDs are associated with the parasitic capacitance and inductance local to or of the circuit-breaker itself. NSDDs also involve the stray capacitance to earth of nearby equipment.

An NSDD exhibits itself as a partial voltage change. Such changes can sometimes be clearly seen with normal time resolution measurements. This is particularly true in three-phase tests when the same polarity and magnitude of voltage change is observed in all three phases as the result of a shift in the voltage of the parasitic neutral capacitance to earth of a non-solidly earthed load produced by an NSDD. An example of this is seen in Figure 50. However, in other cases, a clear identification of an NSDD may require a high time resolution measurement to observe the high frequency current or voltage pulse of an NSDD as seen in Figure 51.

Further examples of NSDDs are given in Figure 52, Figure 53 and Figure 54.

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The occurrence of NSDDs does not affect the performance of the switching device. Therefore, their number is of no significance to interpreting the performance of the device under test. However, they need to be reported in order to distinguish them from restrikes.

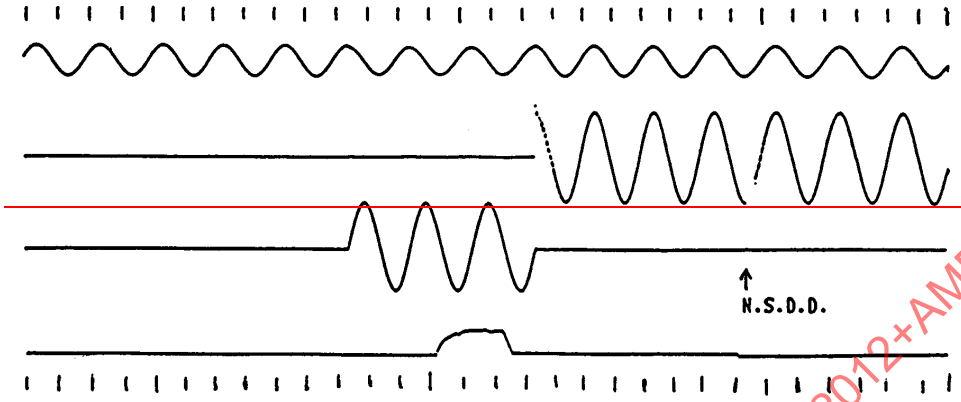
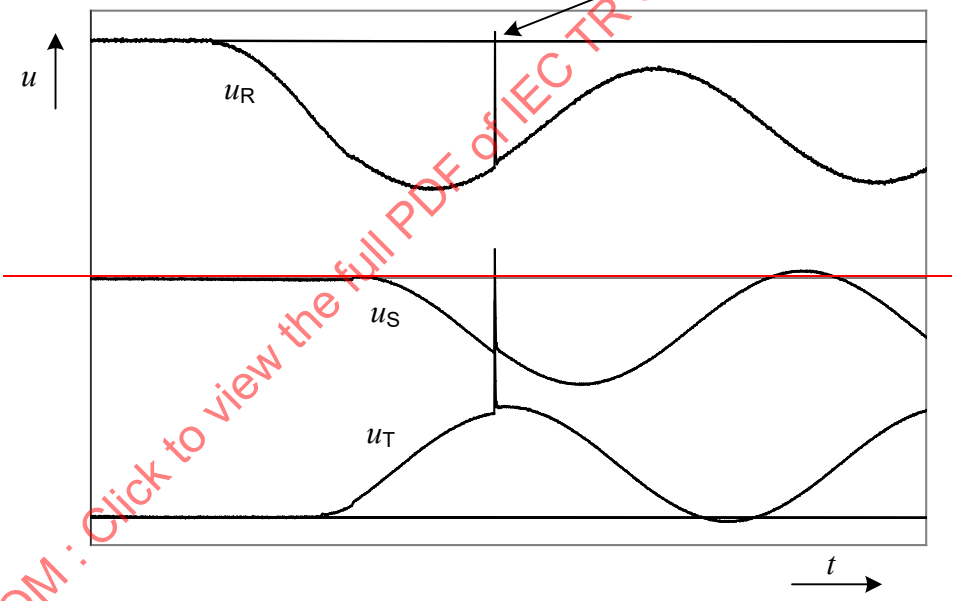


Figure 50 – NSDD in a single-phase test circuit



Key

u_R; u_S; u_T Recovery voltages in R, S and T phase, respectively

Figure 51 – NSDD (indicated by the arrow) in a three-phase test

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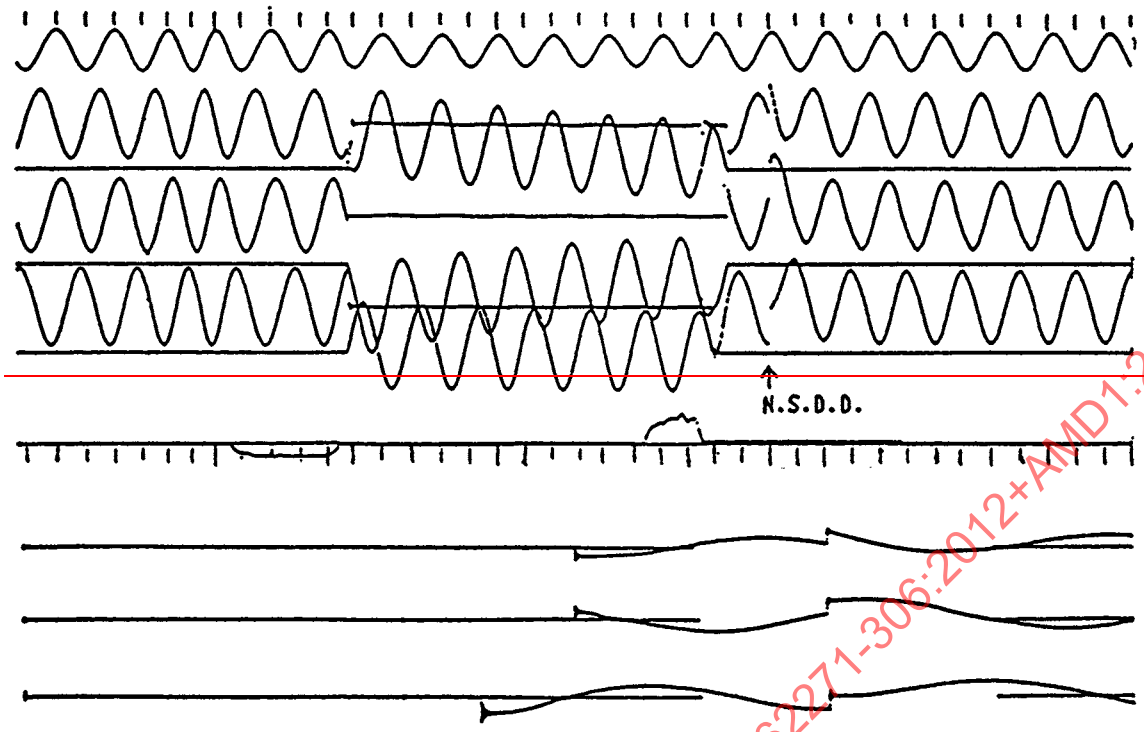
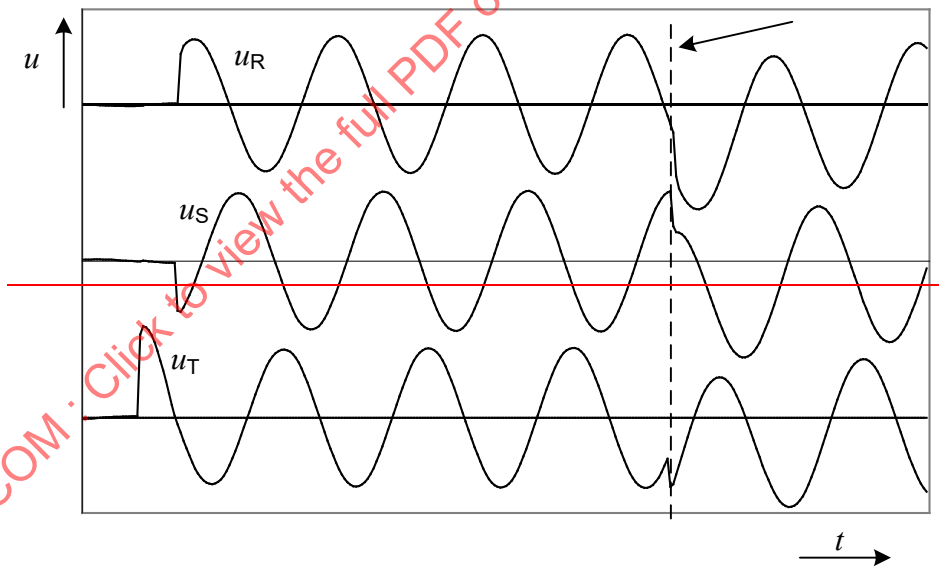


Figure 52 – A first example of a three-phase test with an NSDD causing a voltage shift in all three phases of the same polarity and magnitude



Key

u_R, u_S, u_T Recovery voltages in R, S and T phase, respectively

Figure 53 – A second example of three-phase test with an NSDD (indicated by the arrow) causing a voltage shift in all three phases of the same polarity and magnitude

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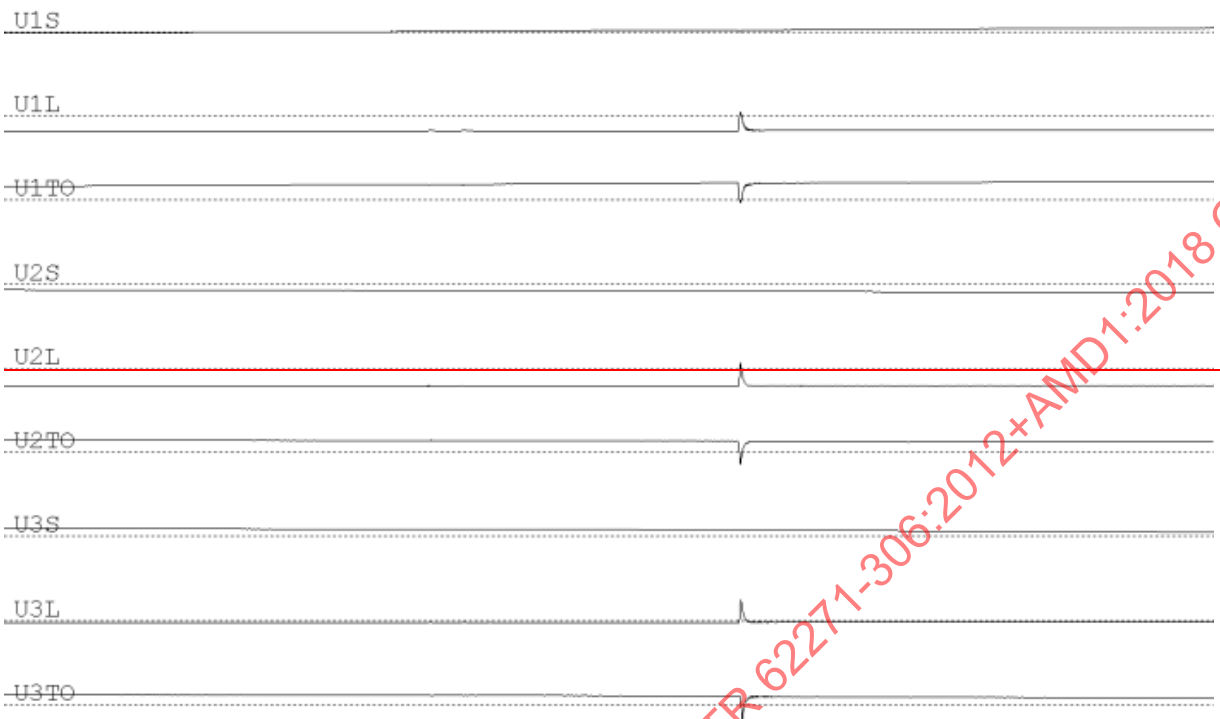

Key

U1S, U2S, U3S	Source side voltages of the first, second and third phase
U1L, U2L, U3L	Load side voltages of the first, second and third phase
U1TO, U2TO, U3TO	Voltage across the first, second and third pole of the circuit-breaker

Figure 54 – A typical oscillogram of an NSDD where a high resolution measurement was used to observe the voltage pulses produced by the NSDD

9.4 General application considerations

9.4.1 General

The capacitive current switching capability of the circuit-breaker is depending on its rated voltage, rated frequency, the particular application (i.e. overhead line, capacitor bank, etc.) and the earthing conditions of the network.

Caution should be exercised when applying older circuit-breakers that have not been tested to IEC 62271-100.

9.4.2 Maximum voltage for application

The operating voltage should not exceed the rated voltage since this is the upper limit for operation.

9.4.3 Rated frequency

The rated frequency for circuit-breakers is 50 Hz or 60 Hz. As described in 9.2.1.1.3 a rated frequency of 60 Hz results in a more severe stress on the circuit-breaker, since the voltage peak occurs earlier (at 8,3 ms) than in the case of 50 Hz (10 ms).

Special consideration should be given when comparing tests performed at 60 Hz to cover 50 Hz requirements or vice versa. At lower frequencies, the capacitance current switching ability

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will be adequate. The switching capability demonstrated at 60 Hz covers the requirements for 50 Hz with the same voltage factor.

9.4.4 Rated capacitive current

9.4.4.1 General

The preferred values of the rated capacitive switching current are given in Table 9 of IEC 62271-100:2008. Not all actual cases of capacitive current switching are covered by that table. The values for lines and cables cover most cases, the values of the current for capacitor banks (single and back-to-back) are typical and representative of actual values in service.

9.4.4.2 Overhead lines and cables

When very long lines and cables are considered, the no-load current may exceed that given in Table 5 of IEC 62271-100:2008.

The following may serve as an example: The no-load current of an overhead line is approximately 1,1 A/km at 50 Hz and 1,3 A/km for 60 Hz. Without considering the Ferranti effect (see 9.2.1.3.3), the charging current of a 500 km line would be 605 A at 50 Hz and 715 A at 60 Hz. Ferranti rise on a 500 km line would increase the charging current by about 4 % at 50 Hz and 6 % at 60 Hz. This is not covered by Table 9 of IEC 62271-100:2008.

The higher current does not pose a problem for circuit-breakers of present design, since the higher current tends to increase the minimum arcing time resulting in a wider contact gap when the recovery voltage reaches its peak. The possible peak recovery voltage present on interruption could be a problem (see 9.2.1.3.3).

For altitudes exceeding 1 000 m the capacitive current does not have to be corrected, provided that it does not exceed the corrected rated normal current.

9.4.4.3 Capacitor and filter banks

The same remark as given under 9.4.4.2 applies to capacitor and filter bank currents. The current is depending on the size of the capacitor bank and in certain cases the capacitor bank considered may have a current rating higher than that given in Table 9 of IEC 62271-100:2008. This does not pose a problem for circuit-breakers of present design.

9.4.5 Voltage and earthing conditions of the network

Subclause 6.111.7 of IEC 62271-100:2008 gives the multiplication factors for single-phase tests for the different conditions, refer to 9.2.1.4. They range from 1,0 for solidly earthed systems to 1,7 for non-effectively earthed systems in the presence of single- or two-phase to earth faults.

Both user and manufacturer must be aware of these earthing conditions in order to specify the correct circuit-breaker suitable for the application.

Harmonic filter switching usually results in a recovery voltage that contains several harmonic components. The recovery voltage may have a shape as indicated in Figure 55. Careful system study should be done to define realistic requirements regarding the recovery voltage. In some cases filter banks switching tests may need to be performed because capacitor bank switching tests do not cover the required recovery voltage waveshape. This needs to be considered when making the proper choice of circuit-breaker. From the voltage waveshape as indicated in Figure 55 it can be seen that the usual definition of re-ignition and restrike may no longer apply to a recovery voltage that does not have a 1 – cos waveshape.

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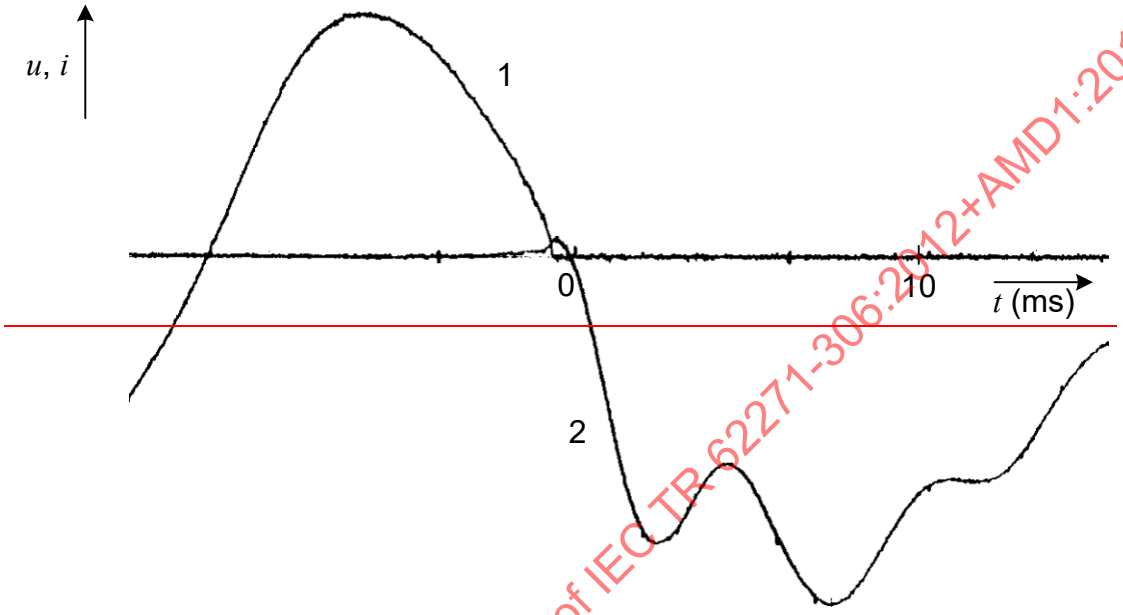
In case of a multi-frequency recovery voltage the definition of re-ignition and restrike should be based on the amplitude of the breakdown voltage. If the amplitude is less than 1,0 p.u. of the system voltage it is a re-ignition. If the amplitude is equal to or above 1,0 p.u. of the system voltage it is a restrike. These definitions of restrike and re-ignition are generally acceptable but may lead to expensive solutions. More economical solutions may be obtained by permitting restrikes in a zone were tests have demonstrated that they are not harmful to the circuit-breaker.



Key

1 Current through circuit-breaker

2 Voltage across circuit-breaker

Figure 55 – Example of the recovery voltage across a filter bank circuit-breaker

9.4.6 Restrike performance

As all circuit-breakers have a certain restrike probability in service, it is not possible to define a restrike-free circuit-breaker. It is more logical to introduce the notion of a restrike performance and this has been done in IEC 62271-100.

The restrike probability in service depends on the service conditions (for example the number of operations per year, network condition, maintenance policy of the user, etc.). So it is impossible to introduce a common probability level related to service condition.

To classify their restrike performance, two classes of circuit-breakers have been introduced: class C1 and class C2. It should be noted that the restrike performance is based on a specified test duty.

9.4.7 Class of circuit-breaker

The choice of the class of circuit-breaker is discussed in 3.3.

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~~**9.4.8 Transient overvoltages and overvoltage limitation**~~

~~**9.4.8.1 General**~~

~~An important consideration for application of circuit-breakers for capacitive current switching is the transient overvoltage which may be generated by restrikes during the opening operation. The transient overvoltage factor is defined as the ratio of the transient voltage appearing between a circuit-breaker disconnected terminal and the neutral of the disconnected capacitance during opening to the operating line-to-neutral crest voltage prior to opening.~~

~~The selection of the class (see 9.4.7) of circuit-breaker to be applied should be coordinated with the insulation capability of other components on the system.~~

~~**9.4.8.2 Overvoltages**~~

~~**9.4.8.2.1 General**~~

~~When switching capacitive currents, transients are generated. These transients are associated with the restrikes when de-energising a capacitive load and with the energisation of capacitive loads. These transients may cause:~~

- ~~insulation degradation and possible failure of the substation equipment,~~
- ~~operation of surge arresters;~~
- ~~interference in the control wiring of the substation;~~
- ~~increase in step potentials in substations;~~
- ~~undesired tripping or damage to sensitive electronic equipment.~~

~~The magnetic fields associated with high inrush currents during back-to-back switching in either the no-load transmission line conductors or the earthing grid during back-to-back switching can induce voltages in control cables by both capacitive and electromagnetic coupling. These induced voltages can be minimised by shielding the cables and using a radial configuration for circuits (circuits completely contained within one cable so that inductive loops are not formed).~~

~~**9.4.8.2.2 Switching of capacitor banks**~~

~~**9.4.8.2.2.1 General**~~

~~The switching of capacitor banks is associated with voltage and current transients (see 9.2.1.1 and 9.2.2.2). As most modern circuit-breakers have a very low probability of restrike, the majority of the switching transients will be generated when energising capacitor bank(s). The effects of the transients will exhibit themselves locally and at remote locations on the power system.~~

~~The high-frequency transient inrush current associated with back-to-back switching can stress other equipment in the circuit as well as the circuit-breaker. Wound-type current transformers will have turn-to-turn insulation stressed because of the high rates of rise of current and the resulting voltage that is developed across inductance in the circuit.~~

~~**9.4.8.2.2.2 Local effects**~~

~~The local effects are as follows:~~

- ~~voltage transients resulting in dielectric stresses on nearby equipment;~~
- ~~electrical, mechanical and electromechanical forces caused by the inrush current.~~

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~~**9.4.8.2.2.3 Remote effects**~~

~~The remote effects are as follows:~~

- ~~transfer of capacitively coupled fast transients through transformer windings;~~
- ~~reflections of travelling wave transients on open ended lines or transformer terminated lines;~~
- ~~excitation of near resonant portions of the power system by the oscillatory transient frequency.~~

~~**9.4.8.2.3 Switching of lines and cables**~~

~~When energising lines and cables, high overvoltages may be created depending on whether or not the line or cable was precharged as a result of a preceding breaking operation (i.e. in the case of an auto-reclosing). These overvoltages may result in damage of insulation.~~

~~**9.4.8.3 Overvoltage limitation**~~

~~There are several means available to reduce the overvoltages generated by the switching of capacitive currents:~~

- ~~**current limiting reactors** are normally used to reduce the current transients associated with back-to-back switching. They do not limit the remote overvoltages.~~
- ~~**pre-insertion resistors** limit the inrush current and remote overvoltages. It is a basic solution widely used on circuit-breakers. They are usually fitted on circuit-breakers and as such add to the complexity of the equipment. Depending on the design, the added complexity may or may not result in a reduced availability of the equipment (see also 9.4.16).~~
- ~~**pre-insertion reactors** also limit the inrush current and remote overvoltages. They are usually fitted on circuit-switchers and their effect on complexity and availability of the equipment is sometimes equivalent to pre-insertion resistors, depending on the design of the devices.~~
- ~~**controlled closing** reduces the magnitude of the inrush current depending on the point-on-wave of the voltage prior to the prestrike between the contacts. A simple way of reducing the transients is to let the circuit-breaker contacts close at a voltage zero. This method is called controlled closing. The controller also adds to the complexity of the equipment and can influence its availability.~~

~~**9.4.9 No-load overhead lines**~~

~~**9.4.9.1 General**~~

~~A circuit-breaker may be required to energize or de-energize a no-load transmission line during its normal operating duties. Prior to energisation, the line may or may not contain a trapped charge (see also 9.2.1.3). Consideration may need to be given to line energisation following load rejection (see [21]).~~

~~**9.4.9.2 Line charging current**~~

~~When considering the assigned line charging current rating, application is determined by the value of the line charging current. This current is a function of system voltage, line length, and line configuration.~~

~~Figure 56 gives an approximation of the line charging current per kilometre of different line configurations at 60 Hz. If the estimated current is greater than 90 % of the preferred line current rating, a more accurate calculation based on the actual line configuration and methods similar to that discussed in [21] should be used.~~

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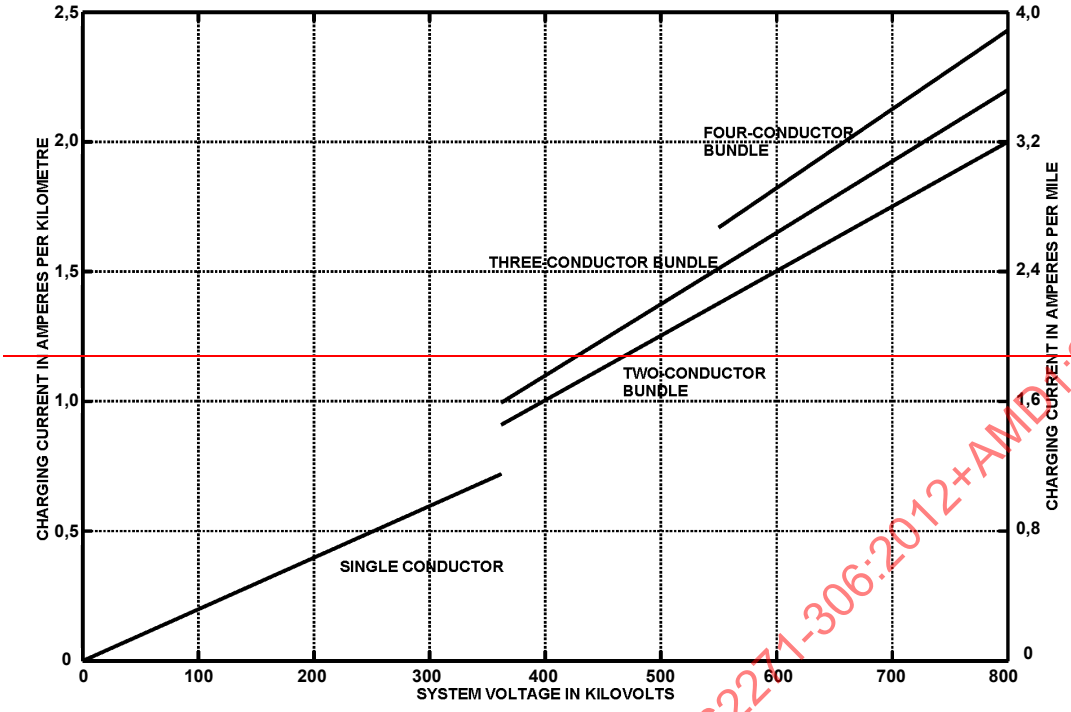

Figure 56 – RMS charging current versus system voltage for different line configurations at 60 Hz

From Figure 56 the capacitive reactance can be derived as follows:

Assume a system with a rated voltage of 245 kV, 60 Hz. The charging current is 0,5 A/km. The linear capacitive reactance X_C' is then:

$$X_C' = \frac{1}{\omega C'} = \frac{U}{I'} = \frac{245\ 000\ \text{V}}{\sqrt{3} \times 0{,}5\ \text{A/km}} = 0{,}283\ \text{M}\Omega\,\text{km},$$

where

X_C' is the linear capacitive reactance of the line in MΩ km;

C' is the capacitance of the line in F/km;

I' is the charging current of the line in A/km.

For a 50 Hz system frequency the corresponding value of X_C' would be

$$0{,}283 \times \frac{60}{50} = 0{,}34\ \text{M}\Omega\,\text{km}$$

To calculate the reactance X_C of a line with a given length l the linear reactance X_C' has to be divided by the length:

$$X_C = \frac{X_C'}{l}$$

Assume a length of 100 km for the example above. The reactance X_C is then:

$$X_C = \frac{X_C'}{l} = \frac{0{,}83\ \text{M}\Omega\text{km}}{100\ \text{km}} = 2{,}83\ \text{k}\Omega.$$

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9.4.9.3 Compensated overhead lines

As described in 9.2.1.3.2, very long lines (> 200 km) are often compensated with shunt reactors to reduce the amount of charging current required of the system. Similar effects as indicated in 9.2.2.3.2 may occur for fully compensated overhead lines.

If the circuit-breaker rating is chosen based on I_{lc}, the line could not be switched without the compensating reactor(s) connected. The voltage rise caused by the Ferranti effect and also the location of the reactor(s) will change the line current slightly.

9.4.9.4 No-load line recovery voltage

The line-charging breaking current rating is assigned on the basis of a standard recovery voltage associated with this type of circuit. For solidly earthed systems, the no-load line charging current switching tests require a maximum voltage of 2,4 times (see also 9.2.1.3.1.2) the rated phase-to-earth voltage across the circuit-breaker one half-cycle after interruption (assumes $C_1 = 2C_0$ where C_1 is the positive-sequence capacitance and C_0 is the zero-sequence capacitance). This is the difference voltage of the source and line sides, including the effects of coupled voltage on the first-pole-to-clear. The test voltage requires a 1-cosine waveshape.

For double-circuit lines with higher voltage factors refer to 9.2.1.4.

Deviations from the test voltage characteristics may increase or decrease the probability of the circuit-breaker restriking. As described in 9.2.1.3.2, a compensated line will have a lower peak of the recovery voltage, which will reduce the restrike probability.

9.4.10 Capacitor banks

9.4.10.1 General

A circuit-breaker may be required to switch a capacitor bank from a bus that does not have other capacitor banks energized (single or isolated) or against a bus that has other capacitor banks energized (back-to-back). In the application of circuit-breakers for capacitor switching duty, consideration must be given to the rated single (isolated) shunt capacitor bank switching current, rated back-to-back shunt capacitor bank switching current, rated transient inrush current, and rated transient inrush current frequency (see also 9.2.1.1 and 9.2.2.2).

9.4.10.2 Capacitor bank current

Circuit-breakers are to be applied according to the actual capacitive current they are required to interrupt. The rating should be selected to include the following effects.

a) *Voltage*. The reactive power rating of the capacitor bank, in kVar, is to be multiplied by the ratio of the maximum service voltage to the capacitor bank nameplate voltage when calculating the capacitive current at the applied voltage. This ratio can be as large as 1,1, since capacitors can be operated continuously up to 10 % above the capacitor rated voltage.

b) *Capacitor tolerance*. The manufacturing tolerance in capacitance is -0 to +15 % with a more frequent average of -0 to +5 %. A multiplier in the range of 1,05 to 1,15 should be used to adjust the nominal current to the value allowed by tolerance in capacitance.

c) *Harmonic component*. Capacitor banks provide a low-impedance path for the flow of harmonic currents. When capacitor banks are non-effectively earthed, no path is provided for zero-sequence harmonics (third, sixth, ninth, etc.), and the multiplier for harmonic currents is less. A multiplier of 1,1 is generally used for a solidly earthed neutral bank and 1,05 for a non-effectively earthed neutral.

In the absence of specific information on multipliers for the above factors, it will usually be conservative to use a total multiplier of 1,25 times the nominal capacitor current at rated

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capacitor voltage for non-effectively earthed neutral capacitor banks and 1,35 times the nominal current for solidly earthed neutral capacitor banks.

9.4.10.3 Methods for calculating transient inrush currents

9.4.10.3.1 Single or isolated capacitor bank

A bank of shunt capacitors is considered single (isolated) when the conditions described in 9.2.2.2.2 are fulfilled. Table 14 gives the equations that apply for calculation of the inrush current for single (isolated) capacitor bank energisation.

9.4.10.3.2 Back-to-back capacitor bank

The inrush current of a single bank will be increased when other capacitor banks are connected to the same bus (see also 9.2.2.2.3).

Table 14 gives the equations for calculating inrush current and frequency for both isolated and back-to-back capacitor bank switching, neglecting resistance. These equations are based on the theory described in 9.2.2.2.

A typical circuit for back-to-back switching is shown in Figure 57. The inductance in the circuit that limits the transient oscillatory current is composed of the inductance of the bus between switching devices, L_{bus}, the inductance between the switching device and the capacitor banks, L_1 and L_2, and the inductance of the capacitor banks, L_{e1} and L_{e2} and any additional reactance inserted. The total inductance between capacitor banks, $L_{e1} + L_1 + L_{bus} + L_2 + L_{e2}$, is very small with respect to the inductance of the source L_s. In most cases, the total inductance between capacitor banks will be less than 1 % of the inductance of the source, and the contribution of transient current from the source can be neglected.

The inductance of the bus can be calculated similar to a transmission line using values from tables available from suppliers of bus conductors for different bus configurations. (See 9.4.10.3.3).

The inductance within the capacitor bank itself is not easy to obtain, but in general it is of the order of 10 μH for banks above 52 kV, and 5 μH for banks below 52 kV. Typical values of inductance per phase between back-to-back capacitor banks and bank inductance for various voltage levels are given in Table 15.

Inherent resistance of the circuit causes rapid decay of the transient current so that the first peak actually may only reach 90 % to 95 % of the maximum value calculated. These values are applicable to both solidly earthed or non-effectively earthed banks and with Y or Δ connections. With a non-effectively earthed neutral, the current in the first two phases to close will be 87 % of calculated, but the current in the last phase will equal the value calculated. However, inherent resistance of the circuit will affect these currents by the factors indicated above.

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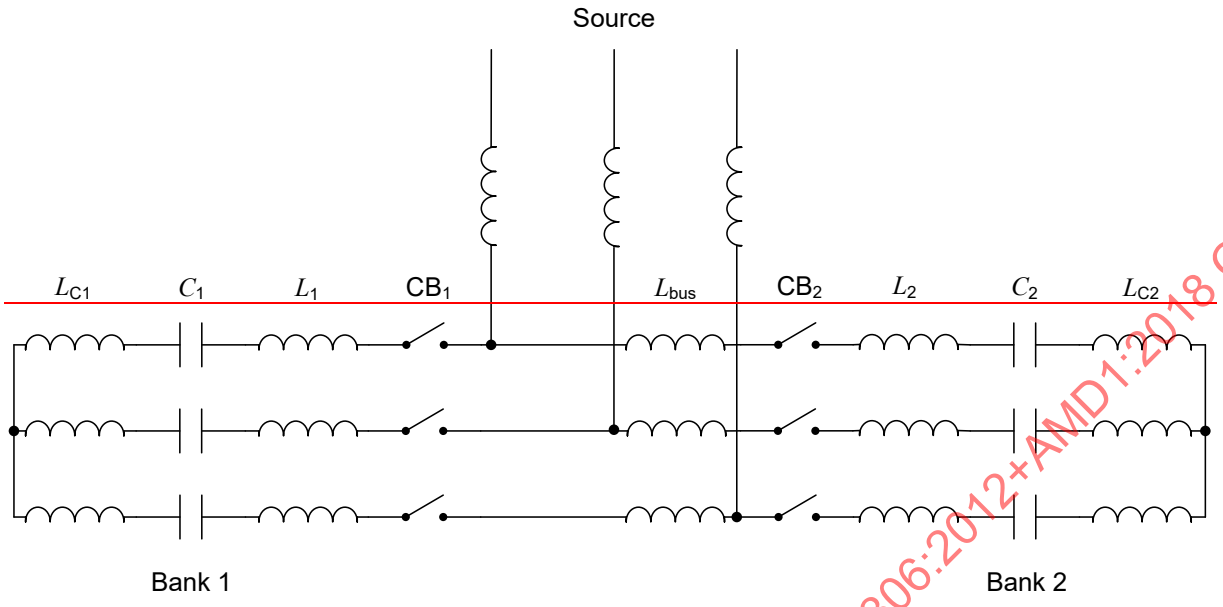

~~**Key**~~

~~CB_1~~	~~Circuit-breaker energising capacitor bank 1~~
~~CB_2~~	~~Circuit-breaker energising capacitor bank 2~~
~~L_S~~	~~Source inductance~~
~~L_{C1}, L_{C2}~~	~~Capacitor bank inductance~~
~~L_1, L_2~~	~~Bus inductance between switching device and capacitor bank~~
~~L_{bus}~~	~~Inductance of bus between switching devices~~

~~Figure 57 – Typical circuit for back-to-back switching~~

~~The equations in Table 14 for back-to-back switching will give correct results when switching a bank against another bank. However, when switching against several other banks connected to the bus, the correct value of equivalent inductance to be used for the combination of banks connected to the bus is not easily obtained. For example, when switching a bank against three other banks energized on the bus, the calculated current will be too high if an inductance of $L/3$ is used. On the other hand, using a value of $3L$ will result in a current which is too low. If exact solutions cannot be made, conservative results should be used in calculating inrush currents by using the inductance divided by the number of capacitor banks, recognising that the results will be 20 % to 30 % higher (see also 9.2.2.2.3). When more than two banks are installed on the same bus, a more exact calculation of the inrush current parameters is obtained using an electromagnetic transient program.~~

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Table 14 – Inrush current and frequency for switching capacitor banks

Condition	Quantity	When using currents
Energising an isolated bank	$i_{i\,peak}$ (A)	$1{,}41\sqrt{I_{sc} \times I_1}$
	f_i (Hz)	$f_s\sqrt{\frac{I_{sc}}{I_1}}$
Energising a bank with another on the same bus	$i_{i\,peak}$ (A)	$13\,500\sqrt{\frac{U_r I_1 I_2}{f_s L_{eq}(I_1 + I_2)}}$
	f_i (kHz)	$9{,}5\sqrt{\frac{f_s U_r (I_1 + I_2)}{L_{eq}(I_1 \times I_2)}}$
Energising a bank with an equal bank energized on the same bus	$i_{i\,peak}$ (A)	$9545\sqrt{\frac{U_r I_1}{f_s L_{eq}}}$
	f_i (kHz)	$13{,}5\sqrt{\frac{f_s U_r}{L_{eq} I_1}}$

Key

f_s is the system frequency (Hz);

L_{eq} is the total equivalent inductance per phase between capacitor banks, in μH;

I_1, I_2 are the currents (in A) of banks being switched and of bank already energized, respectively. The capacitor bank being switched is assumed uncharged, with closing at a voltage crest of the source voltage. The current used should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of capacitance. In the absence of specific information, a multiplier of 1,15 times normal capacitor current would give conservative results;

$I_{i\,peak}$ is the peak value calculated without damping. In practical circuits it will be about 90 % of this value;

U_r is the rated voltage in kV;

I_{sc} is the symmetrical short circuit current, in A r.m.s.

9.4.10.3.3 Considerations for transient inrush currents

The inrush currents of different types of compact multi-section banks with minimum spacing between the individual sections may differ by as much as 20 %. Consequently, these inrush currents can be reduced significantly by increasing the lengths (inductance) of the circuits between the sections.

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Table 15 – Typical values of inductance between capacitor banks

Rated maximum voltage (kV)	Inductance per phase of busbar (μH/m)	Typical inductance between banks [a] (μH)
17,5 and below	0,702	10-20
36	0,781	15-30
52	0,840	20-40
72,5	0,840	25-50
123	0,856	35-70
145	0,856	40-80
170	0,879	60-120
245	0,935	85-170

[a] Typical values of inductance per phase between capacitor banks. This does not include inductance of the capacitor bank itself. Values of 5 μH for banks below 52 kV and 10 μH for banks above 52 kV are typical for the inductance of the capacitor banks.

Another effective measure to reduce transient inrush currents is to add inductance in the circuit between the capacitor banks.

In the first edition of IEC 62271-100 the equivalency rule between the test performed and the service conditions was based on the product of inrush current peak and frequency, $i_{\text{i peak}} \times f_{\text{i}}$ (kAkHz). Calculations have shown that the arc energy during a making operation is independent of the inrush current frequency for cases where the preaching time is greater than half a period of the inrush current frequency. This is usually the case for back-to-back capacitor bank switching. For back-to-back capacitor bank switching, the arc energy during a making operation is only a function of the inrush current peak. On the other hand, it is well known that the shape of the wear on the arcing contacts as well as the effect of the pressure shock waves are somewhat frequency dependent and should not be disregarded. Because of the latter, an upper tolerance of +130 % has been specified on the permissible inrush current frequency that can be used in service. In other words: the inrush current frequency used during the tests should not be lower than 77 % of the inrush current frequency foreseen in service. This concept is limited to inrush current frequencies up to 6 kHz since the information available for higher frequencies is limited.

Although circuit-breakers have usually been tested with inrush currents up to 25 kA_{peak} and 4 kHz, system designers should endeavour to keep the inrush currents far below this value for system quality reasons.

The following example will illustrate the use of the equations in Table 14.

A 123 kV system is assumed as shown in Figure 58.

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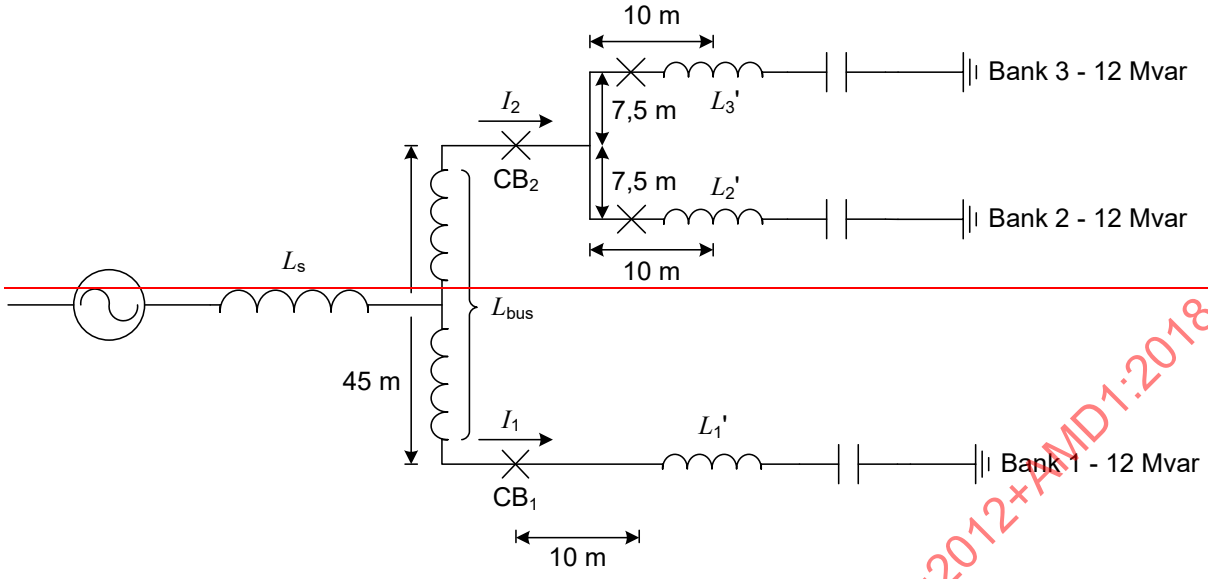

Key

U_r	123 kV (the rated capacitor bank voltage is 115 kV)
L_S	Source inductance, = 3,77 Ω, 10 mH (f_s = 60 Hz)
L_1', L_2', L_3'	Inductance between circuit breaker and capacitor bank, including inductance of capacitor bank
L_{bus}	Inductance of bus between switching devices
CB$_1$, CB$_2$	Circuit breakers
	Short circuit of source: 18 600 A at 123 kV

Figure 58 – Example of 123 kV system

The capacitor banks shown have a nominal rating of 12 Mvar (capacitors rated 100 kVar, 13,28 kV, five series sections with eight capacitors in parallel). Nominal current per bank is 60 A. In determining the rating of the circuit-breaker required, the increase in current due to applied voltage, capacitance tolerance, and harmonics should be considered. The increase in current at maximum rated voltage is: maximum voltage to capacitor rated voltage = 123/115 = 1,07. Assume a positive tolerance of capacitors of +10 %, multiplier of 1,1 and assume a multiplier for harmonic content for a solidly earthed neutral bank of 1,1.

The total multiplier used to determine the single (isolated) and back-to-back current rating is 1,07 × 1,1 × 1,1 = 1,29, giving a current of 1,29 × 60 = 78 A. With capacitor banks 2 and 3 energized, the current through CB$_2$ is 156 A.

The circuit-breakers intended for this duty have the following ratings: rated voltage 123 kV, rated current 1600 A, rated short-circuit current 40 kA, rated single (isolated) and back-to-back capacitive switching current 400 A.

The transient inrush current and frequency are calculated using the equations in Table 14. In the example, L_1', L_2' and L_3' are the inductances between the respective capacitor banks and the circuit-breakers, including the inductance of the capacitor bank. L_{bus} is the inductance of the bus between the circuit-breakers.

The inductance values in Table 15 can be used or values can be calculated for the actual bus configuration used. In the example given below, the added reactance between the circuit-breaker and capacitor bank is:

L_1' = 20,0 µH

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$L_2' = L_3' = 27{,}1\ \mu H$

The inductance of the busbar $L_{bus} = 38{,}5\ \mu H$.

In determining inrush current and frequency, the currents I_1 and I_2 as used in Table 14 should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of capacitance. In the example, the multiplier to be used is 1,07×1,1 = 1,18. The currents are $I_1 = 60 \times 1{,}18 = 71$ A and $I_2 = 71$ A or 142 A, depending on whether bank 2 or 3 or both banks are energized.

Case I. Energisation of capacitor bank 1 with banks 2 and 3 not energized (single or isolated bank switching),

$$i_{\text{max peak}} = 1{,}4\sqrt{I_{sc} \times I_1} = 1{,}4\sqrt{18\,600 \times 71} = 1{,}4\sqrt{132 \times 10^4} = 1\,625\ \text{A}$$

$$f_i = f_s\sqrt{\frac{I_{sc}}{I_1}} = 60\sqrt{\frac{18\,600}{71}} = 971\ \text{Hz}$$

The calculated rate of change of current for the single (isolated) bank switching is

$$\left(\frac{\mathrm{d}i_i}{\mathrm{d}t}\right)_{\max} = 2\pi f_i i_{i\,\text{peak}} = 2\pi \times 971 \times 1\,625 = 9{,}9\ \text{A/}\mu\text{s}$$

This is less than the maximum rate of change for a rated short-circuit current of 40 kA which is equal to $2\pi f_s\sqrt{2}I_{sc} = 21{,}3$ A/μs and therefore meets the requirements of isolated capacitor bank switching.

Case II. Energisation of bank 1 with bank 2 energized on the bus (back-to-back switching against an equal-size bank),

$$i_{i\,\text{peak}} = 9\,545\sqrt{\frac{U_r I_1}{f_s L_{eq}}}$$

The equivalent inductance L_{eq}, is the sum of $L_1' + L_{bus} + L_2' = 20{,}0 + 38{,}5 + 27{,}1 = 85{,}6\ \mu H$.

$$i_{\text{max peak}} = 9\,545\sqrt{\frac{123 \times 71}{60 \times 85{,}6}} = 9\,545\sqrt{170} = 12\,445\ \text{A}_{\text{peak}}$$

$$f_i = 13{,}5\sqrt{\frac{f_s U_r}{L_{eq} I_1}} = 13{,}5\sqrt{\frac{60 \times 123}{85{,}6 \times 71}} = 13{,}5\sqrt{1{,}21} = 14{,}9\ \text{kHz}$$

The calculated back-to-back inrush current and frequency must be compared with the back-to-back switching capability listed in Table 5 of IEC 62271-100:2008. For a maximum voltage of 123 kV, the assumed rated values are 20 kA_{peak} and 4,25 kHz. The calculated value of the inrush current peak is within this rating, the inrush current frequency exceeds that assumed and inductance must be added between the capacitor banks to reduce the inrush current frequency. Adding an inductance of 1 mH will limit the inrush current to 3,5 kA and the frequency to 4,18 kHz, both of which are below the assumed capability.

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Case III. Energisation of bank 1 with banks 2 and 3 energized on the bus. For this case, assume the equivalent inductance of banks 2 and 3 equal to one half of L_2' or (27,1)/2 = 13,6 μH. The total current of banks 2 and 3 is 142 A, which is under the assumed isolated bank switching capability of 400 A as listed in Table 9 of IEC 62271-100:2008. For this case, I_1 = 71 A, I_2 = 142 A, and the equivalent inductance between the capacitor bank being energized and the banks already energized is the sum of L_2'/2 + L_{bus} + L_1' = 13,6 + 38,5 + 20 = 72,1 μH.

$$i_{peak} = 13\,500\sqrt{\frac{U_r(I_1 \times I_2)}{f_s L_{eq}(I_1 + I_2)}} = 13\,500\sqrt{\frac{123 \times 71 \times 142}{60 \times 72{,}1 \times 213}} = 15\,660 \text{ A}_{peak}$$

and

$$f_i = 9{,}5\sqrt{\frac{f_s U_r(I_1 + I_2)}{L_{eq}(I_1 \times I_2)}} = 9{,}5\sqrt{\frac{60 \times 123 \times 213}{72{,}1 \times 71 \times 142}} = 14{,}0 \text{ kHz}$$

Of the calculated values of inrush current peak and frequency, the frequency of 14,0 kHz exceeds the assumed back-to-back switching capability of 4,25 kHz listed in Table 9 of IEC 62271-100:2008. As in the previous case of switching identical banks, adding an inductance of 0,71 mH will limit the inrush current and frequency to 4,7 kA_{peak} and 4,24 kHz, respectively, both of which are below the assumed back-to-back switching capability of 123 kV circuit-breaker.

Based on the system and conditions studied, a circuit-breaker having the following ratings would be applied: rated short-circuit current of 40 kA and rated isolated capacitor bank switching current of 400 A. The assumed back-to-back rating of 20 kA and 4,25 kHz that goes with this rating will be exceeded unless additional inductance is added between the capacitor banks. A value of 0,71 mH is sufficient to keep within the assumed ratings available.

9.4.11 Switching through transformers

Circuit-breakers may be required in some applications to switch capacitors, lines, or cables through an interposed transformer. The current switched by the circuit-breaker will be N times the capacitor, line, or cable current on the other side of the transformer, where N is the transformer turns ratio.

Switching charging current through a transformer may be less difficult than switching the same current directly. The capacitive elements of the circuit will oscillate with the transformer inductance, which may also saturate, producing a less severe transient recovery voltage and a lower probability of restrike. If a restrike should occur, the additional inductance will help to limit the inrush current. Saturation may also occur when de-energizing a remote transformer that is fed through a long cable. The stress on the transformer is not considered harmful.

If the value of N is greater than 1, switching through a transformer will have the effect of increasing the current being switched. De-energising no-load overhead lines with lower voltage circuit-breakers can result in effective line charging currents in the 750 A to 1 000 A range. The capacitive switching rating of circuit-breakers which may be exposed to this type of duty must be carefully checked before application is made.

Voltage and current relations are shown in Figure 59 as an example of capacitor switching through an interposed transformer. It can be seen that due to the reduced recovery voltage, the increased current is not a problem for the circuit-breaker.

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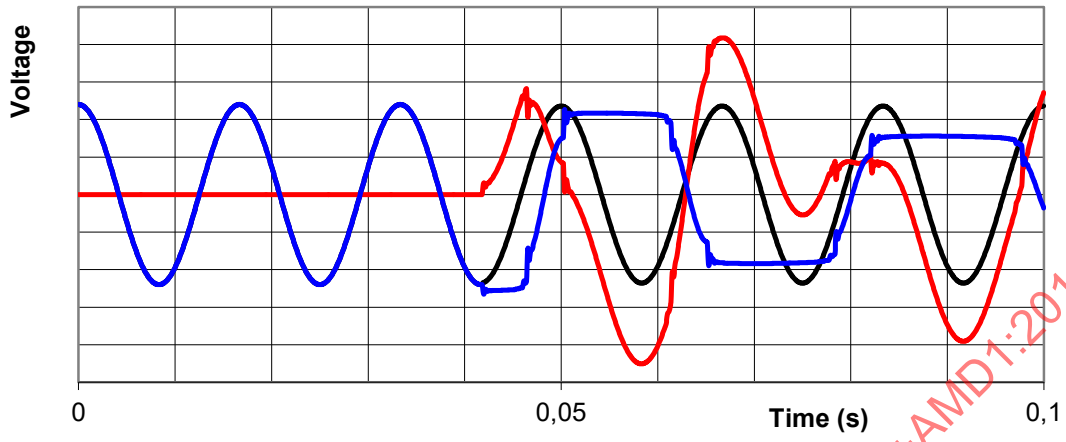


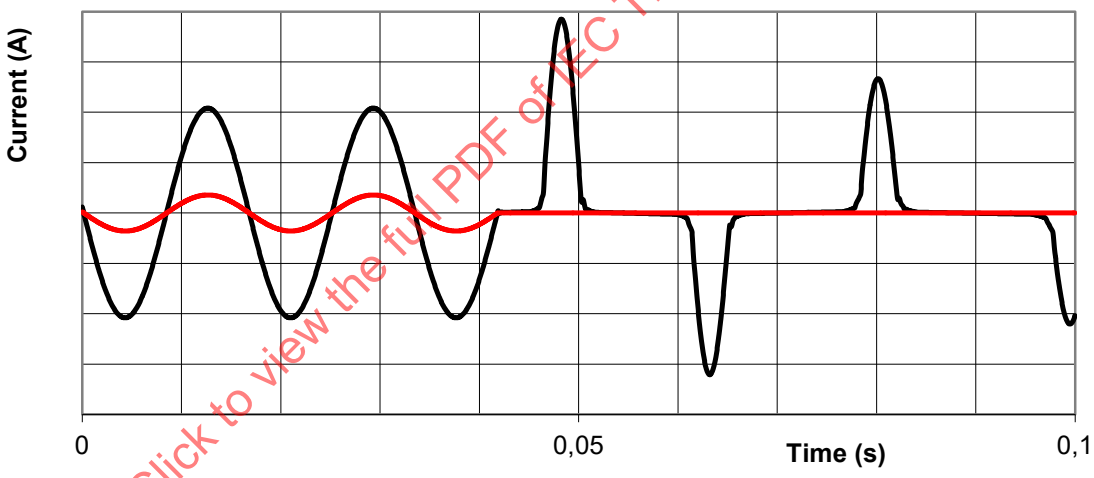
~~Key~~

~~Black line~~ ~~Source voltage~~

~~Blue line~~ ~~Voltage on the load side of the circuit-breaker~~

~~Red line~~ ~~Voltage across the circuit-breaker~~

~~**Figure 59a – Voltage relations**~~



~~Key~~

~~Black line~~ ~~Capacitor bank current (Low voltage side of the transformer~~

~~Red line~~ ~~Current through the circuit-breaker~~

~~**Figure 59b – Current relations**~~

~~Figure 59 – Voltage and current relations for capacitor switching through interposed transformer~~

~~9.4.12 Effect of transient currents~~

~~9.4.12.1 General~~

~~In the application of circuit-breakers in stations having banks of capacitors it may be necessary to investigate the effects of transient currents and other special situations upon circuit-breakers other than those specially equipped for and assigned to the routine capacitor switching.~~

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The transient currents of capacitor banks may be considered in two aspects: the inrush currents upon energising of the banks and the discharge currents into faults. Where the quantity of parallel capacitor banks installed in a station is large, the transient currents may have significant effects upon the circuit-breaker.

The transient currents may have large peaks and high frequencies which may affect circuit-breakers in the following ways:

a) a circuit-breaker may be subjected to a transient inrush current which exceeds its rating. This may occur with the circuit-breaker in the closed position or when closing into solidly earthed faults.

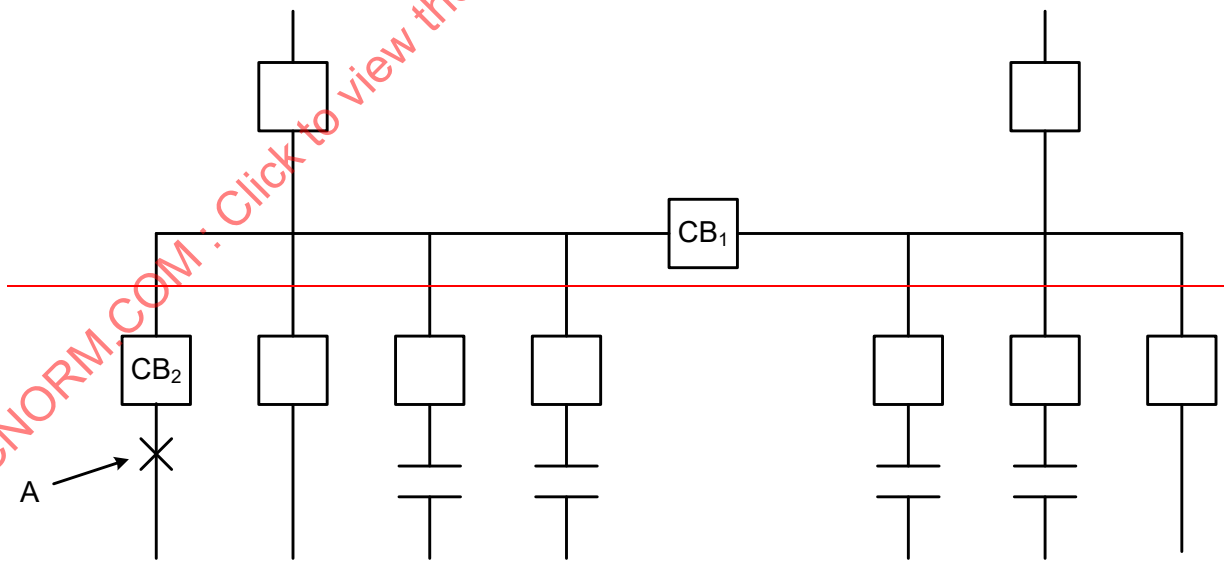
b) the transient inrush current may have sufficient magnitude and rate of change to flash over the secondaries of current transformers or the associated control wiring.

Circuit-breakers located in a position such as a tie circuit-breaker between bus sections (bus section or bus coupler) may be exposed to the transient inrush currents from energising banks of capacitors when they are located on bus sections on both sides of the circuit-breaker (see Figure 60, CB_1).

Seldom will the inrush current exceed the capability of the circuit-breaker. However, a check may be required to determine if the rate of change of inrush current will cause overvoltages on the secondary of current transformers on the circuit-breaker or in the current path between the capacitor banks.

9.4.12.2 Exposure to total capacitor bank discharge current

In a substation where parallel capacitor banks are located near or on a busbar, any circuit-breaker connected to the bus may be exposed during faults to the total discharge current of all the banks located behind the circuit-breaker. In Figure 60, CB_2 will be subjected to this total discharge current with a fault occurring at location A. The worst case, or highest capacitor discharge current, occurs with a bolted three-phase fault where capacitor banks are non-effectively earthed and for a case of a three-phase-to-earth or a line-to-earth fault where capacitor banks are solidly earthed.



Key

CB_1, CB_2 Circuit-breakers

Figure 60 – Station illustrating large transient inrush currents through circuit-breakers from parallel capacitor banks

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The total discharge current (peak) of all banks behind the circuit-breaker is equal to the algebraic sum of the individual banks of capacitors. Neglecting resistance, the discharge current of an individual capacitor bank is equal to:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{C}{L}} \quad (78)$$

where

$I_{\text{d peak}}$ is the crest value of discharge current;

U_{r} is the rated voltage;

C is the capacitance per phase of individual bank;

L is the inductance per phase between capacitor bank and fault location.

The inductance L is primarily made up of bus conductors and any additional inductance added to the bank for limiting the inrush currents.

If there are n capacitor banks of approximately equal capacitance and separated by an approximately equal inductance to the fault, then the total discharge current is approximately equal to the sum of the crest current of each bank or n times that of one bank. This is demonstrated as follows:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{Cn}{L/n}} = \frac{\sqrt{2}}{\sqrt{3}} U_r n \sqrt{C/L} \quad (79)$$

In addition to the checking of the crest current it may be necessary also to check the rate of change of the discharge current with the manufacturer.

The transient discharge current passing through a circuit-breaker must also be examined for its effects upon the current transformers. The discharge currents may substantially exceed the magnitudes and the frequency of the inrush currents described in 9.4.12. This occurs because the contribution may come from a number of capacitor banks and is not limited by the inrush impedance seen when energising a bank of capacitors.

9.4.13 Exposure to capacitive switching duties during fault switching

Where parallel banks of capacitors are located on bus sections in a station, caution must be exercised in the fault switching sequence so that the last circuit-breaker to clear is not subjected to a capacitive switching duty beyond its capability. This is especially a concern for a circuit-breaker used as a bus section tie circuit-breaker with capacitors located on both sides of the circuit-breaker as shown in Figure 60, CB_4.

The worst case occurs in a station where the bus section tie circuit-breaker is last to clear the bus for a fault that leaves one or more phases of the capacitor banks fully energized. In this situation, the bus tie circuit-breaker must be properly equipped and rated for the parallel switching of the capacitor banks remaining on the bus section to be de-energized. In the example of Figure 60, this means that the tie circuit-breaker must be capable of switching two banks of capacitors in parallel with two banks of capacitors on the source side. Another solution is to coordinate if possible the clearing times so that the tie circuit-breaker is always first to clear to avoid the capacitor switching duty.

9.4.14 Effect of load

The situation can occur where a circuit-breaker is called upon to switch a combination of a capacitive current and a load current. The circuit-breaker will have the required switching capability if the total current does not exceed the rated continuous current of the circuit-breaker and either

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a) the power factor is at least 0,8 leading, or

b) the capacitive current does not exceed the rated capacitive switching current of the circuit-breaker.

Where the above conditions are exceeded, the capability and performance of the circuit-breaker is not defined by the standards and the manufacturer should be consulted. When the power factor is below 0,8 leading, the voltage may be sufficiently out-of-phase with the current to cause unacceptable restriking. The situation will be more severe if there is also a bank of capacitors located on the source side of the circuit-breaker.

9.4.15 Effect of reclosing

Up to twice normal inrush currents are possible when reclosing is applied to a circuit-breaker switching capacitive loads. When capacitor bank current is interrupted at or near a normal current zero, the voltage remaining on the bank may be near peak value. Reclosing a circuit-breaker against such a charged capacitor bank may produce high inrush current.

When a capacitor bank is connected to the load side of a feeder circuit-breaker equipped with automatic reclosing, high inrush currents can be avoided by isolating the capacitor bank from other loads after the circuit-breaker is tripped and before reclosing. The switching device used for regular capacitor bank switching can be employed for isolation. This technique is particularly recommended where other capacitor banks are connected to the same station bus.

A second technique to avoid high inrush currents during reclosing is to increase reclosing time delay. Normally, the discharge resistors inside each capacitor unit will reduce residual voltage or other deliberately introduced discharging devices.

Discharge curves are available from the capacitor supplier and should be consulted where reclosing time is delayed.

9.4.16 Resistor thermal limitations

For capacitor bank circuit-breakers equipped with pre-insertion resistors, the thermal capability of the resistors must be considered in determining the time interval between capacitive current switching operations. The resistance value is related to the size of the capacitor bank and the pre-insertion resistors should normally have a thermal capability as defined by the rated duty cycle.

If capacitive current switching field tests are planned which exceed the number of operations as defined by the thermal capacity of the pre-insertion resistors, or which utilise a specially designed circuit-breaker, the manufacturer should be consulted regarding the frequency of operations.

9.4.17 Application considerations for different circuit-breaker types

9.4.17.1 General

The switching of capacitive current poses different stresses on the different types of circuit-breakers. Restrikes on opening and prestrikes on closing may or may not be a problem. The considerations given below are general and are based on experiences gained by laboratory tests, field tests and field experience.

9.4.17.2 Oil circuit-breakers

9.4.17.2.1 Restrikes

Depending on the design (contact speed, electrode shape, etc.) an oil circuit-breaker generally has long arcing times when interrupting. The restrike probability increases with

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increased current, because gas bubbles reduce the effective amount of oil between the contacts causing a reduction of the dielectric strength of the contact gap. These circuit-breakers deserve special consideration when used or relocated to a system where the line charging current exceeds the rating.

Some oil circuit-breakers are pressurised to reduce the size of the bubbles and therewith increasing the dielectric strength of the contact gap. Some oil circuit-breakers may be fitted with breaking resistors, to reduce the effects of a restrike.

An oil circuit-breaker will normally not interrupt the high frequency current associated with the restrike and the high arc impedance introduces an additional damping of the restrike current. This will reduce the risk for multiple restrikes.

Older contraction type oil circuit-breakers are known to produce multiple restrikes that may result in voltage escalation and subsequent development of an evolving fault.

9.4.17.2.2 Prestrikes

Oil circuit-breakers are especially sensitive to high-frequency prestrikes when energising capacitor banks. The prestrikes cause a shock wave in the oil. As oil is not compressible, the shock wave causes mechanical stresses on the internal components of the breaking chamber. As a result of the exposure to these high mechanical stresses, the breaking chamber insulator may shatter and even stationary contacts may crack. Application of an oil circuit-breaker for capacitor bank switching requires a severe reduction of the inrush current frequency or special design of the oil circuit-breaker (e.g. using pre-insertion resistors).

Bulk oil circuit-breakers have been applied using a limitation of 20 kAkHz for over 30 years with no documented problems.

For minimum oil circuit-breakers a value of 1 kAkHz is suggested.

9.4.17.3 Vacuum circuit-breakers

9.4.17.3.1 Restrikes

The voltage withstand of the contact gap of a vacuum circuit-breaker rises very fast and the restrike probability is low. When a restrike occurs, the contact gap is small and the vacuum circuit-breaker is usually capable of interrupting the high-frequency restrike current, which may result in voltage escalation.

9.4.17.3.2 NSDDs

NSDDs (see 9.3) are normally associated with vacuum circuit-breakers and are generally not a concern.

9.4.17.3.3 Prestrikes

The duration of the prestrike in a vacuum circuit-breaker is short. Shock waves are not a problem for this type of circuit-breaker.

The high-frequency discharge together with contact bouncing may lead to micro contact melting, especially when the arc is burning in the anode-spot mode (this occurs with currents higher than 10 kA). The breaking of welded points during a subsequent breaking operation with a very low current can damage the contact surface and this may reduce the dielectric withstand of the contact gap. However, a subsequent breaking operation with higher current may increase the dielectric withstand to its original condition. A subsequent no-load test may flatten the micro spot resulting in an increased dielectric strength.

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~~**9.4.17.4 SF_6 circuit-breakers**~~

~~**9.4.17.4.1 Restrikes**~~

~~The interrupting capacity of SF_6 circuit-breakers is limited by the recovery voltage, which means that the frequency and earthing conditions (i.e. whether the circuit is effectively or non-effectively earthed) are important factors in the determination of the capability of the circuit-breaker.~~

~~The capacity of clearing the high-frequency restrike current is low for puffer circuit-breakers and even lower for self-blast (or arc assisted) circuit-breakers. This also means that the risk for voltage escalation is low. However, a restrike may cause tracking and/or puncture of the insulating material between the contacts (e.g. nozzle, sleeve, etc.).~~

~~**9.4.17.4.2 Prestrikes**~~

~~The duration of the prestrike is depending on many parameters (e.g. the voltage per breaking unit, the closing speed, etc.). Regarding inrush current peak and frequency there is referred to 9.4.10.3.3.~~

~~**9.4.17.5 Air-blast circuit-breakers**~~

~~**9.4.17.5.1 Restrikes**~~

~~In general, the restrike probability of an air-blast circuit-breaker is higher than that of an SF_6 circuit-breaker. The flashover characteristic of air has a wider scatter than that of SF_6. Air-blast circuit-breakers can interrupt the high-frequency discharge current, which means that they have a higher probability of multiple restrikes, which may lead to voltage escalation.~~

~~**9.4.17.5.2 Prestrikes**~~

~~The considerations given in 9.4.17.4.2 also apply to air-blast circuit-breakers.~~

~~**9.5 Considerations of capacitive currents and recovery voltages under fault conditions**~~

~~**9.5.1 Voltage and current factors**~~

~~Some requirements, general ratings and tests for capacitive current switching are based on switching operations in the absence of faults. The presence of a fault can increase the value of both the capacitive switching current and recovery voltage. This is recognised by IEC 62271-100 by the specification of two voltage factors when breaking in the presence of faults. These voltage factors are given in 9.2.1.4 and are 1,4 for effectively earthed systems and 1,7 for non-effectively earthed systems. Tests for these conditions are not mandatory. An example of such a fault is a circuit-breaker switching an overhead line that interrupts fault current in one phase and capacitive current in the other two phases.~~

~~The fact that the capacitive switching current increases in the presence of earth faults is recognised in 6.111.9.3 of IEC 62271-100:2008, where the line and cable charging currents are multiplied by 1,25 for effectively earthed neutral systems and 1,7 for non-effectively earthed systems. The number of tests is reduced to reflect the fact that such operations do not occur frequently.~~

~~For capacitor banks the situation is different. No tests are required for switching of solidly earthed neutral single (isolated) capacitor banks in solidly earthed neutral systems. Switching of non-effectively earthed neutral capacitor banks in solidly earthed neutral systems is not considered a normal system condition and no requirements or tests have been specified. Switching back-to-back is not considered a normal system condition and no requirements and tests have been specified.~~

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9.5.2 Reasons for these specific tests being non-mandatory in the standard

In service, circuit-breakers have been successful in interrupting capacitive circuits under faulted conditions for a number of reasons. Principal reasons for successful operation include:

a) the probability of a fault occurring at minimum operating conditions of the circuit-breaker and its operating mechanism is extremely small;

b) the capacitance of the faulty phase is likely to be discharged before contact separation takes place;

c) the voltage factor used for single-phase tests is in excess of the service condition giving the tested circuit-breaker added margin;

d) laboratory tests are performed using a minimal voltage jump, resulting in short arcing times. This condition is more severe than the actual network condition;

9.5.3 Contribution of a capacitor bank to a fault

Consider the network situation given in Figure 60. A single line simplification is given in Figure 61. A fault has occurred on the line that is interrupted by the circuit-breaker. The capacitance of the capacitor bank will modify the TRV across the circuit-breaker to a 1-cos waveshape having a moderate rate-of-rise with an enlarged amplitude factor compared to the case without the presence of the capacitor bank.

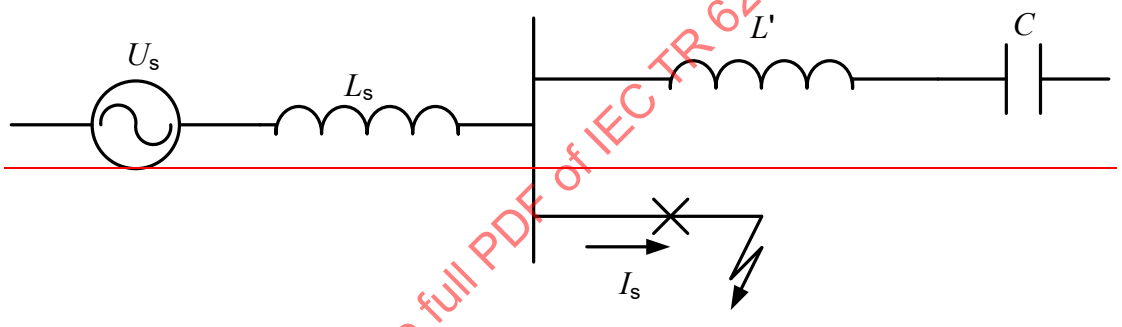

Figure 61 – Fault in the vicinity of a capacitor bank

When the ITRV is negligible, the circuit-breaker will attempt to interrupt at the first available current zero following contact separation, resulting in a relatively small contact gap. As the recovery voltage increases across the gap, a re-ignition might occur and the capacitor bank will discharge into the fault through the circuit-breaker. The amplitude of the discharge current depends on the voltage across the circuit-breaker contacts at the time of re-ignition and the frequency of the discharge current is determined by the inductance between the capacitor bank and the fault location.

The high frequency discharge current is superimposed on the fault current, which creates additional current zeros. Depending on the type of circuit-breaker (oil, air-blast, vacuum or SF_6), the high frequency current may be interrupted causing high overvoltages. For further information, please refer to [24] and [25].

A similar situation may occur, when circuit-breaker CB closes into a fault. The capacitor bank discharges into the fault and depending on the magnitude of the inductance between the capacitor bank and the fault location, the discharge current can reach peak values and frequencies that exceed those given in Table 9 of IEC 62271-100:2008 (see also 9.4.12.2).

For these specific outrush cases the manufacturer should be consulted. For further treatment of this subject, see IEEE 1036 [26].

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~~**9.5.4 Switching overhead lines under faulted conditions**~~

~~The voltages and currents which occur when switching a faulted transmission line are affected by the circuit parameters and the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage for switching an unfaulted transmission line as $2 \times 1{,}2 \frac{U_r \sqrt{2}}{\sqrt{3}} = 2{,}4$ p.u. When switching a faulted line this value may be exceeded, as may be the rated capacitive switching current value as listed in Table 9 of IEC 62271-100:2008 (see also [27]).~~

~~When switching a no-load overhead line with a phase-to-earth fault, the highest voltage occurs on the unfaulted phase which interrupts prior to the faulted phase (see Figure 62a). The highest current occurs on the last phase to interrupt when the faulted phase is the first to interrupt. The current for this case is not a sine wave but is distorted, as shown in Figure 62b. Under these conditions, the voltages and currents may exceed those on which the design tests are based.~~

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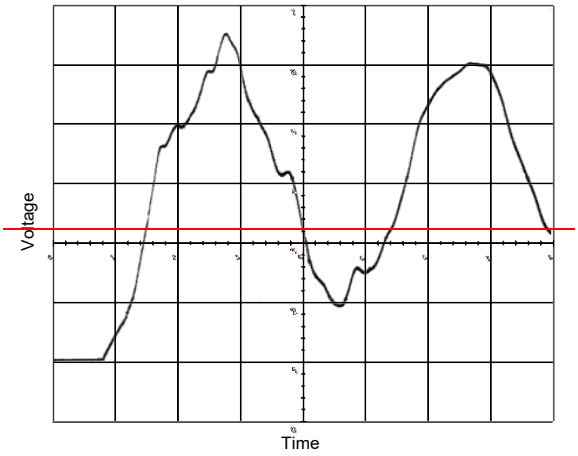
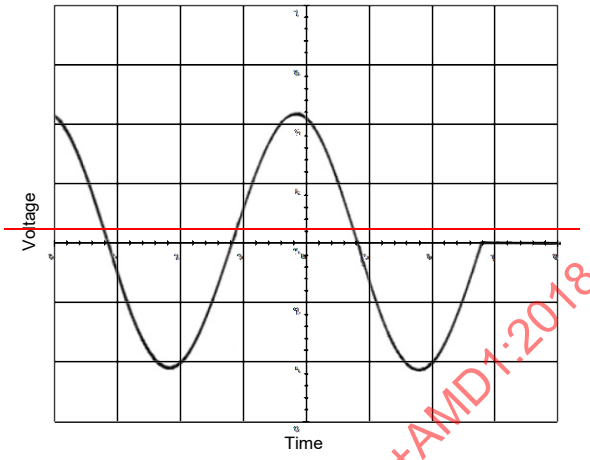
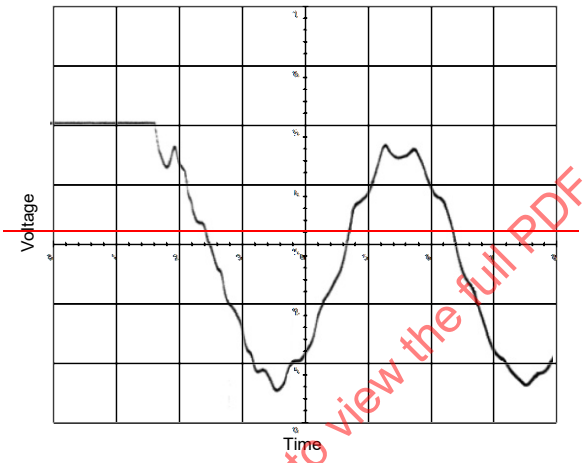


Maximum recovery voltage 2,74 × U_{max} (phase-to-earth)

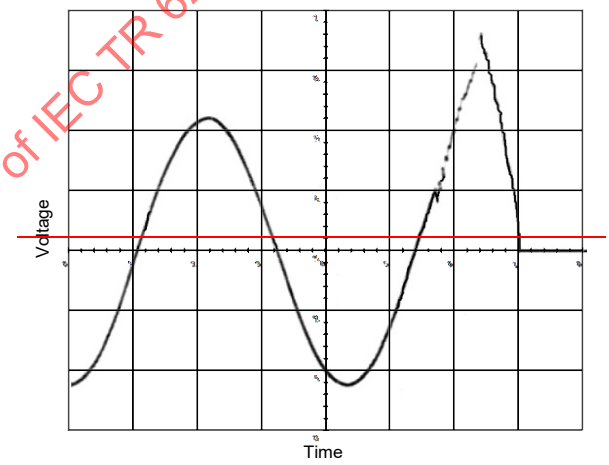


Maximum current 1,09 × rated current

Figure 62a – Recovery voltage and current for first-phase-to-clear when the faulted phase is the second-phase-to-clear



Maximum recovery voltage 2,18 × U_{max} (phase-to-earth)



Maximum current 1,77 × rated current

Figure 62b – Recovery voltage and current for last-phase-to-clear when the faulted phase is the first-phase-to-clear

Figure 62 – Recovery voltages and currents for different interrupting sequences

For the phase-to-phase fault condition, the recovery voltage and capacitive current are less severe than for the two phase-to-earth fault condition, see also [26].

9.5.5 Switching capacitor banks under faulted conditions

9.5.5.1 General

The voltages and currents which can occur when switching a faulted capacitor bank depend upon the earthing conditions, whether the fault is to the bank neutral or to earth, and on the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage in switching an unfaulted shunt capacitor bank as 2,8 p.u. When switching a faulted bank, this value may be exceeded, as may the rated capacitive switching current

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value. In the sections below a comparison is given between the recovery voltages and currents of a reference condition and two faulted conditions: a fault to neutral in the capacitor bank and a fault to earth in one phase.

NOTE The factor 2,8 for the maximum recovery voltage specified in IEC 62271-100 is valid when switching a non-effectively earthed capacitor bank where the second and third phases clear 90 degrees after the first. This is true for modern circuit-breakers. For older circuit-breakers, where the second and third phases do not clear 90 degrees after the first, this factor is 3,0.

9.5.5.2 Reference condition

9.5.5.2.1 General

The reference condition is illustrated in Figure 63. The neutral of the source and the capacitor bank may be solidly earthed and/or non-effectively earthed. The size of the capacitor bank is such that the current is equal to the rated single (isolated) capacitor bank current.

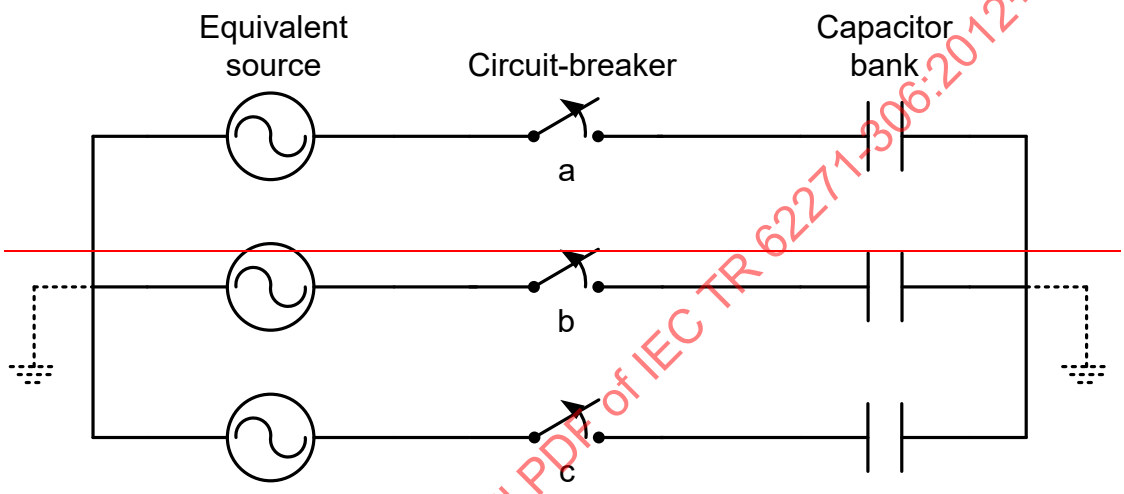

Figure 63 – Reference condition

9.5.5.2.2 Recovery voltage

The highest recovery voltage (2,5 p.u.) is obtained in the first-pole-to-clear when either the neutral of the capacitor bank, the neutral of the source or both are non-effectively earthed and poles 2 and 3 clear 90 degrees after the first.

The voltages obtained with this reference condition (unfaulted balanced system) are covered when testing single-phase with a voltage factor of 1,4 as required in IEC 62271-100. Although the voltage across the last poles to interrupt when at least one of the neutrals (source or bank) is non-effectively earthed can reach $2 \times U_r$ (3,46 p.u.), the two phases are in series so that neither is stressed to more than 2,8 p.u.

9.5.5.2.3 Capacitor bank current

In all cases the capacitor bank current does not exceed the rated single (isolated) capacitor bank current.

9.5.5.3 Fault to neutral in one phase (one capacitor bank phase short-circuited)

9.5.5.3.1 Recovery voltage

The highest recovery voltage ($2 \times U_r \sqrt{2} = 3{,}46$ p.u.) is obtained when at least one neutral is non-effectively earthed and the first-pole-to-clear clears a healthy phase. This is in agreement

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with the voltage factor of 1,7 specified in IEC 62271-100. If the first-pole-to-clear interrupts an unfaulted phase, it is subjected to a recovery voltage of 3,46 p.u. until the second and third phases interrupt.

The highest recovery voltage in the remaining phases is 3,46 p.u., but it is shared by two interrupters in series.

9.5.5.3.2 Current

The highest capacitive current is obtained in the cases described under 9.5.5.3.1 when the faulted phase is the first-pole-to-clear and is equal to 3 times that of the reference case.

9.5.5.4 Fault to earth in one phase

Most systems are effectively earthed and the highest recovery voltage is obtained when the first-pole-to-clear interrupts a non-faulted phase. In this case the maximum recovery voltage peak will be 2,8 p.u.

The most severe case is when the source is non-effectively earthed and the bank neutral is solidly earthed. If an unfaulted pole is the first to interrupt, the current may reach √3 times that of the reference condition and the recovery voltage 3,46 p.u. The remaining poles are subjected to the same current, but upon interrupting, share the 3,46 p.u. recovery voltage. When the faulted pole is the first-pole-to-clear, the current may be 3 times the rated current value and the recovery voltage $2 \times 1{,}25 \times \frac{U_r \sqrt{2}}{\sqrt{3}}$. The second pole to interrupt will have a lower current but a higher recovery voltage of $2 \times U_r \sqrt{2} = 3{,}46\ \text{p.u.}$ which will be shared with the third pole. If the faulted pole reignites, one of the unfaulted poles will then interrupt and the conditions will be as previously described when an unfaulted pole was the first to interrupt.

9.5.5.5 Other fault cases

For phase-to-phase earth faults, or phase-to-phase non-effectively earthed faults, with the source solidly earthed and the bank neutral non-effectively earthed, recovery voltages and currents are no more severe than for the standard no-fault condition.

9.5.6 Switching cables under faulted conditions

The normal frequency capacitive currents and recovery voltages on a faulted cable circuit will be the same as for a solidly earthed capacitor bank under faulted conditions.

9.5.7 Examples of application alternatives

Other application options available are listed below.

a) Use a circuit-breaker of a higher rating in those cases of earth faults on non-effectively earthed systems where the recovery voltage and current, or both, exceed the requirements of IEC 62271-100.

b) Reduce the capacitance of the existing capacitor bank size so that the current under faulted conditions does not exceed the rated capacitive switching current of the circuit-breaker.

c) Use a high-speed switch to earth the source or capacitor bank neutral before switching the capacitor bank under faulted conditions.

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d) Use a Δ configuration for the capacitor bank instead of a non-effectively earthed Y.

9.6 Explanatory notes regarding capacitive current switching tests

9.6.1 General

Subclause 6.111 of IEC 62271-100:2008 deals with capacitive current switching tests. In the 1st edition of IEC 62271-100 a new test procedure has been introduced for the two classes of capacitive current switching that deserve some explanation.

9.6.2 Restrike performance

See 9.4.6.

9.6.3 Test programme

In defining the test programme for these two classes, the following elements have been taken into account:

- the average number of operations per year carried out by circuit-breakers switching capacitive loads;
- the ability to reduce the number of tests by performing an increased number of switching operations at the minimum arcing time, usually the most difficult capacitive switching operation for circuit-breakers, thus keeping a high level of reliability;
- the recommendations of CIGRE working group A3.04. The expected restrike probability is exclusively related to the type tests

The proposed number of tests may be questioned because of different assumptions for probability calculations. Nevertheless, these values represent a good compromise (which is the role of the standard where conflicting views exist), reflecting the needs of users (in response to market demand) and above all they avoid unrealistic demands. These tests are not reliability tests but type tests to demonstrate a satisfactory capacitive current switching capability of the equipment in service.

9.6.4 Subclause 6.111.3 of IEC 62271-100:2008 – Characteristics of supply circuit

The paragraph concerning factor k_e / k_{pp} (from earlier versions of the standard) where k_e is the voltage factor as described in 9.2.1.4 and k_{pp} is the first-pole-to-clear factor has been deleted because there is neither use nor need for testing.

The variation of the power frequency voltage has been chosen as 5 % for test-duty 2 (LC2, CC2 and BC2) and 2 % for test-duty 1 (LC1, CC1 and BC1). These values are a compromise, taking limitations of testing laboratories into account. Considering the type test as a whole, because of the different stresses in the individual test-duties, any undue reduction of the electric stress during the tests is avoided. The actual values for the power frequency voltage variation (depending on the short-circuit power of the system and the capacitive load) is in the range of 1 % to 2 %.

9.6.5 Subclause 6.111.5 of IEC 62271-100:2008 – Characteristics of the capacitive circuit to be switched

The interval after final arc extinction, in which the voltage decay shall not exceed 10 %, has been changed from 100 ms to 300 ms based on service conditions.

9.6.6 Subclause 6.111.9.1.1 of IEC 62271-100:2008 – Class C2 test duties

Performing these capacitive current switching tests for class C2 equipment on a preconditioned circuit-breaker is, on the one hand, a recommendation of CIGRE working group A3.04; on the other hand, it draws closer to the real conditions of service, without

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prejudice as to whether this preconditioning improves the capacitive current switching performance of the circuit-breaker or not.

Close-open operations may be performed with no-load closing operations. In any case, the complete sequence shall be tested in order to test the circuit-breaker during opening in a dynamic condition, i.e. during the motion of the fluid caused by the previous closing operation.

9.6.7 Subclauses 6.111.9.1.1 and 6.111.9.2.1 of IEC 62271-100:2008 – Class C1 and C2 test duties

The tolerance of the testing current values for test-duty 1 (LC1, CC1 and BC1) were increased from the old range 20 % to 40 % to the new range 10 % to 40 % in order to give more freedom during testing for combined test-duties for different applications.

The proposed test sequences have been tested in a laboratory (particularly the adjustment of the minimum arcing time by steps of 6°) and are well adapted to the philosophy of the tests.

Performing some tests at rated pressure is a more pragmatic approach to the notion of type testing, knowing that the circuit-breaker does not always stand under the worst functioning conditions.

9.6.8 Subclauses 6.111.9.1.2 and 6.111.9.1.3 of IEC 62271-100:2008 – Single-phase and three-phase line- and cable-charging current switching tests

In test-duty 2 of single-phase line-charging and cable-charging tests (LC2 and CC2), the tests are split into open operations and close-open operations (6.111.9.1.3) to follow more or less the actual service conditions. However, for practical reasons, due to the small number of tests, in three-phase tests (6.111.9.1.2) in test-duty 2 (LC2 and CC2), close-open operations are performed exclusively.

9.6.9 Subclauses 6.111.9.1.2. to 6.111.9.1.5 of IEC 62271-100:2008 – Three-phase and single-phase line, cable and capacitor bank switching tests

Close-open operations are important for capacitor bank switching because of the effect of inrush current. Close-open operations are not significant for line- or cable-switching applications, therefore for line- and cable-switching tests, only a small number of close-open operations are requested (closing may be performed as a no-load operation).

A rough parity of the number of three-phase and single-phase tests has been maintained.

The mandatory nature for capacitor bank switching tests is due to the necessity to introduce the effect of inrush current at the beginning of the tests.

9.6.10 Subclauses 6.111.9.1.4 and 6.111.9.1.5 of IEC 62271-100:2008 – Three-phase and single-phase capacitor bank switching tests

Because of the large number of operations in actual service compared with the limited number of operations during type testing, a high number (80 or 120 respectively) of close-open operations shall be carried out in capacitor bank tests to simulate the wear in service even if the close-open operation is not the normal switching sequence.

For capacitor bank switching tests test-duty 1 (BC1) also needs to be performed, even if the actual service switching duty is always at 100 % nominal current, for the following reasons:

– the tests at 10 % to 40 % nominal current cover an increased number of actual currents;

– knowledge of the capacitive current switching performance is improved.

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9.1 General

Preferred values for capacitive current switching are given in Table 9 of IEC 62271-100:2008. The values include both de-energisation and energisation of capacitive loads as follows:

– shunt capacitor banks in single and parallel configurations;

– no-load cables in single and parallel configurations;

– no-load transmission lines.

The values given in Table 9 of IEC 62271-100:2008 for inrush current peak and frequency are not linked to the back-to-back capacitor bank breaking current.

Capacitive currents are typically in the order of up to a few hundred amperes and interruption is generally considered a light duty for a circuit-breaker. However, restriking is an issue since it may lead to undesirable overvoltages or high-frequency transients affecting power quality and also may cause damage to the interrupting unit or units. Circuit-breakers are therefore rated according to their restriking probability, i.e. restrike performance class C1 or C2 as discussed in 3.3.

Energisation of capacitive loads is usually associated with transient voltages and currents. Those transients are the following:

– inrush currents;

– overvoltages caused by the system response to the voltage dip when energizing capacitor banks;

– overvoltages caused by travelling waves on transmission lines and cables.

These transients also present power quality issues and some form of mitigation may be necessary as discussed later. IEC 62271-100 contains preferred values of inrush current magnitude and frequency, namely 20 kA peak and 4 250 Hz.

Type testing is designed to be representative of the service conditions up to the point of either clearing, reigniting or restriking. Because the actual value of overvoltage and transient response is totally system-dependent, tests cannot replicate these effects. By providing a means of assessing the likelihood of restrike occurrence, the user can determine what best suits their application. It is assumed that since capacitor switching is not the only source of overvoltage, other protection systems are employed and in the case of unacceptable power quality for sensitive electronic equipment, a sufficiently low number of likely events are selected. A separate study of actions relative to power quality on energisation should also be made.

In the selection of the rating for the circuit-breaker for capacitive current switching, the following needs to be considered:

a) application, i.e. capacitor bank (single or back-to-back), cable or transmission line;

b) power frequency of the network;

c) earthing situation of the network;

d) neutral earthing of the capacitor bank, i.e. solidly earthed or isolated;

e) presence of single or two phase-to-earth faults.

Based on the application, the required restrike performance class of the circuit-breaker can be chosen (C1 or C2) and also the mechanical endurance class (M1 or M2). Network earthing, presence of single and two phase-to-earth faults are important factors that determine the recovery voltage across the circuit-breaker, which, in turn, determines the test voltage of the circuit-breaker.

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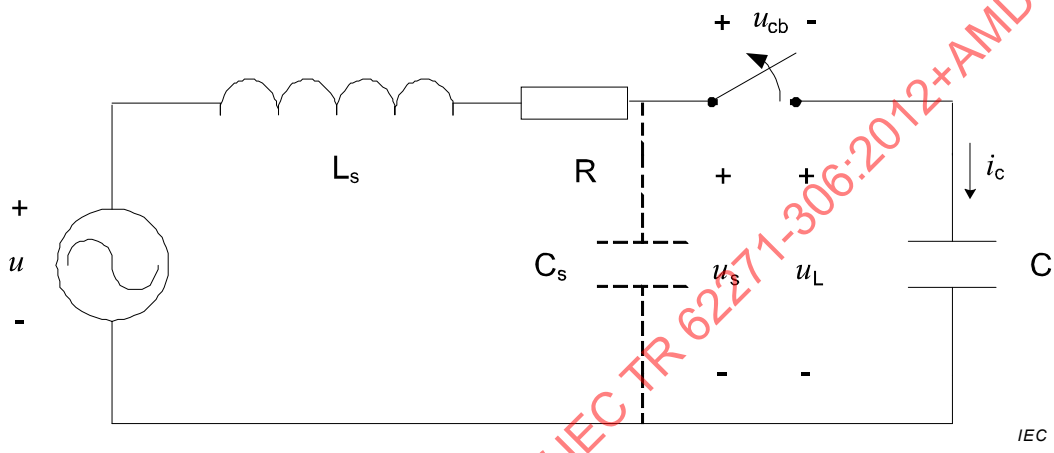
In 9.2, the general theory of capacitive current switching is given as well as the application and testing considerations.

9.2 General theory of capacitive current switching

9.2.1 De-energisation of a capacitive load

9.2.1.1 General

The single-phase equivalent circuit shown in Figure 98 may be used to illustrate the conditions when de-energising a capacitive load. The capacitive load is in this case represented by a concentrated capacitor.



Key

u	Source voltage (r.m.s.)	u_{cb}	Voltage across the circuit-breaker (r.m.s.)
L_s	Source inductance	u_L	Voltage across the capacitive load (r.m.s.)
R	Resistor representing the losses in the circuit	i_c	Capacitive current (r.m.s.)
C_s	Source side capacitance (stray capacitance)	C	Capacitive load (capacitor bank, transmission line or cable)
u_s	Source side voltage (r.m.s.)		

Figure 98 – Single-phase equivalent circuit for capacitive current interruption

9.2.1.2 Capacitive current

The capacitive current i_c flowing in the circuit is given by Equation (147):

$$i_c = \frac{\omega_s C \times u}{1 - \omega_s^2 L_s C} = \frac{\omega_s C \times u}{1 - \frac{\omega_s^2}{\omega_l^2}} \quad (147)$$

where

C is the capacitance of capacitor bank C (F).

$$\omega_s = 2\pi f_s ,$$

where

f_s is the system frequency (Hz).

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$$\omega_i = \frac{1}{\sqrt{L_s C}} = 2\pi f_i \ ,$$

where

f_i is the inrush current frequency in Hz (see also 9.2.3);

L_s is the inductance of the source inductance L_s (H).

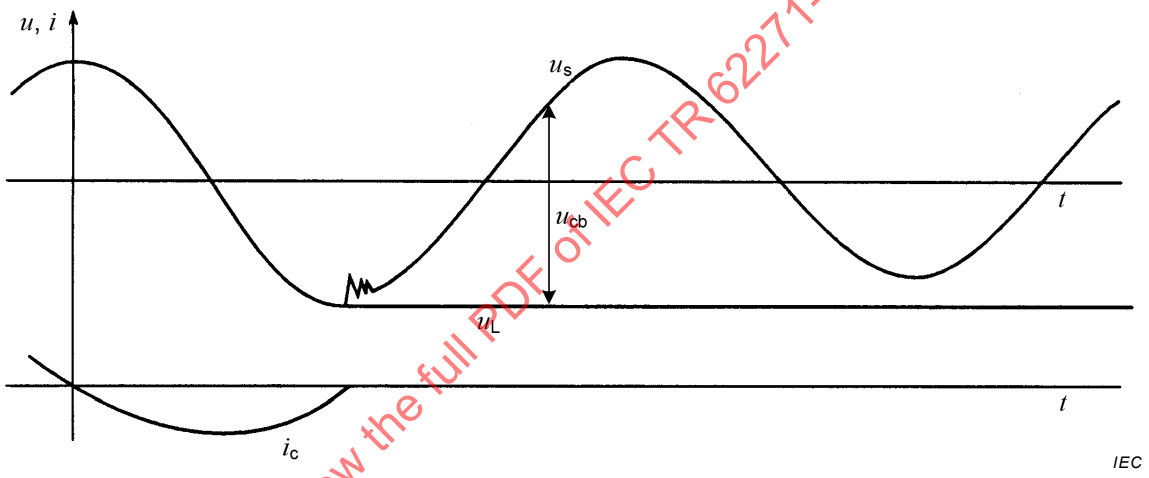
With $\omega_i >> \omega_s$, Equation (147) transforms to $i_c = \omega_s C \times u$.

In the determination of the power frequency capacitive current the influence of the resistance R is usually negligible and is ignored in Equation (147).

9.2.1.3 Recovery voltage

9.2.1.3.1 Recovery voltage in a single-phase circuit

Figure 99 shows the current and voltage shapes at interruption.



Key

i_c	Capacitive current
u_L	Voltage on the load side of the circuit-breaker
u_{cb}	Voltage across the circuit-breaker
u_s	Voltage on the source side of the circuit-breaker

Figure 99 – Voltage and current shapes at capacitive current interruption

After interruption of the current, the supply side voltage u_s will be more or less unaffected. There is only a minor decrease in amplitude, associated with the removal of the capacitive load. The transition to the new amplitude value is associated with a slight oscillation, the frequency of which is determined by L_s and C_s.

The interruption of the current leaves a trapped charge on the capacitor bank. The voltage u_L will remain constant at the value it had at current zero (namely the peak value of the supply voltage).

Together with the low-current amplitude to be interrupted, the low initial rate-of-rise of the recovery voltage makes it relatively easy for the circuit-breaker to interrupt. Some circuit-breakers may interrupt even if the current zero occurs immediately after contact separation. Half a cycle after current zero, the recovery voltage increases to an amplitude of twice the

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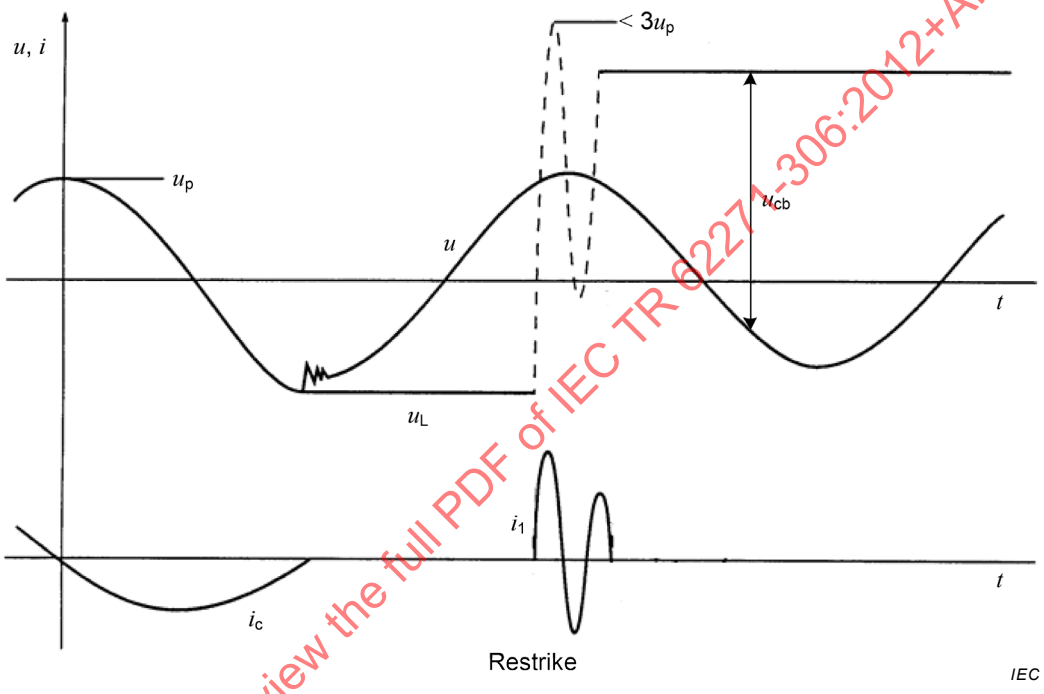
peak value of the supply voltage. Consequently, a rated frequency of 60 Hz is more severe than 50 Hz. The circuit-breaker may then not be able to withstand the high value of the recovery voltage across a relatively small contact gap. Dielectric breakdown may occur between the contacts and the current is re-established between the contacts.

Figure 100 shows current and voltage wave shapes in a case where voltage breakdown occurs relatively close to the recovery voltage peak. The load side voltage will swing up to a voltage that ideally (without damping present) reaches three times the supply voltage peak u_p. The oscillation frequency of the current and voltage after the breakdown is determined by L_s and C (assuming $C >> C_s$). The circuit-breaker may interrupt the oscillatory current at one of its current zeros, with the result that the voltage across the capacitor may attain a new constant value, perhaps higher than before. Further breakdowns associated with even higher overvoltages across the load may then occur (Figure 101).



Key

u_p	Peak of the source voltage
i_c	Power frequency capacitive current
i_1	Restrike current through the circuit-breaker
u_L	Voltage on the load side of the circuit-breaker
u_{cb}	Voltage across the circuit-breaker

Figure 100 – Voltage and current wave shapes in the case of a restrike

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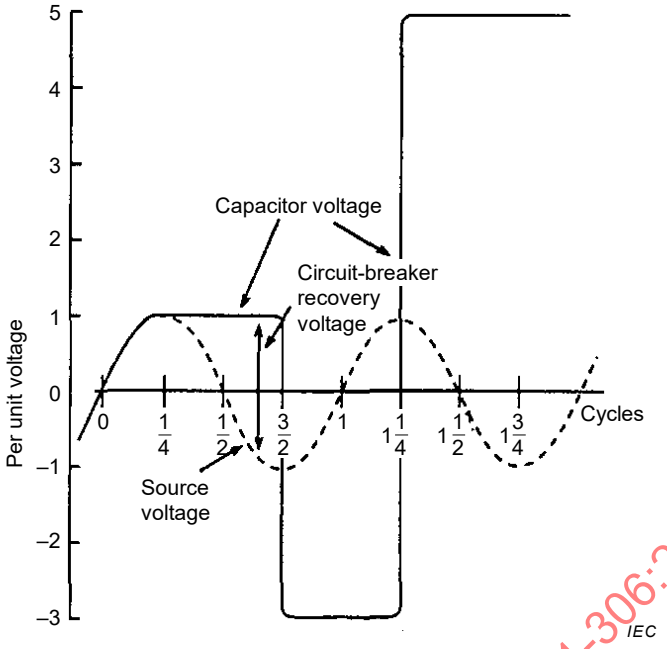

Key

1 p.u. is the peak value of the phase-to-earth voltage

Figure 101 – Voltage build-up by successive restrikes

Voltage breakdowns at capacitive current interruption are divided into two categories:

1) Re-ignitions: Voltage breakdown during the first 1/4 cycle following current interruption.
2) Restrikes: Voltage breakdown 1/4 of a cycle or more following current interruption.

The definitions of re-ignition and restrike are valid only when the recovery voltage has a 1-cosine frequency waveshape.

Restrikes will lead to overvoltages across the capacitive load (maximum 3 p.u. for a single restrike, where 1 p.u. is the peak value of the phase-to-earth voltage) while re-ignitions will not produce any overvoltages (theoretically maximum 1 p.u.). Re-ignitions are acceptable but may cause power quality problems.

In reality, there are no restrike-free circuit-breakers. It would take an infinite number of test shots to verify this. For this reason, the concept of restrike performance was introduced in IEC 62271-100.

Another phenomenon, which has been observed predominantly on vacuum circuit-breakers, may occur during three-phase capacitive current and short-circuit breaking current tests, but also at lower currents and voltages. This phenomenon is known as a *non-sustained disruptive discharge* (NSDD).

An NSDD is defined as a disruptive discharge associated with current interruption that does not result in the resumption of power frequency current or, in the case of capacitive current interruption does not result in current at the natural frequency of the circuit. An NSDD is considered as a late local breakdown across the interrupter and leads to a resumption of high-frequency current. The high-frequency oscillation is determined by stray capacitance and inductance locally across the interrupter. An example of an NSDD is given in Figure 102.

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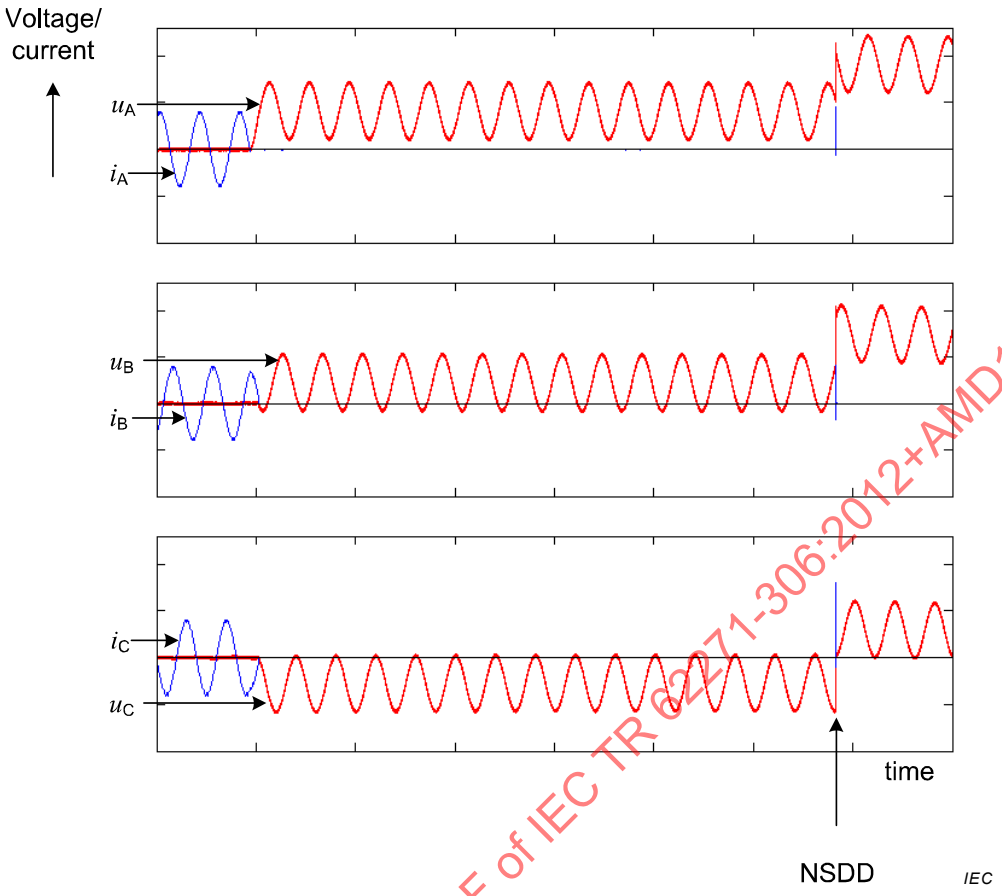

Key

i_A, i_B, i_C	Currents in phase A, B and C, respectively
u_A, u_B, u_C	Voltages across the contacts of phase A, B and C, respectively

Figure 102 – Example of an NSDD during capacitive current interruption

9.2.1.3.2 Recovery voltage in a three-phase circuit

The recovery voltages in three-phase circuits are more complicated than in the single-phase case. Figure 103 shows as an example the recovery voltage of the first-pole-to-clear in a case with a non-effectively earthed capacitive load. Due to the neutral shift, the recovery voltage initially has a shape that will lead to a peak value equal to three times the supply voltage peak (dotted line). The neutral shift is then 1,0 p.u. When the two last poles interrupt 90 electrical degrees after the first, there is however, a discontinuity in the slope (the neutral shift remains at 0,5 p.u.) and the final peak value for the first-pole-to-clear is 2,5 times the supply voltage peak (see also 9.6).

NOTE The recovery voltage peak of a circuit-breaker having a non-simultaneity between poles of more than ¼ cycle will be 3 times the supply voltage peak.

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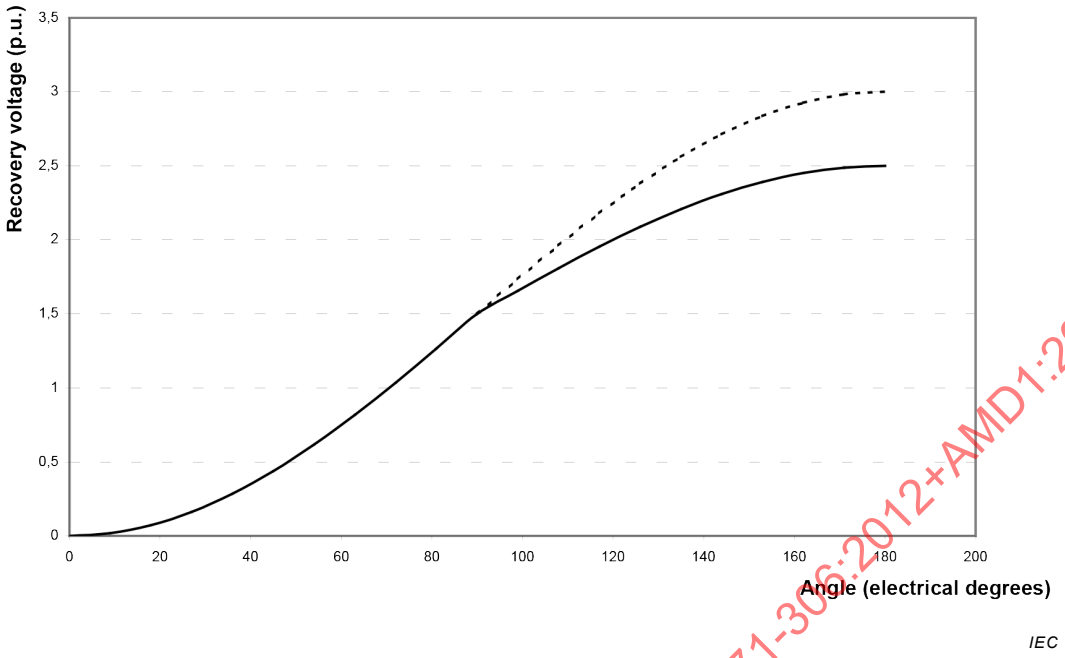

Figure 103 – Recovery voltage of the first-pole-to-clear at interruption of a three-phase non-effectively earthed capacitive load

9.2.2 Energisation of a capacitive load

With reference to Figure 98, L_s, R and C form a series RLC circuit. Applying a voltage u to such a circuit, the inrush current i can be calculated in general as follows:

$$u = Ri + L_s \frac{di}{dt} + \frac{q}{C}$$

Differentiating and treating u as a step voltage, i.e. energisation at the instant of the voltage peak:

$$\frac{d^2i}{dt^2} + \frac{R}{L_s}\frac{di}{dt} + \frac{1}{L_sC}i = 0 \qquad (148)$$

Equation (148) is a second order linear homogenous differential equation with three possible solutions depending on the degree of damping in the circuit. Taking $\alpha = R/2L_s$ and $\omega_0 = 1/\sqrt{L_sC}$, the three solutions are:

1) Overdamped $\alpha^2 > \omega_0^2$

$$i(t) = \frac{u}{L_s\sqrt{\alpha^2 - \omega_0^2}} e^{-\alpha t} \sinh\sqrt{\alpha^2 - \omega_0^2}\, t \qquad (149)$$

2) Critically damped $\alpha^2 = \omega_0^2$

$$i(t) = \frac{u}{L_s} te^{-\alpha t} \qquad (150)$$

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3) Underdamped $\omega_0^2 > \alpha^2$

$$i(t) = \frac{u}{L_s\sqrt{\omega_0^2 - \alpha^2}} e^{-\alpha t} \sin\sqrt{\omega_0^2 - \alpha^2}\, t \tag{151}$$

The resistance value R_{cd} that results in critical damping is given by:

$$R_{cd} = 2\sqrt{\frac{L_s}{C}} \tag{152}$$

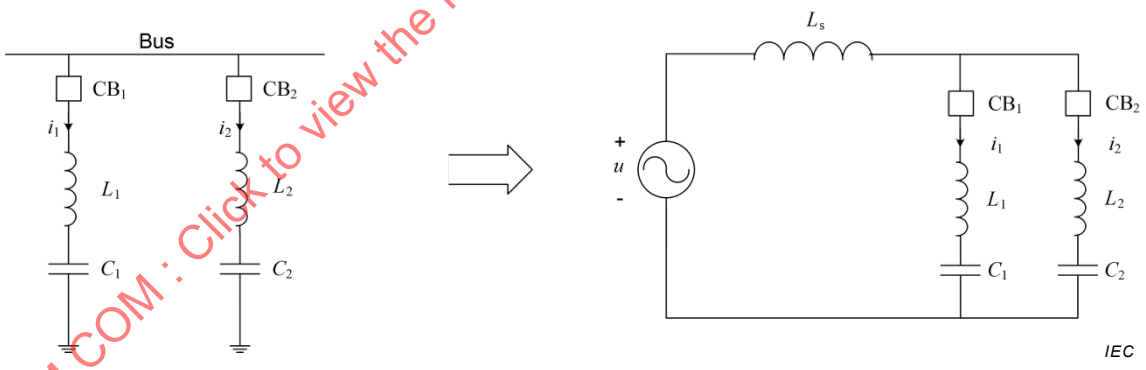
In most cases, the inrush current oscillation is underdamped and Equation (151) is of most interest. If closing resistors are applied to limit the inrush current, then Equation (149) or (150) may be applicable.

9.3 Capacitor bank switching

9.3.1 General

Since the use of capacitor banks for compensation purposes is increasing, it is common that more than one capacitor bank is connected to the same bus (back-to-back capacitor bank switching). This has no influence on the conditions at interruption. The current at closing, however, is affected to a high degree.

To describe the phenomena associated with capacitor bank switching, a general single-phase equivalent circuit is shown in Figure 104 showing a single-line diagram of the case where two capacitor banks (C_1 and C_2) are connected in back-to-back to a busbar. L_1 and L_2 represent the stray inductance (or stray inductance plus additional damping inductance). The inductance L_s of the source network will be several orders of magnitude higher than that of L_1 or L_2.



Key

CB_1	circuit breaker considered
CB_2	circuit breaker, open for single capacitor bank switching by CB_1, closed for back-to-back capacitor bank switching by CB_1
L_s	source inductance
L_1, L_2	inductance between capacitor bank 1 and 2 and bus, respectively
C_1, C_2	capacitor bank 1 and 2
i_1, i_2	capacitive currents
u	source voltage

Figure 104 – General circuit for capacitor bank switching

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Single capacitor bank switching occurs when C_1 is switched and C_2 is not connected in the circuit described in Figure 104. The circuit consists then of the source inductance L_s in series with the capacitor bank C_1. The inductance L_1 can be disregarded here, since the value of the source inductance L_s>>L_1.

Back-to-back capacitor bank switching occurs when switching C_1, with C_2 being in service, or vice versa.

The conditions for single and back-to-back capacitor bank switching are given in 9.3.3.1 and 9.3.3.2. In some cases, energised capacitor banks in nearby substations may contribute to the inrush current such that a back-to-back situation occurs.

Especially, the second case may give rise to an inrush current of very high amplitude and frequency, which may have to be limited in order not to be harmful to the circuit-breaker, the capacitor banks and/or the network. The magnitude and frequency of this inrush current is a function of the following:

a) applied voltage (point on the voltage wave at closing); the magnitude will be maximum on closing at the voltage peak;

b) capacitance of the circuit;

c) inductance in the circuit (amount and location);

d) any charge on the capacitor bank at the instant of closing;

e) any damping of the circuit due to closing resistors or other resistances in the circuit.

It is assumed that the capacitor bank is discharged prior to energisation. This is a reasonable assumption, as capacitor units are fitted with discharging resistors that will discharge the capacitor bank. Typical discharge times are in the order of 5 min.

The transient inrush current to a single bank is less than the available short-circuit current at the capacitor bank terminals. It rarely exceeds 20 times the rated current of the capacitor bank at a frequency that approaches 1 kHz. Since a circuit-breaker shall meet the making current requirements of the system, transient inrush current is not a limiting factor in single capacitor bank applications. For this reason making tests with inrush current are not required for single-capacitor bank switching.

When capacitor banks are switched back-to-back, transient currents of prospective high magnitude and with a high natural frequency may flow between the banks on closing of the circuit-breaker. The effects are similar to that of a restrike on opening. This oscillatory current is limited only by the impedance of the capacitor bank and the circuit between the energised bank or banks and the switched bank. This transient current usually decays to zero in a fraction of a cycle of the system frequency. In the case of back-to-back switching, the component supplied by the source is at a lower frequency and so small that it may be neglected.

9.3.2 De-energisation of capacitor banks

De-energisation of capacitor banks follows the theory outlined in 9.2.2.

9.3.3 Energisation of capacitor banks

9.3.3.1 Single capacitor bank

Energising a single capacitor bank is equal to energisation of capacitor bank C_1 when capacitor bank C_2 is not connected in the circuit described in Figure 104. The circuit consists then of the source inductance L_s in series with the capacitor bank C_1. L_1 can be disregarded here, since the inductance of the source is several orders of magnitude higher than that of L_1 (i.e. L_s >> L_1). In this case, the peak of the inrush current ($i_{i\ peak}$) and inrush current frequency (f_i) are limited by the source impedance L_s.

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A bank of shunt capacitors is considered single when the inrush current on energisation is limited by the inductance of the source and the capacitance of the bank being energised. A capacitor bank is also considered single if the maximum rate of change, with respect to time, of transient inrush current on energisation of an uncharged bank does not exceed the maximum rate of change of the rated short-circuit current at the voltage at which the current is applied. The limiting value is equal to

$$\left(\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}\right)_\mathrm{max} = \omega_\mathrm{s} I_\mathrm{sc}\sqrt{2} \tag{153}$$

where

$\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}$ is the rate of change of inrush current, A/s;

I_sc is the rated short-circuit current, in A r.m.s;

$\omega_\mathrm{s} = 2\pi f_\mathrm{s}$ is the angular frequency, in rad/s and f_s is the power frequency, in Hz.

Assuming that bank 1 is to be connected to the busbar and bank 2 is not connected, from Equation (151):

$$i_\mathrm{i} = \frac{\hat{u}}{L\sqrt{\omega_0^2 - \alpha^2}} e^{-\alpha t} \sin\left(\sqrt{\omega_0^2 - \alpha^2}\right)t \tag{154}$$

where $L = L_\mathrm{s} + L_1$ and $\omega_0 = 1/\sqrt{LC_1}$

If $\omega_0 >> \alpha$, then Equation (154) can be re-written in the simplified form:

$$i_\mathrm{i} = \frac{\hat{u}}{Z} e^{-\alpha t} \sin \omega_0 t \tag{155}$$

where $Z = \sqrt{\frac{L}{C_1}}$

The two quantities of interest for circuit-breaker application are the peak value of the inrush current $i_{\mathrm{i\,peak}}$ and its frequency f_i:

$$i_{\mathrm{i\,peak}} = \frac{\sqrt{2}u}{Z} \tag{156}$$

$$f_\mathrm{i} = \frac{1}{2\pi\sqrt{L_\mathrm{s}C_1}} \tag{157}$$

where $Z = \sqrt{\frac{L_\mathrm{s}}{C_1}}$ and $L_\mathrm{s} >> L_1$ is assumed.

9.3.3.2 Back-to-back capacitor bank switching

The inrush current of a single bank will be increased when other capacitor banks or parallel cables are connected to the same bus.

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If, in Figure 104, bank 1 is connected to the busbar and initially uncharged bank 2 is to be connected, the inrush current associated with the charging of bank 2 is supplied by bank 1 (back-to-back switching).

Equations (156) and (157) are applicable and adjusted as follows:

$$i_{\mathrm{i}} = \frac{\sqrt{2}u}{Z_{\mathrm{eq}}} \tag{158}$$

$$f_{\mathrm{i}} = \frac{1}{2\pi\sqrt{L_{\mathrm{eq}}C_{\mathrm{eq}}}} \tag{159}$$

where $Z_{\mathrm{eq}} = \sqrt{L_{\mathrm{eq}} / C_{\mathrm{eq}}}$, $L_{\mathrm{eq}} = L_1 + L_2$ and $C_{\mathrm{eq}} = \frac{C_1 C_2}{C_1 + C_2}$

Equations (158) and (159) can be applied in general to multiple bank switching cases. Assume that bank C with series inductance L is to be switched in with banks C_1 to C_{n} and associated series inductances L_1 to L_{n} already in service. The simplified calculation procedure is as follows:

a) Ignore the capacitances and calculate L_{eq}

$$L_{\mathrm{eq}} = L + L'$$

where $L' = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + \ldots\ldots \frac{1}{L_n}}$

b) Ignore the inductances and calculate C_{eq}

$$C_{\mathrm{eq}} = \frac{CC'}{C + C'}$$

where $C' = C_1 + C_2 + \ldots\ldots + C_n$

Typical amplitudes of the inrush currents for back-to-back energisation of capacitor banks are several kA with frequencies of 2 kHz to 5 kHz. Typical values are given in Table 9 of IEC 62271-100:2008. Capacitors can normally withstand amplitudes up to 100 times their rated current.

If the inrush current amplitude and frequency exceed those stated in Table 9 of IEC 62271-100:2008, it may be necessary to limit them. This can be done by insertion of additional series inductance in the circuit, or by using pre-insertion resistors (see 9.5.3). Another possibility is to use controlled switching.

9.4 No-load cable switching

9.4.1 General

To describe the phenomena associated with no-load cable switching, a general single-phase equivalent circuit is shown in Figure 105, showing the case where two cables (cable 1 and cable 2) are connected back-to-back to a system. The cables are represented by their capacitance C_1 and C_2 and their surge impedances Z_1 and Z_2, respectively.

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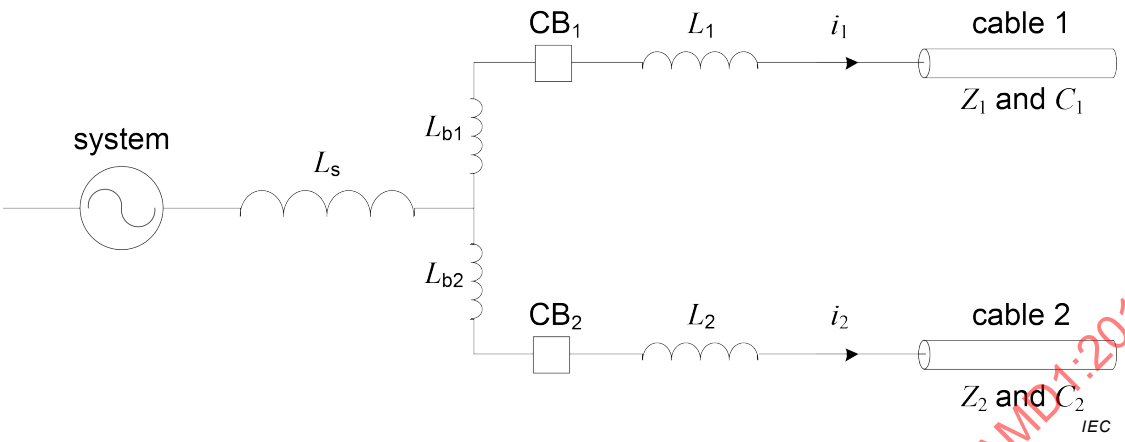

Key

CB_1	circuit-breaker
CB_2	circuit-breaker, open for single cable switching, closed for back-to-back switching
L_s	source inductance
L_1, L_2	inductance between cables 1 and 2 and the bus
Z_1, Z_2	surge impedance of cables 1 and 2 (Ω)
C_1, C_2	capacitance of cables 1 and 2 (F)
L_{b1}, L_{b2}	inductance of the bus connecting the cables

Figure 105 – Typical circuit for no-load cable switching

Single cable switching occurs when cable 1 is switched and cable 2 is not connected in the circuit described in Figure 10. The circuit then consists of the source inductance L_s in series with the bus inductance L_{b1} and the inductance L_1 between bus and cable.

Back-to-back cable switching occurs when cable 1 is switched, with cable 2 being in service.

Three phase cables can be individually screened (Figure 106) or belted (Figure 107). As the equivalent circuits show, individually screened cables represent a load similar to earthed capacitor banks and belted cables a load similar to unearthed capacitor banks.

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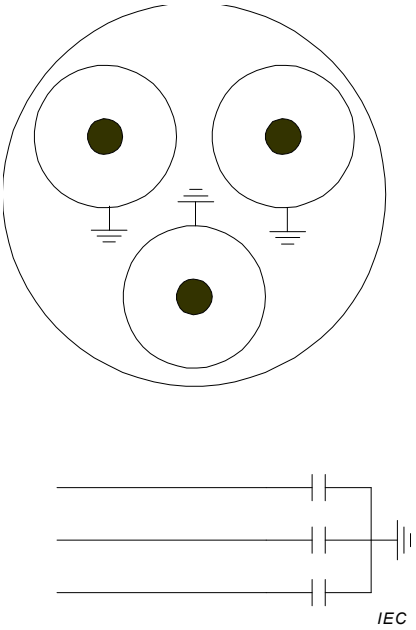

Figure 106 – Individually screened cable with equivalent circuit

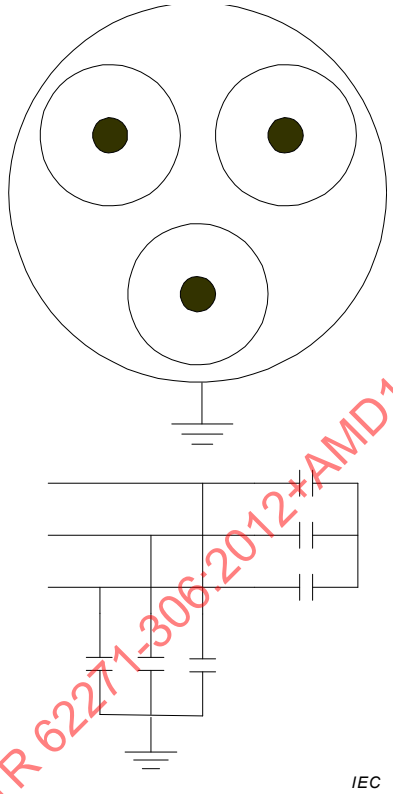

Figure 107 – Belted cable with equivalent circuit

9.4.2 De-energisation of no-load cables

9.4.2.1 General

A cable represents a distributed capacitive load. For de-energisation of a no-load cable, the principles discussed for capacitor bank switching are equally applicable with some variations as discussed later in Subclause 9.4.2. For example, in transient calculations, the cable surge impedance is applicable rather than its capacitance.

9.4.2.2 Cable charging current

The cable charging current is a function of the following characteristics:

a) system voltage;

b) cable geometry;

c) insulation dielectric constant;

d) cable length.

The shunt capacitive reactance can be obtained from the cable manufacturer, or if the physical constants of the cable are known, the shunt capacitive reactance can be calculated. Figure 108 shows the cross-section of a high-voltage cable.

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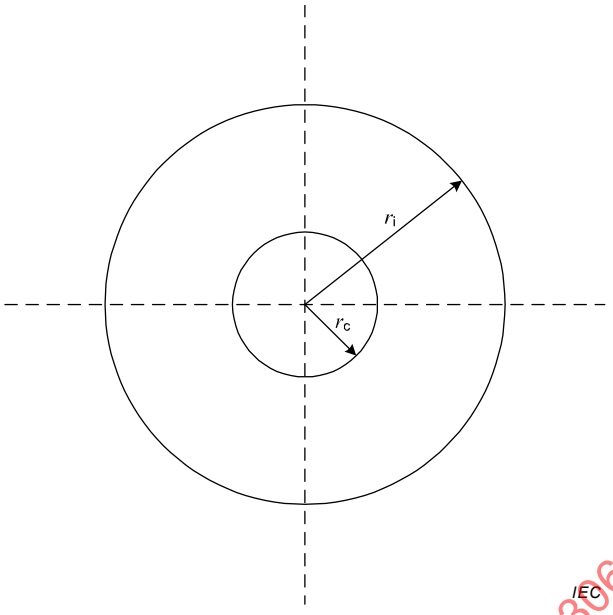

Key

r_c Conductor radius (m)

r_i Inside diameter of the shield

Figure 108 – Cross-section of a high-voltage cable

The shunt capacitance per unit length of a cable is expressed in Equation (160).

$$C = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln(\frac{r_i}{r_c})} \text{ F/m} \quad (160)$$

The series inductance per unit length of a cable is expressed in Equation (161).

$$L = \frac{\mu_0\mu_r}{2\pi}\ln(\frac{r_i}{r_c}) \text{ H/m} \quad (161)$$

For single-conductor and three-conductor shielded cables (for the different cable configurations see Figure 106 and Figure 107) the shunt capacitive reactance per km (X_c) can be written as shown in Equation (162).

$$X_c = \frac{1}{\omega_s C} = \frac{\ln(\frac{r_i}{r_c})}{l \times \omega_s \times 2\pi\varepsilon_0\varepsilon_r} (\text{M}\Omega) \quad (162)$$

Using the relationship $\ln(x) = 2{,}3\lg(x)$ and l = 1 000 m = 1 km, Equation (162) transforms to Equation (163).

$$X_c = \frac{6{,}58}{f_s\varepsilon_r}\lg\frac{r_i}{r_c} \text{ (M}\Omega \text{ per phase, see NOTE and Figure 108)} \quad (163)$$

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where

f_s is the system frequency (Hz);

ε_0 is the dielectric constant of vacuum, $\varepsilon_0 = 8{,}85\times10^{-12}$ (F/m);

ε_r is the relative dielectric constant of cable dielectric material;

r_i is the inside radius of shield (mm);

r_c is the conductor radius (mm);

l is the cable length (m);

μ_0 is the magnetic permeability of vacuum, $\mu_0 = 4\pi \times 10^{-7}$ (H/m);

μ_r is the relative magnetic permeability of the cable dielectric material ($\mu_r \approx 1$);

ω_s is the angular power frequency, $\omega_s = 2\pi f_s$ (rad/s);

f_s is the power frequency (Hz);

ln is the natural logarithm based on e, $^{e}\log x$;

lg is the logarithm based on 10, $^{10}\log x$.

NOTE When using the quantity MΩ per phase per km, the shunt capacitive reactance in MΩ for more than 1 km decreases because the capacitance increases. For more than 1 km of cable, therefore, the value of shunt capacitive reactance as given above is divided by the number of km of cable.

Using the capacitive reactance, the cable charging current can be calculated and compared with the rated cable charging current of the circuit-breaker given in IEC 62271-100. If the calculation exceeds the rating, the manufacturer should be consulted. Before an application can be made, the inrush current rating should also be checked (see 9.4.3).

The surge impedance (Z) of a single-conductor and three-conductor shielded cables can be expressed using Equation (164).

$$Z = \sqrt{\frac{L}{C}} = \sqrt{\frac{\frac{\mu_0\mu_r}{2\pi}\ln\left(\frac{r_i}{r_c}\right)}{\frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{r_i}{r_c}\right)}}} = \sqrt{\frac{4\pi\times10^{-7}}{4\pi^2 8.85\times10^{-12}\varepsilon_r}}\times\ln\left(\frac{r_i}{r_c}\right) = \frac{138}{\sqrt{\varepsilon_r}}\times\log\left(\frac{r_i}{r_c}\right) \quad (\Omega) \qquad (164)$$

Typical values of ε_r range from 2,3 (polyethylene) to 4 (fluid impregnated paper); a typical value for Z is 50 Ω.

9.4.2.3 Recovery voltage

The recovery voltage is similar to that of a capacitor bank (see 9.2.2.3).

9.4.3 Energisation of no-load cables

9.4.3.1 General

A circuit breaker may be required to energize a no-load cable during its normal operating duties. Prior to energisation the cable is usually at ground potential, but can have a trapped charge from a previous switching operation. A cable may be switched from a bus that does not have other cables energized (single cable) or against a bus that has one or more cables energized (i.e. back-to-back cable).

The energisation of a cable by the closing of a circuit breaker will result in a transient inrush current. The magnitude and rate of change of this inrush current is a function of the following:

– applied voltage (including the point on the voltage wave at closing);

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– cable surge impedance;
– cable capacitive reactance;
– inductance in the circuit (amount and location);
– any charges on the cable at the instant of closing;
– any damping of the circuit because of closing resistors or other resistance in the circuit.

The transient inrush current to a single cable is less than the available short-circuit current at the circuit breaker terminals. Because a circuit breaker shall meet the making current requirements of the system, transient inrush current is not a limiting factor in single cable applications.

When cables are switched back-to-back (that is, when one cable is switched while other cables are connected to the same bus), transient currents of high magnitude and initial high rate of change may flow between cables when the switching circuit-breaker is closed or restrikes on opening. This surge current is limited by the cable surge impedances and any inductance connected between the energised cable(s) and the switched cable. This transient current usually decays to zero in a fraction of a cycle of the system frequency. During back-to-back cable switching, the component of current supplied by the source is at a lower rate of change and so small that it may be neglected. Due to the very high damping of the inrush current, the switching of parallel cables usually does not represent a problem for modern circuit-breakers. Therefore no problems are expected for back-to-back cable configurations. The case of back-to-back cable switching is not addressed in IEC 62271-100.

Cables are considered being switched back-to-back if the maximum rate of change of transient inrush current on energizing an uncharged cable exceeds that specified for a single cable.

9.4.3.2 Single cable energisation

A cable is defined as single if the maximum rate of change, with respect to time, of transient inrush current on energizing an uncharged cable does not exceed the rate of change of current associated with the rated short-circuit current. This limiting value is numerically equal to

$$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max} = \omega_{\mathrm{s}}\sqrt{2}\,I_{\mathrm{sc}} = 2\pi f_{\mathrm{s}}\sqrt{2}\,I_{\mathrm{sc}} \qquad (165)$$

where

$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max}$ is the maximum rate of change of inrush current in A/s;

I_{sc} is the rated r.m.s. short-circuit current, in A;

$\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$ is the angular frequency in rad/s, where f_{s} is the power frequency in Hz.

By this definition, it is possible to have cable circuits that are physically back-to-back, but are considered single for application purposes provided a large inductance is located between the two cable circuits. The inductance should be large enough so that by itself it would limit fault current to a value less than or equal to the circuit-breaker rating.

In switching a single cable, if the source inductance is greater than 10 times the cable inductance, the cable can be represented as a capacitor. Otherwise, under transient conditions the cable can be represented by its surge impedance.

To calculate the inrush current for a single cable, Figure 105 may be used, with circuit-breaker CB_2 open.

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$$i_i(t) = \frac{U_m - U_t}{Z_1}\left[1 - \exp(-\frac{Z_1}{L}t)\right] \quad (166)$$

where

$$i_{i\,peak} = \frac{U_m - U_t}{Z_1}$$

U_m is the crest of applied voltage;
U_t is the trapped voltage on the cable being switched;
f_s is the source frequency (power frequency);
i_i is the inrush current;
$i_{i\,peak}$ is the peak of the inrush current;
Z_1 is the cable surge impedance;
L is the source inductance.

The initial rate-of-rise (di/dt at t = 0) of the inrush current is $\frac{U_m - U_t}{L}$. For application purposes, $i_{i\,peak}$ should be compared to the value given in Table 9 of IEC 62271-100:2008.

The cable inrush current is not oscillatory in the usual frequency-related sense, but the initial slope can be used to determine an equivalent frequency that can be compared with the inrush frequency. In general,

$$\left(\frac{di_i}{dt}\right) = 2\pi f_i I_i \quad (167)$$

where

$\left(\frac{di_i}{dt}\right)$ is the rate-of-change of inrush current in A/s;
f_i is the inrush current frequency;
I_i is the peak inrush current.

The equivalent frequency f_{eq} for a cable inrush current is then obtained as follows:

$2\pi f_{eq} I_i = \frac{U_m - U_t}{L}$ that gives $f_{eq} = \frac{U_m - U_t}{2\pi L I_i}$ and for proper circuit-breaker application, f_{eq} should be less than the preferred inrush current frequency.

9.4.3.3 Back-to-back cable energisation

Back-to-back cable switching occurs when cable 2 is in service and cable 1 is being energized in Figure 105. The values of the inductances of L_1, L_2, and L_{b1} and L_{b2} between the cables are often very small with respect to the inductance of L_s. In many cases they will be less than 1 % of the source inductance. They consist of the inductances from the cables to the circuit-breakers, the circuit-breaker inductances, and the bus inductance of the current path. Values of inductance depend upon the physical configuration and are hence site specific and unable to be standardized. However, a representative range is 0,66 µH to 1,0 µH per phase per m.

Neglecting the source contribution, the back-to-back cable switching case can be represented as shown in Figure 109.

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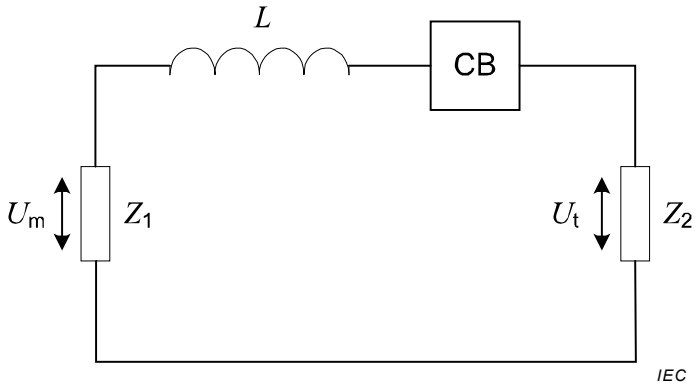

Key

U_m	Crest of applied voltage
U_t	Trapped voltage on cable being switched
Z_1, Z_2	Cable surge impedance
L	Total inductance between cable terminals
CB	Circuit-breaker

Figure 109 – Equivalent circuit for back-to-back cable switching

The initial pulse of current has a front expressed as

$$i(t) = \frac{U_m - U_t}{Z_1 + Z_2}\left[1 - \exp\left(-\frac{Z_1 + Z_2}{L}t\right)\right] \quad (168)$$

Assuming that the $L/(Z_1 + Z_2)$ time constant is less than 1/5 of the travel time of the cable out and back, the initial crest of the inrush current is then $(U_m - U_t)/(Z_1 + Z_2)$, which for application should be less than the rated peak inrush current.

The peak inrush current when energizing a cable with another already connected to the bus is given by

$$i_{\text{i peak}} = \frac{U_m - U_t}{Z_1 + Z_2} \quad (169)$$

and

$$f_{eq} = \frac{U_m - U_t}{\omega(L_1 + L_2)I_{ir}} \quad (170)$$

The inrush current when energizing a cable with an equal cable already connected to the bus is given by

$$i_{\text{i peak}} = \frac{U_m - U_t}{2Z} \text{ (A)} \quad (171)$$

and

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$$f_{eq} = \frac{U_m - U_t}{\omega(L_1 + L_2)I_{ir}} \text{ (Hz)} \quad (172)$$

Differentiating the expression for the current at t = 0 will give the maximum initial rate of change of the inrush current, in Equation (173).

$$\left(\frac{di}{dt}\right)_0 = \frac{U_m - U_t}{L} \text{ (A/s)} \quad (173)$$

This can reach extreme values since the magnitude of L can be arbitrarily small.

Additional inductance may be added in series with the inductances making up L to meet the preferred inrush frequency.

9.4.4 Compensated cable energisation

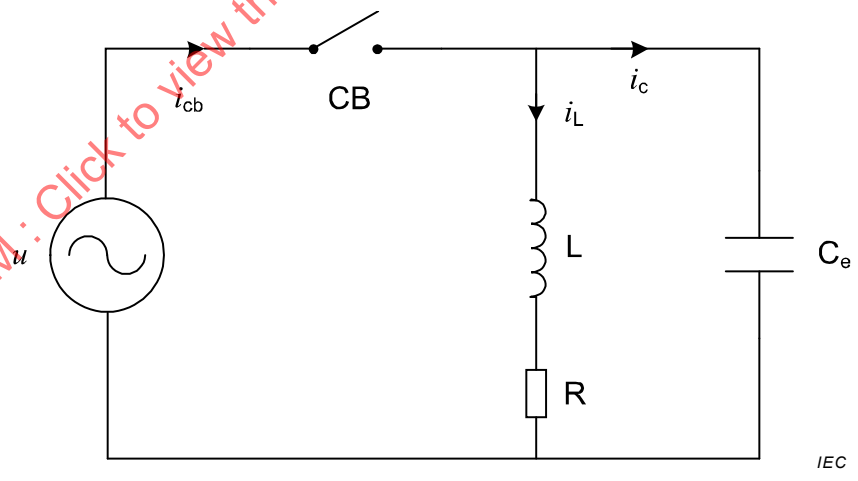
9.4.4.1 General

A circuit-breaker may be required to energise a no-load cable during its normal operating duties. Prior to energisation, the cable is usually at earth potential, but can have a trapped charge from a previous switching operation.

Besides these widely known effects, other phenomena may occur during cable energisation at rated voltages of 420 kV and above.

When operating the cable nearly fully compensated the phenomenon of delayed current zero crossings may occur. This phenomenon is similar to the one described at faults close to generators (see Annex B).

The simplified single-phase equivalent circuit is shown in Figure 110.



Key

u	Phase-to-earth voltage	R	Resistance to earth of compensating reactor
CB	Circuit-breaker	i_{cb}	Current through the circuit-breaker
C_e	Cable capacitance to earth	i_L	Current through the compensating reactor
L	Inductance to earth of compensating reactor	i_c	Current through the cable

Figure 110 – Equivalent circuit of a compensated cable

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When energizing the compensated cable by closing the circuit-breaker, the current starts flowing in the cable (i_C, momentary value of the current is not continuous and may change suddenly) and in the reactor (i_L, momentary value of the current is continuous due to the fact that di/dt at a inductance is zero at the instant of closing the circuit-breaker). The sum of both currents flows through the circuit-breaker (i_{cb}).

Due to the fact that the instantaneous current value in the reactor before energizing and the current value directly after energizing shall be identical ($di/dt = 0$), a DC equalizing current flows depending on the making angle and the instantaneous value of the making voltage, respectively. The change of the current through the inductance when closing the circuit-breaker causes a magnetic field. Due to the continuity requirement, this magnetic field is compensated. The equalizing magnetic field causes the DC equalizing current.

If the circuit-breaker is closed at voltage maximum, the equalizing current is zero and when closing at voltage zero, the equalizing current is at its maximum due to the 90° phase shift between voltage and current for an inductance.

This DC equalizing is superimposed on the inductive AC current of the reactor to the total reactor current i_L. Due to the resistance of the reactor, the DC current decays over time.

The following two different cases are distinguished: fully compensated cables and partly compensated cables.

9.4.4.2 Fully compensated cables

When operating a fully compensated cable, the inductive AC current and the capacitive AC current will be of the same amount. Hereby the capacitive current i_c has the opposite sign of the inductive current i_L.

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 111 for making at voltage maximum and full compensation.

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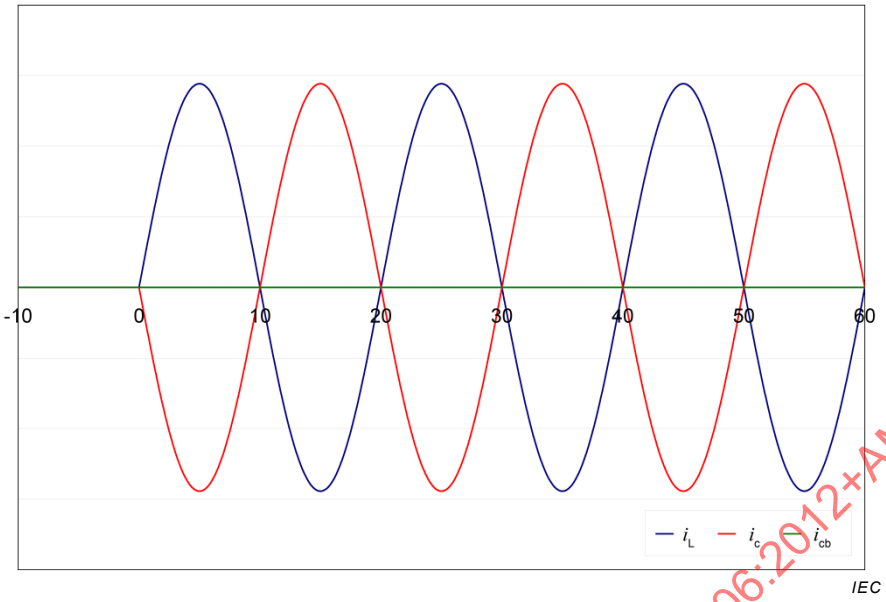

Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Dotted green line	Total current through the circuit-breaker i_{cb}

Figure 111 – Currents when making at voltage maximum and full compensation

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 112 for making at voltage zero and full compensation. The transient effects of the suddenly changing capacitive current when closing the circuit-breaker are not considered.

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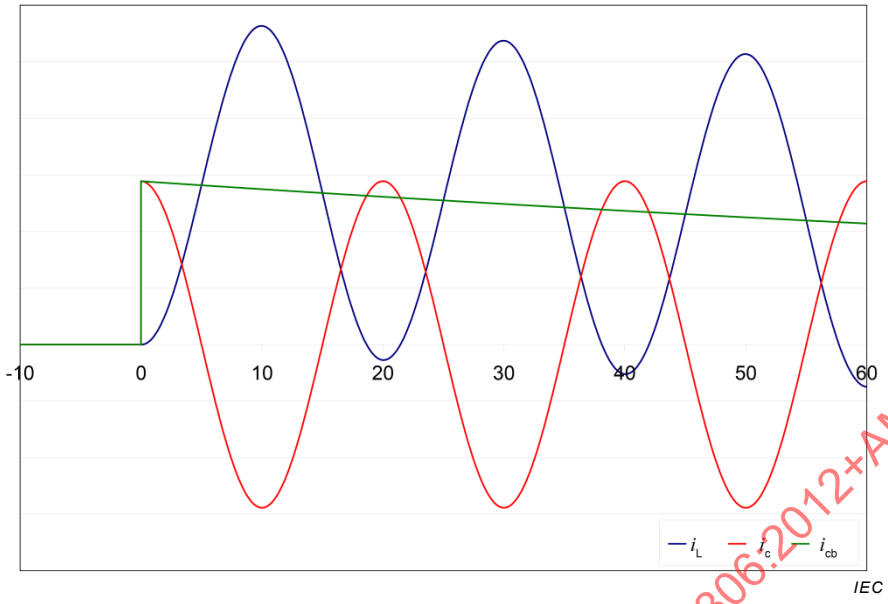

Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 112 – Currents when making at voltage zero and full compensation

It can be seen that the inductive current i_L and the capacitive current i_c in both cases always show zero crossings.

In the case of making at voltage maximum, the current through the circuit-breaker for a fully compensated cable is zero due to the fact that the inductive current i_L and the capacitive current i_c have the same magnitude and opposite polarity.

In the case of making at voltage zero, the current through the circuit-breaker does not show zero crossings for several periods. If within this time period the circuit-breaker is tripped, it may have severe difficulties to interrupt the current. This will be described in detail further in this subclause.

9.4.4.3 Partly compensated cables

If the cable is partly compensated (undercompensated), the inductive AC current is smaller than the capacitive AC current. The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 113 for making at voltage maximum and partial compensation (e.g. 80 %).

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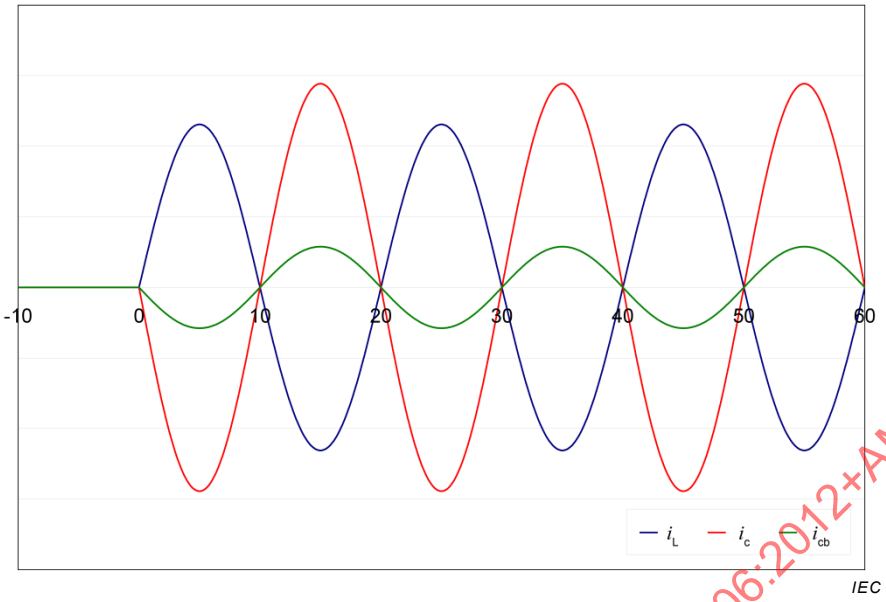
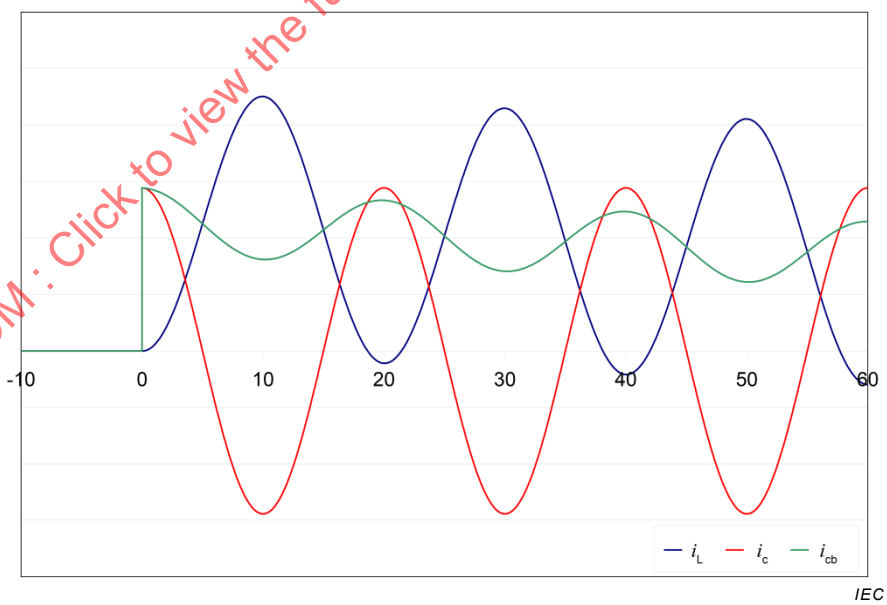


Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 113 – Currents when making at voltage maximum and partial compensation

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 114 for making at voltage zero and partial compensation (e.g. 80 %). The transient effects of the suddenly changing capacitive current when closing the circuit-breaker are not considered.



Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 114 – Currents when making at voltage zero and partial compensation

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Also, in the case of undercompensated operated cables, it can be seen that the inductive current i_L and the capacitive current i_c in all cases always show zero crossings.

In the case of making at voltage zero, the current through the circuit-breaker also does not show zero crossings for several periods even if the amplitude of the DC equalizing current is smaller due to the lower inductive current at partial compensation.

9.4.4.4 Summary

The amplitude of the DC equalizing current depends on the degree of compensation and the instant of making. The duration of the time period of missing current zero crossings depends on the X/R ratio, the damping of the compensation reactor and the degree of compensation.

In the past, the resistance of the compensation reactors was comparably high. Therefore the X/R ratio (related to the DC time constant τ) was low and the DC equalizing current was damped fast enough to create current zeros. Nowadays, the resistance of the compensation reactors is reduced further in order to minimize the ohmic losses.

The phenomenon of delayed current zero crossings may become problematic if the circuit-breaker is tripped during the time period of missing zero crossings. To solve this problem two basic approaches are possible:

a) prevention of the occurrence of currents with delayed zero crossings;

b) choice of a circuit-breaker suitable for the application.

To prevent currents with delayed zero crossings, the making should always occur around the voltage maximum in each phase. This can be done using controlled closing (point-on-wave closing). Controlled closing ensures that the making occurs in all phases at or near voltage maximum. The disadvantage of this method is the occurrence of switching overvoltages.

If the making at voltage zero cannot be prevented, the decay of the DC equalizing currents can be increased by using circuit-breaker types equipped with pre-insertion resistors. Owing to the additional resistance, the X/R ratio is decreased and hence the first zero crossing of the current i_{cb} occurs significantly earlier. The resistance value of the pre-insertion resistor should be dimensioned in a way that the first zero crossing occurs about 10 ms after making. In this case, a successful opening operation can also be ensured for the worst-case (e.g. opening command is already given during closing of the circuit-breaker). For each application an individual calculation should be performed due to the different parameters of reactor and network parameters as well as a different degree of compensation.

If no suitable resistance value can be determined or controlled switching is not possible, the current shows delayed zero crossings. Hence a suitable circuit-breaker type should be chosen to ensure a successful current interruption at all cases. The arc in the circuit-breaker during the breaking operation represents a non-linear resistance, which also leads to a decreased X/R ratio, and therefore to an earlier occurrence of zero crossings. With special tests, the parameters for an arc model can be determined for each circuit-breaker type. Using this arc model, the influence on the current i_{cb} can be determined. Depending on the amplitude and time constant of the DC equalizing current circuit-breaker types with high arc voltages may be necessary. Also with this method, for each application an individual calculation should be performed due to the different parameters of reactor and network parameters, different parameters of the circuit-breaker arc as well as a different degree of compensation.

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9.5 No-load transmission line switching

9.5.1 De-energisation of uncompensated transmission lines

9.5.1.1 Line charging current

A no-load overhead line can generally be represented by a capacitance. In the case of short lines (< 200 km), this capacitance can be considered concentrated, but in the case of long lines, it should be considered distributed. Typical capacitance values vary from 9 nF/km per phase for single conductor overhead lines to 14 nF/km per phase for four-conductor bundle overhead lines (see also [127]).

Owing to the distributed nature of the inductance and the capacitance of the line, the peak value of the power frequency voltage at the remote (or receiving) end is higher than that at the circuit breaker (sending) end of the line. This effect is called the *Ferranti effect*. For a line length of 500 km, the voltage increase is approximately 4 % and approximately 1 % for a line of 200 km. That is why the Ferranti effect is not considered for line lengths below 200 km.

Figure 115 gives an approximation of the line charging current per km of different line configurations at 60 Hz. If the estimated current is greater than 90 % of the preferred line current rating, a more accurate calculation based on the actual line configuration and methods similar to that discussed in Gabrielle, et al. [127] should be used.

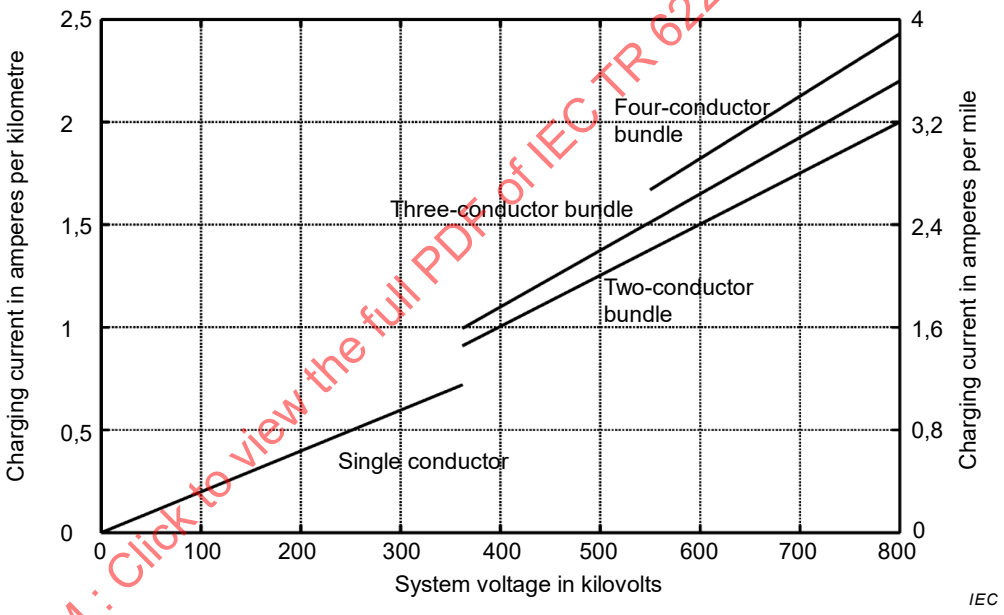

Figure 115 – RMS charging current versus system voltage for different line configurations at 60 Hz

From Figure 115, the capacitive reactance can be derived as follows.

Assume a system with a rated voltage of 245 kV, 60 Hz. The charging current is 0,5 A/km. The linear capacitive reactance X_C' is then:

$$X_c' = \frac{1}{\omega C'} = \frac{U}{I'} = \frac{245\,000\ \text{V}}{\sqrt{3} \times 0{,}5\ \text{A/km}} = 0{,}283\ \text{M}\Omega\ \text{km}\ ,$$

where

X_c' is the linear capacitive reactance of the line (MΩ km);

C' is the capacitance of the line (F/km);

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I' is the charging current of the line (A/km);

U is the system voltage (kV).

For a 50 Hz system frequency, the corresponding value of X_c' would be

$$0{,}283 \times \frac{60}{50} = 0{,}34\,\text{M}\Omega\,\text{km}$$

To calculate the reactance X_c of a line with a given length l, the linear reactance X_c' has to be divided by the length:

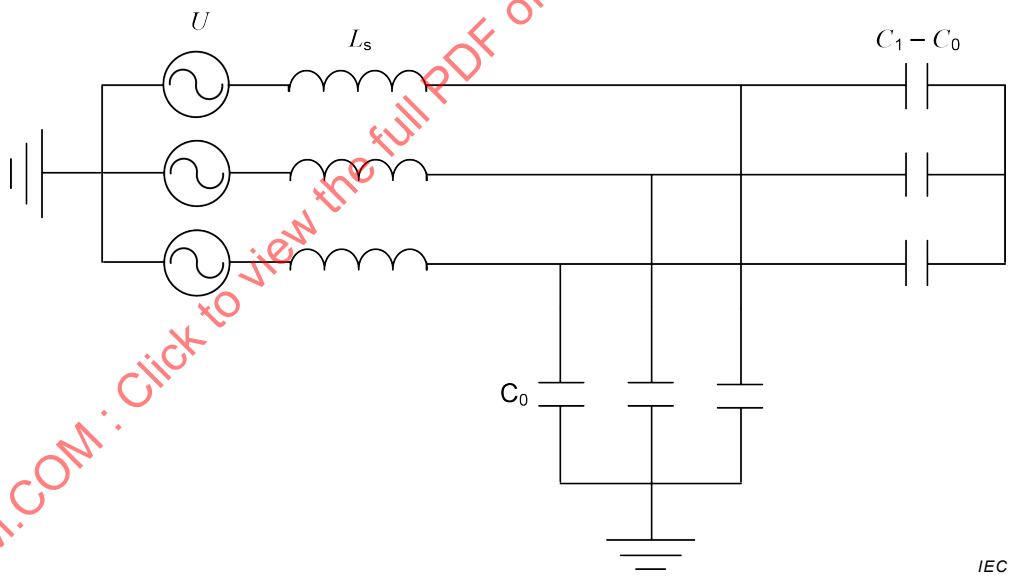
$$X_c = \frac{X_c'}{l}$$

Assume a length of 100 km for the example above. The reactance X_c is then:

$$X_c = \frac{X_c'}{l} = \frac{0{,}283\,\text{M}\Omega\text{km}}{100\,\text{km}} = 2{,}83\,\text{k}\Omega\,.$$

9.5.1.2 Recovery voltage

Transmission lines have capacitance both between phases and to ground. Figure 116 shows a general circuit that can be used to analyse the phenomena associated with no-load transmission line switching.



Key

U	Source voltage
L_s	Source inductance
C_0	Zero sequence capacitance
C_1	Positive sequence capacitance

Figure 116 – General circuit for no-load transmission line switching

Overhead lines in transmission systems typically have C_1/C_0 ratios in the order of 2,0. Figure 117 shows the peak value of the recovery voltage in the first-pole-to-clear as a function of the capacitance ratio C_1/C_0 (positive to zero sequence capacitance). The recovery

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voltage peak is the differential voltage of the source and line sides, including the effects of coupled voltage on the first cleared pole. In this case Figure 117 shows that the recovery voltage peak is approximately 2,4 p.u. It follows that the voltage factor for single-phase testing to cover three-phase interruption is equal to 1,2. It has been assumed that the amplitude approaches 3 p.u. This is the case without capacitance to earth and delayed interruption of the second phase. An example of the voltages in such a case is given in Figure 103. The other extreme, C_1 = C_0, is the case where each phase has capacitance to earth only. The recovery voltage peak is then 2 p.u. as in a single-phase case.

Overhead lines in transmission systems typically have capacitance both between phases and to earth. Figure 103 and Figure 117 assume that the second and third poles interrupt 90° after the first.

When the characteristics of the voltage in service (shape and peak value) are deviating from those of the test voltage, the restrike probability may increase. For example, if the line is compensated, the line side component is not a trapped voltage resulting from the trapped charge, but a voltage oscillating with a frequency determined by the compensating reactors and the line side capacitance (see 9.5.2).

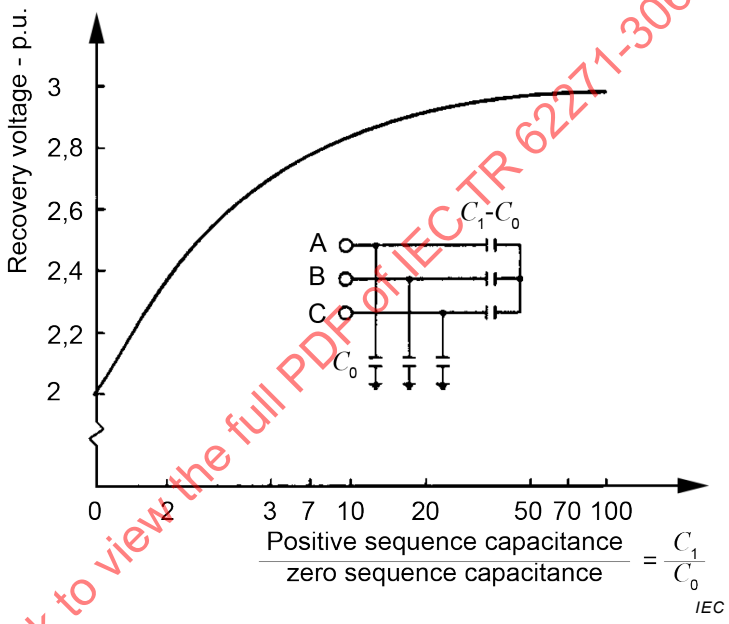

Figure 117 – Recovery voltage peak in the first-pole-to-clear as a function of C_1/C_0, delayed interruption of the second phase

If the C_1/C_0 ratio is greater than 2, higher voltages may be coupled to the first pole-to-clear, resulting in increased probability of restrike. In this case, the manufacturer should also be consulted since circuit-breaker designs are sensitive to both current magnitude and recovery voltage waveshapes.

9.5.2 De-energisation of compensated transmission lines

9.5.2.1 General

Long overhead lines are often compensated with shunt reactors to reduce the charging current of the line. The compensation factor (k_L) of an overhead line is given by the ratio of the capacitive reactance ($X_{C,line}$) to the inductive reactance ($X_{L,reactor}$) of the compensating reactor, in Equation (174):

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$$k_L = \frac{X_{C,line}}{X_{L,reactor}} \quad (174)$$

If $X_{L,reactor} > X_{C,line}$, the line is undercompensated, a line with $X_{L,reactor} < X_{C,\ line}$ is called overcompensated.

9.5.2.2 Line charging current

The compensated line charging current is given by $I_{Lc} = I_c'(1 - k_L)$

where

I_{Lc} is the line charging current of the compensated line;

I_c' is the line charging current of uncompensated line;

k_L is the compensation factor.

Assuming a line compensated at 60 % (i.e. k_L = 0,60), the line charging current is $I_{lc} = I_c' \times (1 - 0{,}6) = 0{,}4 I_c'$, or 40 % of the uncompensated value.

9.5.2.3 Recovery voltage

If the line is compensated, the line side component of the recovery voltage is no longer a DC voltage, but an oscillation of which the frequency is determined by the compensating reactor and the line capacitance.

The resonant frequency is approximated by:

$$f_L \approx \frac{1}{2\pi\sqrt{LC}} = f_s \sqrt{\frac{X_{C,line}}{X_{L,reactor}}} = f_s \sqrt{k_L} \quad (175)$$

where

f_L is the resonance frequency of the compensated line (Hz);

L is the inductance of the reactor (H);

C is the total capacitance of the line (F);

f_s is the system frequency (Hz);

k_L is the compensation factor.

In other words: the resonance frequency of a compensated line is dependent on the degree of compensation. Since the compensation usually is less than 1, this resonance frequency is less than the system frequency, resulting in a reduction of the rate-of-rise of the recovery voltage. Typical current and voltage waveshapes are given in Figure 118.

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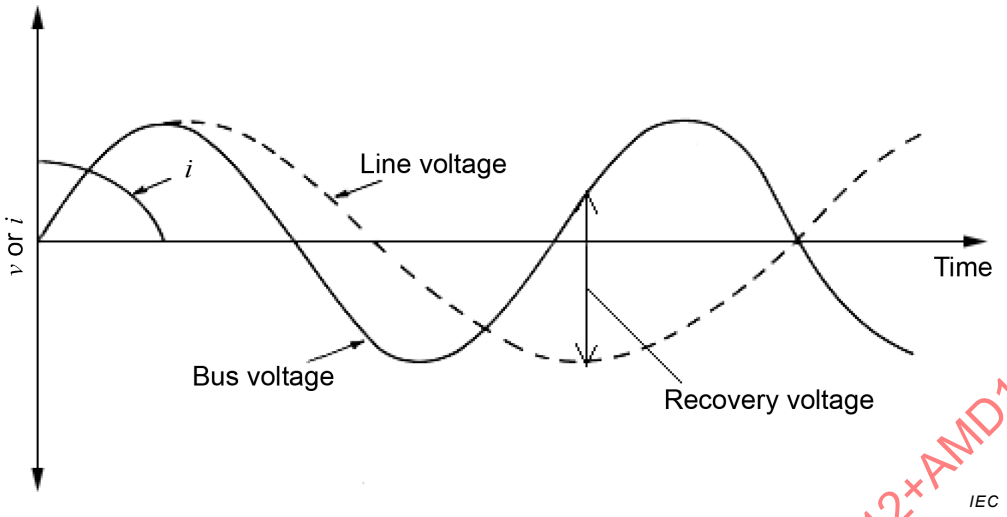

Figure 118 – Typical current and voltage relations for a compensated line

The first half-cycle of recovery voltage is, for this example, as shown in Figure 119. Compensation thus results in a decrease of the probability of restrike at a particular current. Under these conditions, improved performance may result, the circuit-breaker having a lower probability of restrike. The manufacturer should be consulted on applications which markedly alter the recovery voltage.

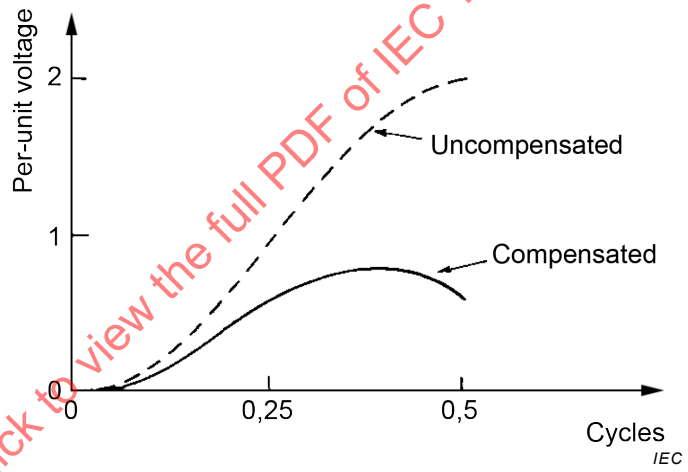

Figure 119 – Half cycle of recovery voltage

9.5.3 Energisation and re-energising transmission lines

9.5.3.1 General

For this case inrush currents are of no significance due to the high surge impedance of the lines. However, overvoltages are an issue due to travelling waves on the lines. Typically, the line is uncharged when being switched but voltage doubling is possible due to reflections from the open end of the line. A worst case can occur during high-speed reclosing when a restrike occurs at a source voltage peak of opposite polarity to the trapped charge on the line.

At voltages of 300 kV and above, mitigation measures are applied to limit the above switching overvoltages. The measures include opening resistors, metal oxide surge arresters and controlled switching.

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When a transmission line is switched onto an energised network, a voltage wave is imposed on the line. The resulting phenomena are similar to those of energizing a cable. The imposed wave will be reflected at the far end of the line and when the line is open at the far end (or terminated by a high-impedance load for high frequencies), the reflected wave results in doubling of the amplitude as shown in Figure 120.

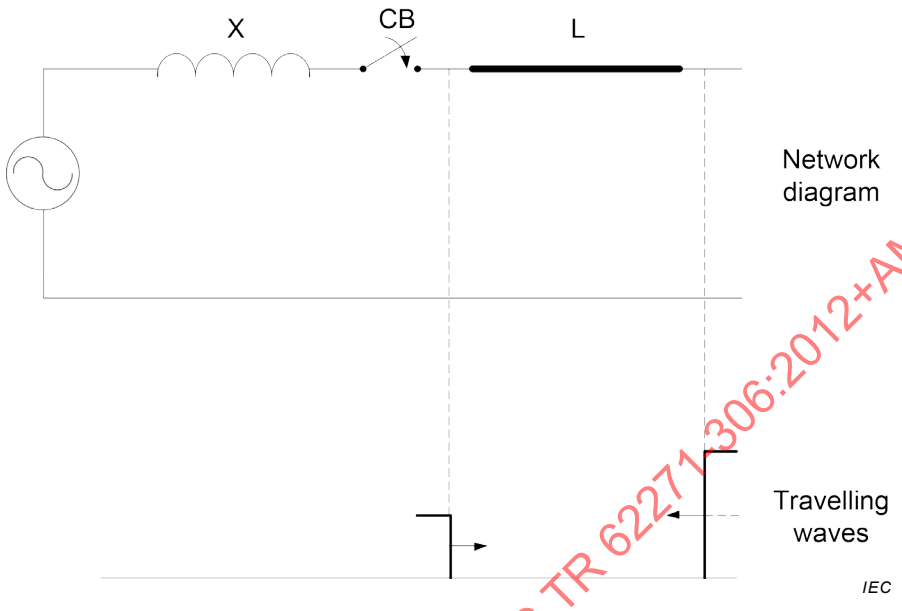

Figure 120 – Energisation of no-load lines: basic phenomena

An even higher voltage is obtained when the line has a trapped charge before being energized and the circuit-breaker happens to close at an instant when the polarity of the network voltage is opposite to that of the voltage that was present on the line. The voltage on the line can, after reflection of the wave, theoretically be up to three times the network voltage. This situation can occur in conjunction with auto-reclosing of a line.

Even higher voltages can develop on a three-phase line, when the three circuit-breaker poles are not closing simultaneously. A wave on one phase will then generate induced waves on the other phases and under unfavourable circumstances this can lead to a further rise in voltage on another phase.

9.5.3.2 Reclosing on a compensated transmission line

Similar phenomena as described under 9.4.4.2 also apply to fully compensated lines. Especially during reclosing of the healthy phases after the interruption of a single-phase short-circuit, the circuit-breaker may close at or near source voltage zero. This will result in delayed current zero crossings. Not all circuit-breakers may be suited for this application. For further information, refer to Annex B.

9.5.3.3 Long transmission line switching considerations

Overhead lines exceeding 200 km, even those of simple construction type, present a special case not covered by the requirements of 6.111.7 of IEC 62271-100:2008 or its notes. Where such long lines are to be switched, consideration should be given to the higher value of peak recovery voltage present on interruption. Some idea of the ability of a particular circuit-breaker for making and breaking of this requirement can be gained by considering any out-of-phase switching evidence that may exist. Such evidence will usually provide adequate demonstration of the elevated recovery voltage. For full compliance, evidence will be required to satisfy the capacitive current switching requirements of 6.111 of IEC 62271-100:2008, but to the elevated values required by the specific application.

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Some users may be concerned about rare or occasional switching operations from one end on a series of long lines. This can occur during the early development stages of a system when intermediate substations may not be fully equipped or may even be by-passed. In such cases, it may be appropriate to consider the out-of-phase capability in relation to the combined load presented by the series of lines. If satisfactory for the current and voltage conditions, then specific testing for the severe capacitive current switching duty of IEC 62271-100 would not be necessary at the enhanced levels of the extended line. They would be required for the switching duty of the individual lines of the series, as normal.

9.6 Voltage factors for capacitive current switching tests

Depending on the capacity of a high-power laboratory, capacitive current switching tests may be performed as three-phase tests or single-phase tests. For the higher voltages (362 kV, 420 kV, 550 kV and 800 kV), unit tests are generally carried out.

Especially when single-phase tests are made to cover three-phase application, the test voltage should reflect the application of the circuit-breaker in the field. One of the factors influencing this is the earthing situation of the network. The other is the presence of single or two-phase faults (see 9.8 of this document and Annex S of IEC 62271-100:2008/AMD2:2017.

Subclause 6.111.7 of IEC 62271-100:2008 gives the following voltage factors for single-phase test voltage (see Table 43). In accordance with IEC 62271-100, the test voltage measured at the circuit-breaker location prior to interruption shall not be less than the rated voltage $U_r/\sqrt{3}$ and the voltage factors given in Table 43.

Table 43 – Voltage factors for single-phase capacitive current switching tests

Voltage factor k_c	Application
1,0	Tests corresponding to normal service in solidly earthed neutral systems without significant mutual influence of adjacent phases of the capacitive circuit, typically capacitor banks with solidly earthed neutral and screened cables.
1,2	Test on belted cables and line-charging current switching [a] corresponding to normal service conditions in solidly earthed neutral systems with mutual influence of adjacent phases of the capacitive circuit for rated voltages 52 kV and above.
1,4	1. breaking during normal service conditions in systems having a non-effectively earthed neutral including screened cables [b]; 2. breaking of capacitor banks having a non-effectively earthed neutral; 3. test on belted cables and line-charging current switching [b] corresponding to normal service conditions in effectively earthed systems for rated voltages less than 52 kV;
NOTE 1 The voltage factors for line-charging current switching tests of 1,2 and 1,4 are applicable to single-circuit line construction. Requirements for multiple overhead line constructions may be greater than these factors. NOTE 2 The 1,4 factor is a compromise and is valid for breaking of capacitive currents in non-effectively earthed systems, where the second and third-pole-to-clear interrupt 90° after the first. NOTE 3 When the non-simultaneity of contact separation in the different poles of the circuit-breaker exceeds 1/6th of a cycle of rated frequency, IEC 62271-100 recommends to raise the voltage factor or to make only three-phase tests. Such circuit-breakers fall outside the scope of the standard. [a] Under the condition that the line can be replaced partly or fully by a concentrated capacitor bank. [b] When a significant capacitance to earth on the source side is present, the factor will be reduced.	

The voltage factor 1,4 is explained as follows (see Figure 121):

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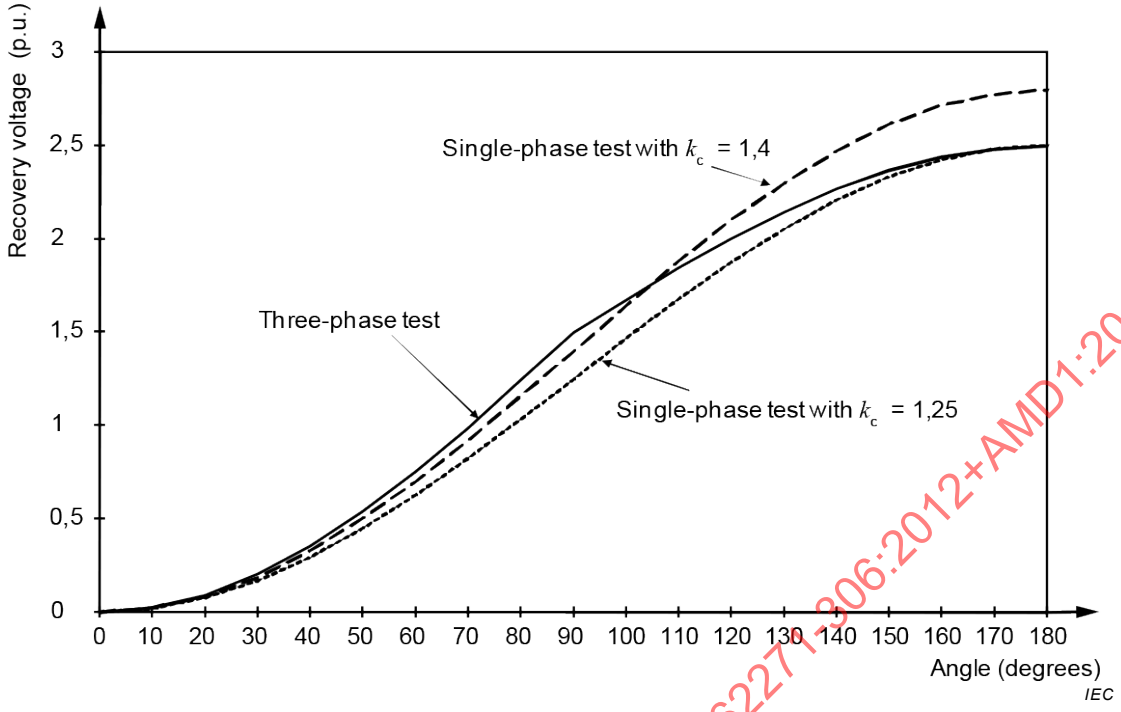

Figure 121 – Recovery voltage on first-pole-to-clear for three-phase interruption: capacitor bank with isolated neutral

When the current in the first pole is interrupted, the voltage across the circuit-breaker will rise as if the voltage factor would have been 1,5. When the second and third pole interrupt 90° later, there is a discontinuity and the recovery voltage across the first-pole-to-clear will follow a 1-cosine wave with a voltage factor of 1,25. The recovery voltage is indicated by the solid line in Figure 121. By using a voltage factor of 1,25 (dotted line in Figure 121), the initial portion of the recovery voltage across the first pole is not adequately covered. Using a voltage factor of 1,5 will result in too high a stress. A voltage factor of 1,4 as indicated by the dashed curve in Figure 121 is a compromise that adequately covers the actual recovery voltage.

Careful consideration should be given to these voltage factors when circuit-breakers are relocated to other parts of the system where the application is different from that of the original location.

As indicated in footnote a) to Table 43, the voltage factors given in Table 43 are associated with single circuit line constructions and are chosen to accommodate all known physical arrangements of the conductors of such circuits. Footnote b) to Table 43 indicates that energisation of the case of multiple overhead line constructions that have parallel circuits may require a voltage factor greater than 1,2 and 1,4. This is because such circuits are likely to have an enhancement to the line side residual voltage following interruption. This is associated with the coupling (pick-up) from the parallel circuit and may add a power frequency peak voltage of up to 0,2 p.u. This is dependent upon the geometry of the conductor systems of the two circuits.

In addition, the effect of these changes on the line side voltage, following interruption by the first-pole-to-clear, does affect the shape of the TRV across that opening pole. Consideration of this may require additional testing if the existing factor does not adequately cover the combined effects. Alternatively, the higher of the given values, e.g. 1,4 for 1,2, can be selected to encompass the specific waveshape.

On occasion, utilities have specified a voltage factor of 1,3 instead of 1,2 for double circuit lines.

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9.7 General application considerations

9.7.1 General

The capacitive current switching capability of the circuit-breaker is depending on its rated voltage, rated frequency, the particular application (i.e. overhead line, capacitor bank, etc.) and the earthing conditions of the network.

Caution should be exercised when applying older circuit-breakers that have not been rated to IEC 62271-100.

9.7.2 Maximum voltage for application

The operating voltage should not exceed the rated voltage since this is the upper limit for operation.

9.7.3 Rated frequency

The rated frequency for circuit-breakers is 50 Hz or 60 Hz. As described in 9.2.1.3, a rated frequency of 60 Hz results in a more severe stress on the circuit-breaker, since the voltage peak occurs earlier (at 8,3 ms) than in the case of 50 Hz (10 ms).

Special consideration should be given when comparing tests performed at 60 Hz to cover 50 Hz requirements or vice versa. At lower frequencies, the capacitance current switching ability will be adequate. The switching capability demonstrated at 60 Hz covers the requirements for 50 Hz with the same voltage factor.

9.7.4 Rated capacitive current

9.7.4.1 General

The preferred values of the rated capacitive switching current are given in Table 9 of IEC 62271-100:2008. Not all actual cases of capacitive current switching are covered by that table. The values for lines and cables cover most cases, the values of the current for capacitor banks (single and back-to-back) are typical for some capacitor banks in service.

9.7.4.2 Overhead lines and cables

Depending on length, the no-load current of lines and cables may exceed that given in Table 9 of IEC 62271-100:2008.

The following may serve as an example: the no-load current of a two bundle conductor 550 kV transmission line is approximately 1,1 A/km at 50 Hz and 1,3 A/km for 60 Hz.

Without considering the Ferranti effect (see 9.5.3.3), the charging current of a 500 km line would be 605 A at 50 Hz and 715 A at 60 Hz. Ferranti rise on a 500 km line would increase the charging current by about 4 % at 50 Hz and 6 % at 60 Hz. This is not covered by Table 9 of IEC 62271-100:2008.

The higher current does not pose a problem for circuit-breakers of present design, since the higher current tends to increase the minimum arcing time resulting in a wider contact gap when the recovery voltage reaches its peak. The possible peak recovery voltage present on interruption could be a problem (see 9.5.3.3).

9.7.4.3 Capacitor banks

The same remark as given under 9.7.4.2 applies to capacitor bank currents. The current is dependent on the size of the capacitor bank and, in certain cases, the capacitor bank

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considered may have a current rating higher than that given in Table 9 of IEC 62271-100:2008. This does not pose a problem for circuit-breakers of present design.

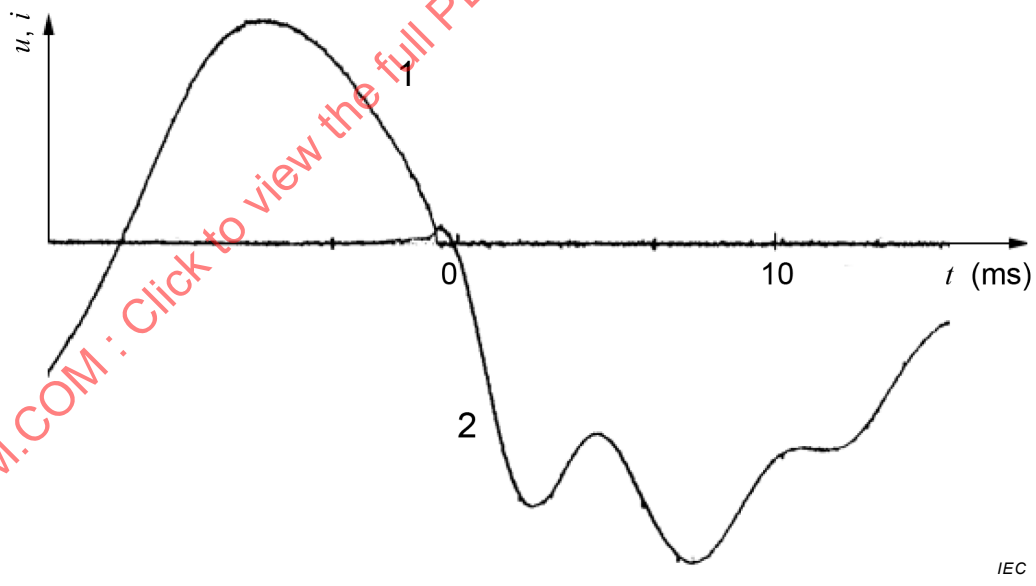
9.7.5 Voltage and earthing conditions of the network

Subclause 6.111.7 of IEC 62271-100:2008 gives the multiplication factors for single-phase tests for the different conditions, refer to 9.6. They range from 1,0 for solidly earthed systems to 1,7 for non-effectively earthed systems in the presence of single- or two-phase to earth faults.

Both user and manufacturer should be aware of these earthing conditions in order to specify the correct circuit-breaker suitable for the application.

Harmonic filter switching usually results in a recovery voltage that contains several harmonic components. The recovery voltage may have a shape as indicated in Figure 122. Careful system study should be done to define realistic requirements regarding the recovery voltage. In some cases, filter banks switching tests may need to be performed because capacitor bank switching tests do not cover the required recovery voltage waveshape. This needs to be considered when making the proper choice of circuit-breaker. From the voltage waveshape as indicated in Figure 122, it can be seen that the usual definition of re-ignition and restrike may no longer apply to a recovery voltage that does not have a 1-cosine waveshape.

In the case of a multi-frequency recovery voltage, the definition of re-ignition and restrike should be based on the amplitude of the breakdown voltage. If the amplitude is less than 1,0 p.u. of the system voltage, it is a re-ignition. If the amplitude is equal to or above 1,0 p.u. of the system voltage, it is a restrike. These definitions of restrike and re-ignition are generally acceptable but may lead to expensive solutions. More economical solutions may be obtained by permitting restrikes in a zone where tests have demonstrated that they are not harmful to the circuit-breaker.



Key

1 Current through circuit-breaker

2 Voltage across circuit-breaker

Figure 122 – Example of the recovery voltage across a filter bank circuit-breaker

9.7.6 Restrike performance

See 3.3.

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9.7.7 Class of circuit-breaker

The choice of the class of circuit-breaker is discussed in 3.3.

9.7.8 Transient overvoltages and overvoltage limitation

9.7.8.1 General

An important consideration for application of circuit-breakers for capacitive current switching is the transient overvoltage that may be generated by restrikes during the opening operation. The transient overvoltage factor is defined as the ratio of the transient voltage appearing between a circuit-breaker disconnected terminal and the neutral of the disconnected capacitance during opening to the operating line-to-neutral crest voltage prior to opening.

The selection of the class (see 9.7.7) of circuit-breaker to be applied should be coordinated with the insulation capability of other components on the system.

9.7.8.2 Overvoltages

9.7.8.2.1 General

When switching capacitive currents, transients are generated. These transients are associated with the restrikes when de-energising a capacitive load and with energisation of capacitive loads. These transients may cause:

– insulation degradation and possible failure of the substation equipment;
– operation of surge arresters;
– interference in the control wiring of the substation;
– increase in step potentials in substations;
– undesired tripping or damage to sensitive electronic equipment.

The magnetic fields associated with high inrush currents during back-to-back energisation of either the no-load transmission line conductors or the earthing grid during back-to-back switching can induce voltages in control cables by both capacitive and electromagnetic coupling. These induced voltages can be minimized by shielding the cables and using a radial configuration for circuits (circuits completely contained within one cable so that inductive loops are not formed).

9.7.8.2.2 Switching of capacitor banks

9.7.8.2.2.1 General

The switching of capacitor banks is associated with voltage and current transients. As most modern circuit-breakers have a very low probability of restrike, the majority of the switching transients will be generated when energizing capacitor bank(s). The effects of the transients will exhibit themselves locally and at remote locations on the power system.

The high-frequency transient inrush current associated with back-to-back switching can stress other equipment in the circuit as well as the circuit-breaker. Wound-type current transformers will have turn-to-turn insulation stressed because of the high rates of rise of current and the resulting voltage that is developed across inductance in the circuit.

9.7.8.2.2.2 Local effects

– voltage transients resulting in dielectric stresses on nearby equipment;
– electrical, mechanical and electromechanical forces caused by the inrush current.

9.7.8.2.2.3 Remote effects

– transfer of capacitively coupled fast transients through transformer windings;

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– reflections of travelling wave transients on open ended lines or transformer terminated lines;

– excitation of near resonant portions of the power system by the oscillatory transient frequency.

9.7.8.2.3 Switching of lines and cables

When energizing lines and cables, high overvoltages may be created depending on whether or not the line or cable was precharged as a result of a preceding breaking operation (i.e. in the case of an auto-reclosing). These overvoltages may result in damage of insulation.

9.7.8.3 Overvoltage limitation

There are several means available to reduce the overvoltages generated by the switching of capacitive currents:

– **current limiting reactors** are normally used to reduce the current transients associated with back-to-back switching. They do not limit the remote overvoltages.

– **pre-insertion resistors** limit the inrush current and remote overvoltages. It is a basic solution used on circuit-breakers. They are usually fitted on circuit-breakers and as such add to the complexity of the equipment. Depending on the design, the added complexity may or may not result in a reduced availability of the equipment (see also 9.7.16).

– **pre-insertion reactors** also limit the inrush current and remote overvoltages. They are usually fitted on circuit-switchers and their effect on complexity and availability of the equipment is sometimes equivalent to pre-insertion resistors, depending on the design of the devices.

– **controlled closing** reduces the magnitude of the inrush current depending on the point-on-wave of the voltage prior to the prestrike between the contacts. A simple way of reducing the transients is to let the circuit-breaker contacts close at a voltage zero. This method is called controlled closing. The controller also adds to the complexity of the equipment and can influence its availability.

9.7.9 No-load overhead lines

9.7.9.1 General

A circuit-breaker may be required to energise or de-energise a no-load transmission line during its normal operating duties. Prior to energisation, the line may or may not contain a trapped charge (see also 9.5.3). Consideration may need to be given to line energisation following load rejection (see [127]).

9.7.9.2 Line charging current

When considering the assigned line charging current rating, application is determined by the value of the line charging current. This current is a function of system voltage, line length, and line configuration (see also 9.5.1.1).

9.7.9.3 Compensated overhead lines

As described in 9.5.2 very long lines (> 200 km) are often compensated with shunt reactors to reduce the amount of charging current required of the system.

If the circuit-breaker rating is chosen based on I_{Lc}, the line could not be switched without the compensating reactor(s) connected. The voltage rise caused by the Ferranti effect and also the location of the reactor(s) will change the line current slightly.

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9.7.9.4 No-load line recovery voltage

The line-charging breaking current rating is assigned on the basis of a standard recovery voltage associated with this type of circuit. For solidly earthed systems, the no-load line charging current switching tests require a maximum voltage of 2,4 times (see also 9.5.1.2) the rated phase-to-earth voltage across the circuit-breaker one half-cycle after interruption (assumes $C_1 = 2C_0$ where C_1 is the positive-sequence capacitance and C_0 is the zero-sequence capacitance). This is the difference voltage of the source and line sides, including the effects of coupled voltage on the first-pole-to-clear. The test voltage requires a 1-cosine waveshape.

For double circuit lines with higher voltage factors refer to 9.6.

Deviations from the test voltage characteristics may increase or decrease the probability of the circuit-breaker restriking. As described in 9.5.2, a compensated line will have a lower rate-of-rise of the recovery voltage, which will reduce the restrike probability.

9.7.10 Capacitor banks

9.7.10.1 General

A circuit-breaker may be required to switch a capacitor bank from a bus that does not have other capacitor banks energised (single) or against a bus that has other capacitor banks energised (back-to-back). In the application of circuit-breakers for capacitor switching duty, consideration should be given to the preferred single shunt capacitor bank switching current, preferred back-to-back shunt capacitor bank switching current, preferred transient inrush current, and preferred transient inrush current frequency (see also 9.3.2 and 9.2.2).

9.7.10.2 Capacitor bank current

Circuit-breakers are to be applied according to the actual capacitive current they are required to interrupt. The rating should be selected to include the following effects.

a) *Voltage.* The reactive power rating of the capacitor bank, in kvar, is to be multiplied by the ratio of the maximum service voltage to the capacitor bank nameplate voltage when calculating the capacitive current at the applied voltage. This ratio can be as large as 1,1, since capacitors can be operated continuously up to 10 % above the capacitor rated voltage.

b) *Capacitor tolerance.* The manufacturing tolerance in capacitance is −0 to +15 % with a more frequent average of −0 to +5 %. A multiplier in the range of 1,05 to 1,15 should be used to adjust the nominal current to the value allowed by tolerance in capacitance.

c) *Harmonic component.* Capacitor banks provide a low-impedance path for the flow of harmonic currents. When capacitor banks are non-effectively earthed, no path is provided for zero-sequence harmonics (third, sixth, ninth, etc.), and the multiplier for harmonic currents is less. A multiplier of 1,1 is generally used for a solidly earthed neutral bank and 1,05 for a non-effectively earthed neutral.

In the absence of specific information on multipliers for the above factors, it will usually be conservative to use a total multiplier of 1,25 times the nominal capacitor current at rated capacitor voltage for non-effectively earthed neutral operation and 1,35 times the nominal current for solidly earthed neutral operation.

9.7.10.3 Methods for calculating transient inrush currents

9.7.10.3.1 General

The capacitor bank being switched is assumed uncharged, with closing at a voltage crest of the source voltage. The current used should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of

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capacitance. In the absence of specific information, a multiplier of 1,15 times normal capacitor current would give conservative results.

9.7.10.3.2 Single capacitor bank

A bank of shunt capacitors is considered single when the conditions described in 9.3.3.1 are fulfilled. Table 44 gives the equations that apply for calculation of the inrush current for single capacitor bank energisation, neglecting resistance.

Table 44 – Inrush current and frequency for switching capacitor banks

Duty	Quantity	Equation
Energisation of single bank	$i_{\text{i peak}}$ (A)	$\frac{\sqrt{2}U_{\text{r}}}{\sqrt{3}} \times \sqrt{\frac{C}{L_{\text{s}}}}$
	f_{i} (Hz)	$\frac{1}{2\pi\sqrt{L_{\text{s}}C}}$
Back-to-back switching	$i_{\text{i peak}}$ (A)	$\frac{\sqrt{2}U_{\text{r}}}{\sqrt{3}} \times \sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}}$
	f_{i} (Hz)	$\frac{1}{2\pi\sqrt{L_{\text{eq}}C_{\text{eq}}}}$

Key

U_{r}: rated voltage (V)*
C: bank capacitance (F)*
L_{s}: source inductance (H)*
C_{eq}: equivalent capacitance (F)**
L_{eq}: equivalent inductance (H)**
* See 9.3.3.1.
** See 9.3.3.2.

9.7.10.3.3 Back-to-back capacitor bank

The inrush current of a single bank will be increased when other capacitor banks are connected to the same bus (see also 9.3.3.2).

Table 44 gives the equations for calculating inrush current and frequency for back-to-back capacitor bank switching, neglecting resistance. These equations are based on the theory described in 9.2.2.

A typical circuit for back-to-back switching is shown in Figure 123. The inductance in the circuit that limits the transient oscillatory current is composed of the inductance of the bus between switching devices, L_{bus}, the inductance between the switching device and the capacitor banks, L_1 and L_2, and the inductance of the capacitor banks, L_{c1} and L_{c2} and any additional reactance inserted. The total inductance between capacitor banks, L_{c1} + L_1 + L_{bus} + L_2 + L_{c2}, is very small with respect to the inductance of the source L_{s}. In most cases, the total inductance between capacitor banks will be less than 1 % of the inductance of the source, and the contribution of transient current from the source can be neglected.

The inductance of the bus can be calculated similar to a transmission line using values from tables available from suppliers of bus conductors for different bus configurations (see 9.7.10.3.4).

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The inductance within the capacitor bank itself is not easy to obtain, but in general it is of the order of 10 µH for banks above 52 kV, and 5 µH for banks below 52 kV. Typical values of inductance per phase between back-to-back capacitor banks and bank inductance for various voltage levels are given in Table 45.

Table 45 – Typical values of inductance between capacitor banks

Rated maximum voltage (kV)	**Inductance per phase of busbar** (µH/m)	**Typical inductance between banks** [a] (µH)
17,5 and below	0,702	10 to 20
36	0,781	15 to 30
52	0,840	20 to 40
72,5	0,840	25 to 50
123	0,856	35 to 70
145	0,856	40 to 80
170	0,879	60 to 120
245	0,935	85 to 170

[a] Typical values of inductance per phase between capacitor banks. This does not include inductance of the capacitor bank itself. Values of 5 µH for banks below 52 kV and 10 µH for banks above 52 kV are typical for the inductance of the capacitor banks.

Inherent resistance of the circuit causes rapid decay of the transient current so that the first peak actually may only reach 90 % to 95 % of the maximum value calculated. These values are applicable to both solidly earthed or isolated capacitor banks and with Y or Δ connections. With a non-effectively earthed neutral, the current in the first two phases to close will be 87 % of calculated, but the current in the last phase will equal the value calculated. However, inherent resistance of the circuit will affect these currents by the factors indicated above.

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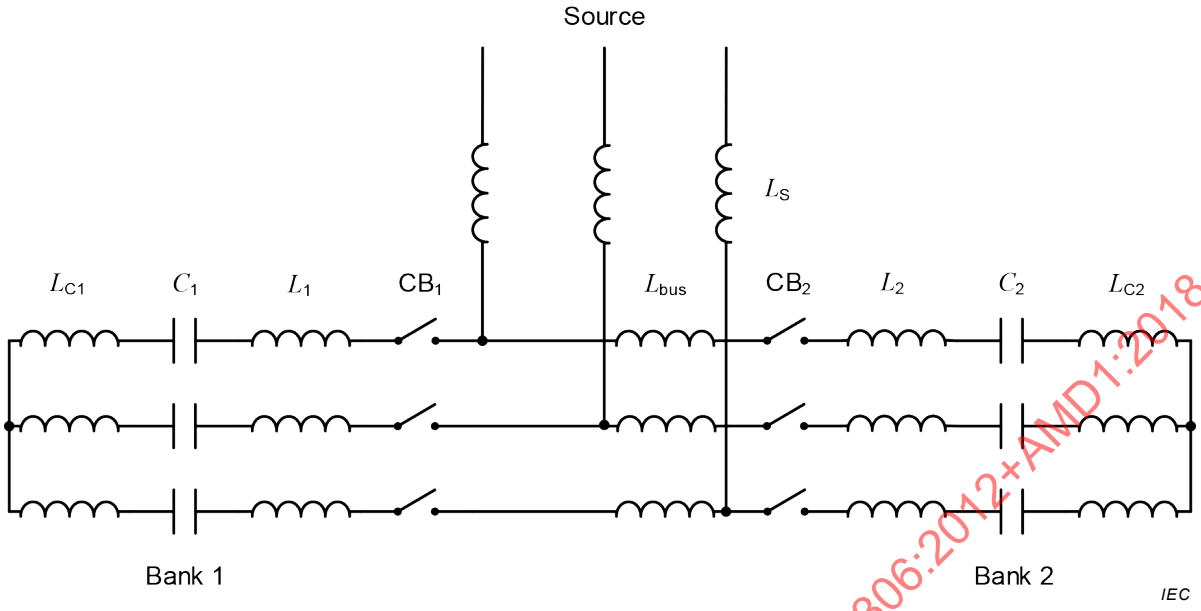

Key

CB_1	circuit-breaker energizing capacitor bank 1
CB_2	circuit-breaker energizing capacitor bank 2
L_S	source inductance
C_1	capacitor bank 1
C_2	capacitor bank 2
L_{C1}, L_{C2}	capacitor bank inductance
L_1, L_2	bus inductance between switching device and capacitor bank
L_{bus}	inductance of bus between switching devices

Figure 123 – Typical circuit for back-to-back switching

The equations in Table 44 for back-to-back switching will give correct results when switching a bank against another bank. However, when switching against several other banks connected to the bus, the correct value of equivalent inductance to be used for the combination of banks connected to the bus is not easily obtained. For example, when switching a bank against three other banks energised on the bus, the calculated current will be too high if an inductance of $L/3$ is used. On the other hand, using a value of $3L$ will result in a current that is too low. If exact solutions cannot be made, conservative results should be used in calculating inrush currents by using the inductance divided by the number of capacitor banks, recognizing that the results will be 20 % to 30 % higher (see also 9.3.3.2). When more than two banks are installed on the same bus, a more exact calculation of the inrush current parameters is obtained using an electromagnetic transient program.

9.7.10.3.4 Considerations for transient inrush currents

The inrush currents of different types of compact multi-section banks with minimum spacing between the individual sections may differ by as much as 20 %. Consequently, these inrush currents can be reduced significantly by increasing the lengths (inductance) of the circuits between the sections.

Another effective measure to reduce transient inrush currents is to add inductance in the circuit between the capacitor banks.

In IEC 62271-100:2001, the equivalency rule between the test performed and the service conditions was based on the product of inrush current peak and frequency, $i_{i\ peak} \times f_i$ (kAkHz). Calculations have shown that the arc energy during a making operation is independent of the inrush current frequency for cases where the pre-arcing time is greater than half a period of the inrush current frequency. This is usually the case for back-to-back

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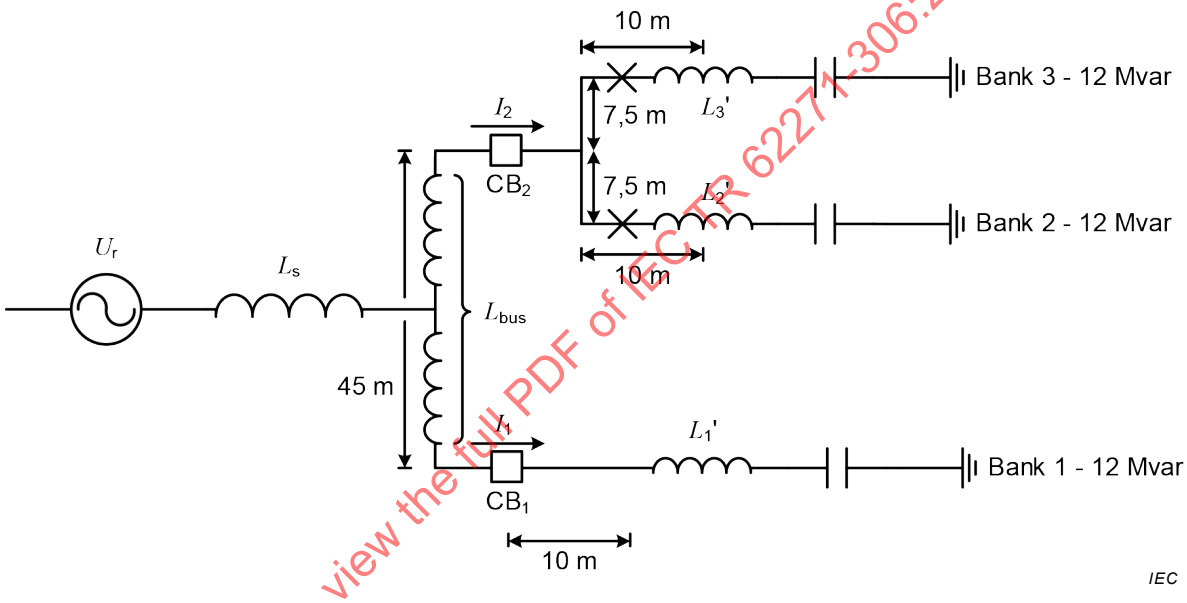
capacitor bank switching. For back-to-back capacitor bank switching, the arc energy during a making operation is only a function of the inrush current peak. On the other hand, it is well known that the shape of the wear on the arcing contacts as well as the effect of the pressure shock waves are somewhat frequency-dependent and should not be disregarded. Because of the latter, an upper tolerance of +130 % has been specified on the permissible inrush current frequency that can be used in service. In other words: the inrush current frequency used during the tests should not be lower than 77 % of the inrush current frequency foreseen in service. This concept is limited to inrush current frequencies up to 6 kHz since the information available for higher frequencies is limited.

Although circuit-breakers have usually been tested with inrush current peaks up to 20 kA and 4,25 kHz, system designers should endeavour to keep the inrush currents far below this value for system quality reasons.

The following example will illustrate the use of the equations in Table 44.

A 123 kV system is assumed as shown in Figure 124.



Key

U_r	123 kV (the rated capacitor bank voltage is 115 kV)
L_S	Source inductance is 3,77 Ω, 10 mH (f_s = 60 Hz)
L_1', L_2', L_3	Inductance between circuit-breaker and capacitor bank; including inductance of capacitor bank
L_{bus}	Inductance of bus between switching devices
CB_1, CB_2	Circuit-breakers
	Short-circuit of source: 18 600 A at 123 kV

Figure 124 – Example of 123 kV system

The capacitor banks shown have a nominal rating of 12 Mvar (capacitors rated 100 kvar, 13,28 kV, 5 series sections with eight capacitors in parallel per phase). Nominal current per bank is 60 A. In determining the rating of the circuit-breaker required, the increase in current due to applied voltage, capacitance tolerance, and harmonics should be considered. The increase in current at maximum rated voltage is: maximum voltage to capacitor rated voltage = 123/115 = 1,07. Assume a positive tolerance of capacitors of +10 %, multiplier of 1,1 and assume a multiplier for harmonic content for a solidly earthed neutral bank of 1,1.

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The total multiplier used to determine the single and back-to-back current rating is 1,07 × 1,1 × 1,1 = 1,29, giving a current of 1,29 x 60 = 78 A. With capacitor banks 2 and 3 energised, the current through CB_2 is 156 A.

The circuit-breakers intended for this duty have the following ratings: rated voltage 123 kV, rated current 1 600 A, rated short-circuit current 40 kA, rated single and back-to-back capacitive switching current 400 A.

The transient inrush current and frequency are calculated using the equations in Table 44. In the example, L_1', L_2' and L_3' are the inductances between the respective capacitor banks and the circuit-breakers, including the inductance of the capacitor bank. L_{bus} is the inductance of the bus between the circuit-breakers.

The inductance values in Table 45 can be used or values can be calculated for the actual bus configuration used. In the example given below, the added reactance between the circuit-breaker and capacitor bank is:

L_1' = 20,0 µH

L_2' = L_3' = 27,1 µH

The inductance of the busbar L_{bus} = 38,5 µH.

In determining inrush current and frequency, the currents I_1 and I_2 as used in Table 44 should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of capacitance. In the example, the multiplier to be used is 1,07 × 1,1 = 1,18. The currents are I_1 = 60 × 1,18 = 71 A and I_2 = 71 A or 142 A, depending on whether bank 2 or 3 or both banks are energised.

Case I. Energisation of capacitor bank 1 with banks 2 and 3 not energised (single bank switching).

Bank capacitance C for calculation:

$$C = 1{,}1 \times \frac{\text{Mvar}}{\omega U_r^2}\,(\text{F}) \text{ with } U_r \text{ in kV} \rightarrow C = 1{,}1 \times \frac{12}{377 \text{ x } (115)^2} = 2{,}65\ \mu\text{F}$$

L_s = 10 mH

$$i_{ipeak} = \frac{\sqrt{2}\left(123 \times 10^3\right)}{\sqrt{3}} \times \sqrt{\frac{2{,}65 \times 10^{-6}}{10 \times 10^{-3}}} = 1\ 635\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{10 \times 10^{-3} \times 2{,}65 \times 10^{-6}}} = 977\ \text{Hz}$$

This is less than the maximum rate of change for a rated short-circuit current of 40 kA which is equal to $2\pi f_s \sqrt{2} I_{sc} = 21{,}3$ A/µs and therefore meets the requirements of single capacitor bank switching.

Case II. Energisation of bank 1 with bank 2 energised on the bus (back-to-back switching against an equal size bank).

$$C_{eq} = \frac{2{,}65}{2} = 1{,}325\ \mu\text{F}$$

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L_{eq} = 20 + 38,5 + 27,1 = 85,6 µH

$$i_{ipeak} = \frac{\sqrt{2}(123\times10^{3})}{\sqrt{3}} \times \sqrt{\frac{1{,}325\times10^{-6}}{85{,}6\times10^{-6}}} = 12\,495\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{85{,}6\times10^{-6}\times1{,}325\times10^{-6}}} = 14\,944\ \text{Hz}$$

The calculated back-to-back inrush current and frequency should be compared with the back-to-back switching capability listed in Table 5 of IEC 62271-100:2008. For a maximum voltage of 123 kV, the assumed rated values are 20 kA for the peak current and 4,25 kHz for the inrush current frequency. The calculated value of the inrush current peak is within this rating, the inrush current frequency exceeds that assumed and inductance should be added between the capacitor banks to reduce the inrush current frequency. Adding an inductance of 1 mH will limit the inrush current to 3,5 kA and the frequency to 4,18 kHz, both of which are below the assumed capability.

Case III. Energisation of bank 1 with banks 2 and 3 energised on the bus.

$$C_{eq} = \frac{(2{,}65+2{,}65)2{,}65}{(2{,}65+2{,}65)+2{,}65} = 1{,}76\ \mu\text{F}$$

$$L_{eq} = \frac{(27{,}1)}{2} + 38{,}52 + 20 = 72{,}07\ \mu\text{H}$$

$$i_{ipeak} = \frac{\sqrt{2}(123\times10^{3})}{\sqrt{2}} \times \sqrt{\frac{1{,}76\times10^{-6}}{72{,}07\times10^{-6}}} = 15\,694\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{72{,}07\times10^{-6}\times1{,}76\times10^{-6}}} = 14\,131\ \text{Hz}$$

Of the calculated values of inrush current peak and frequency, the frequency of 14,1 kHz exceeds the assumed back-to-back switching capability of 4,25 kHz listed in Table 9 of IEC 62271-100:2008. As in the previous case of switching identical banks, adding an inductance of 0,71 mH will limit the inrush current peak to 4,7 kA and the inrush current frequency to 4,3 kHz, both of which are below the assumed back-to-back switching capability of a 123 kV circuit-breaker.

Based on the system and conditions studied, a circuit-breaker having the following ratings would be applied: rated short-circuit current of 40 kA and rated single capacitor bank switching current of 400 A. The assumed back-to-back rating of 20 kA and 4,25 kHz that goes with this rating will be exceeded unless additional inductance is added between the capacitor banks. A value of 0,71 mH is sufficient to keep within the assumed ratings available.

9.7.11 Switching through transformers

Circuit-breakers may be required in some applications to switch capacitors, lines, or cables through an interposed transformer. The current switched by the circuit-breaker will be N times the capacitor, line, or cable current on the other side of the transformer, where N is the transformer turns ratio.

Switching charging current through a transformer may be less difficult than switching the same current directly. The capacitive elements of the circuit will oscillate with the transformer

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inductance, which may also saturate, producing a less severe transient recovery voltage and a lower probability of restrike. If a restrike should occur, the additional inductance will help to limit the inrush current. Saturation may also occur when de-energizing a remote transformer that is fed through a long cable. The stress on the transformer is not considered harmful.

If the value of N is greater than 1, switching through a transformer will have the effect of increasing the current being switched. De-energizing no-load overhead lines with lower voltage circuit-breakers can result in effective line charging currents in the 750 A to 1 000 A range. The capacitive switching rating of circuit-breakers which may be exposed to this type of duty should be carefully checked before application is made.

Figure 125 shows the voltage and current relations that are the result of a single-phase simulation of capacitor switching through an interposed transformer. It can be seen that due to the reduced recovery voltage, the increased current is not a problem for the circuit-breaker.

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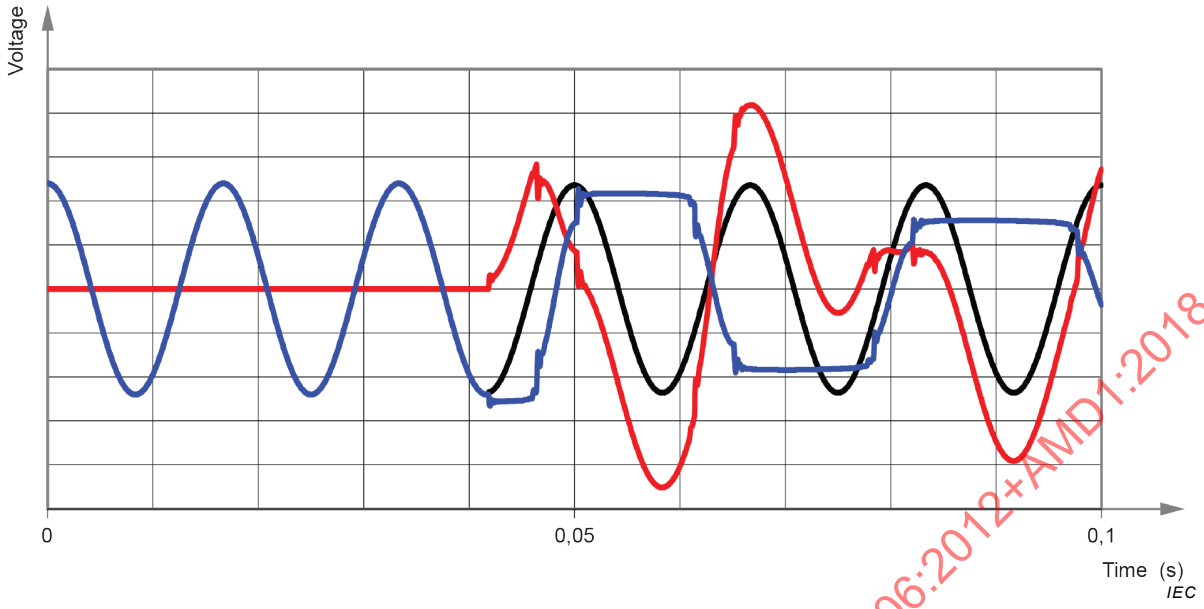
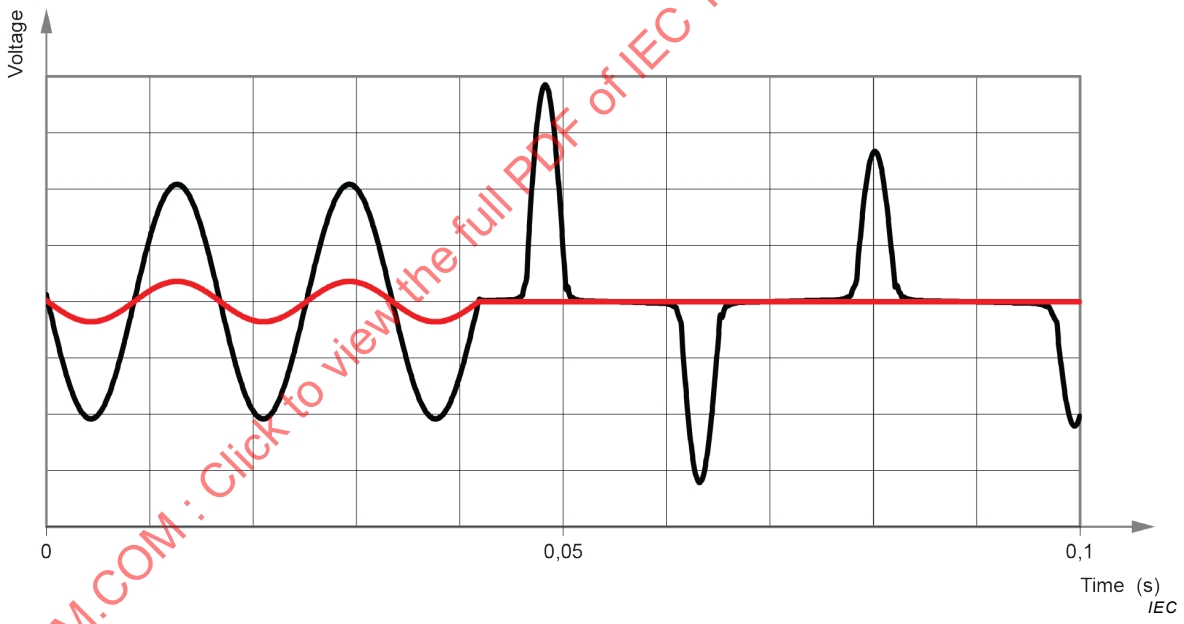


Black line Source voltage

Blue line Voltage on the load side of the circuit-breaker

Red line Voltage across the circuit-breaker

Figure 125a – Voltage relations



Black line Capacitor bank current (low voltage side of the transformer)

Red line Current through the circuit-breaker

Figure 125b – Current relations

Figure 125 – Voltage and current relations for capacitor switching through interposed transformer

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9.7.12 Effect of transient currents

9.7.12.1 General

In the application of circuit-breakers in stations having banks of capacitors, it may be necessary to investigate the effects of transient currents and other special situations upon

circuit-breakers other than those specially equipped for and assigned to the routine capacitor switching.

The transient currents of capacitor banks may be considered in two aspects: the inrush currents energisation of the banks and the discharge currents into faults. Where the quantity of parallel capacitor banks installed in a station is large, the transient currents may have significant effects upon the circuit-breaker.

The transient currents may have large peaks and high frequencies which may affect circuit-breakers in the following ways:

a) a circuit-breaker may be subjected to a transient inrush current that exceeds its rating. This may occur with the circuit-breaker in the closed position or when closing into solidly earthed faults;

b) the transient inrush current may have sufficient magnitude and rate of change to flash over the secondaries of current transformers or the associated control wiring.

Circuit-breakers located in a position such as a tie circuit-breaker between bus sections (bus section or bus coupler) may be exposed to the transient inrush currents from energizing banks of capacitors when they are located on bus sections on both sides of the circuit-breaker (see Figure 126, CB_1).

The inrush current will seldom exceed the capability of the circuit-breaker. However, a check may be required to determine if the rate of change of inrush current will cause overvoltages on the secondary of current transformers on the circuit-breaker or in the current path between the capacitor banks.

9.7.12.2 Exposure to total capacitor bank discharge current

In a substation where parallel capacitor banks are located near or on a busbar, any circuit-breaker connected to the bus may be exposed during faults to the total discharge current of all the banks located behind the circuit-breaker. In Figure 126, CB_2 will be subjected to this total discharge current with a fault occurring at location A. The worst case, or highest capacitor discharge current, occurs with a bolted three-phase fault where capacitor banks are non-effectively earthed and for a case of a three phase-to-earth or a line-to-earth fault where capacitor banks are solidly earthed.

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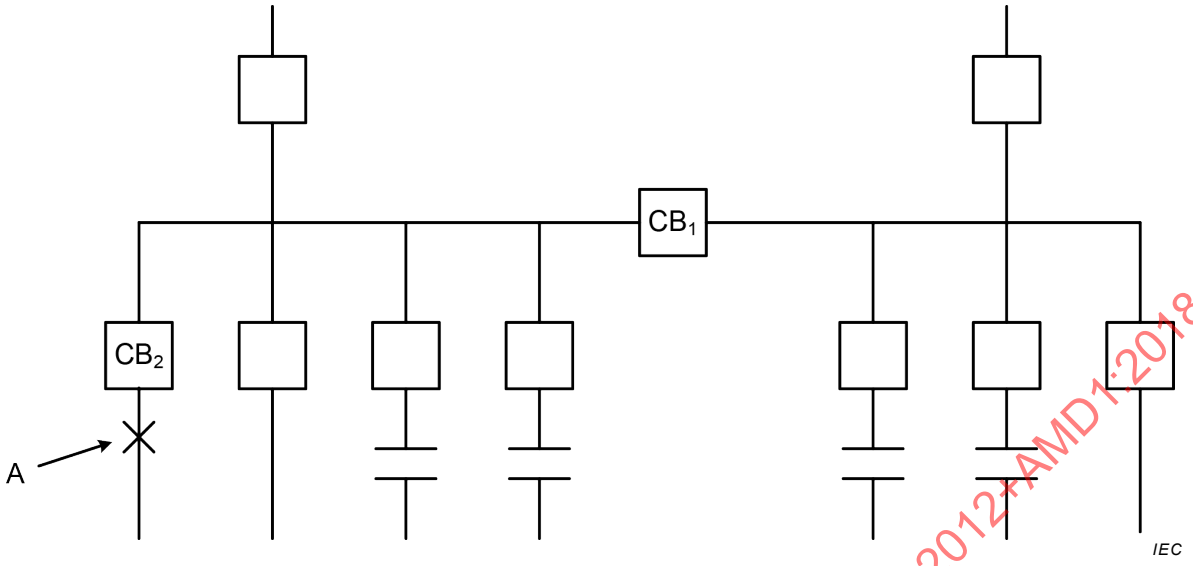

Key

CB_1, CB_2 Circuit-breakers

Figure 126 – Station illustrating large transient inrush currents through circuit-breakers from parallel capacitor banks

The total discharge current (peak) of all banks behind the circuit-breaker is equal to the algebraic sum of the individual banks of capacitors. Neglecting resistance, the discharge current of an individual capacitor bank is equal to:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{C}{L}} \tag{33}$$

where

$I_{\text{d peak}}$ is the crest value of discharge current;

U_{r} is the rated voltage;

C is the capacitance per phase of individual bank;

L is the inductance per phase between capacitor bank and fault location.

The inductance L is primarily made up of bus conductors and any additional inductance added to the bank for limiting the inrush currents.

If there are n capacitor banks of approximately equal capacitance and separated by an approximately equal inductance to the fault, then the total discharge current is approximately equal to the sum of the crest current of each bank or n times that of one bank. This is demonstrated as follows:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{Cn}{L/n}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} n \sqrt{C/L} \tag{177}$$

In addition to the checking of the crest current, it may be necessary also to check the rate of change of the discharge current with the manufacturer.

The transient discharge current passing through a circuit-breaker should also be examined for its effects upon the current transformers. The discharge currents may substantially exceed the magnitudes and the frequency of the inrush currents described in Table 9 of

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IEC 62271-100:2008. This occurs because the contribution may come from a number of capacitor banks and is not limited by the inrush impedance seen when energizing a bank of capacitors.

9.7.13 Exposure to capacitive switching duties during fault switching

Where parallel banks of capacitors are located on bus sections in a station, caution should be exercised in the fault switching sequence so that the last circuit-breaker to clear is not subjected to a capacitive switching duty beyond its capability. This is especially a concern for a circuit-breaker used as a bus section tie circuit-breaker with capacitors located on both sides of the circuit-breaker as shown in Figure 126, CB_1.

The worst case occurs in a station where the bus section tie circuit-breaker is last to clear the bus for a fault that leaves one or more phases of the capacitor banks fully energised. In this situation, the bus tie circuit-breaker should be properly equipped and rated for the parallel switching of the capacitor banks remaining on the bus section to be de-energised. In the example of Figure 126, this means that the tie circuit-breaker should be capable of switching two banks of capacitors in parallel with two banks of capacitors on the source side. Another solution is to coordinate if possible the clearing times so that the tie circuit-breaker is always first to clear to avoid the capacitor switching duty.

9.7.14 Effect of load

The situation can occur where a circuit-breaker is called upon to switch a combination of a capacitive current and a load current. The circuit-breaker will have the required switching capability if the total current does not exceed the rated continuous current of the circuit-breaker and either

a) the power factor is at least 0,8 leading, or

b) the capacitive current does not exceed the rated capacitive switching current of the circuit-breaker.

Where the above conditions are exceeded, the capability and performance of the circuit-breaker is not defined by the standards and the manufacturer should be consulted. When the power factor is below 0,8 leading, the voltage may be sufficiently out-of-phase with the current to cause unacceptable restriking. The situation will be more severe if there is also a bank of capacitors located on the source side of the circuit-breaker.

9.7.15 Effect of reclosing

Up to twice normal inrush currents are possible when reclosing is applied to a circuit-breaker switching capacitive loads. When capacitor bank current is interrupted at or near a normal current zero, the voltage remaining on the bank may be near peak value. Reclosing a circuit-breaker against such a charged capacitor bank may produce high inrush current.

When a capacitor bank is connected to the load side of a feeder circuit-breaker equipped with automatic reclosing, high inrush currents can be avoided by isolating the capacitor bank from other loads after the circuit-breaker is tripped and before reclosing. The switching device used for regular capacitor bank switching can be employed for isolation. This technique is particularly recommended where other capacitor banks are connected to the same station bus.

A second technique to avoid high inrush currents during reclosing is to increase reclosing time delay. Normally, the discharge resistors inside each capacitor unit, or other deliberately introduced discharge devices will reduce residual voltage.

Discharge curves are available from the capacitor supplier and should be consulted where reclosing time is delayed.

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9.7.16 Resistor thermal limitations

For capacitor bank circuit-breakers equipped with pre-insertion resistors, the thermal capability of the resistors should be considered in determining the time interval between capacitive current switching operations. The resistance value is related to the size of the capacitor bank and the pre-insertion resistors should normally have a thermal capability as defined by the rated operating sequence.

If capacitive current switching field tests are planned which exceed the number of operations as defined by the thermal capacity of the pre-insertion resistors, or which utilize a specially designed circuit-breaker, the manufacturer should be consulted regarding the frequency of operations.

9.7.17 Application considerations for different circuit-breaker types

9.7.17.1 General

The switching of capacitive current poses different stresses on the different types of circuit-breakers. Restrikes on opening and prestrikes on closing may or may not be a problem. The considerations given below are general and are based on experiences gained by laboratory tests, field tests and field experience.

9.7.17.2 Oil circuit-breakers

9.7.17.2.1 Restrikes

Depending on the design (contact speed, electrode shape, etc.), an oil circuit-breaker generally has long arcing times when interrupting. The restrike probability increases with increased current, because gas bubbles reduce the effective amount of oil between the contacts causing a reduction of the dielectric strength of the contact gap. These circuit-breakers deserve special consideration when used or relocated to a system where the line charging current exceeds the rating.

Some oil circuit-breakers are pressurized to reduce the size of the bubbles and therewith increasing the dielectric strength of the contact gap. Some oil circuit-breakers may be fitted with opening resistors, to reduce the effects of a restrike.

An oil circuit-breaker will normally not interrupt the high-frequency current associated with the restrike and the high arc impedance introduces an additional damping of the restrike current. This will reduce the risk for multiple restrikes.

Older contraction type oil circuit-breakers are known to produce multiple restrikes that may result in voltage escalation and subsequent development of an evolving fault.

9.7.17.2.2 Prestrikes

Oil circuit-breakers are especially sensitive to high-frequency prestrikes when energizing capacitor banks. The prestrikes cause a shock wave in the oil. As oil is not compressible, the shock wave causes mechanical stresses on the internal components of the breaking chamber. As a result of the exposure to these high mechanical stresses, the breaking chamber insulator may shatter and even stationary contacts may crack. Application of an oil circuit-breaker for capacitor bank switching requires a severe reduction of the inrush current frequency or special design of the oil circuit-breaker (e.g. using pre-insertion resistors).

Bulk oil circuit-breakers have been applied using a limitation of 20 kAkHz for over 30 years with no documented problems.

For minimum oil circuit-breakers, a value of 1 kAkHz is suggested.

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9.7.17.3 Vacuum circuit-breakers

9.7.17.3.1 Restrikes

The voltage withstand of the contact gap of a vacuum circuit-breaker rises very fast and the restrike probability is low. When a restrike occurs, the contact gap is small and the vacuum circuit-breaker is usually capable of interrupting the high-frequency restrike current, which may result in voltage escalation.

9.7.17.3.2 NSDDs

NSDDs (see 9.2.1.3) are normally associated with vacuum circuit-breakers and are generally not a concern.

9.7.17.3.3 Prestrikes

The duration of the prestrike in a vacuum circuit-breaker is short. Shock waves are not a problem for this type of circuit-breaker.

The high-frequency discharge together with contact bouncing may lead to micro contact melting, especially when the arc is burning in the anode-spot mode (this occurs with currents higher than 10 kA). The breaking of welded points during a subsequent breaking operation with a very low current can damage the contact surface and this may reduce the dielectric withstand of the contact gap. However, a subsequent breaking operation with higher current may increase the dielectric withstand to its original condition. A subsequent no-load operation may flatten the micro spot resulting in an increased dielectric strength.

9.7.17.4 SF_6 circuit-breakers

9.7.17.4.1 Restrikes

The interrupting capacity of SF_6 circuit-breakers is limited by the recovery voltage, which means that the frequency and earthing conditions (i.e. whether the circuit is effectively or non-effectively earthed) are important factors in the determination of the capability of the circuit-breaker.

The capacity of clearing the high-frequency restrike current is low for puffer circuit-breakers and even lower for self-blast (or arc assisted) circuit-breakers. This also means that the risk for voltage escalation is low. However, a restrike may cause tracking and/or puncture of the insulating material between the contacts (e.g. nozzle, sleeve, etc.).

9.7.17.4.2 Prestrikes

The duration of the prestrike is depending on the voltage per breaking unit and the closing speed. In general this duration is short. Regarding the limit of inrush current peak and frequency there is referred to 9.7.10.3.4.

9.7.17.5 Air-blast circuit-breakers

9.7.17.5.1 Restrikes

In general, the restrike probability of an air-blast circuit-breaker is higher than that of an SF_6 circuit-breaker. The flashover characteristic of air has a wider scatter than that of SF_6. Air-blast circuit-breakers can interrupt the high-frequency discharge current, which means that they have a higher probability of multiple restrikes, which may lead to voltage escalation.

9.7.17.5.2 Prestrikes

The considerations given in 9.7.17.4.2 also applies to air-blast circuit-breakers.

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9.8 Considerations of capacitive currents and recovery voltages under fault conditions

9.8.1 Voltage and current factors

Some requirements, general ratings and tests for capacitive current switching are based on switching operations in the absence of faults. The presence of a fault can increase the value of both the capacitive switching current and recovery voltage. This is recognized by IEC 62271-100 by the specification of two voltage factors when breaking in the presence of faults. These voltage factors are given in Annex S of IEC 62271-100:2008/AMD2:2017 and are 1,4 for effectively earthed systems and 1,7 for non-effectively earthed systems. Tests for these conditions are not mandatory. An example of such a fault is a circuit-breaker switching an overhead line that interrupts fault current in one phase and capacitive current in the other two phases.

The fact that the capacitive switching current increases in the presence of earth faults is recognized in Annex S of IEC 62271-100:2008/AMD2:2017, where the line and cable charging currents are multiplied by 1,25 for effectively earthed neutral systems and 1,7 for non-effectively earthed systems. The number of tests is reduced to reflect the fact that such operations do not occur frequently. The test procedure given in Annex S of IEC 62271-100:2008/AMD2:2017 is based on a class C1 test procedure (i.e. no pre-conditioning of the circuit-breaker) and is common for both class C1 and class C2 circuit-breakers.

For capacitor banks, the situation is different. No tests are required for switching of solidly earthed neutral single capacitor banks in solidly earthed neutral systems. Switching of non-effectively earthed neutral capacitor banks in solidly earthed neutral systems is not considered a normal system condition and no requirements or tests have been specified. Switching back-to-back is not considered a normal system condition and no requirements and tests have been specified.

9.8.2 Reasons for these specific tests being non-mandatory in the standard

In service, circuit-breakers have been successful in interrupting capacitive circuits under faulted conditions for a number of reasons. Principal reasons for successful operation include:

a) the probability of a fault occurring at minimum operating conditions of the circuit-breaker and its operating mechanism is extremely small;

b) the voltage factor used for single-phase tests is in excess of the service condition giving the tested circuit-breaker added margin;

c) laboratory tests are performed using a minimal voltage jump, resulting in short arcing times. This condition is more severe than the actual network condition where the voltage jump is generally higher.

9.8.3 Contribution of a capacitor bank to a fault

Consider the network situation given in Figure 126. A single line simplification is given in Figure 127. A fault has occurred on the line that is interrupted by the circuit-breaker (CB). The capacitance of the capacitor bank will modify the TRV across the circuit-breaker to a 1-cosine waveshape having a moderate rate-of-rise with a higher amplitude factor as compared to the case without the presence of the capacitor bank.

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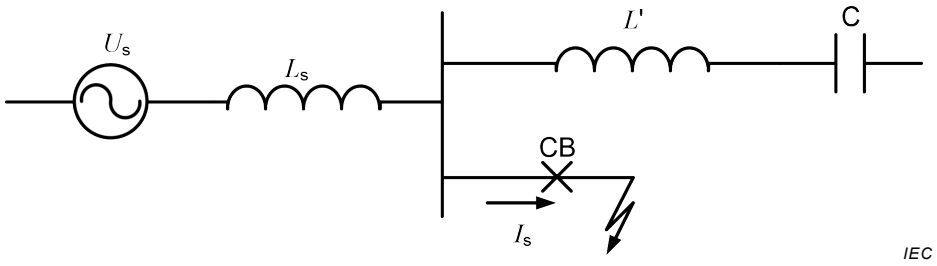

Key

U_s	Source voltage	CB	Circuit-breaker
L_s	Short-circuit inductance	I_s	Short-circuit current
L'	Busbar inductance		

Figure 127 – Fault in the vicinity of a capacitor bank

When the ITRV is negligible, the circuit-breaker will attempt to interrupt at the first available current zero following contact separation, resulting in a relatively small contact gap. As the recovery voltage increases across the gap, a re-ignition might occur and the capacitor bank will discharge into the fault through the circuit-breaker. The amplitude of the discharge current depends on the voltage across the circuit-breaker contacts at the time of re-ignition and the frequency of the discharge current is determined by the inductance between the capacitor bank and the fault location.

The high-frequency discharge current is superimposed on the fault current, which creates additional current zeros. Depending on the type of circuit-breaker (oil, air-blast, vacuum or SF_6), the high-frequency current may be interrupted causing high overvoltages. For further information refer to [128] and [129].

A similar situation may occur, when circuit-breaker CB closes into a fault. The capacitor bank discharges into the fault and depending on the magnitude of the inductance between the capacitor bank and the fault location, the discharge current can reach peak values and frequencies that exceed those given in Table 9 of IEC 62271-100:2008 (see also 9.7.12.2).

For these specific outrush cases the manufacturer should be consulted. For further treatment of this subject, see IEEE 1036 [130].

9.8.4 Switching overhead lines under faulted conditions

The voltages and currents that occur when switching a faulted transmission line are affected by the circuit parameters and the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage for switching an unfaulted transmission line as $2 \times 1{,}2 \times U_r \sqrt{(2/3)} = 2{,}4$ p.u. When switching a faulted line this value may be exceeded, as may be the rated capacitive switching current value as listed in Table 9 of IEC 62271-100:2008 (see also [131]).

When switching a no-load overhead line with a phase-to earth fault, the highest voltage occurs on the unfaulted phase, which interrupts prior to the faulted phase (see Figure 128). The highest current occurs on the last phase to interrupt when the faulted phase is the first to interrupt. The current for this case is not a sine wave but is distorted, as shown in Figure 129. Under these conditions, the voltages and currents may exceed those on which the design tests are based.

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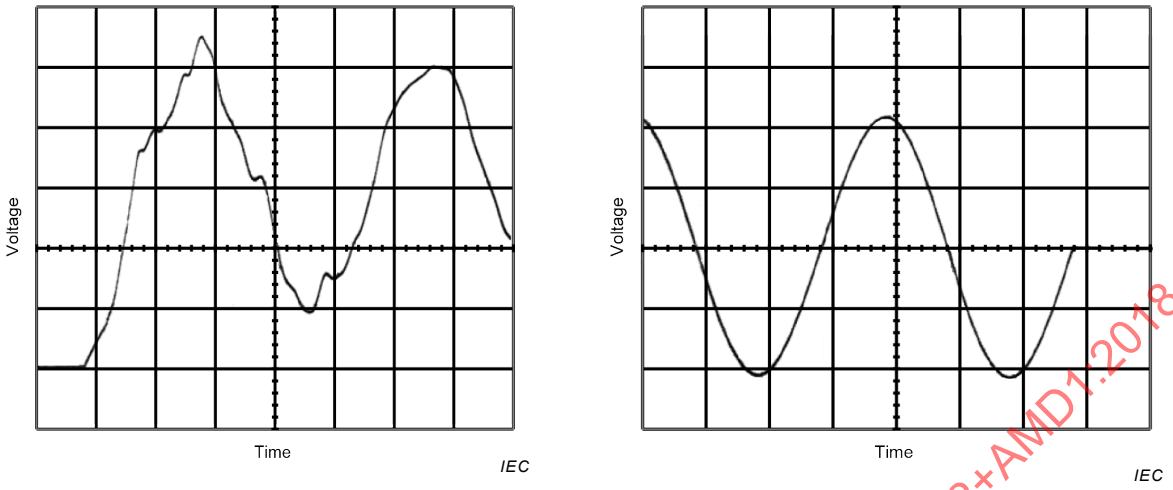
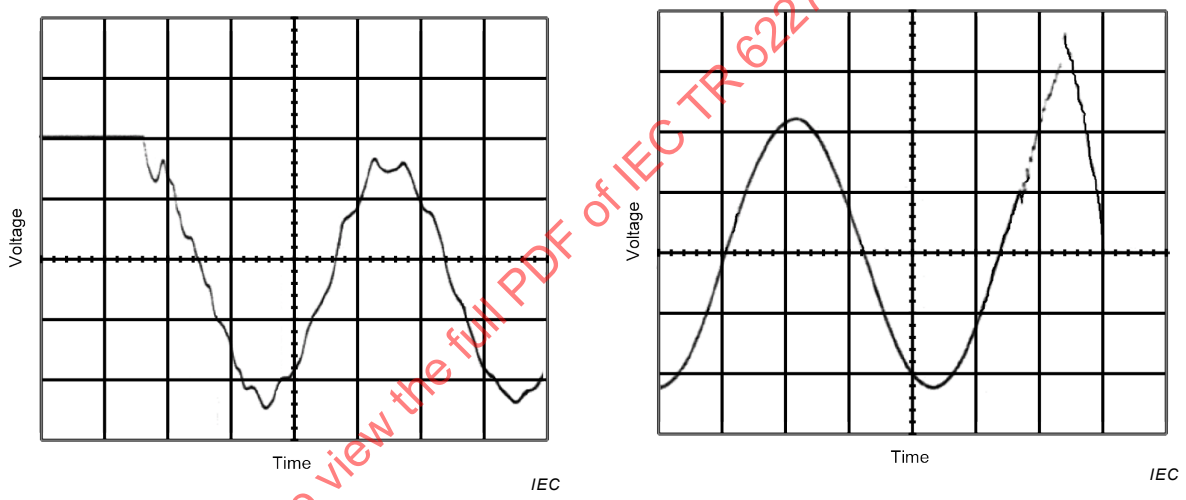


Maximum recovery voltage 2,74 × U_{max} (phase-to-earth) Maximum current 1,09 × rated current

Figure 128 – Recovery voltage and current for first-phase-to-clear when the faulted phase is the second phase-to-clear



Maximum recovery voltage 2,18 × U_{max} (phase-to-earth) Maximum current 1,77 × rated current

Figure 129 – Recovery voltage and current for last-phase-to-clear when the faulted phase is the first-phase-to-clear

For the phase-to-phase fault condition, the recovery voltage and capacitive current are less severe than for the two phase-to-earth fault condition, see also [130].

9.8.5 Switching capacitor banks under faulted conditions

9.8.5.1 General

The voltages and currents that can occur when switching a faulted capacitor bank depend upon the earthing conditions, whether the fault is to the bank neutral or to earth, and on the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage in switching an unfaulted shunt capacitor bank as 2,8 p.u. When switching a faulted bank, this value may be exceeded, as may the rated capacitive switching current value. In the following subclauses, a comparison is given between the recovery voltages and currents of a reference condition and two faulted conditions: a fault to neutral in the capacitor bank and a fault to earth in one phase.

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NOTE The factor 2,8 for the maximum recovery voltage specified in IEC 62271-100 is valid when switching a non-effectively earthed capacitor bank where the second and third phases clear 90° after the first. This is true for modern circuit-breakers. For older circuit-breakers, where the second and third phases do not clear 90° after the first, this factor is 3,0.

9.8.5.2 Reference condition

9.8.5.2.1 General

The reference condition is illustrated in Figure 130. The neutral of the source and the capacitor bank may be solidly earthed and/or non-effectively earthed. The size of the capacitor bank is such that the current is equal to the preferred single capacitor bank current.

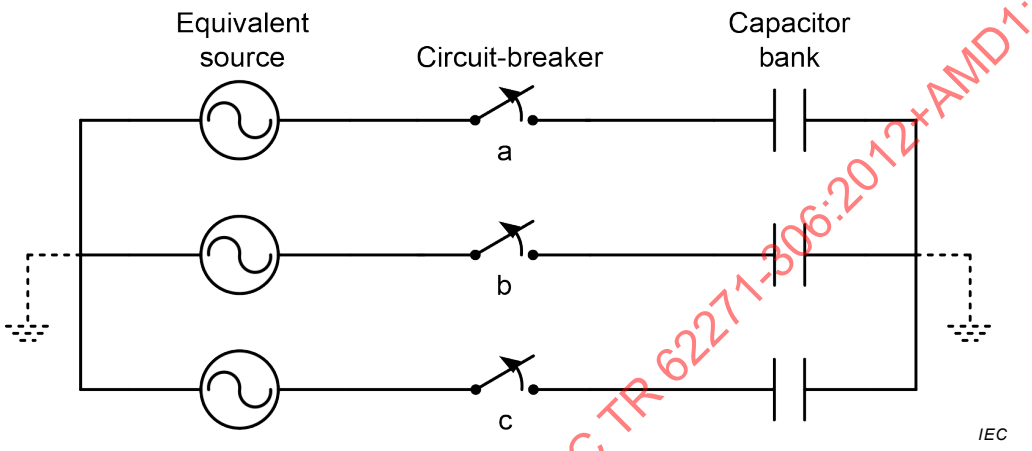

Figure 130 – Basic circuit for shunt capacitor bank switching

9.8.5.2.2 Recovery voltage

The highest recovery voltage (2,5 p.u.) is obtained in the first-pole-to-clear when either the neutral of the capacitor bank, the neutral of the source or both are non-effectively earthed and poles 2 and 3 clear 90° after the first.

The voltage across the last poles to interrupt when at least one of the neutrals (source or bank) is non-effectively earthed can reach $2 \times \sqrt{3} = 3{,}46$ p.u. However, the two phases are in series so that neither is stressed to more than 1,73 p.u.

9.8.5.2.3 Capacitor bank current

In all cases, the capacitor bank current does not exceed the preferred single capacitor bank current.

9.8.5.3 Fault to neutral in one phase (one capacitor bank phase short-circuited)

9.8.5.3.1 Recovery voltage

The highest recovery voltage ($2 \times \sqrt{3} = 3{,}46$ p.u.) is obtained when at least one neutral is non-effectively earthed and the first-pole-to-clear clears a healthy phase. This is in agreement with the voltage factor of 1,7 specified in IEC 62271-100. If the first-pole-to-clear interrupts an unfaulted phase, it is subjected to a recovery voltage of 3,46 p.u. until the second and third phases interrupt.

The highest recovery voltage in the remaining phases is 3,46 p.u., but it is shared by two poles in series.

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9.8.5.3.2 Current

The highest capacitive current is obtained in the cases described under 9.8.5.3.1 when the faulted phase is the first-pole-to-clear and is equal to 3 times that of the reference case.

9.8.5.4 Fault to earth in one phase

For systems that are effectively earthed, the highest recovery voltage is obtained when the first-pole-to-clear interrupts a non-faulted phase. In this case, the maximum recovery voltage peak will be 2,8 p.u.

The most severe case is when the source is non-effectively earthed and the bank neutral is solidly earthed. If an unfaulted pole is the first to interrupt, the current may reach $\sqrt{3}$ times that of the reference condition and the recovery voltage 3,46 p.u. The remaining poles are subjected to the same current, but upon interrupting, share the 3,46 p.u. recovery voltage. When the faulted pole is the first-pole-to-clear, the current may be 3 times the rated current value and the recovery voltage $2 \times 1{,}25 \times \frac{U_r \sqrt{2}}{\sqrt{3}}$. The second pole to interrupt will have a lower current but a higher recovery voltage of $2 \times \sqrt{3} = 3{,}46$ p.u. which will be shared with the third pole. If the faulted pole reignites, one of the unfaulted poles will then interrupt and the conditions will be as previously described when an unfaulted pole was the first to interrupt.

9.8.5.5 Other fault cases

For phase-to-phase earth faults, or phase-to-phase non-effectively earthed faults, with the source solidly earthed and the bank neutral non-effectively earthed, recovery voltages and currents are no more severe than for the standard unfaulted condition.

9.8.6 Switching cables under faulted conditions

The normal frequency capacitive currents and recovery voltages on a faulted cable circuit will be the same as for a solidly earthed capacitor bank under faulted conditions.

9.8.7 Examples of application alternatives

Application options available are:

a) Use a circuit-breaker of a higher rating in those cases of earth faults on non-effectively earthed systems where the recovery voltage and current, or both, exceed the requirements of IEC 62271-100.

b) Reduce the capacitance of the existing capacitor bank size so that the current under faulted conditions does not exceed the rated capacitive switching current of the circuit-breaker.

c) Use a high-speed switch to earth the source or capacitor bank neutral before switching the capacitor bank under faulted conditions.

d) Use a Δ configuration for the capacitor bank instead of a non-effectively earthed Y.

9.9 Explanatory notes regarding capacitive current switching tests

9.9.1 General

Subclause 6.111 of IEC 62271-100:2008 deals with capacitive current switching tests. In the 1st edition of this standard, a new test procedure has been introduced for the two classes of capacitive current switching that deserve some explanation.

9.9.2 Restrike performance

See 9.7.6.

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9.9.3 Test programme

In defining the test programme for these two classes, the following elements have been taken into account:

– the average number of operations per year carried out by circuit-breakers switching capacitive loads;

– the ability to reduce the number of tests by performing an increased number of switching operations at the minimum arcing time, usually the most difficult capacitive switching operation for circuit-breakers, thus keeping a high level of reliability;

– the recommendations of CIGRE working group A3.04. The expected restrike probability is exclusively related to the type tests.

The proposed number of tests may be questioned because of different assumptions for probability calculations. Nevertheless, these values represent a good compromise (which is the role of the standard where conflicting views exist), reflecting the needs of users (in response to market demand) and above all they avoid unrealistic demands. These tests are not reliability tests but type tests to demonstrate a satisfactory capacitive current switching capability of the equipment in service.

9.9.4 Characteristics of supply circuit

The paragraph concerning factor k_c/k_{pp} (from earlier versions of the standard) where k_c is the voltage factor as described in 9.6 and k_{pp} is the first-pole-to-clear factor has been deleted because there is neither use nor need for testing.

The variation of the power frequency voltage has been chosen as 5 % for test-duty 2 (LC2, CC2 and BC2) and 2 % for test-duty 1 (LC1, CC1 and BC1). These values are a compromise, taking limitations of testing laboratories into account. Considering the type test as a whole, because of the different stresses in the individual test-duties, any undue reduction of the electric stress during the tests is avoided. The actual values for the power frequency voltage variation (depending on the short-circuit power of the system and the capacitive load) is in the range of 1 % to 2 %.

9.9.5 Common features for class C1 and class C2 test-duties

The interval after final arc extinction, in which the voltage decay should not exceed 10 %, has been changed from 100 ms to 300 ms based on service conditions.

9.9.6 Specific feature for class C2 test-duties

Performing these capacitive current switching tests for class C2 equipment on a preconditioned circuit-breaker is, on the one hand, a recommendation of CIGRE working group A3.04; on the other hand, it draws closer to the real conditions of service, without prejudice as to whether this preconditioning improves the capacitive current switching performance of the circuit-breaker or not.

Close-open operations may be performed with no-load closing operations. In any case, the complete sequence should be tested in order to test the circuit-breaker during opening in a dynamic condition, i.e. during the motion of the fluid (if any) caused by the previous closing operation.

9.9.7 Class C1 and C2 test duties

The tolerance of the testing current values for test-duty 1 (LC1, CC1 and BC1) was increased from the old range 20 % to 40 % to the new range 10 % to 40 % in order to give more freedom during testing for combined test-duties for different applications.

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The proposed test sequences have been tested in a laboratory (particularly the adjustment of the minimum arcing time by steps of 6°) and are well adapted to the philosophy of the tests.

Performing some tests at rated pressure is a more pragmatic approach to the notion of type testing, knowing that the circuit-breaker does not always stand under the worst functioning conditions.

9.9.8 Single-phase and three-phase line- and cable-charging current tests

In test-duty 2 of single-phase line-charging and cable-charging tests (LC2 and CC2), the tests are split into open operations and close-open operating cycles to follow more or less the actual service conditions. However, for practical reasons, owing to the small number of tests, in three-phase tests in test-duty 2 (LC2 and CC2), close-open operating cycles are performed exclusively.

9.9.9 Three-phase and single-phase line, cable and capacitor bank switching tests

Close-open operating cycles are important for capacitor bank switching because of the effect of inrush current. Close-open operating cycles are not significant for line- or cable-switching applications, therefore for line- and cable-switching tests, only a small number of close-open operations are requested (closing may be performed as a no-load operation).

A rough parity of the number of three-phase and single-phase tests has been maintained.

The mandatory order for capacitor bank switching tests (single- or back-to-back) is due to the necessity to introduce the effect of inrush current at the beginning of the tests.

9.9.10 Three-phase and single-phase capacitor bank switching tests

Because of the large number of operations in actual service compared with the limited number of operations during type testing, a high number (80 or 120 respectively) of close-open operating cycles is carried out in capacitor bank tests to simulate the wear in service even if the close-open operation is not the normal switching sequence.

For capacitor bank switching tests test-duty 1 (BC1) also needs to be performed, even if the actual service switching duty is always at 100 % nominal current, for the following reasons:

– the tests at 10 % to 40 % nominal current cover an increased number of actual currents;
– knowledge of the capacitive current switching performance is improved.

10 Gas tightness

10.1 Specification

From a maintenance or environmental approach, it would be advisable to specify a "leakage-free" or "fully-tight" equipment. Unfortunately it is not realistic for at least two reasons:

– perfect tightness does not exist: every wall allows gas to get through (the flow of SF_6 gas through a cast aluminium wall has been measured);
– tightness is measured by the leakage rate, and the smaller the specified leakage rate, the more difficult to measure it, in particular to cover decades of years.

As a result, specification should be based on the actual need, which depends on the system class and on the use. Since the standard was addressed to any type of high-voltage circuit-breaker, it was necessary to classify the different pressure systems. At the time of the first issue of tightness specification for high-voltage circuit-breakers, the main concern was to link the tightness to the maintenance schedule.

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"Controlled pressure systems" are automatically replenished. This class applies mainly to air-blast circuit-breakers and pneumatic operating mechanisms. For external tightness of compressed air systems, there is no ecological question and the specification for tightness is only linked to the compressor plant performance. Controlled SF_6 gas pressure systems are not recommended for SF_6 switchgear and controlgear.

"Closed pressure systems" are those which are replenished only periodically, for instance during maintenance. Tightness can be specified from an ecological approach. By specifying the annual gas leakage rate in %/year, easy calculation of the amount of gas escaped per year is possible. Subclause 5.15.2 of IEC 62271-1:2007 specifies tightness for SF_6 with values of 1 % and 0,5 %/year. The original value of 3 %/year specified in Annex EE of the 4th edition of IEC 60056 published in 1987 is no longer specified, because service records show that 1 %/year can usually be met.

"Sealed pressure systems" are designed not to need replenishment during their whole expected service life. The tightness of gas insulated switchgear and controlgear should be demonstrated accordingly, to show that the minimum functional density will not be attained before the expected end of life.

10.2 Testing

~~The leakages rates used in IEC 62271-1 to specify the tightness characteristic of sealed and closed pressure systems for gas at ambient, high and low temperatures can be measured directly with a fairly good accuracy. To check these characteristics, the method generally used during type tests is to measure the leakage rate of the complete assembled circuit-breaker using a cumulative test method as mentioned in 6.8 of IEC 62271-1:2007. In case that a measurement of the complete assembled circuit-breaker is not possible, the leakage measurement may be performed on parts, components or subassemblies. In such cases, the leakage rate of the total gas system is to be determined by summation of the component leakage rates as described in Annex E of IEC 62271-1:2007.~~

~~During routine tests, a cumulative test method is preferred but such a test may be impractical in industrial environments. For routine tests, as mentioned in 7.4 of IEC 62271-1:2007, a leak detection using a sniffing device may be used instead of using a cumulative test method. IEC 62271-1 specifies a minimum sensitivity of sniffing device of 10^{-8} Pa m^3/s.~~

~~This required minimum sensitivity corresponds to a single leak of less than 0,04 %/year for a typical 245 kV SF_6 circuit-breaker having an internal volume of 200 litre filled at a pressure of 0,5 MPa(abs) and if the moving speed of the sniffer detector around sealing joints is relatively slow, for instance, not exceeding 1 cm/s. Obviously, if the filling pressure, volume or moving speed of the leak detector are different then the leakage rate sensitivity changes. Each case shall be evaluated individually.~~

~~If a leak is detected when using a sniffing device, then the leakage rate cannot be quantified since this device is only giving an alert if a leak is detected. As mentioned in 7.4 of IEC 62271-1:2007, in case of a detection of a leak with the sniffing device, the leakage rate should be then quantified by repeating the tightness test by using a cumulative test method. Only cumulative test method can be used to quantify a leakage rate.~~

10.2.1 General

To check the tightness characteristics for closed and sealed pressure systems for gas, the method generally used during type tests is to measure the leakage rate of the complete assembled circuit-breaker using a cumulative test method as mentioned in 6.8 of IEC 62271-1:2007. In case a measurement of the complete assembled circuit-breaker is not possible, the leakage measurement may be performed on parts, components or subassemblies. In such cases, the leakage rate of the total gas system is to be determined by summation of the component leakage rates as described in Figure 131.

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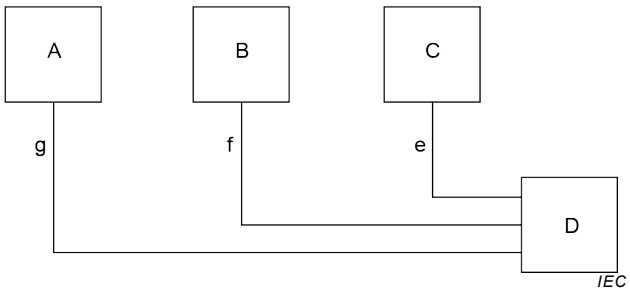
Table 46 provides an overview of the different leakage detection methods and their sensitivity.



Example:

Gas-insulated metal-enclosed switchgear, single-phase encapsulated circuit-breaker compartments of the three phases connected to the same gas-system.

Leakage rate of the system:

Compartment A	9×10^{-6} Pa × m^3/s
Compartment B	9×10^{-6} Pa × m^3/s
Compartment C	9×10^{-6} Pa × m^3/s
Control box D (including valves, gauges, monitoring devices)	$2{,}3 \times 10^{-6}$ Pa × m^3/s
Piping e	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Piping f	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Piping g	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Complete system	$29{,}9 \times 10^{-6}$ Pa × m^3/s

Filling pressure	p_{re}: 700 kPa (relative)
Alarm pressure	p_{ae}: 640 kPa (relative)
Total internal volume	270 dm^3

$$F_{rel} = \frac{29{,}9 \times 10^{-6} \times 60 \times 60 \times 24 \times 365}{700 \times 10^{3} \times 270 \times 10^{-3}} = 0{,}5\ \%\ \text{per year}$$

$$t_r = \frac{\ln(p_{re} / p_{ae})}{\ln(1 + F_{rel}/100)} = \frac{\ln(700/640)}{\ln(1 + 0{,}005)} \approx 18\ \text{years}$$

NOTE F_{rel} is the leakage rate and t_r is the time between replenishment.

Figure 131 – Example of a tightness coordination chart, TC, for closed pressure systems

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Table 46 – Sensitivity and applicability of different leak-detection methods for tightness tests

Measurement methodology	Sensitivity of leakage rate (best case)	Test result	Comments	Suitable for leakage rate determination		Suitable for major leaks detection
				High-voltage equipment	Medium-voltage equipment	
Vacuum/pressure increase test	100 P/h (approximately 10 kg/year of SF_6)	Qualitative	Normally used to verity equipment integrity before SF_6 filling	No	No	Yes if the cumulative test method is used
Infrared camera using BAGI (Backscatter/ Absorption Gas Imaging)	1 kg/year of SF_6 at a distance range of 35 m	Qualitative	Suitable for remotely determining the approximate location of major leaks	No	No	Yes
Bubble test with soap or special fluids	1 kg/year of SF_6	Qualitative	Simple and useful for determining the exact location of major leaks. Can also be used for other gases	No	No	Yes and for major leak localisation
Density monitoring (pressure drop)	600 g/year of SF_6 for an observation time of 1 year	Quantitative	Suitable for long term trend analysis of leakage detection or for equipment integrity test. Can also be used for other gases	No	No	Yes if the observation time is long enough
Infrared absorption spectroscopy	60 mg/year of SF_6 or 3 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type, routine and commissioning test. Not influenced by other common gases and water	Yes if the cumulative test method is used. Can be also used for minor leak localisation	Hardly suitable	Yes if the cumulative test method is used. Can also be used for major leak localisation
Negative ion capture detector (using corona discharge)	20 mg/year of SF_6 or 1 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type test, routine test, commissioning test and maintenance. Reading may be influenced by other gases and moisture content.	Yes if the cumulative test method is used Can be also used for minor leak localisation	Yes if the cumulative test method is used Hardly suitable for minor leak localisation	Yes if the cumulative test method is used. Can also be used for major leak localisation

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Measurement methodology	Sensitivity of leakage rate (best case)	Test result	Comments	Suitable for leakage rate determination		Suitable for major leaks detection
				High-voltage equipment	Medium-voltage equipment	
Electron capture leak detector (using radioactive emitter)	2 mg/year of SF_6 or 0,1 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type test, routine test, commissioning test and maintenance. Reading may be influenced by other gases and moisture content.	Yes if the cumulative test method is used Can be also used for minor leaks localisation	Yes if the cumulative test method is used Hardly suitable for minor leak localisation	Yes if the cumulative test method is used. Can also be used for major leak localisation
Helium mass spectrometer	2 mg/year of SF_6 if checked by a calibration source	Quantitative	Type test and routine test. Can only be used with the cumulative test method	Yes Can also be used on equipment components	Yes	Yes. Cannot be used for leak localisation.
Photo-acoustic infrared spectroscopy	0,2 mg/year of SF_6 or 0,01 ppm_v	Quantitative	Type test and routine test. Can only be used with the cumulative test method	Yes	Yes	Yes. Cannot be used for leak localisation

See CIGRE Technical Brochure 430 [144] for more detailed information.

NOTE 1 "minor leak" qualitatively indicates a leak having a leakage rate "L" in the order of the permissible leakage rate L_p ($L \approx L_p$).

NOTE 2 "major leak" qualitatively describes leaks having at least one order of magnitude higher than the permissible leakage rate L_p ($L >> L_p$).

NOTE 3 The "cumulative test method" can also be called "integral test".

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During routine tests, a cumulative test method is preferred but such a test may be impractical in industrial environments. For routine tests, as mentioned in 7.5 of IEC 62271-1:2007, a leak detection using a sniffing device may be used instead of using a cumulative test method. IEC 62271-1 specifies a minimum sensitivity of sniffing device of 10^{-8} Pa m^3/s.

This required minimum sensitivity corresponds to a single leak of less than 0,04 %/year for a typical 245 kV SF_6 circuit-breaker having an internal volume of 200 l filled at an absolute pressure of 0,5 MPa and if the moving speed of the sniffer detector around sealing joints is relatively slow, for instance, not exceeding 1 cm/s. Obviously, if the filling pressure, volume or moving speed of the leak detector are different, then the leakage rate sensitivity changes. Each case should be evaluated individually.

If a leak is detected when using a sniffing device, then the leakage rate cannot be quantified since this device is only giving an alert if a leak is detected. As mentioned in 7.5 of IEC 62271-1:2007, in the case of a detection of a leak with the sniffing device, the leakage rate should be then quantified by repeating the tightness test by using a cumulative test method. Only the cumulative test method can be used to quantify a leakage rate.

10.2.2 Cumulative test method and calibration procedure for type tests on closed pressure systems

10.2.2.1 Description of the cumulative test method

10.2.2.1.1 General

The cumulative test method is the recommended test method for the determination of gas leaks that can occur in closed pressure systems such as for SF_6 circuit-breakers. This method consists of erecting a relatively gastight enclosure (e.g. plastic tent or similar enclosure, see NOTE 2) around the complete test object or by erecting several smaller relatively gastight enclosures (plastic tents or similar enclosures, see NOTE 2) around each part, component or subassembly. The circuit-breaker should be filled as in service, at its rated filling pressure. The measurement consists of measuring the tracer gas content increase (e.g. SF_6) within the enclosure(s) during a sufficient time period. With today's available measuring equipment, a time period of 1 h is generally sufficient. If an enclosure(s) of small volume are used, then this measuring period can be reduced. For very large enclosures, this time period may need to be increased. As a rule of thumb, the time period should be long enough that the calculated tracer gas content in the enclosure for the maximum permissible leakage rate should be at least 3 times the minimum resolution of the measuring equipment. From the tracer gas content increase within the enclosure(s) during a given time period, then the annual leakage rate can be calculated. This method is considered to be very accurate and has been widely used during type tests on circuit-breakers at ambient, low and high temperatures.

The tightness of the enclosure should be demonstrated for the duration of the measuring time period. This can be done at the same time as the calibration of the enclosure.

The cumulative test method steps can be summarized as follows:

– install a relatively gastight enclosure(s) over the entire test object or over parts, components or subassemblies;
– pressurize the circuit-breaker at its rated filling pressure with its specified gas or gas mixture, pure SF_6 instead of gas mixture, or with a tracer gas such as helium;
– determine the enclosure(s) volume V_m (m^3);
– measure the tracer gas concentration C_0 (p.p.m_v. or cc/m^3) within the enclosure(s) at reference time t_0 (s);
– measure the final gas concentration C_1 (p.p.m_v. or cc/m^3) within the enclosure(s) at time t_1 (s);
– calculate the leak rate using the following equation:

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$$F = V_m \times P_e \times \frac{\Delta C}{\Delta t} \times 10^{-6}$$

where

F is the leakage rate in m^3Pa/s;

V_m is the enclosure gas volume in m^3;

P_e is the atmospheric pressure in Pa;

ΔC is the tracer gas concentration increase (C_1-C_0) in $p.p.m_v$. during the measuring time period;

Δt is the measuring time period in seconds.

NOTE 1 A fan installed inside the enclosure helps to get an homogeneous gas tracer content within the enclosure. This recommendation applies mainly to large enclosure used around a complete circuit-breaker.

NOTE 2 The enclosure does not need to be as tight as a pressure vessel since the pressure within the enclosure is equal to the atmospheric pressure outside the enclosure. Thus, the air inside the enclosure (including traces of the tracer gas) is not forced to escape from the enclosure nor the air outside the enclosure is forced to enter within the enclosure.

10.2.2.1.2 Sensitivity, accuracy and calibration

The accuracy of the cumulative method depends on three main factors: sensitivity of the tracer gas detector, volume of enclosure and duration of the measuring period. For example, a minimum threshold sensitivity and resolution of 0,01 $p.p.m_v$ is recommended when SF_6 is used as the tracer gas. Such gas detectors are commercially available.

NOTE 1 Infrared photo acoustic spectroscopy method is widely used to measure SF_6 concentration.

The uncertainty concerning the enclosure volume can be considerably reduced by using a suitable calibration technique. The recommended calibration procedure consists of injecting a known quantity of tracer gas into the enclosure.

NOTE 2 Experience gained from measurements showed that the estimation error of the enclosure volume is less than 10 %.

The enclosure volume (V_m in m^3) should be determined by calibration. A small tracer gas quantity, $V_{injected}$ (cm^3), is injected into the enclosure volume V_m. The injected gas quantity should be in the same order of magnitude than the gas quantity corresponding to the maximum allowable leakage rate.

The tracer gas concentration C_0 ($p.p.m_v$.) is measured before and after injection by the gas detector. The enclosure volume is then calculated as follows:

$$V_m = V_{injected} / \Delta C_0$$

This procedure should be repeated twice in order to get a better evaluation of the enclosure volume. The average value of the two measurements should be used as the enclosure volume V_m.

10.2.2.1.3 Test set-up and test procedure

For type test, the test object should be pressurized at its nominal filling pressure with its assigned gas mixture (if applicable). Nevertheless, industrial environments and local safety rules may force a deviation from service conditions. For instance, some tests could be performed using pure SF_6 instead of the assigned gas mixture, or other tracer gases such as helium may be used. All deviations from service conditions have to be carefully evaluated to see their impacts on the measurement sensitivity.

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In order to have an effective test set-up, the following is recommended:

– the enclosure volume should be as small as possible in order to obtain a better sensitivity of the tracer gas concentration within the enclosure;

– a fan should be installed inside the enclosure in order to provide an homogeneous gas content within the enclosure;

– the gas detector device should be able to measure accurately 1/3 of the maximum allowable leakage rate.

For low and high ambient temperature tests, the following additional recommendations are given:

– Thermocouples should be installed at different heights along the test object inside the enclosure. The ambient temperature to be reached during test is the temperature measured inside the enclosure.

– Controllable electric heaters should be installed inside the enclosure in order to help to fulfill the temperature increase of 10 K/h specified during the low temperature test sequence. For the high-temperature test, the temperature decrease of 10 K/h within the enclosure can be met by making a temporary opening of the enclosure since the leak rate determination is not required during this test part of the test. Required temperature variations have to be met within the enclosure.

NOTE 1 One way to obtain the desired temperature inside the enclosure is to lower the ambient temperature in the climatic room such that it is slightly lower than the required temperature for low temperature test or slightly higher for high temperature test.

The maximum leakage rate (m^3Pa/s) based on acceptance leakage rate limit of 0,5 % per year (see 5.15.2 of IEC 62271-1:2007) is calculated as follows:

$$F = \frac{0{,}005 \times V_{to} \times \left(P_{to} \times \frac{273 + T_{test}}{273\,\mathrm{K} + 20} - 101{,}3 \times 10^3 \right) \times \gamma}{365 \times 24 \times 60 \times 60}$$

where

F is the leakage rate in m^3Pa/s;

V_{to} is the circuit-breaker gas volume in m^3;

P_{to} is the circuit-breaker absolute filling pressure at T = 20 °C in Pa (see NOTE 2);

T_{test} is the ambient temperature during leakage measurement in °C;

γ is the percentage of tracer gas in the circuit-breaker gas volume.

NOTE 2 It is assumed only gas exceeding the atmospheric pressure can escape from the breaker. Other leakage mechanisms such as atomic migration through solid materials are considered to be negligible. The pressure correction for the test temperature is applied to the absolute gas pressure.

Finally, the leakage rate per year (%/year) can also be directly expressed by the following equation:

$$F_{year} = \frac{P_{atm} \times 365 \times 24 \times 60 \times 60 \times V_m \times \Delta C \times 10^{-6}}{V_{to} \times \left(P_{to} \times \frac{273 + T_{test}}{273 + 20} - 101{,}3 \times 10^3 \right) \times \gamma \times t}$$

where

F_{year} is the leakage rate in %/year;

P_{atm} is the atmospheric pressure during measurement (a default value of 101,3 kPa can be used);

ΔC is the tracer gas concentration increase (C_1-C_0) in p.p.m_v. during the measuring time period;

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V_m is the enclosure gas volume in m^3;

V_{to} is the circuit-breaker gas volume in m^3;

P_{to} is the circuit-breaker absolute gas pressure in Pa;

T_{test} is the ambient temperature during leakage measurement in °C;

γ is the percentage of tracer gas in the circuit-breaker gas volume;

t is the measuring time period in s.

10.2.2.1.4 Example: leakage rate measurement of a circuit breaker during low temperature test

The test object is filled with its gas mixture SF_6/N_2 at nominal filling pressure and ambient temperature. A relatively gastight enclosure is installed over the circuit-breaker. A calibration by injection method is performed in order to evaluate the enclosure volume.

Table 47 shows the results of a calibration of the enclosure.

Table 47 – Results of a calibration procedure prior to a low temperature test

Description	Quantity of SF_6 gas injected within the enclosure	Concentration of SF_6 gas measured within the enclosure	Variation of concentration of SF_6 gas within the enclosure	Calculated volume V_m
	(cm^3)	(p.p.m_v)	(p.p.m_v)	(m^3)
Before test	-	0,05	-	
First Injection	10	1,03	0,98	10,20
Second injection	10	2,06	1,03	9,71

Thus, the enclosure volume is considered to be the average value of the volumes determined with both injections e.g. 9,96 m^3.

Then, if a circuit-breaker having an internal volume of 0,375 m^3 filled with a gas mixture consisting of SF_6 and N_2 at an absolute pressure of 1,0 MPa and the SF_6/N_2 mixture is 30 % SF_6 and 70 % N_2, the 0,5 %/year permissible maximum leakage rate at ambient temperature (20 °C) corresponds to a maximum concentration of tracer gas within the enclosure during a measuring period of 1,0 h of:

$$\Delta C = \frac{F_{year} \times V_{to} \times \left(P_{to} \times \frac{273 + T_{test}}{273 + 20} - 101{,}3 \times 10^3 \right) \times \gamma \times t}{P_{atm} \times 365 \times 24 \times 60 \times 60 \times V_m \times 10^{-6}}$$

$$\Delta C = \frac{0{,}005 \times 0{,}375 \times \left(1 \times 10^6 \times \frac{273 + 20}{273 + 20} - 101{,}3 \times 10^3 \right) \times 0{,}3 \times 3600}{101{,}3 \times 10^3 \times 365 \times 24 \times 60 \times 60 \times 9{,}96 \times 10^{-6}} = 0{,}057 \text{ p.p.m}_v.$$

Accordingly, if the same enclosure is used for the low-temperature test, the maximum allowable gas concentration increase for a measuring time period of 1 h at an ambient temperature of −25 °C will be:

$$3 \times F_{year} = 3 \times 0{,}057 \times \left(1 \times 10^6 \times \frac{273 - 25}{273 + 20} - 101{,}3 \times 10^3 \right) = 0{,}127 \text{ p.p.m}_v.$$

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and accordingly at −50 °C

$$6 \times F_{year} = 6 \times 0{,}057 \times \left(1 \times 10^6 \times \frac{273 - 50}{273 + 20} - 101{,}3 \times 10^3 \right) = 0{,}226 \text{ p.p.m}_v.$$

It should be noted that the relative leakage rate of N_2 cannot be measured using this method. It may be higher than the value obtained by relating the leakage rate of N_2 to that of SF_6, i.e. $\Delta C(N_2) \neq \Delta C(SF_6) \times 0{,}7 / 0{,}3$.

10.2.2.2 Time between replenishment

With a given leakage rate F in %/year, the time between replenishments t_r is obtained from the following equation. t_r is the number of periods on which the leakage rate is defined (in this case 1 year):

$$t_r = \frac{\ln(p_{re} / p_{ae})}{\ln(1 + F/100)}$$

where

t_r is the time between replenishments;

p_{re} is the relative filling pressure in Pa;

p_{ae} is the relative alarm pressure in Pa;

F is the measured leakage rate in %/year.

10.3 Cumulative test method and calibration procedure for type tests on closed pressure systems

10.3.1 Description of the cumulative test method

The cumulative test method is the recommended test method for the determination of gas leaks which can occur in closed pressure systems such as for SF_6 circuit-breakers. This method consists of erecting a relatively gastight enclosure (e.g. plastic tent or similar enclosure, see NOTE 2) around the complete test object or by erecting several smaller relatively gastight enclosures (plastic tents or similar enclosures, see NOTE 2) around each part, components or subassemblies. The circuit-breaker should be filled as in service, at its rated filling pressure. The measurement consists of measuring the tracer gas content increase (e.g. SF_6) within the enclosure(s) during a sufficient time period. With the today's available measuring equipment, a time period of 1 h is generally sufficient. If enclosure(s) of small volume are used, then this measuring period can be reduced. For very large enclosures, this time period may need to be increased. As a rule of thumb, the time period should be long enough that the calculated tracer gas content in the enclosure for the maximum permissible leakage rate should be at least 3 times the minimum resolution of the measuring equipment. From the tracer gas content increase within the enclosure(s) during a given time period, then the annual leakage rate can be calculated. This method is considered to be very accurate and has been widely used during type tests on circuit-breakers at ambient, low and high temperatures.

The cumulative test method steps can be summarized as follows:

– install a relatively gastight enclosure(s) over the entire test object or over parts, components or subassemblies;

– pressurize the circuit-breaker at its rated filling pressure with its specified gas or gas mixture, pure SF_6 instead of gas mixture, or with a tracer gas such as helium;

– determine the enclosure(s) volume V_m (m^3);

– measure the tracer gas concentration C_0 (p.p.m_v. or cc/m^3) within the enclosure(s) at time reference time t_0 (s);

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– measure the final gas concentration C_1 (p.p.m$_v$. or cc/m^3) within the enclosure(s) at time t_1 (s);
– calculate the leak rate using the following equation:

$$F = V_m \times P_e \times \frac{\Delta C}{\Delta t} \times 10^{-6}$$

where

F is the leakage rate, in m^{3}Pa/s;

V_m is the enclosure gas volume, in m^3;

P_e is the atmospheric pressure, in Pa;

ΔC is the tracer gas concentration increase (C_1-C_0), in p.p.m$_v$. during the measuring time period;

Δt is the measuring time period, in s.

NOTE 1 A fan installed inside the enclosure helps to get an homogeneous gas tracer content within the enclosure. This applies mainly to large enclosures used around a complete circuit-breaker.

NOTE 2 The enclosure does not need to be as tight as a pressure vessel since the pressure within the enclosure is equal to the atmospheric pressure outside the enclosure. Thus, the air inside the enclosure (including traces of the tracer gas) is not forced to escape from the enclosure nor the air outside the enclosure is forced to enter within the enclosure.

10.3.2 Sensitivity, accuracy and calibration

The accuracy of the cumulative method depends on three main factors: sensitivity of the tracer gas detector, volume of enclosure and duration of the measuring period. For example, a minimum threshold sensitivity and resolution of 0,01 p.p.m$_v$. is recommended when SF_6 is used as the tracer gas. Such gas detectors are commercially available.

NOTE 1 Infrared photo acoustic spectroscopy method is widely used to measure SF_6 concentration.

The uncertainty concerning the enclosure volume can be considerably reduced by using a suitable calibration technique. The recommended calibration procedure consists of injecting a known quantity of tracer gas into the enclosure.

NOTE 2 Experience gained from measurements showed that the estimation error of the enclosure volume is less than 10 %.

The enclosure volume (V_m) should be determined by calibration. A small tracer gas quantity, $V_{injected}$ (cm^3), is injected into the enclosure volume V_m. The injected gas quantity should be in the same order of magnitude than the gas quantity corresponding to the maximum allowable leakage rate.

The tracer gas concentration C_{ppm} (p.p.m$_v$.) has to be measured before and after injection by the gas detector. The enclosure volume is then calculated as follows:

$$V_m(m^3) = V_{injected}(cm^3) / \Delta C_{ppm}$$

This procedure should be repeated twice in order to get a better evaluation of the enclosure volume. The average value of the two measurements should be used as the enclosure volume V_m.

10.3.3 Test set-up and test procedure

For type test, the test object should be pressurized at its nominal filling pressure with its assigned gas mixture (if applicable). Nevertheless, industrial environments and safety rules may require a deviation from service conditions. For instance, some tests could be performed

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using pure SF_6 instead of the assigned gas mixture or other tracer gas such as helium may be used. The filling pressure may also be reduced. Nevertheless, for type tests it is not recommended to use a lower filling pressure since the applied forces on the circuit-breaker seals are reduced. All deviations from service conditions have to be carefully evaluated to see their impacts on the measurement sensitivity.

In order to have an effective test set-up, the following is recommended:

– the enclosure volume shall be as small as possible in order to obtain a better sensitivity of the tracer gas concentration within the enclosure;
– a fan should be installed inside the enclosure in order to provide an homogeneous gas content within the enclosure;
– the gas detector device should be able to measure accurately half of the maximum allowable leakage rate.

For low and high ambient temperature tests, the following additional recommendations are given:

– thermocouples should be installed at different heights along the test object inside the enclosure. The ambient temperature to be reached during test is the temperature measured inside the enclosure;
– controllable electric heaters should be installed inside the enclosure in order to help to fulfil the temperature increase of 10°C/h specified during the low temperature test sequence. For the high temperature test, the temperature decrease of 10°C/h within the enclosure can be met by making a temporary opening of the enclosure since the leak rate determination is not required during this test part of the test. Required temperature variations have to be met within the enclosure.

NOTE It may be necessary to use an ambient temperature in the climatic room slightly lower than the required temperature for low temperature test or slightly higher for high temperature test in order to get the required test temperature inside the enclosure.

The maximum leakage rate (m^3Pa/s) based on acceptance leakage rate limit of 0,5 % per year (see 5.15.2 of IEC 62271-1:2007) is calculated as follow:

$$F = \frac{0{,}5\,\% \times V_{to} \times P_{to} \times \left(\left(273\,\mathrm{K} + T_{test}\right) \Big/ \left(273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}\right) \right) \times \gamma}{365\ \text{days} \times 24\ \text{hours} \times 60\ \text{minutes} \times 60\ \text{seconds}}$$

where

F is the leakage rate, in m^3Pa/s;
V_{to} is the circuit-breaker gas volume, in m^3;
P_{to} is the rated filling pressure at T = 20 °C, in Pa absolute;
T_{test} is the ambient temperature during leakage measurement, in °C;
γ is the percentage of tracer gas in the circuit-breaker gas volume.

Finally, the leakage rate per year (%/year) can also be directly expressed by the following equation:

$$F(\%) = \frac{P_{atm} \times 365\ \text{days} \times 24\ \text{hours} \times \Delta C \times V_m}{V_{to} \times P_{to} \times \left(\left(273\,\mathrm{K} + T_{test}\right) \Big/ \left(273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}\right) \right) \times \gamma \times t}$$

where

$F(\%)$ is the leakage rate, in %/year;

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P_{atm} is the atmospheric pressure during measurement (a default value of 101,3 kPa can be used);

ΔC is the tracer gas concentration increase (C_1-C_0), in p.p.m_v. during the measuring time period;

V_m is the enclosure gas volume, in m^3;

T_{test} is the ambient temperature during leakage measurement, in °C;

γ is the percentage of tracer gas in the circuit-breaker gas volume;

t is the measuring time period.

10.3.4 Example: leakage rate measurement of a circuit-breaker during low temperature test

The test object is filled with its gas mixture SF_6/N_2 at nominal filling pressure and ambient temperature. A relatively gastight enclosure is installed over the circuit-breaker. A calibration by injection method is performed in order to evaluate the enclosure volume.

Table 16 shows the results of a calibration of the enclosure.

Table 16 – Results of the calibration of the enclosure

Description	Quantity of SF_6 gas injected within the enclosure	Concentration of SF_6 gas measured within the enclosure	Variation of concentration of SF_6 gas within the enclosure	Calculated volume V_m
	(cm^3)	(p.p.m_v)	(p.p.m_v)	(m^3)
Before test	-	0,05	-	
First injection	10	1,03	0,98	10,20
Second injection	10	2,06	1,03	9,71

Thus, the enclosure volume is considered to be the average value of the volumes determined with both injections e.g. 9,96 m^3.

Then, if a circuit-breaker having an internal volume of 0,375 m^3 filled with a gas mixture consisting of SF_6 and N_2 at a pressure of 1,0 MPa(abs) and the SF_6/N_2 mixture is 30 % SF_6 and 70 % N_2, the 0,5 %/year permissible maximum leakage rate at ambient temperature (20 °C) corresponds to a maximum concentration of tracer gas within the enclosure during a measuring period of 1 h is:

$$\Delta C = \frac{F(\%) \times V_{to} \times P_{to} \times \left((273\,\mathrm{K} + T_{test}) / (273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}) \right) \times \gamma \times t}{P_{atm} \times 365\ \mathrm{days} \times 24\ \mathrm{h} \times V_m}$$

$$\Delta C = \frac{0{,}5\,\% \times 0{,}375\ \mathrm{m}^3 \times 1\mathrm{MPa\ abs} \times \left((273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}) / (273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}) \right) \times 30\,\% \times 1\mathrm{h}}{0{,}1013\ \mathrm{MPa} \times 365\ \mathrm{days} \times 24\ \mathrm{h} \times 9{,}96\ \mathrm{m}^3} = 0{,}063\ \mathrm{p.p.m_v}.$$

Accordingly, if the same enclosure is used for low temperature test, the maximum allowable gas concentration increase for a measuring time period of 1 h at an ambient temperature of -25 °C will be:

$$3 \times F(\%) = 3 \times 0{,}063\ \mathrm{p.p.m_{v.}} \times \left((273\,\mathrm{K} - 25\,^{\circ}\mathrm{C}) / (273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}) \right) = 0{,}159\ \ \mathrm{p.p.m_{v.}}$$

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and accordingly at -50 °C

$$6 \times F(\%) = 6 \times 0{,}063 \text{ p.p.m}_{\text{v.}} \times \left(\frac{(273\,\text{K} - 50\,^{\circ}\text{C})}{(273\,\text{K} + 20\,^{\circ}\text{C})} \right) = 0{,}287 \text{ p.p.m}_{\text{v.}}$$

11 Miscellaneous provisions for breaking tests

11.1 Energy for operation to be used during demonstration of the rated operating sequence during short-circuit making and breaking tests

For circuit-breakers equipped with operating mechanisms having the possibility to store more energy than consumed by a single operation (for example hydraulic and pneumatic operating mechanisms), it is needed to specify the minimum levels of energy at which the breaking capacity still is guaranteed. Consequently, each test operating sequence shall be carried out at the relevant minimum energy level. In particular, minimum energy levels are specified for O, CO and O-CO operating sequences, which will ensure that the circuit-breaker will interrupt at the last O operation.

For the auto-reclose operating sequence O-*t*-CO-*t*'-CO the following conditions shall be fulfilled:

– the capability of the circuit-breaker for each short-circuit type-test duty must be demonstrated during performance of the rated operating sequence O-*t*-CO-*t*'-CO;

– demonstration is by three valid breaking operations during the sequence O-*t*-CO-*t*'-CO;

– the minimum and maximum arc duration shall be demonstrated during the tests;

– the starting energy for the O-*t*-CO part of the operating sequence cannot be less than the energy that takes account of the energy consumption of the O-*t*-C operating sequence to enable the final O operation to be performed at an energy down to (in practice during testing, at) the opening lock-out condition;

NOTE This O-*t*-CO start energy is often termed the auto-reclose lock-out setting.

– the circuit-breaker shall be able to perform the required three valid shots at the minimum functional pressure (i.e. minimum operating energy) for the specified operating sequence as described in 6.102.3.1 of IEC 62271-100:2008;

– where appropriate, the gas pressure for interruption shall also be at its lock-out setting.

The combination of events necessary to produce such boundary condition requirements are credible in practice, i.e. lowest gas, lowest operating pressure, minimum and/or maximum arc duration operation, and full short-circuit current rating and as such they should be tested.

Each operating sequence shall be initiated at the lowest applicable energy: the O-CO and CO test sequence should be performed setting the operating energy at the declared O-CO and CO lockout energy, respectively.

If single-phase tests in substitution for three-phase conditions are performed under direct or synthetic conditions, the rated operating sequence may be split in sub sequences.

For example, for synthetic testing the O-CO will be split in a single Os (breaking operation using synthetic circuit) for the 1st O and in a subsequent Od-COs, where Od is a breaking operation using a direct circuit (i.e. at reduced voltage).

The single O operation is here reproducing the 1st O of an O-CO sequence and shall be carried out at the O-CO lockout energy.

Even if a single O operation performed at minimum operation energy is not explicitly foreseen in the symmetrical test cases, the last O in the O-CO and CO sequences are performed at an

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operating energy equal to the O lock-out condition, since the operation energy has been consumed by previous operations (O-C and C, respectively).

The breaking capacity for single O operations carried out at O lockout condition is verified in the T100a test duty, since that test duty consists of single O operations (minimum, maximum and intermediate arcing time).

11.2 Alternative operating mechanisms

11.2.1 General

During the lifetime of a circuit-breaker or due to new developments of operating mechanisms a type tested circuit-breaker may be operated with an alternative operating mechanism that is different from the one type tested. To limit the quantity of tests for this new combination of operating mechanism and circuit-breaker, a statement is included in 6.102.7 of IEC 62271-100:2008 that repetition of type tests is not necessary for short-circuit, out-of-phase and capacitive current switching tests.

This statement applies if the type tested combination of operating mechanism and circuit-breaker and the alternative operating mechanism with the same circuit-breaker if the following conditions are fulfilled.

a) the mechanical characteristics under no-load conditions of the circuit-breaker with the alternative operating mechanism shall be within the limits defined in 6.101.1.1 of IEC 62271-100:2008;

b) a T100s test shall be done with the circuit-breaker and both operating mechanisms. Also here the mechanical characteristics shall be compared according to 6.101.1.1 of IEC 62271-100:2008;

c) a mechanical endurance test shall be performed in accordance with the specified class of the circuit-breaker;

Additionally, the circuit-breaker with alternative operating mechanisms shall pass a T100a test if the operating times are such that the circuit-breaker will fall into a different category of minimum clearing time (see 11.2.4.3 and subclause 3.7.159 of IEC 62271-100:2008);

If all requirements are met, the alternative operating mechanism combined with the type tested circuit-breaker is deemed to have the same characteristics and all type tests performed on the original combination are also valid for this new configuration.

11.2.2 Comparison of the mechanical characteristics

The mechanical characteristics of both operating mechanisms shall be recorded under the same no-load conditions with the same type of circuit-breaker. The sensor used during the alternative drive tests should be of the same type as for the original operating mechanism. The position of the sensor should be at the same position as during the original test to allow a direct comparison of the travel curves. If it is not possible to use the same position or type of sensor during the alternative drive test, because the design of the alternative drive does not allow this, the manufacturer should provide a transfer function to calculate the corresponding travel characteristic for comparison. The evaluation of the transfer function should be explained in detail for easy check of validity. The position of the type and sensor for the record of the mechanical characteristics should be stated in the test report. In the ideal case both closing and opening travel curves of the alternative operating mechanism should fall into the ±5 % tolerance band of the type tested operating mechanism. The tolerance band is drawn from the beginning of the mechanical characteristics to the instant of contact touch for the closing operation and from the instant of contact separation to the end of the contact travel for the opening operation. The mechanical characteristics of the alternative operating mechanism is placed into the envelope of reference curve. The envelope can be moved in the vertical direction until one of the envelope curves covers the curve of the alternative operating mechanism. This gives the following maximum tolerances over the mechanical characteristics:

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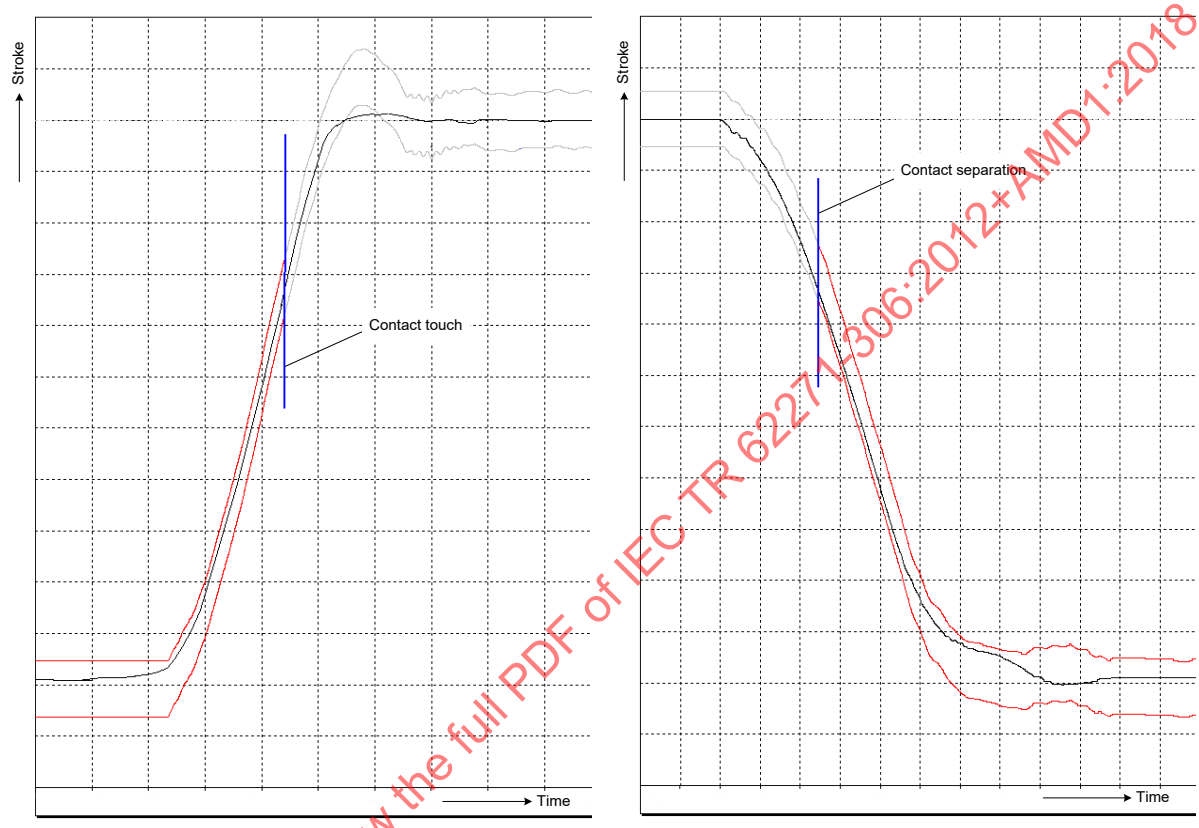
– $^{+10}_{-0}$ %;

– 0 %;

– $^{+0}_{-10}$ %.

The displacement of the envelope can be used only once for the complete procedure in each test in order to obtain a maximum total deviation from the reference characteristic of 10 %. An example is shown in Figure 64.



Closing operation **Opening operation**

Key

Red traces	Envelope of the reference mechanical characteristics
Black trace	Mechanical characteristics of the alternative operating mechanism

Figure 64 – Comparison of reference and alternative mechanical characteristics

Example 1:

As can be seen in Figure 64, the alternative operating mechanism (solid black line) has a slightly different travel curve. But the comparison fulfils the requirements of 6.101.1.1 of IEC 62271-100:2008. Even in the case that the curve during closing is leaving the reference travel boundaries is acceptable as the travel during closing shall be within the boundaries only until contact touch has taken place. This is before the end position of the circuit-breaker.

For the given example the requirement of the no-load characteristic is fulfilled.

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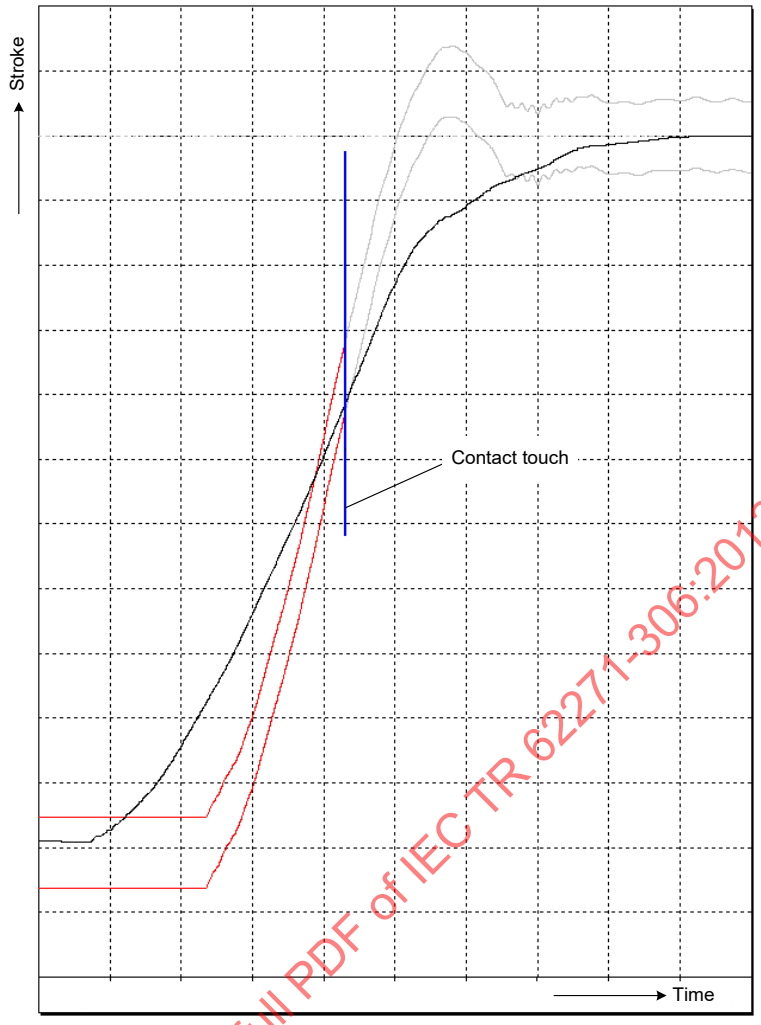

Key

Red traces	Envelope of the reference mechanical characteristics
Black trace	Mechanical characteristics of the alternative operating mechanism

Figure 65 – Closing operation outside the envelope

Example 2:

In Figure 65 the closing operation of another alternative operating mechanisms is shown. In this case the closing speed of the alternative operating mechanism is different. According to the requirements of 6.101.1.1 of IEC 62271-100:2008 the mechanical characteristics for closing do not fulfil the requirements.

Therefore the alternative operating mechanism should be tested for all relevant short-circuit, out-of-phase and capacitive current switching duties.

11.2.3 Comparison of T100s test results

As mentioned in IEC 62271-100, the number of tests shall be limited when qualifying an alternative operating mechanism. One test-duty to be performed is T100s. This test was chosen as it should demonstrate the ability of the circuit-breaker to close against a short-circuit and to clear a 100 % short-circuit current. As the original circuit-breaker is deemed to be fully type tested, results of the T100s tests are available. Therefore only the new combination of the type tested circuit-breaker and the alternative operating mechanism has to

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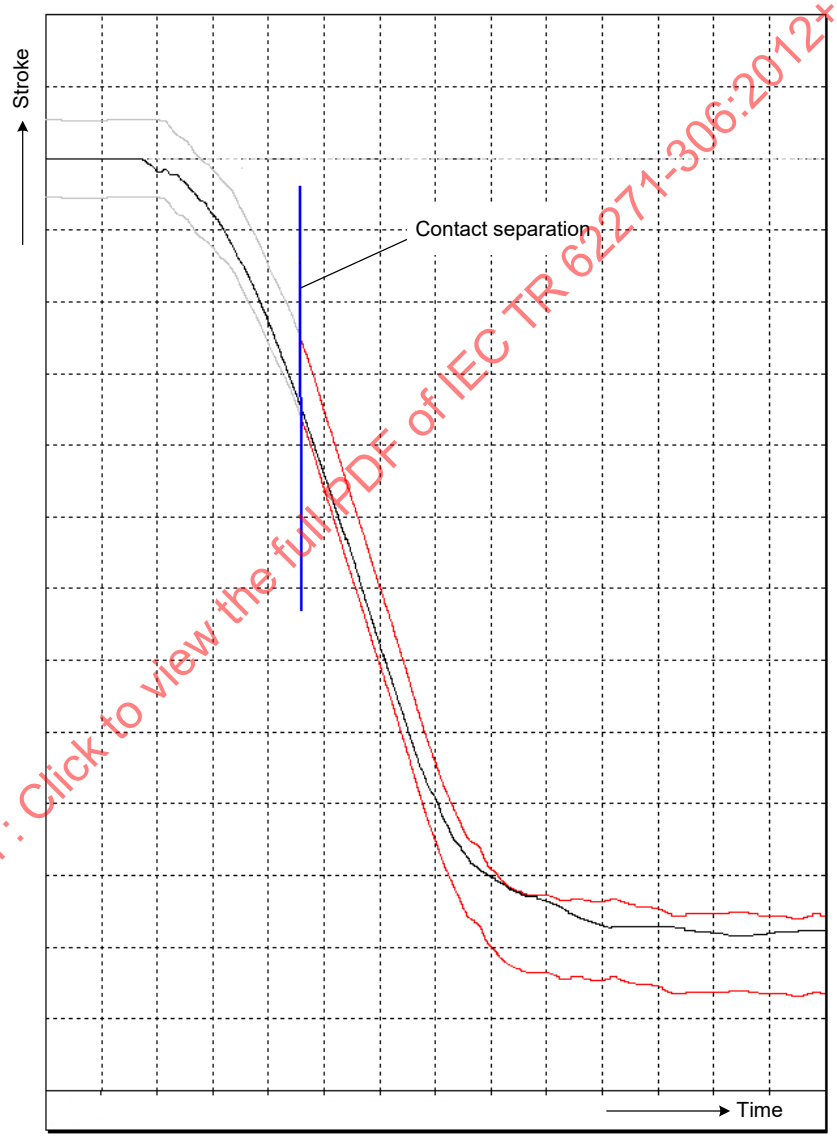
be subjected to a T100s test. The test shall be done under the same conditions as during the original type test.

The new combination shall pass the test according to the procedure of IEC 62271-100. Additionally, the mechanical characteristic during opening under the conditions of longest arcing time shall be compared with the travel curve of the original type test. The travel curve shall fulfil the requirements according to 6.101.1.1 of IEC 62271-100:2008.

In Figure 66 an example of the comparison of travel curves is given. The reference curve (red) was taken during a T100s test with the original operating mechanism, longest arcing time 18 ms. The alternative operating mechanism had a longest arcing of time 19 ms (black curve). The requirement to stay in the ±5 % tolerance band (or the shifted envelope curves) after contact separation is fulfilled. Therefore the alternative operating mechanism fulfils the requirement B of 6.102.7 of IEC 62271-100:2008.



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Key

Red traces	Envelope of the reference mechanical characteristics
Black trace	Mechanical characteristics of the alternative operating mechanism

Figure 66 – Mechanical characteristics during a T100s test

11.2.4 Additional test T100a

11.2.4.1 General

In some cases the opening time of the operating mechanisms can vary and the alternative operating mechanism may fall into a different category of minimum clearing time (see 3.7.157 of IEC 62271-100:2008 and Tables 15 to 22 of IEC 62271-100:2008). According to IEC 62271-100, in this case a test duty T100a shall be performed on the circuit-breaker with alternative operating mechanism.

As the aim of the test procedure of 6.102.7 of IEC 62271-100:2008 is to reduce the number of tests during qualification of an alternative operating mechanism two cases are investigated.

11.2.4.2 Case 1

Data of the original test:

– Opening time 25 ms
– Shortest arcing time 12 ms
– Test frequency 50 Hz → Relay time 10 ms
– Network time constant 45 ms → Table 15 of IEC 62271-100:2008

The circuit-breaker was tested according to row 3 of Table 15 of IEC 62271-100:2008 as the minimum clearing time $t_{clear\ min}$ is

$t_{clear\ min}$ = 25 ms + 12 ms + 10 ms = 47 ms

43,5 ms < $t_{clear\ min}$ ≤ 64 ms → row 3 of Table 15 of IEC 62271-100

Data of the alternative operating mechanism:

– Opening time 19 ms
– Shortest arcing time 12,5 ms

The travel curve of the alternative operating mechanism will be within the boundaries if a comparison is made according to 6.101.1.1 of IEC 62271-100:2008. The difference of opening time is only a result of a longer reaction time on the trip command of the drive used for the original tests.

$t_{clear\ min}$ = 19 ms+ 12,5 ms + 10 ms = 41,5 ms

$t_{clear\ min}$ < 43,5 ms → not row 3 of Table 15 of IEC 62271-100:2008

22,5 ms < $t_{clear\ min}$ ≤ 43,5 ms → row 2 of Table 15 of IEC 62271-100:2008

As the combination of circuit-breaker with alternative operating mechanism falls into a higher severity class for the T100a test, this test has to be performed with the alternative operating mechanism.

11.2.4.3 Case 2

Data of the original test:

– Opening time 17 ms
– Shortest arcing time 12 ms
– Test frequency 50 Hz → Relay time 10 ms

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– Network time constant 45 ms → Table 15 of IEC 62271-100:2008

The circuit-breaker was tested according to row 2 of Table 15 of IEC 62271-100:2008 as the minimum clearing time is

$t_{clear\ min}$ = 17 ms+ 12 ms + 10 ms = 39 ms

22,5 ms < $t_{clear\ min}$ ≤ 43,5 ms → row 2 of Table 15 of IEC 62271-100:2008

Data of the alternative operating mechanism:

– Opening time 23 ms
– Shortest arcing time 12,5 ms

The travel curve of the alternative operating mechanism will be within the boundaries if a comparison is made according to 6.101.1.1 of IEC 62271-100:2008. The difference of opening time is only a result of a longer reaction time of trip command.

$t_{clear\ min}$ = 23 ms + 12,5 ms + 10 ms = 45,5 ms

43,5 ms < $t_{clear\ min}$ ≤ 64 ms → row 3 of Table 15 of IEC 62271-100:2008

As the combination of circuit-breaker with the alternative operating mechanism falls into a less severe class for the T100a test, this test does not need to be performed with the alternative operating mechanism. The stress for the circuit-breaker under the conditions of an asymmetric short-circuit is less for the circuit-breaker with the alternative operating mechanism as the d.c. component will be smaller during the arcing time. The original test with the higher d.c.-component covers the smaller dc-component.

11.2.5 Conclusions

An alternative operating mechanism is qualified when the requirements of 6.102.7 of IEC 62271-100:2008 are fulfilled.

Test duty T100a should only be performed when the minimum clearing time of the alternative operating mechanism is shorter, such that the circuit-breaker should be tested with a higher d.c. component.

12 Rated and test frequency

12.1 General

Two different frequencies are used in electric power systems. These frequencies are 50 Hz and 60 Hz.

All circuit-breakers have to operate properly for each test duty and their rated frequency.

The rated frequency has an influence on the following tests:

– temperature rise;
– short-time withstand current;
– terminal fault tests;
– short-line fault test;
– capacitive current switching.

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The different test circuits used during testing also have an influence on the switching performance. These circuits are:

– direct test circuits;
– synthetic test circuit with voltage injection;
– synthetic test circuits with current injection.

12.2 Basic considerations

12.2.1 Temperature rise tests

The maximum temperature rise is dependent on the test frequency and the type of apparatus (GIS or AIS equipment) to be tested.

12.2.2 Short-time withstand current and peak withstand current tests

The short-time withstand current test is characterised by the duration of the short-circuit.

The tolerance of the frequency is ±10 %, but for convenience of testing a wider tolerance is allowed. IEC 62271-1 contains a cautionary note that care should be taken when interpreting test results when 50 Hz test are used to cover 60 Hz and vice versa.

The highest dynamic stress on the contacts and connections occurs during the peak withstand current test. The peak of the current is determined by the time constant of the network (see Annex A) and the rated frequency. IEC 62271-1 specifies three values for the peak factor (k = I_{peak}/i_{sym}). They are:

– 2,5 for a rated frequency of 50 Hz and a time constant of 45 ms;
– 2,6 for a rated frequency of 60 Hz and a time constant of 45 ms;
– 2,7 for rated voltages higher than 800 kV, where the standard time constant is 120 ms, independent of the frequency.

The special cases time constants are covered by a preferred peak factor of 2,7.

12.2.3 Short-circuit making current

The peak of the making current is determined by the time constant of the network and the rated frequency. IEC 62271-100 states the following values for the peak factor (k = I_{peak}/i_{sym}):

– 2,5 for a rated frequency of 50 Hz and a time constant of 45 ms;
– 2,6 for a rated frequency of 60 Hz and a time constant of 45 ms;
– 2,7 for rated voltages higher than 800 kV, where the standard time constant is 120 ms, independent of the frequency;
– 2,7 for all special cases time constants, independent of the frequency.

12.2.4 Terminal faults

A higher frequency leads to a shorter arcing window, because the time between two current zeros is correspondingly lower. For example, when the minimum arcing time of a circuit-breaker is 12 ms, the maximum arcing time that has to be demonstrated for single-phase testing at 50 Hz is 21 ms (12 – 1 + 10 ms). At 60 Hz the maximum arcing time is 19,5 ms (12 – 0,8 + 8,3 ms).

For test-duty T100a, a separate test may be necessary to prove that the operating mechanism has sufficient energy in case of 50 Hz application when the test has been performed using a 60 Hz current source, even if longer arcing times derived from 50 Hz requirements have been tested. The same is applicable for metal enclosed and dead tank circuit-breakers due to

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higher exhaust energy at longer arcing times, which can influence the phase-to-phase or phase-to-earth insulation.

The ITRV stress for different rated frequencies in live-tank circuit-breaker application is not taken into consideration when:

– the short-line fault test is carried out with a line-side time-delay t_{dL} equal to zero without significant differences in arcing time between short-line fault and terminal fault tests;
– the arcing window covers the corresponding frequency.

In the case that the terminal fault test is tested in a synthetic test circuit with voltage injection and the short-line fault test is not carried out with a line-side time delay less than 100 ns, the terminal fault test has to be performed with ITRV, where applicable.

12.2.5 Short-line fault

For short-line fault tests both the rate-of-decay of the short-circuit current before current zero and the arcing window are important factors. A higher rated frequency means a higher rate-of-rise of the line side TRV. Since the rate-of-rise of the line side TRV influences mainly the thermal interrupting behaviour of a circuit-breaker, it is important that the di/dt in the test report equal to or higher than required for the specified frequency.

For example a 90 % short-line fault test performed at 50 Hz with a line impedance of 450 Ω for a rated short-circuit current of 40 kA results in a line-side rate-of-rise of the TRV of 7,2 kV/μs, whereas the same test performed at 60 Hz would have a 20 % higher rate-of-rise of the line side TRV.

Therefore tests performed at 50 Hz are only valid for 60 Hz provided that the tests are performed with a synthetic test circuit where the di/dt is adjusted to 60 Hz.

If the test is performed at 60 Hz, it is only valid for a rated frequency of 50 Hz provided that the maximum arcing time for 50 Hz is covered. However, this is only possible in synthetic test circuit because any arcing time can be chosen.

12.2.6 Capacitive current switching

When the interrupting performance of a circuit-breaker for different rated frequencies is compared in capacitive switching tests, the only important factor is the recovery voltage as function of time. It is characterised by the voltage peak and the time to peak. Since the withstand capability of a circuit-breaker is a function of time, the higher frequency results in a higher stress on the circuit-breaker at arcing times close to zero. For example, the time to peak for 50 Hz is 10 ms, whereas it is only 8,3 ms in 60 Hz applications.

When interrupting with arcing times longer than the minimum arcing time, the contact gap is wider and therefore the voltage withstand of the circuit-breaker is higher. Maximum arcing time is therefore not an important factor when comparing tests performed at different frequencies.

To obtain the correct voltage stress between circuit-breaker contacts, synthetic capacitive circuits can be used.

12.3 Applicability of type tests at different frequencies

12.3.1 Temperature rise tests

Applicability of the tests for the different frequencies is given in Table 17.

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Table 17 – Temperature rise tests

Test frequency (Hz)	Test results acceptable at other frequency?
50	Yes, see NOTE
60	Yes
NOTE Tests performed at 50 Hz on circuit-breakers having no ferrous components adjacent to the current-carrying parts cover the performance at 60 Hz, provided that the temperature-rise values recorded during the tests at 50 Hz do not exceed 95 % of the maximum permissible values.	

12.3.2 Short-time withstand current and peak withstand current tests

Applicability of the tests for the different frequencies is given in Table 18 and Table 19.

Table 18 – Short-time withstand current tests

Test frequency (Hz)	Test results acceptable at other frequency?
50	Yes
60	Yes

Table 19 – Peak withstand current tests

Test frequency (Hz)	Test results acceptable at other frequency?
50	Yes, if 60 Hz peak factor is used
60	Yes

12.3.3 Short-circuit making current test

Applicability of the tests for the different frequencies is given in Table 20.

Table 20 – Short-circuit making current tests

Test frequency (Hz)	Test results acceptable at other frequency?
50	Yes, if 60 Hz peak factor is used
60	Yes

12.3.4 Terminal faults (direct and synthetic tests)

It is widely accepted that, for presently available technologies, the applicability of the tests for different frequencies is as presented in Table 21 and Table 22. However, in order to ensure the best possible clarity and accuracy for (type) testing, and to avoid any doubt about the applicability of results, IEC 62271-100 requires that tests be made at the rated frequency.

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Table 21 – Terminal faults: symmetrical test duties

Test frequency		Test method		Test results acceptable at other frequency?
50 Hz	60 Hz	Direct	Synthetic	
X		X		No, di/dt for 60 Hz not covered, see NOTE
X			X	Yes, provided di/dt for 60 Hz covered
	X	X		Yes, if arcing window for 50 Hz is covered
	X		X	Yes, provided arcing window for 50 Hz is covered
NOTE It is recognized that for vacuum circuit-breakers di/dt is not a relevant criterion for comparison and tests at 50 Hz are acceptable for 60 Hz ratings, but not vice versa.				

Table 22 – Terminal faults: asymmetrical test duties

Test frequency		Test results acceptable at other frequency?
50 Hz	60 Hz	
X	X	Yes, if the asymmetry requirements and arcing times of IEC 62271-100 are met

12.3.5 Short-line fault (direct and synthetic tests)

It is widely accepted that, for presently available technologies, the applicability of the tests for different frequencies is as presented in Table 23. However, in order to ensure the best possible clarity and accuracy for (type) testing, and to avoid any doubt about the applicability of results, IEC 62271-100 requires that tests be made at the rated frequency.

Table 23 – Short-line faults

Test frequency		Test method		Test results acceptable at other frequency?
50 Hz	60 Hz	Direct	Synthetic	
X		X		No, di/dt for 60 Hz not covered, see NOTE
X			X	Yes, if di/dt for 60 Hz covered
	X	X		Yes, if arcing window for 50 Hz is covered
	X		X	Yes, if arcing window for 50 Hz is covered
NOTE It is recognized that for vacuum circuit-breakers di/dt is not a relevant criterion for comparison and tests at 50 Hz are acceptable for 60 Hz ratings, but not vice versa.				

12.3.6 Capacitive current switching

Applicability of the tests for the different frequencies is given in Table 24.

Table 24 – Capacitive current switching

Test frequency (Hz)	Test results acceptable at other frequency?
50	No
60	Yes

Tests performed at 50 Hz are only applicable to 60 Hz if the recovery voltage at any point from zero to the first peak equals to or exceeds the required 60 Hz recovery voltage waveshape. This means that a higher test voltage needs to be used. To fully cover a 60 Hz

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test with a 50 Hz voltage, the test voltage needs to be increased with a factor of 1,44 compared to the 50 Hz test voltage.

13 ~~Terminal faults~~ Symmetrical and asymmetrical currents

~~13.1 General~~

~~This clause treats short-circuit currents and their arcing time and the associated transient recovery voltages.~~

~~Test requirements for symmetrical terminal fault conditions are covered by short-circuit test duties T100s, T60, T30, and T10. The asymmetrical duty T100a and the various short-line fault and out-of-phase duties are considered elsewhere in this document.~~

~~The purpose of this clause is to provide a background framework for some of these requirements where it may not be clear from the latest revision of the standard, or from readily available text books, how they were derived. Aspects covered in this clause are those relating to the short-circuit current, particularly to the arcing time and the voltages, both power frequency and transient recovery voltage (TRV), associated with terminal faults.~~

~~The system may be earthed in different ways depending on system voltage and application. The following definitions apply (Clause 3 of IEC 62271-100:2008 and as noted below):~~

~~**solidly earthed (neutral) system** (3.1.106 of IEC 62271-100:2008)~~
~~a system whose neutral point(s) is (are) directly earthed~~

~~[IEC 60050-601, 601-02-25]~~

~~**effectively earthed neutral system** (3.1.128 of IEC 62271-100:2008)~~
~~system earthed through a sufficiently low impedance such that for all system conditions the ratio of the zero-sequence reactance to the positive-sequence reactance (X_0/X_1) is positive and less than three, and the ratio of the zero-sequence resistance to the positive-sequence reactance (R_0/X_1) is positive and less than one. Normally such systems are solidly earthed (neutral) systems or low impedance earthed (neutral) systems.~~

~~NOTE 1 For the correct assessment of the earthing conditions the physical earthing conditions of the total system should be considered rather than just at the relevant location.~~

~~**non-effectively earthed neutral system** (3.1.129 of IEC 62271-100:2008)~~
~~system other than effectively earthed neutral system, not meeting the conditions given in 3.1.128. Normally such systems are isolated neutral systems, high impedance earthed (neutral) systems or resonant earthed (neutral) systems~~

~~NOTE 2 For the correct assessment of the earthing conditions the physical earthing conditions of the total system should be considered rather than just at the relevant location.~~

~~13.2 Demonstration of arcing time~~

~~Throughout IEC 62271-100 and related documents the terms arcing time, arcing window and interrupting window are used, especially in relation to the interruption of short-circuit currents. To understand the requirements of the various subclauses of IEC 62271-100:2008, such as 6.102.10, it is necessary to understand the meaning of these terms and that of the terms minimum and maximum arcing time in particular.~~

~~A circuit-breaker is required to interrupt short-circuit currents regardless of the point on the cycle of power frequency current its interrupter contacts separate mechanically. When this mechanical separation occurs the contacts are said to have parted and when the subsequent arcing ceases, the current is interrupted. The time between contact parting and current interruption in all three phases is the arcing time that is being considered here. Arcing time is measured in milliseconds (ms), or in electrical degrees (e.g. 10,0 ms at 50 Hz and 8,3 ms at~~

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60 Hz are 180°). The shortest arcing time at which the circuit-breaker is able to interrupt is the minimum arcing time.

Depending on the point of contact parting and the particular current, the arcing time of a circuit-breaker will vary between this minimum value and a maximum value. The difference between these values is called the arcing window (or more rarely the interrupting window). Although different designs of circuit-breaker will be capable of interruption over different ranges there is a basic requirement which is applicable to all modern designs of circuit-breaker. For these circuit-breakers the minimum arcing time is short or relatively short, and in addition they have limited capability for prolonged arcing as their quenching period is also short.

During each test-duty series (e.g. T100s or T60) it is necessary to demonstrate this basic arcing window. The minimum and maximum arcing times cannot be demonstrated in a single valid test. In the case of fault interruptions involving three-phases, the minimum arcing time is obtained in one of the valid tests of a test-duty with the first-pole-to-clear and the maximum arcing time is obtained in another valid test with the last pole(s) to clear.

For single-phase faults the maximum arcing time is the period to the end of the arcing window of the faulted phase, consisting of the minimum arcing time plus one loop of fault current minus 18°. This 18° is related to a deliberately specified step, of equal duration for 50 Hz and 60 Hz, giving a point of contact separation a short time later than that giving the minimum arcing time. At this setting the arcing time is too short for satisfactory clearance as a minimum, by definition, and an additional loop i.e.180° has to be endured until the next current zero. Clearance at this later zero gives the maximum arcing time and the end of the arcing window. The specified step of 18° is the smallest practical value for such a step generally achievable at testing stations being 1 ms at 50 Hz and 0,8 ms at 60 Hz.

13.3 Demonstration of the arcing time for three-phase tests

The arcing time requirement must be demonstrated during the sequence of three valid tests of each of the specified short-circuit test duties.

When three-phase symmetrical current tests are to be demonstrated using direct test techniques, the possible arcing times are automatically obtained by changing the setting of contact separation by a duration of 40° between each of the three required opening operations of the operating sequence (refer to 6.102.10.1.1 of IEC 62271-100:2008). In this way, taking into account that current passes through zero on one of the phases every 60°, the minimum arcing time is determined with a precision of less than 20°.

For synthetic testing the procedure is defined in IEC 62271-101.

13.4 Power frequency recovery voltage and the selection of the first-pole-to-clear factors 1,0; 1,2; 1,3 and 1,5

13.4.1 General

The first-pole-to-clear factor (k_{pp}) is a function of the earthing arrangements of the system. As defined in 3.7.152 of IEC 62271-100:2008 it is the ratio of the power frequency voltage across the interrupting pole before current interruption in the other poles, to the power frequency voltage occurring across the pole or poles after interruption in all three poles. For non-effectively earthed neutral systems this ratio is or tends towards 1,5. For rated voltages less than 170 kV such systems are quite common, particular within Europe and Japan.

For effectively earthed neutral systems, the realistic and practical value is dependent upon the sequence impedances of the actual earth paths from the location of the fault to the various system neutral points (the ratio X_0/X_1). The value used in IEC 62271-100 is taken to be ≤ 3 (see Equation (80)). The X_0/X_1 value is a standard value confirmed by system studies of various networks. Hence, for rating purposes, IEC 62271-100 considers two values for the

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three-phase short-circuit condition. These are adequate for the many, different, system earthing arrangements:

a) the non-effectively earthed, to cover all unearthed systems and those with some deliberate additional impedance in the neutral system. A standardised value for k_{pp} of 1,5 is used for all such systems;

b) all effectively earthed systems where it is accepted that some impedance exists. For standardization purposes for power systems operating at 800 kV and below the value for k_{pp} used is 1,3. For ultra-high-voltage (UHV) power systems operating above 800 kV, k_{pp} is 1,2 based on an X_0/X_1 ratio of 2.

A third condition does exist, this is where the fault is single-phase in a solidly earthed system and the last-pole-to-clear is considered. For this condition k_{pp} is 1,0.

At transmission voltages there has been an increase in interconnection and transformation particularly in major urban systems. The high number of transformer neutrals connected effectively to earth causes the value of 1,3 to be questioned. Although this has been considered, the text of IEC 62271-100 does not take these developments into account. It is important for users with such systems to note that as k_{pp} decreases towards unity the value of the second-pole-to-clear factor will fall. In addition, the value of the phase currents will change. The three phases become three independent single phases each with k_{pp} approaching 1,0. In general the users of such systems are aware of this possibility and of the need to consider the actual system conditions when assessing the suitability of their specified requirements and the test evidence they are offered against these.

For rated voltages higher than 800 kV, systems are characterized by long transmission lines and large transformers that contribute a relatively large part of the total short-circuit current. The first-pole-to-clear factor is function of the X_0/X_1 ratio that is in this case equal or lower than 2,0, as a consequence k_{pp} is equal or less than 1,2 and has been standardized to 1,2.

Where the ratio of three-phase to single-phase earth fault current is 1,0, k_{pp} is also 1,0. However, although this is normally assumed to be adequately covered by the use of the three-phase requirements and the associated k_{pp} of 1,2 or 1,3, it is important that evidence is provided to demonstrate the extended arc condition of the single-phase fault. For a single-phase fault an appropriate full arcing window must be demonstrated.

It should be noted that in accordance with 6.108 of IEC 62271-100:2008 specific recovery voltage conditions are required to demonstrate the ability of a circuit-breaker to clear single-phase and double earth faults.

Regarding earthing of the test circuit, reference is made to 6.103.3 of IEC 62271-100:2008.

13.4.2 Equations for the first, second and third-pole-to-clear factors

The equation for the first-pole-to-clear factor is :

$$k_{pp} = \frac{3X_0}{X_1 + 2X_0} \qquad (80)$$

where X_0 is the zero sequence, and X_1 the positive sequence reactance of the system. Table 25 gives the k_{pp} values for various earthing arrangements based on the definitions given in 13.1.

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Table 25 – First-pole-to-clear factors k_{pp}

Earthing arrangement	X_0/X_1	System voltage	k_{pp}
Solidly earthed	1	≤ 800 kV	1
Effectively earthed	3		1,3
Effectively earthed	2	> 800 kV	1,2
Non-effectively earthed	∞	≤ 170 kV	1,5
NOTE Calculation of k_{pp} for the effectively earthed case (X_0/X_1 = 3) gives k_{pp} = 1,286 which is then rounded to 1,3.			

Following interruption of the first pole, the remaining two phases continue to conduct fault current.

In systems with non-effectively earthed neutrals the second and third poles interrupt in series under the phase-to-phase voltage so that for the second and third pole,

$k_p = \frac{\sqrt{3}}{2}$, where k_p is the pole-to-clear factor of the individual poles.

In systems with effectively earthed neutrals the second pole clears with a pole-to-clear factor of,

$$k_p = \frac{\sqrt{3(X_0^2 + X_0X_1 + X_1^2)}}{X_0 + 2X_1} \quad (81)$$

Equation (81) can be expressed as a function of the ratio $\alpha = X_0/X_1$:

$$k_p = \frac{\sqrt{3}\sqrt{\alpha^2 + \alpha + 1}}{2 + \alpha}$$

For the third-pole-to-clear in an effectively earthed system k_p = 1.Table 26 gives k_p for each clearing pole as a function of X_0/X_1 as appropriate.

Table 26 – Pole-to-clear factors for each clearing pole

X_0/X_1	Pole-to-clear factor		
Ratio	First	Second	Third
3	1,3	1,27	1,0
2	1,2	1,15	1,0
1	1,0	1,00	1,0
∞	1,5	0,866	0,866

The respective multiplying factors for the peak value of the TRV (u_c) are given in Table 6 of IEC 62271-100:2008. It is important to note that the amplitude factor is the same for each pole. The multiplying factors are as applied to the power frequency voltages.

13.4.3 Standardised values for the second- and third- pole-to-clear factors

As discussed above, IEC 62271-100 has standardised values for the second and third-pole to clear factors for three-phase testing. Subclause 13.7 deals with this topic in relation to

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demonstration of arcing times for these poles and the appropriate pole factors relevant to each opening pole. It is important to note that on systems where the neutral earthing is solid, both the first-pole-to-clear factor of 1,3 and the values provided above for second- and third-pole-to-clear factor, may be significantly different to the actual system requirements. This is likely to be a rare occurrence, generally associated with urban systems where there are numerous effectively earthed transformers in close proximity. Where such differences are significant, the user is generally aware that it may be necessary to consider specifying system specific requirements and tests. NOTE 1 to 6.103.3 b) of IEC 62271-100:2008 makes reference to this matter.

Circuit-breakers are rated on the basis of their ability to interrupt a three-phase to earth fault in either an effectively or non-effectively earthed system. Taking former case, the three poles clear in sequence:

- First pole clears with k_{pp} given by Equation (80) leaving a two-phase to earth fault.
- Second pole clears with k_p given by Equation (81) leaving a single-phase to earth fault. For the case of a two-phase to earth, the k_{pp} for the first clearing pole is also given by Equation (81).
- Third pole with k_p = 1 which is also applicable to the single-phase to earth fault case.

Similar logic can be applied to faults in non-effectively earthed systems. A summary of the pole-to-clear factors for the different fault cases is given in Table 27.

Table 27 – Pole-to-clear factors for various types of faults

Type of fault	First-pole-to-clear	Second-pole-to-clear	Third-pole-to-clear
Phase-to-earth	1	-	-
Two-phase not involving earth	Simultaneous opening of both poles: $\frac{\sqrt{3}}{2}$	Simultaneous opening of both poles: $\frac{\sqrt{3}}{2}$	-
Two-phase-to-earth	$k_{pp} = \frac{\sqrt{3}\sqrt{\alpha^2+\alpha+1}}{2+\alpha}$	1	-
Three-phase not involving earth	1,5	Simultaneous opening of both poles: $\frac{\sqrt{3}}{2}$	Simultaneous opening of both poles: $\frac{\sqrt{3}}{2}$

13.5 Characteristics of recovery voltage

13.5.1 Values of rate-of-rise of recovery voltage and time delays

The values for the rate-of-rise-of-recovery-voltage (RRRV) for the first-pole-to-clear, and the associated time-delay values, were derived from system studies, supported by system tests performed in and before the mid-1970s. The values adopted (2 kV/µs etc.) have been shown by this work to be adequate for all developed systems, and are generally acceptable for others. IEC 62271-100 gives multipliers for the RRRV for the second and third poles-to-clear. These values were derived by calculation.

13.5.2 Amplitude factors

The values of the amplitude factors are given in 6.104.5 of IEC 62271-100:2008. These values where adopted into IEC 62271-100 as a result of system studies and generally remain acceptable.

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13.6 Arcing window and k_p requirements for testing

Separate procedures exist for tests performed in substitution for three-phase conditions by using a single pole of the circuit-breaker.

The procedure as defined is for circuit-breakers to be installed in systems with non-effectively earthed neutral and separately for those with effectively earthed neutrals. The relevant subclauses in IEC 62271-100:2008 are 6.102.10.2.1 and 6.102.10.2.2.

The required arcing window must be demonstrated for each condition in the case of interruptions with symmetrical currents, as for test duties T10, T30, T60, and T100s. (Note, this also applies to short-line fault and the out-of-phase test-duties OP1 and OP2). Whether the testing is for three-phase test requirements, or single-phase tests in substitution for the three-phase condition, it is important that the arcing window and associated TRV are demonstrated for the relevant system condition. In the case of a single-phase test, the three tests of the duty are demonstrated on that single pole, as it is the representative sample of the circuit-breaker, as allowed in 6.102.2 of IEC 62271-100:2008.

The required arcing windows for circuit-breakers applied in a non-effectively earthed system is shown graphically in Figure 67. If contact parting is at the minimum arcing time ($t_{arc\ min}$) on one pole, then that pole clears at 0° in Figure 67 and is followed by the other two poles 90° later. The minimum three-phase arcing time is $t_{arc\ min}$ + 90°. If contact parting is now delayed by 18°, the first-pole-to-clear on one of the other two phases will interrupt the current at ($t_{arc\ min}$ – 18°) + 60° = $t_{arc\ min}$ + 42°. As before, the other two poles will clear 90° later giving a maximum three-phase arcing time of $t_{arc\ min}$ + 132°.

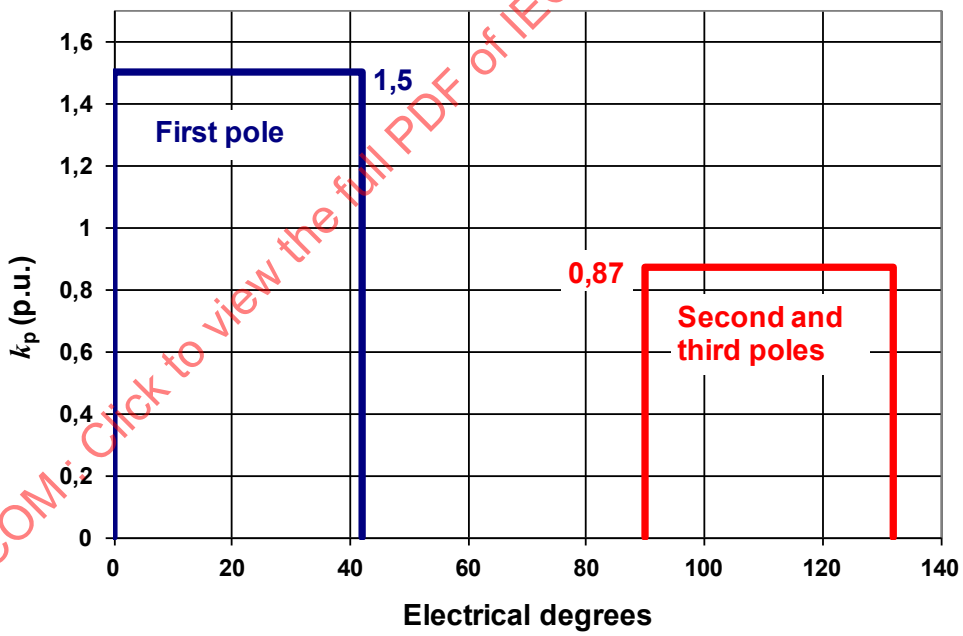

Figure 67 – Arcing windows and k_p value for three-phase fault in a non-effectively earthed system

A practical example of this case is shown in Figure 68. In the upper trace, the blue phase clears first at the minimum arcing time of 12 ms at 50 Hz and the currents the red and green each phase shift by 30° to become equal and opposite and are interrupted 90° later. In the lower trace, contact parting is delayed by 18° and the first suitable zero crossing for current interruption occurs on the red phase at 12 ms + 42°. The blue and green phases then clear at 12 ms + 42° + 90° = 12 ms + 132° = 19,33 ms. At 60 Hz the corresponding maximum arcing time is 18,1 ms.

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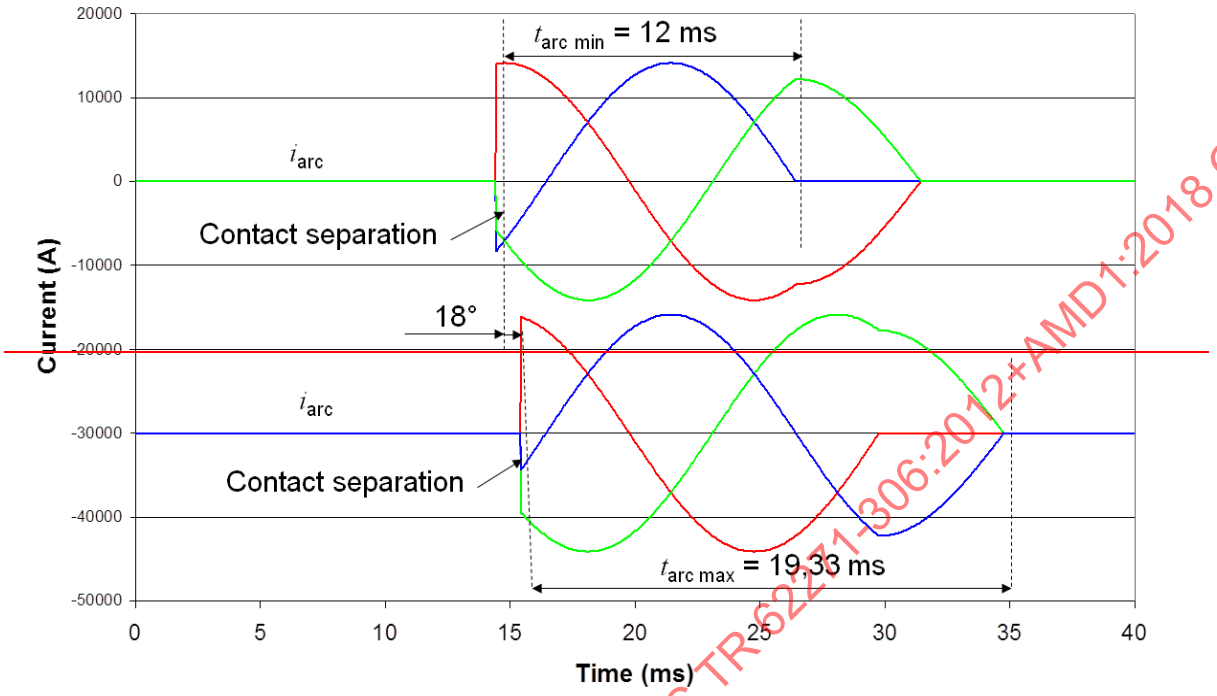
~~The required arcing windows for circuit-breakers applied in effectively earthed systems at 800 kV and below are shown in Figure 69 and at voltages above 800 kV are shown in Figure 70.~~



~~**Figure 68 – Three-phase unearthed fault current interruption**~~

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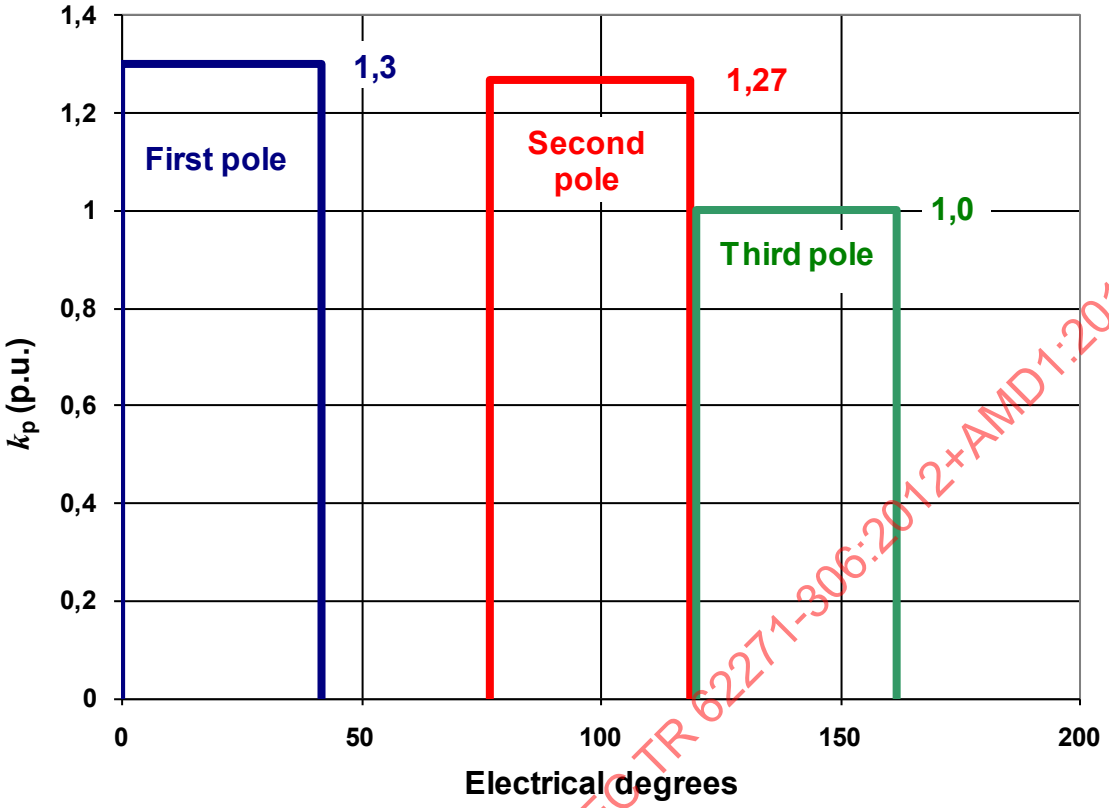

~~Figure 69 – Arcing windows and *kp* values for three-phase fault to earth in an effectively earthed system at 800 kV and below~~

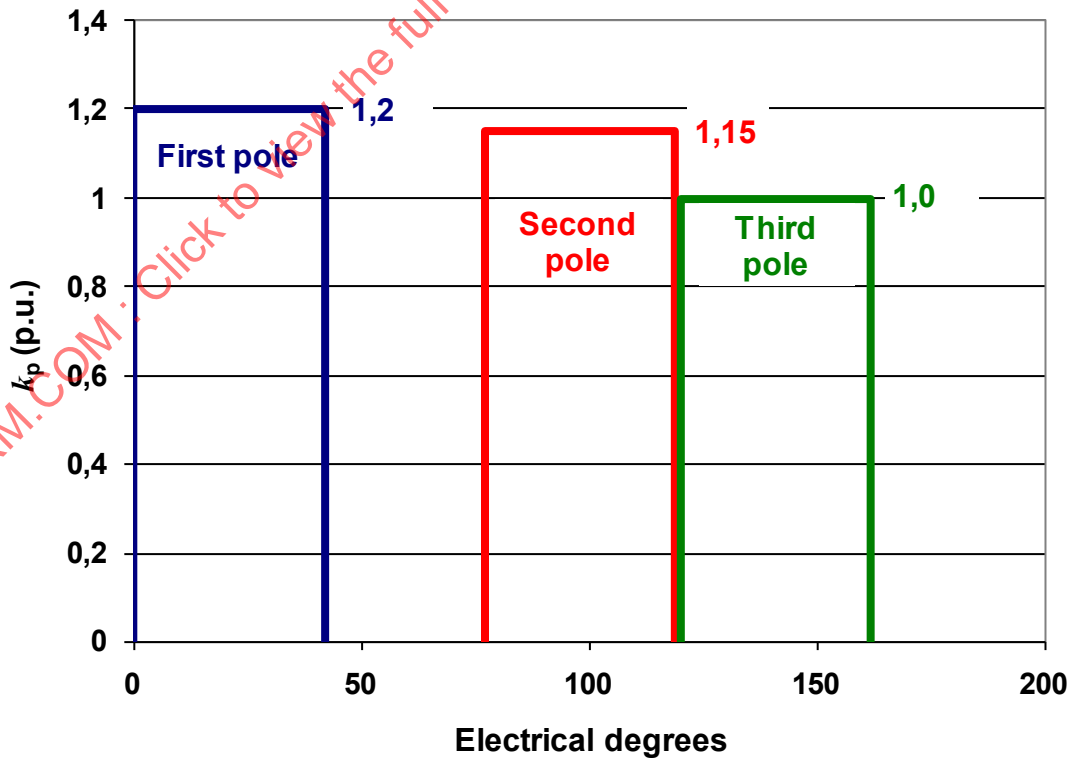

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Figure 70 – Arcing windows and k_p values for three-phase fault to earth in an effectively earthed system above 800 kV

Referring to Figure 69 and Figure 70, if contact parting is at the minimum arcing time on one pole, then that pole clears at 0° in either figure. The transition from a three-phase to a two-phase fault causes a phase shifting of the currents in the other phases and the second pole will clear at 77°. A further transition and phase shift results in the third pole clearing 43° later. The minimum three-phase arcing time is $t_{arc\ min}$ + 77° + 43° = $t_{arc\ min}$ + 120°. If contact parting is delayed by 18°, the first-pole-to-clear will interrupt the current at ($t_{arc\ min}$ – 18°) + 60°, the second pole 77° later and the third pole 43° later still. The maximum three-phase arcing time is given by ($t_{arc\ min}$ – 18°) + 60° + 77° + 43° = $t_{arc\ min}$ + 162°. Figure 71 shows a simulation of a three-phase fault current interruption. The first-pole-to-clear interrupts the current at about 156 ms followed by the second and third poles at approximately 161 ms and 163 ms, respectively. The phase shifting of the current at first and second pole clearing is obvious.

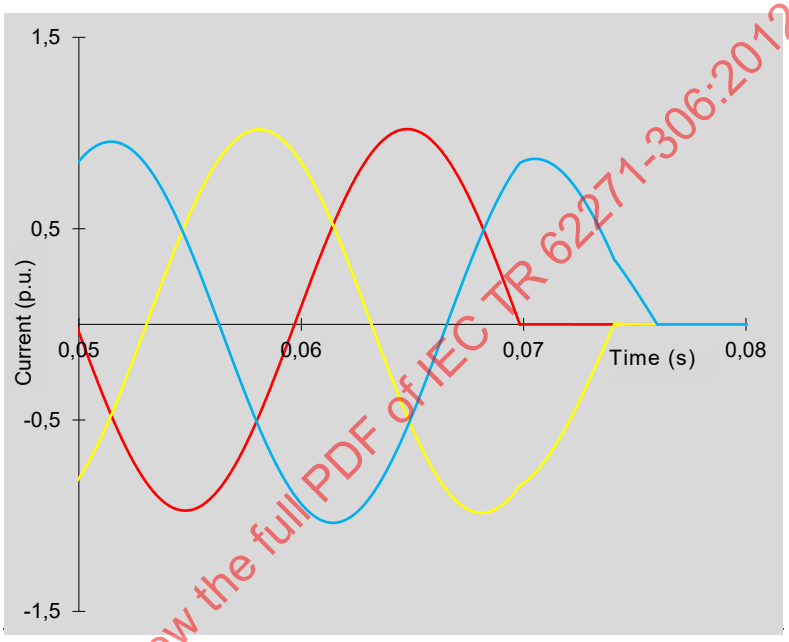

Figure 71 – Simulation of three-phase to earth fault current interruption at 50 Hz

13.7 Single-phase testing to cover three-phase testing requirements

As discussed in 13.6, Figure 67, Figure 69 and Figure 70 show the arcing windows and associated k_p values for individual pole clearing of three-phase faults. From Figure 67 it is acceptable to perform a single-phase test with k_{pp} = 1,5 and arcing times in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 132°. Likewise from Figure 69 and Figure 70, it is acceptable to perform a single-phase test with either k_{pp} = 1,2 or 1,3 as applicable and arcing times in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 162°. These tests are acceptable because the test requirements for each pole are equalled or exceeded and has the advantage that only three valid interruptions are required.

IEC 62271-100 recognizes that the testing described above is more onerous and allows the tests may be split into individual for each pole and earthing arrangement case (see subclause 6.102.10.2.5 of IEC 62271-100:2008). For the non-effectively earthed case (Figure 67), two test series are: the first at k_{pp} = 1,5 and arcing time in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 42° and the second at k_p = 0,87 and arcing times in the range $t_{arc\ min}$ + 90° to $t_{arc\ min}$ + 132°. For the effectively earthed cases (Figure 69 and Figure 70), three test series are correspondingly required to address all three pole-clearing requirements.

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13.8 Combination tests for k_{pp} = 1,3 and 1,5

For a requirement with a first-pole-to-clear factor of 1,3 it is possible to adapt the test procedure during tests for a factor of 1,5. Two alternatives exist:

a) test with k_{pp} = 1,5 but ensure the arcing window (see 13.2) covers the range (180° – dα);

b) test with k_{pp} = 1,5 for its normal arcing window of (150 – dα) plus an additional test with k_{pp} = 1,3 and an arcing time of minimum arc time plus (180 – dα). As stated in 6.102.10 of IEC 62271-100:2008 all additional testing of this nature should be performed as CO operations.

13.9 Suitability of a particular short-circuit current rated circuit-breaker for use at an application with a lower short-circuit requirement

Subclause 8.101 of IEC 62271-100:2008 states that:

Circuit-breakers which have satisfactorily completed type tests for a combination of rated values (i.e. voltage, normal current, making and/or breaking current) are suitable for any lower rated values (with the exception of rated frequency), without further testing.

The reason for this is related to the combination of the transient recovery voltage (TRV) requirements and the current values for the basic short-circuit test duties. This can be demonstrated by using the following example where a circuit-breaker tested for a rated voltage U_r of 420 kV, 50 kA rating is considered for an application requirement of 420 kV, 30 kA.

At 420 kV the T100, T60, T30 and T10 duty TRV values are detailed in Table 26 of IEC 62271-100:2008 and reproduced in an abbreviated form below for convenience.

The circuit-breaker being considered satisfies the TRV peak and rate-of-rise etc. of the duties shown in the upper part of Table 28. Those for the application are shown in a similar form in the lower part of the table and are compared as illustrated by the arrows.

Table 28 – Example of comparison of rated values against application (U_r = 420 kV)

Duty for circuit-breaker (current)	T100 (50 kA)	T60 (30 kA)	T30 (15 kA)	T10 (5 kA)
TRV peak value	624	669	669	787
Rate of rise	2,0	3,0	5,0	7,0

		↓	↓	↓ ——— ↓	↓
Duty of application (current)	-	T100 (30 kA)	T60 (18 kA)	T30 (9 kA)	T10 (3 kA)
TRV peak value	-	624	669	669	787
Rate of rise	-	2,0	3,0	5,0	7,0

As can be seen from Table 28, the evidence from the upper part of the table provides significant overlapping evidence for the application shown in the lower part. This is the reason why 8.101 of IEC 62271-100:2008 is acceptable in this case.

Users should exercise due diligence in all cases and most particularly where the difference between the rating and the requirement is so great that the requirements of the application become far removed from the evidence provided by type testing. In such cases discussions may be required with the supplier. Additional test evidence may be required.

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~~**13.10 Basis for the current and TRV values of the basic short-circuit test-duty T10**~~

~~Test duty T10 is detailed in 6.104.5.5 of IEC 62271-100:2008 and represents a transformer limited fault condition with the circuit-breaker under consideration clearing a fault on the remote side of the transformer. In such circumstances the fault current is limited by the impedance of the transformer to a value, chosen for standardization purposes, of approximately 10 %. The value of 10 % is historic having been established from system studies and modelling using the typical impedance values of transformers of standardised ratings.~~

~~For this duty, the fault-current is limited by the value of the impedance of the transformer. The TRV is also dominated by the transformer characteristics which give it a (1-cos) wave-shape form. The values given in IEC 62271-100 for amplitude factor, time coordinates and delay line have been established from system studies and modelling during the 1960s and before. The present values are accepted as being adequate for the vast majority of systems.~~

~~It must be recognised that the first-pole-to-clear factor is 1,5 for all rated voltages. As the damping of the TRV oscillation in a high-voltage transformer is less than in a network, an amplitude factor of 1,7 has been standardised except for line systems, with a voltage reduction across the transformer of 0,9 for voltages of 100 kV and above. Thus, the TRV peak u_c for test-duty T10 becomes:~~

~~a) for rated voltages below 100 kV~~

~~1) for circuit-breakers in cable systems~~

~~$u_c = k_{pp} \times k_{af} \sqrt{(2/3)} \times U_r$ where k_{af} is equal to 1,7.~~

~~2) for circuit-breakers in line systems~~

~~$u_c = k_{pp} \times k_{af} \sqrt{(2/3)} \times U_r$ where k_{af} is equal to 1,8.~~

~~b) for rated voltages of 100 kV and above: $u_c = k_{pp} \times k_{af} \sqrt{(2/3)} \times U_r$, where k_{af} is equal to 0,9 × 1,7 = 1,53.~~

~~Some large transformers, particularly those of present design, have different impedances and characteristics to those considered above giving rise to different current and TRV requirements. If users have a specific transformer installation where, by extrapolation between the standard T10 and T30 values, the present characteristics for the controlling circuit-breaker(s) do not adequately cover the site specific requirements, then additional testing may be needed.~~

13.1 General

This clause treats symmetrical and asymmetrical short-circuit currents and their arcing times.

Test requirements for symmetrical terminal fault conditions that are covered by short-circuit test duties T100s, T60, T30, and T10 are covered in 13.3. The asymmetrical duty T100a is covered in 13.4 and the various short-line fault and out-of-phase duties are considered elsewhere in this document.

The purpose of this clause is to provide a background framework for some of these requirements where it may not be clear from the latest revision of the standard, or from readily available text books, how they were derived. Aspects covered in this clause are those relating to the short-circuit current, particularly to the arcing time and the voltages, both power frequency and transient recovery voltage (TRV), associated with terminal faults.

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13.2 Arcing time

The arcing time of a pole of a circuit-breaker is defined as the interval of time between the instant of the first initiation of an arc in a pole and the instant of arc extinction in that pole.

There are several possible methods to determine the arcing time.

a) Using the opening time of the circuit-breaker

When a tripping coil current signal is available, the arcing time is determined by subtracting the opening time from the break time of the pole considered.

b) Using a travel recorder

The arcing time is the duration between the contact separation point identified on the travel curve, and the instant of interruption. The instant of contact separation is determined during the no load measurements before the test.

c) Using amplified arc voltage

The arcing time is the duration between the contact separation, determined on the amplified arc voltage, and the instant of current interruption.

For gas circuit-breakers method b) is the preferred method. This method is considered more accurate as it eliminates the possible error in method a) due to mechanical scatter of the operating mechanism. For circuit-breakers having butt contacts, method c) is recommended.

13.3 Symmetrical currents

13.3.1 Demonstration of arcing time

Throughout IEC 62271-100 and related documents the terms arcing time and interrupting window are used, especially in relation to the interruption of short-circuit currents. To understand the requirements of the various subclauses of IEC 62271-100:2008, such as 6.102.10, it is necessary to understand the meaning of these terms and that of the terms minimum and maximum arcing time in particular.

The arcing time of a three-pole circuit-breaker is defined as the interval of time between the instant of first initiation of an arc (typically at contact separation) and the instant of final arc extinction in all three phases. Arcing time is measured in ms, or in electrical degrees (e.g. 10,0 ms at 50 Hz and 8,3 ms at 60 Hz are 180°). The shortest arcing time at which the circuit-breaker is able to interrupt is the minimum arcing time.

Depending on the point of contact separation and the particular current, the arcing time of a circuit-breaker will vary between this minimum value and a maximum value. The difference between these values is called the interrupting window (or more rarely the arcing window). Although different designs of circuit-breaker will be capable of interrupting with different duration of their interrupting windows there is a basic requirement which is applicable to all modern designs of circuit-breaker. For these circuit-breakers the minimum arcing time is short or relatively short, and in addition they have limited capability for prolonged arcing as their quenching period is also short.

The aim of each test-duty (e.g. T100s or T60) is to demonstrate the breaking capacity with any arcing time within this interrupting window. This requirement is fulfilled by demonstration of interruption at minimum, maximum and medium arcing time. The minimum and maximum arcing times cannot be demonstrated in a single valid test. In the case of fault interruptions involving three-phases, the minimum arcing time is obtained in one of the valid tests of a test-duty with the first-pole-to-clear and the maximum arcing time is obtained in another valid test with the last pole(s) to clear.

For single-phase faults the maximum arcing time is the period to the end of the interrupting window of the faulted phase, consisting of the minimum arcing time plus one loop of fault current minus 18°. This 18° is related to a deliberately specified step, of equal duration for 50 Hz and 60 Hz, giving a point of contact separation a short time later than that giving the minimum arcing time. At this setting the arcing time is too short for satisfactory clearance as a

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minimum, by definition, and an additional loop i.e.180° will follow until the next current zero. Clearance at this later current zero results in the maximum arcing time and the end of the interrupting window. The specified step of 18° is the smallest practical value for such a step generally achievable at testing stations being 1 ms at 50 Hz and 0,8 ms at 60 Hz.

13.3.2 Demonstration of the arcing time for three-phase tests

In accordance with IEC 62271-100, each test-duty consists of demonstration of interruption within the interrupting window. This requirement is fulfilled by demonstration of interruption at minimum, maximum and medium arcing time, i.e. by three valid tests of each of the specified short-circuit test duties.

When three-phase symmetrical current tests are to be demonstrated using direct test techniques, the possible arcing times are automatically obtained by changing the setting of contact separation by a duration of 40° between each of the three required opening operations of the operating sequence (refer to 6.102.10.1.1 of IEC 62271-100:2008). In this way, taking into account that current passes through zero on one of the phases every 60°, the minimum arcing time is determined with a accuracy of less than 20°.

For synthetic testing the procedure is defined in IEC 62271-101.

13.3.3 Interrupting window and k_p requirements for testing

Separate procedures exist for tests performed in substitution for three-phase conditions by using a single pole of the circuit-breaker.

The procedure as defined is for circuit-breakers to be installed in systems with non-effectively earthed neutral and separately for those with effectively earthed neutrals. The relevant subclauses in IEC 62271-100:2008 are 6.102.10.2.1 and 6.102.10.2.2.

In accordance with IEC 62271-100, the required interrupting window shall be demonstrated for each condition in the case of interruptions with symmetrical currents, as for test duties T10, T30, T60, and T100s. (Note, this also applies to short-line fault and the out-of-phase test-duties OP1 and OP2). Whether the testing is for three-phase test requirements, or single-phase tests in substitution for the three-phase condition, it is important that the interrupting window and associated TRV are demonstrated for the relevant system condition. In the case of a single-phase test, the three tests of the duty are demonstrated on that single pole, as it is the representative sample of the circuit-breaker, as allowed in 6.102.2 of IEC 62271-100:2008.

The interrupting windows required by IEC 62271-100:2008 for circuit-breakers applied in a non-effectively earthed system are shown graphically in Figure 132. If contact parting is at the minimum arcing time ($t_{arc\ min}$) on one pole, then that pole clears at 0° in Figure 132 and is followed by the other two poles 90° later. The minimum three-phase arcing time is $t_{arc\ min}$ + 90°. If contact parting is now delayed by 18°, the first-pole-to-clear on one of the other two phases will interrupt the current at ($t_{arc\ min}$ – 18°) + 60° = $t_{arc\ min}$ + 42°. As before, the other two poles will clear 90° later giving a maximum three-phase arcing time of $t_{arc\ min}$ + 132°.

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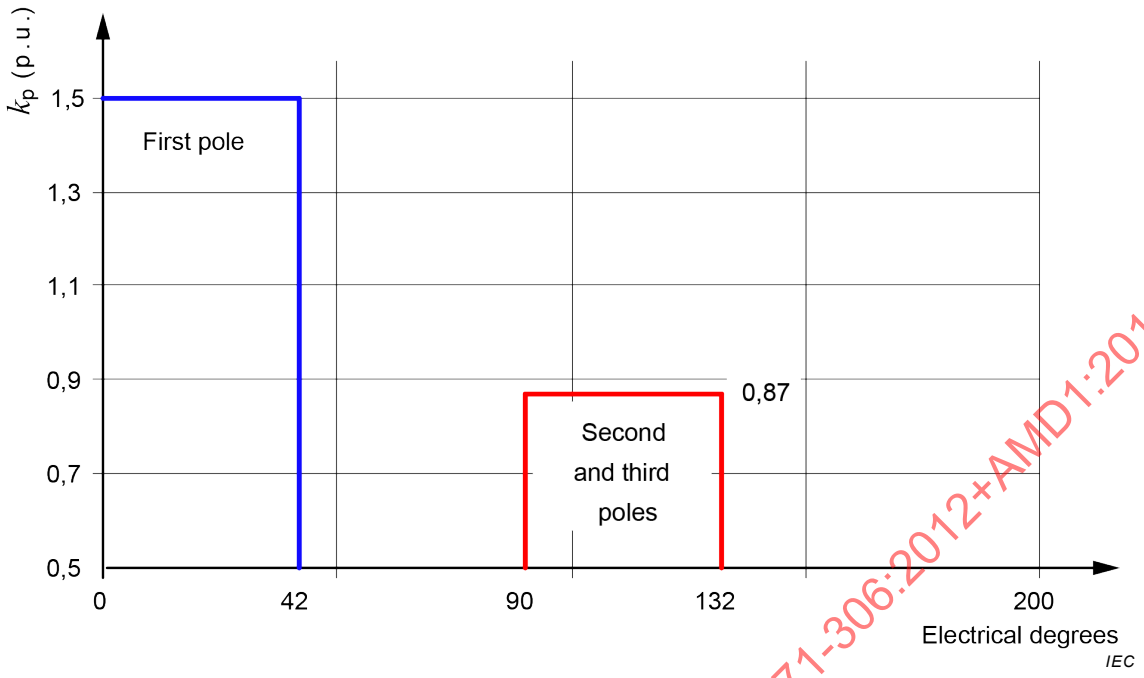

Figure 132 – Interrupting windows and k_p value for three-phase fault in a non-effectively earthed system

A practical example of this case is shown in Figure 133. In the upper trace, the blue phase clears first at the minimum arcing time of $t_{arc\ min}$ and the currents in the red and green each phase shift by 30° to become equal and opposite and are interrupted 90° later. In the lower trace, contact parting is delayed by 18° and the first suitable zero crossing for current interruption occurs on the red phase at ($t_{arc\ min}$ + 42° / 360° × T) ms, where T is the duration of one cycle of current (20 ms for 50 Hz and 16,7 ms for 60 Hz). The blue and green phases then clear at ($t_{arc\ min}$ (42° + 90°) / 360° × T)) ms.

The required interrupting windows for circuit-breakers applied in effectively earthed systems at 800 kV and below are shown in Figure 134 and at voltages above 800 kV are shown in Figure 135.

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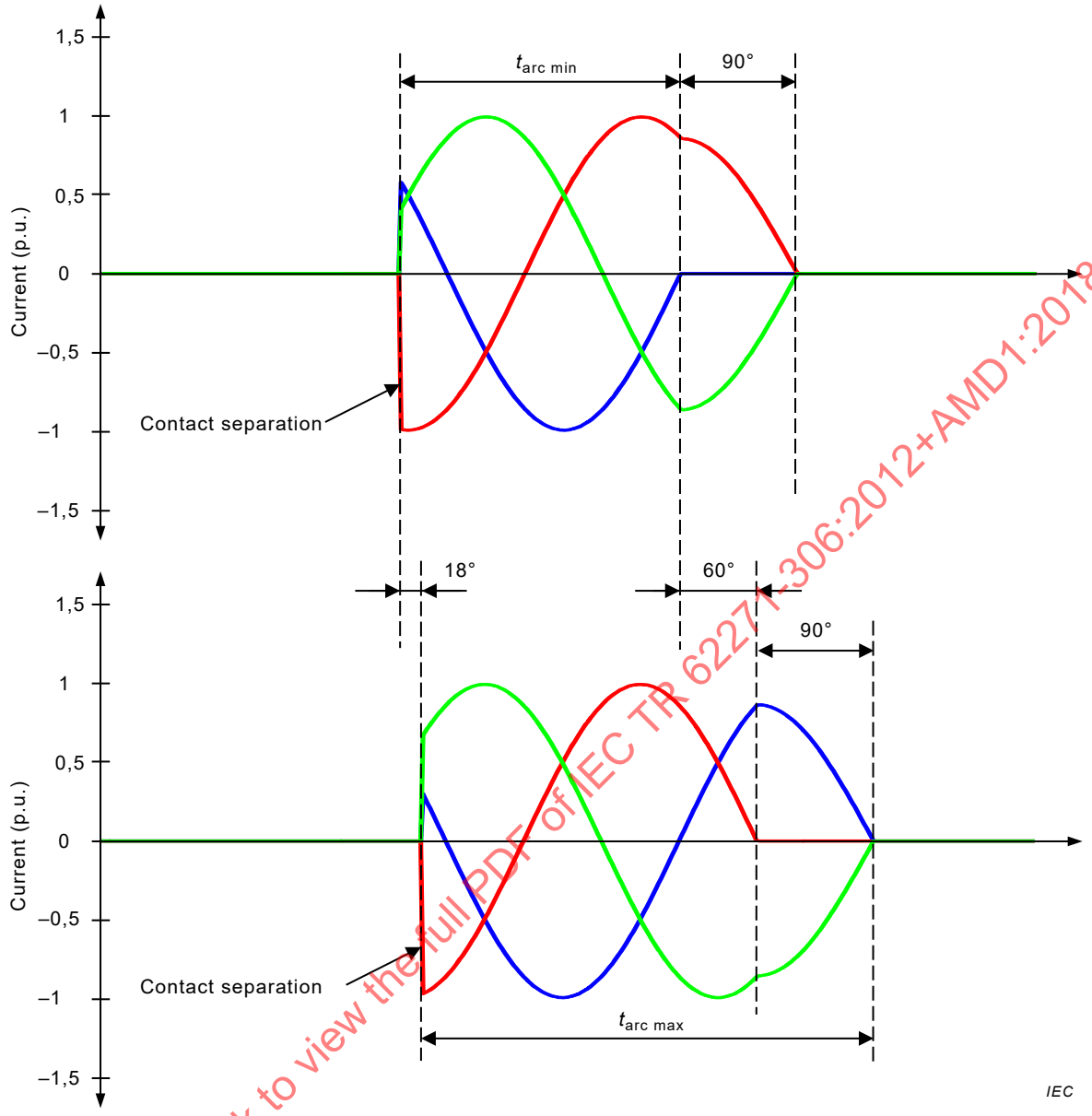

Figure 133 – Three-phase unearthed fault current interruption

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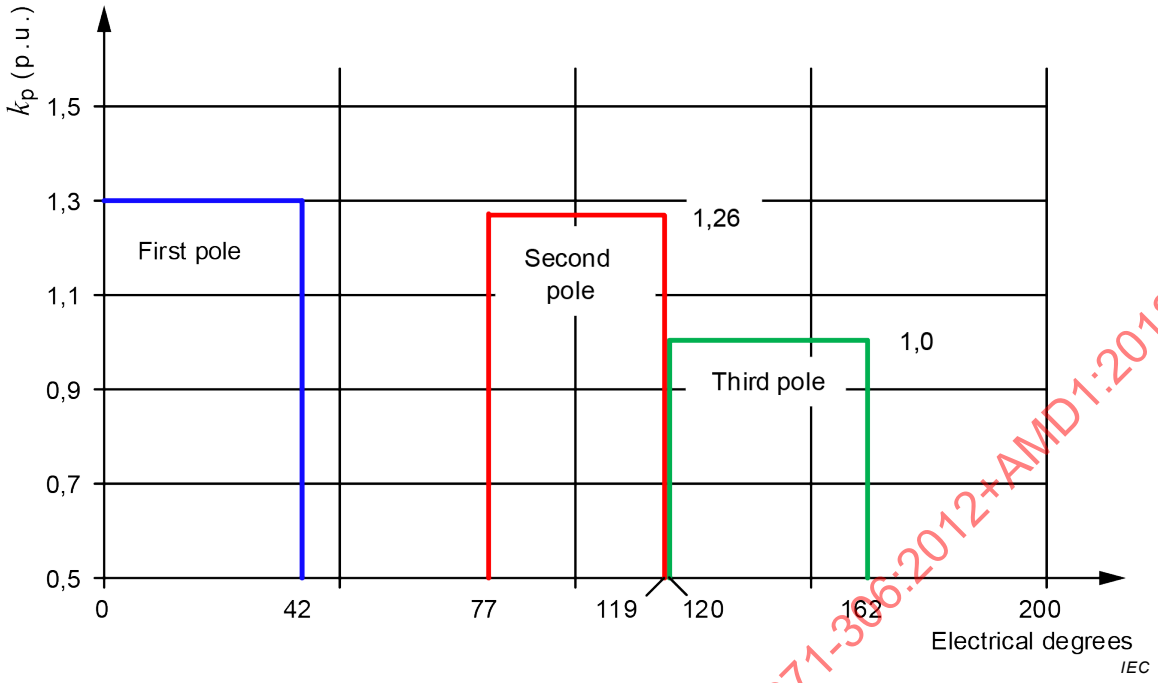

Figure 134 – Interrupting windows and k_p values for three-phase fault to earth in an effectively earthed system at 800 kV and below

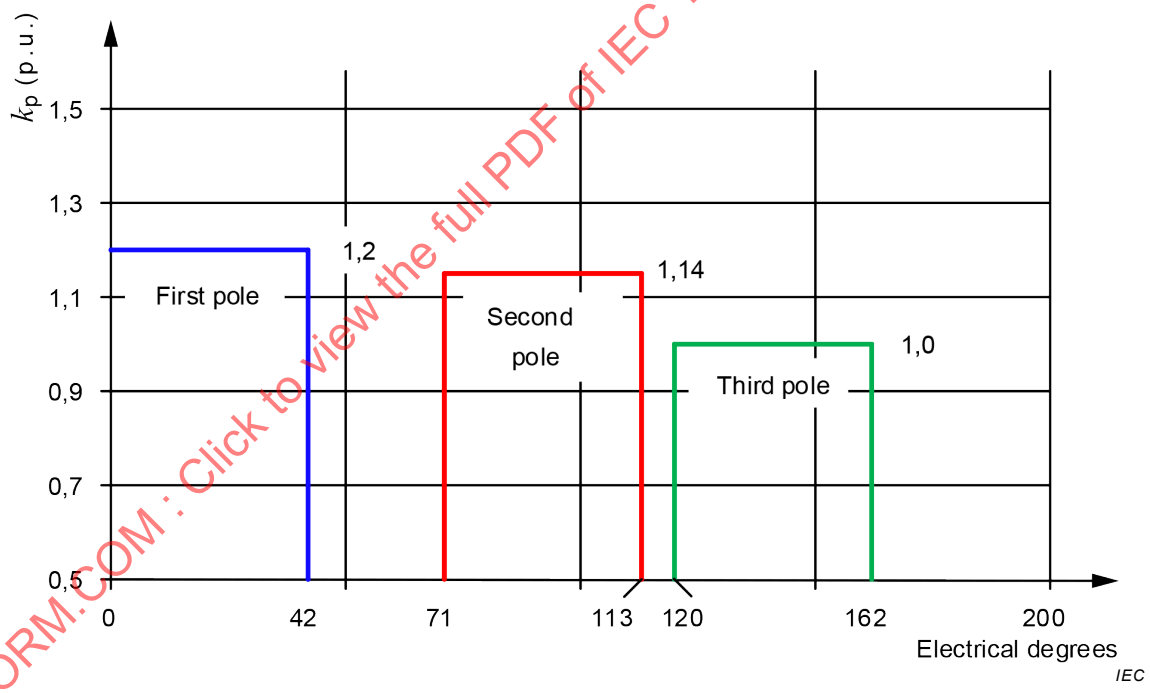

Figure 135 – Interrupting windows and k_p values for three-phase fault to earth in an effectively earthed system above 800 kV

Referring to Figure 134 and Figure 135, if contact parting is at the minimum arcing time on one pole, then that pole clears at 0° in either figure. The transition from a three-phase to a two-phase fault causes a phase shifting of the currents in the other phases and the second pole will clear at 77°. A further transition and phase shift results in the third pole clearing 43° later. The minimum three-phase arcing time is $t_{arc\ min}$ + ((77° + 43°) / 360°) × T = $t_{arc\ min}$ + 120° / 360° × T. If contact parting is delayed by 18°, the first-pole-to-clear will interrupt the current at ($t_{arc\ min}$ – 18° / 360° × T) + 60° / 360° × T, the second pole 77° / 360° × T later and the third pole 43° / 360° × T later still. The maximum three-phase arcing time is given by

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$t_{arc\ max}$ = ($t_{arc\ min}$ – 18° / 360° × T) + 60° / 360° × T + 77° / 360° × T + 43° / 360° × T = $t_{arc\ min}$ + 162° / 360° × T. Figure 136 shows a simulation of a three-phase fault current interruption. The first-pole-to-clear interrupts the current at $t_{arc\ min}$ followed by the second and third poles at 77° and 43°, respectively. The phase shifting of the current at first and second pole clearing is obvious.

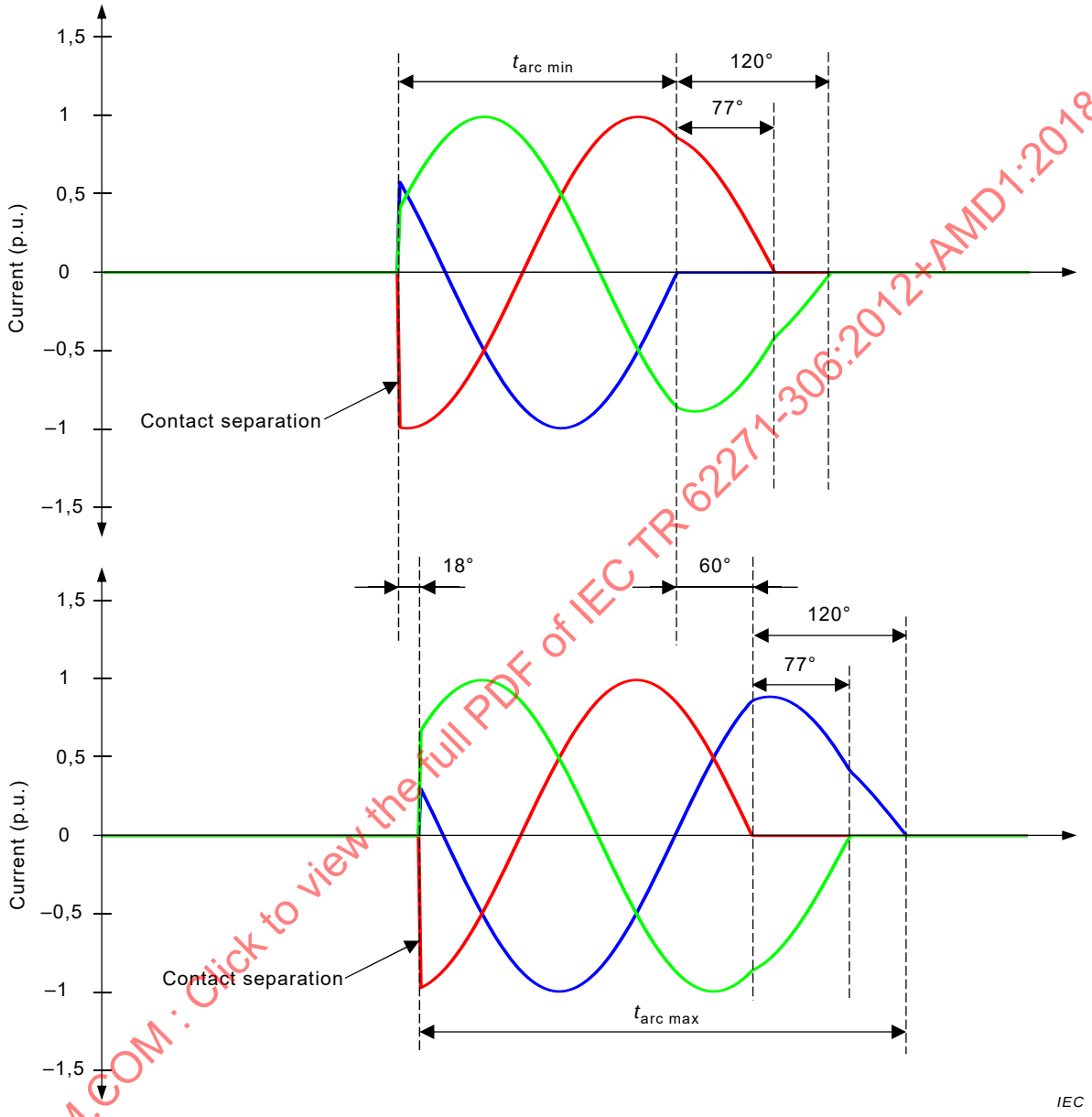

Figure 136 – Simulation of three-phase to earth fault current interruption at 50 Hz

13.3.4 Single-phase testing to cover three-phase testing requirements

As discussed in 13.3.3, Figure 132, Figure 134 and Figure 135 show the interrupting windows and associated k_p values for individual pole clearing of three-phase faults. From Figure 132, it is acceptable to perform a single-phase test with k_{pp} = 1,5 and arcing times in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 132°. Likewise from Figure 134 and Figure 135, it is acceptable to perform a single-phase test with either k_{pp} = 1,2 or 1,3 as applicable and arcing times in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 162°. These tests are acceptable because the test requirements for each pole are equalled or exceeded and this has the advantage that only three valid interruptions are required.

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IEC 62271-100 recognizes that the testing described above is more onerous and allows that the tests be split into individual tests for each pole and earthing arrangement case (see 6.102.10.2.5 of IEC 62271-100:2008). For the non-effectively earthed case (Figure 132), two test series are: the first at k_{pp} = 1,5 and arcing time in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 42° and the second at k_p = 0,87 and arcing times in the range $t_{arc\ min}$ + 90° to $t_{arc\ min}$ + 132°. For the effectively earthed cases (Figure 134 and Figure 135), three test series are correspondingly required to address all three-pole clearing requirements.

13.3.5 Combination tests for k_{pp} = 1,3 and 1,5

For a requirement with a first-pole-to-clear factor of 1,3, it is possible to adapt the test procedure during tests for a factor of 1,5. In accordance with IEC 62271-100, two alternatives exist:

– For three-phase tests, if a complete series of test-duties demonstrating the circuit-breaker performance for k_{pp} = 1,5 is already performed, test-duties T100s and T100a shall be repeated with a test-circuit simulating the earthing condition of an effectively earthed neutral system. The repetition of test-duties T100s and T100a with a three-phase circuit for an effectively earthed neutral system can, as an alternative, be replaced by additional single-phase tests.

– For single-phase tests both conditions (k_{pp} = 1,5 and k_{pp} = 1,3) may be combined in one test series. The transient and power frequency voltages to be used shall be those applicable to a non-effectively earthed neutral system and the arcing times shall be those applicable to an effectively earthed neutral system.

  For test-duty T100a, the arcing times shall be those applicable to a non-effectively earthed neutral system.

13.3.6 Suitability of a particular short-circuit current rated circuit-breaker for use at an application with a lower short-circuit requirement

In accordance with 8.101 of IEC 62271-100:2008, circuit-breakers that have satisfactorily completed type tests for a combination of rated values (i.e. voltage, normal current, making and/or breaking current) are suitable for any application with lower service values (with the exception of frequency), without further testing.

The reason for this is related to the combination of the transient-recovery-voltage (TRV) requirements and the current values for the basic short-circuit test duties. This can be demonstrated by using the following example where a circuit-breaker tested for a rated voltage U_r of 420 kV, 50 kA rating is considered for an application requirement of 420 kV, 30 kA.

At 420 kV, the T100, T60, T30 and T10 duty TRV values are detailed in Table 26 of IEC 62271-100:2008 and reproduced in an abbreviated form below for convenience.

The circuit-breaker being considered satisfies the TRV peak and rate-of-rise etc. of the duties shown in the upper part of Table 48. Those for the application are shown in a similar form in the lower part of the table and are compared as illustrated by the arrows.

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Table 48 – Example of comparison of rated values against application (U_r = 420 kV)

Duty for circuit-breaker (current)	T100 (50 kA)	T60 (30 kA)	T30 (15 kA)	T10 (5 kA)
TRV peak value	624	669	669	787
Rate of rise	2,0	3,0	5,0	7,0
		↓	↓	↓ ↓ ↓
Duty of application (current)	-	T100 (30 kA)	T60 (18 kA)	T30 (9 kA)	T10 (3 kA)
TRV peak value	-	624	669	669	787
Rate of rise	-	2,0	3,0	5,0	7,0

As can be seen from Table 48, the evidence from the upper part of the table provides significant overlapping evidence for the application shown in the lower part. This is the reason why 8.101 of IEC 62271-100:2008 is acceptable in this case.

Users should exercise due diligence in all cases and most particularly where the difference between the rating and the requirement is so great that the requirements of the application become far removed from the evidence provided by type testing. In such cases, discussions may be required with the supplier. Additional test evidence may be required.

13.4 Asymmetrical currents

13.4.1 Test procedure for test-duty T100a

13.4.1.1 General

A new test procedure was introduced for test-duty T100a in IEC 62271-100:2008/AMD:2017 in order to obtain a better correspondence between the test conditions during three-phase tests and single-phase tests made in substitution for three-phase tests (same amplitude of the major loop, arcing times, etc.). The new test procedure is based on the fact that the relevant major loop of current with full asymmetry to consider before current interruption for the two main test conditions depends on the capability of the circuit-breaker to interrupt after a minor loop of current with intermediate asymmetry. The two main test conditions are as follows:

– interruption of the first-pole-to-clear after a major loop of current with required asymmetry and longest arcing time;

– interruption of a last-pole-to-clear after a major extended loop of current with required asymmetry and longest arcing time in case the of k_{pp} = 1,5 or interruption of the second pole to clear after a major extended loop of current with the required asymmetry and longest arcing time in the case of k_{pp} = 1,3.

This consideration is explained in 13.4.1.2 using the case with k_{pp} = 1,5. In IEC 62271-100:2008, it is not considered necessary to prove interruption of the third-pole-to-clear in case of k_{pp} = 1,3 because the peak of the TRV, di/dt at current zero and the energy in the arc are lower than that of the second-pole-to-clear. The performance of the third-pole-to-clear is verified during test-duty T100s.

A definition has been introduced in IEC 62271-100:2008 to define the minimum clearing time of a circuit-breaker: it is the sum of the minimum opening time, minimum relay time (0,5 cycle) and the shortest arcing time of a minor loop interruption in the phase with intermediate asymmetry that starts with a minor loop at short-circuit current initiation. It will be illustrated by the examples in 13.4.1.2.

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13.4.1.2 Basis for test-duty T100a

To illustrate the different cases of three-phase fault interruption presented hereafter the following parameters are chosen:

– rated frequency is 50 Hz, the relay time is 10 ms, k_{pp} = 1,5;

– opening time = 11,5 ms and the shortest arcing time (blue phase) is 5 ms;

– the minimum clearing time is then 10 + 11,5 + 5 = 26,5 ms.

Figure 137 illustrates a first case of three-phase fault interruption in which a first pole (blue phase) clears after minor loop of current with intermediate asymmetry. This is possible as the minimum clearing time is lower than the duration of 27 ms between initiation of the short-circuit current and passage through zero of current in the blue phase.

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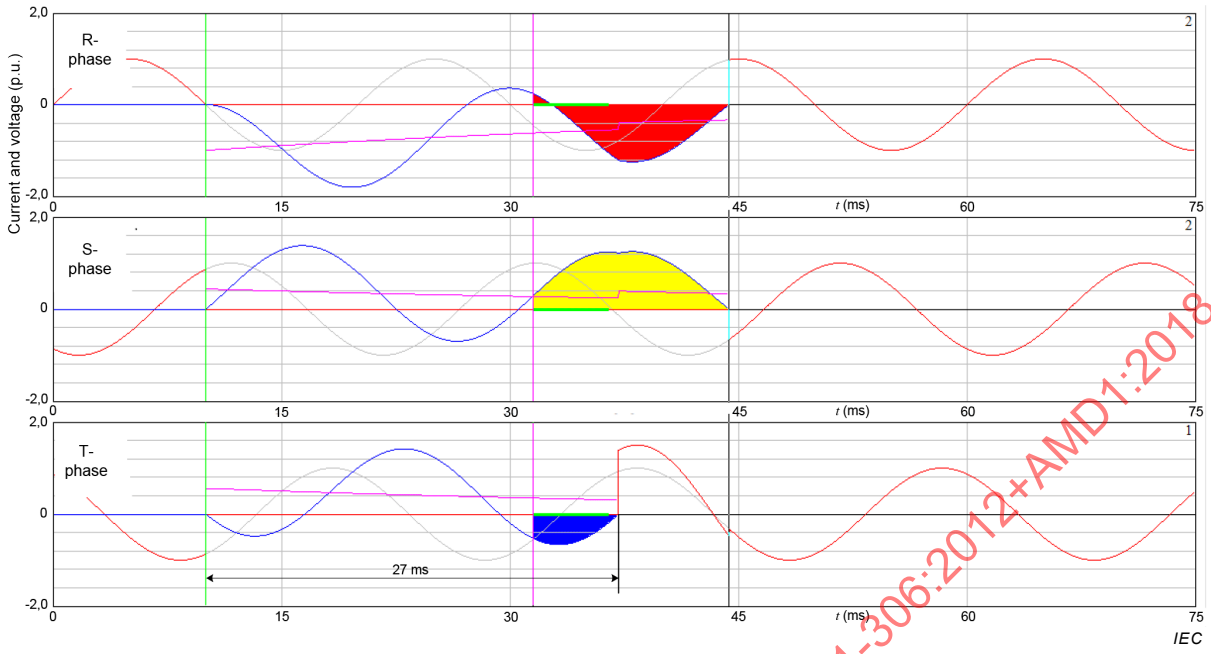

Figure 137a – Case 1 with k_{pp} = 1,5

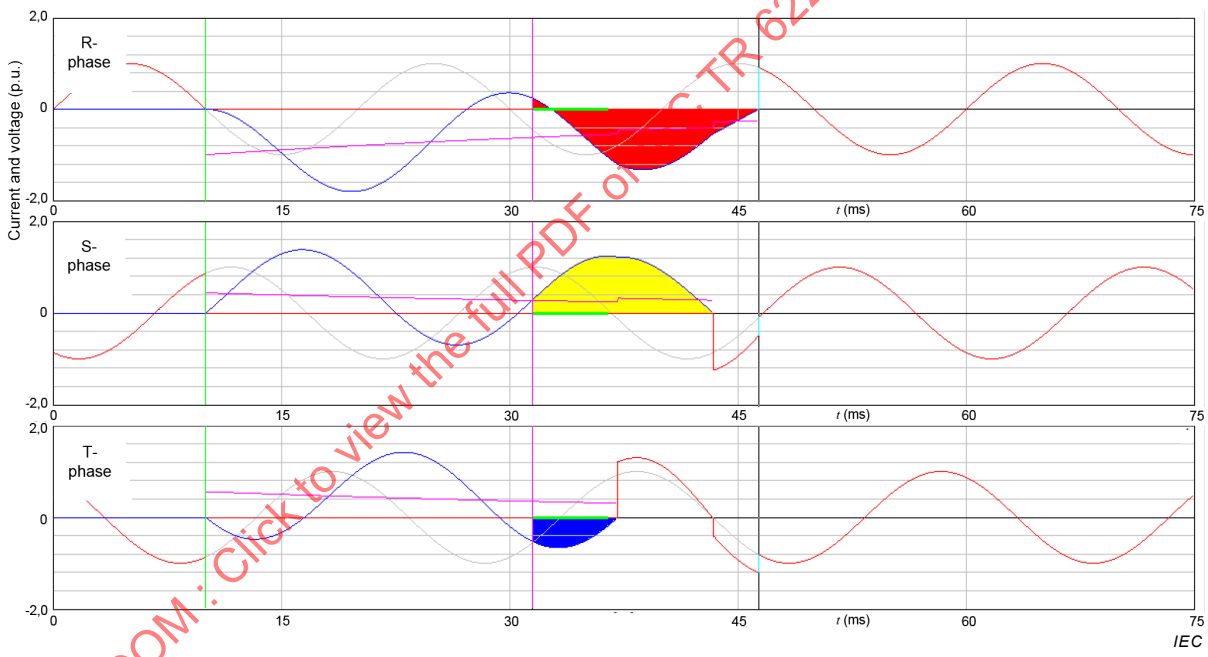

Figure 137b – Case 1 with k_{pp} = 1,3

Figure 137 – Case 1 with interruption by a first pole (blue phase) after minor loop of current with intermediate asymmetry

Figure 138 illustrates case 2 obtained when contact separation is delayed by 18° (1 ms at 50 Hz), a first pole interrupts after a major loop of current with intermediate asymmetry (yellow phase). For the case with k_{pp} = 1,5 a last pole clears a major extended loop with required asymmetry and the longest possible arcing time. For the case with k_{pp} = 1,3 the second pole clears a major loop with required asymmetry and the longest possible arcing time. This is one of the two breaking conditions for which interruption shall be proved.

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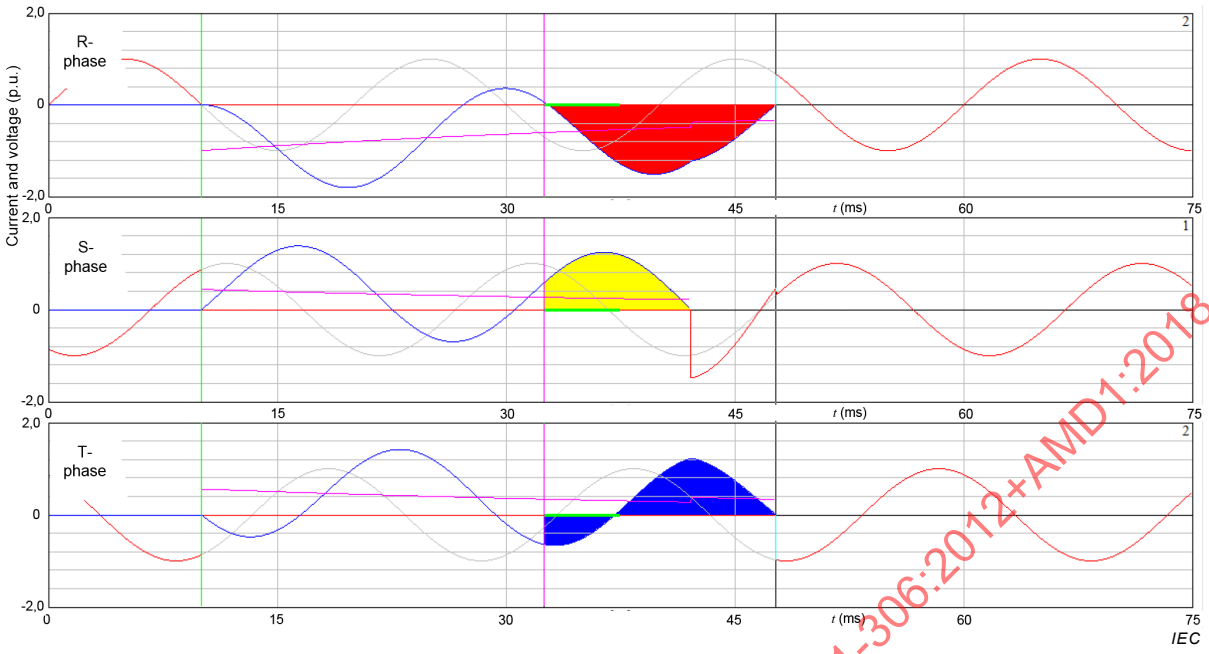

Figure 138a – Case 2 with k_{pp} = 1,5

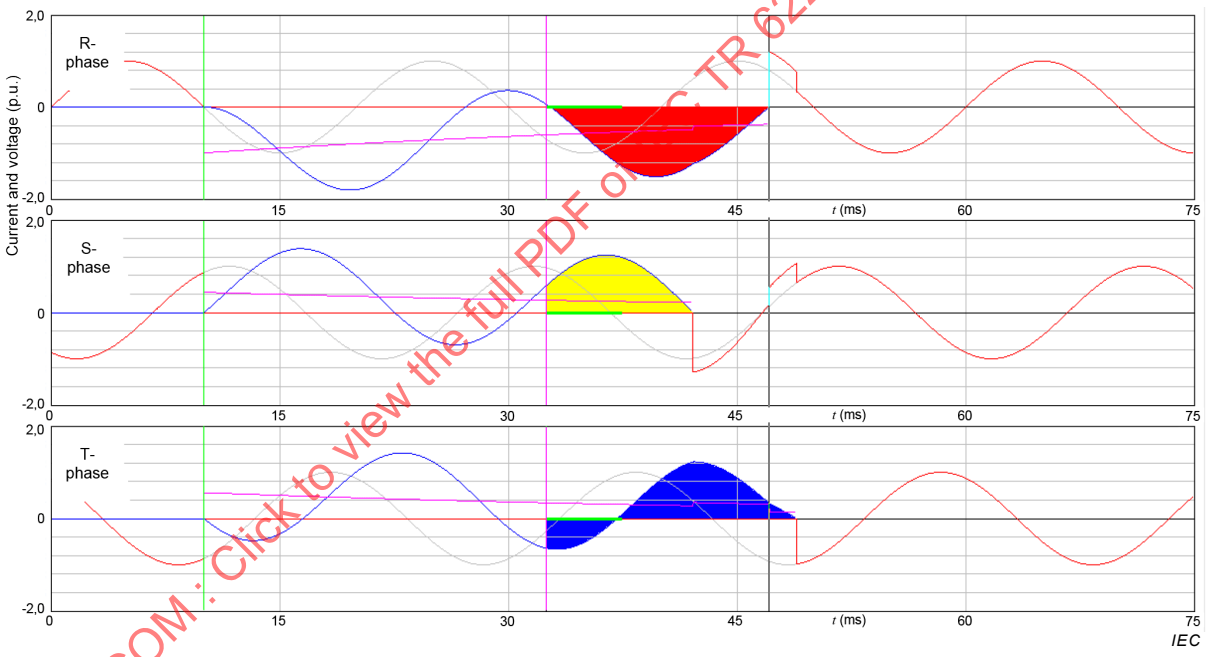

Figure 138b – Case 2 with k_{pp} = 1,3

Figure 138 – Case 2 with interruption of a last pole-to-clear after a major extended loop of current with required asymmetry and longest arcing time

Figure 139 illustrates case 3 obtained when contact separation is delayed by 72°, this test condition is less severe, as last pole that clears in the red phase with a major extended loop has a shorter arcing time.

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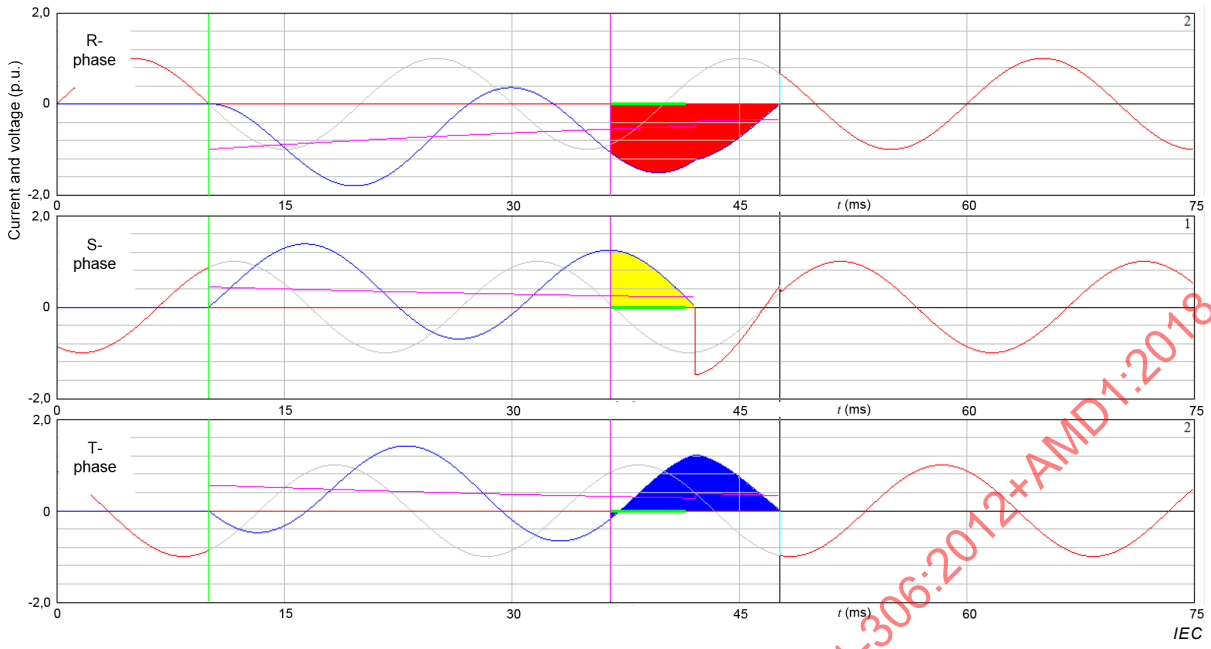

Figure 139 – Case 3 with interruption of a last pole-to-clear after a major extended loop of current with required asymmetry but not the longest arcing time

Figure 140 illustrates case 4 obtained when contact separation is further delayed by 18°. It shows that the first pole clears in the red phase after a major loop with required asymmetry and the longest arcing time for a first-pole-to-clear. It is the second breaking condition for which interruption shall be proved. It should be noted that the major loop with maximum asymmetry to consider for the first-pole-to-clear is the same as seen in case 2 (for a last-pole-to-clear). It is function of the minimum clearing time.

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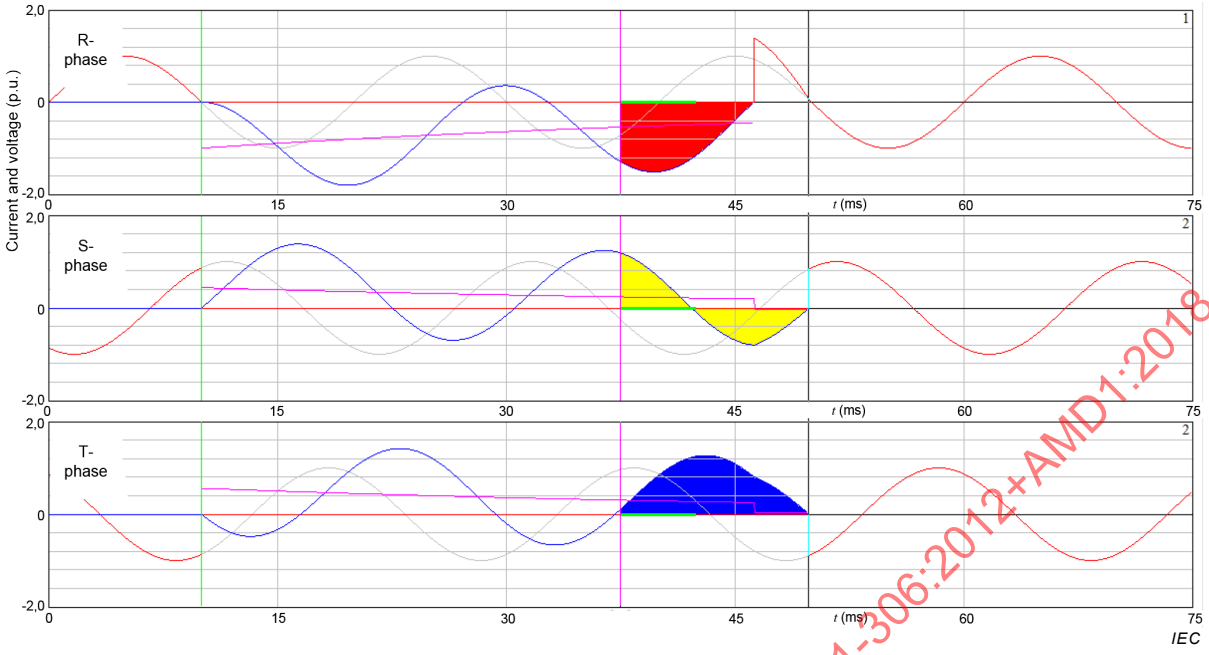

Figure 140 – Case 4 with interruption by the first pole in the red phase after a major loop of current with required asymmetry and the longest arcing time (for a first-pole-to-clear)

The case considered in this example corresponds to the first line of Table 41 in IEC 62271-100:2008/AMD2:2017, i.e. with a minimum clearing time in the interval higher than 10 ms and equal to or lower than 27 ms. The other intervals of minimum clearing time given in Table 41 are the intervals between each possible instant of interruption after a minor loop in the blue phase.

13.4.2 Advice for the choice of the appropriate time constant

A DC time constant of 45 ms is adequate for the majority of actual cases except for rated voltages higher than 800 kV for which the standard DC time constant is 120 ms. Special case time constants, related to the rated voltage of the circuit-breaker, should cover such cases where the standard time constant 45 ms is not sufficient. This may apply, for example, to systems with very high rated voltage (for example 800 kV systems with higher X/R ratio for lines), to some medium voltage systems with radial structure or to any systems with particular system structure or line characteristics. Special case time constants have been defined, taking into account the results of the survey by CIGRE WG13.04 [139] .

When specifying a special case time constant, the following considerations should be taken into account:

a) The time constants referred to in IEC 62271-100:2008 are only valid for three-phase fault currents. The single-phase to ground short-circuit time constant is lower than that for three-phase fault currents.

b) For maximum asymmetrical current, the initiation of the short-circuit current has to take place at system voltage zero in at least one phase.

c) The time constant is related to the maximum rated short-circuit current of the circuit-breaker. If, for example, higher time constants than 45 ms are expected but with a short-circuit current lower than rated, such a case may be covered by the asymmetrical rated short-circuit current test using a 45-ms time constant.

d) The time constant of a complete system is a time-dependent parameter considered to be an equivalent constant derived from the decay of the short-circuit currents in the various branches of that system and is not a real, single time constant.

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e) Various methods for the calculation of the DC time constant are in use, the results of which may differ considerably. Caution should be taken in choosing the right method.

f) When choosing a special case time constant, it has to be kept in mind, that the circuit-breaker is stressed by the asymmetrical current after contact separation. The time instant of contact separation corresponds to the opening time of the circuit-breaker and the reaction time of the protection relay. In this document, this relay time is one half-cycle of power frequency. If the protection time is longer this should be taken into account.

13.4.3 DC component during T100a testing

With the introduction of the special case time constants in IEC 62271-100:2001, the decisive parameters with their respective tolerances that should be followed during interruption of asymmetrical faults need to be defined in order to:

– be able to perform asymmetrical tests with a test circuit having a DC time constant different from the rated DC time constant of the rated short-circuit breaking current, because laboratories are not able to tune the DC time constant of the test circuit. For direct tests, when the DC time constant of the test circuit is higher than the rated DC time constant of the rated short-circuit breaking current, the resulting di/dt and TRV peaks are lower than those that can be seen in service conditions. The reverse situation is also true, mainly with the special case DC time constants (60 ms, 75 ms and 120 ms) introduced in IEC 62271-100:2001;

– be able to use the results obtained from one specific test to cover more than one DC time constant ratings. This concept of asymmetry equivalence may also help the user in establishing equivalence between system needs and the rating requirements.

A lot of calculations made confirm that the former concept of DC component at contact separation (for example IEC 60056 and the first edition of IEC 62271-100:2001) leads to stresses during the tests (including minor and major loop interruptions) being different from those expected under service conditions. That is why IEC 62271-308 was published in 2002. IEC 62271-308 was incorporated in the first amendment to IEC 62271-100:2001.

The only way to obtain that equivalence is to introduce the concept of DC component at current zero. This concept is also applied in IEC 62271-101.

The maximum prospective DC component at current zero required during tests is determined by using the DC component given for the next complete current loop following the minimum interrupting time.

The parameters concerned by general equivalence criteria are:

a) the amplitude of the last current loop (both major loop or major extended loop);

b) duration of the last current loop (both major loop or major extended loop) before interruption;

c) arcing time;

d) di/dt at current zero;

e) TRV peak voltages, waveshape.

The three first points are linked to the arc energy.

To reach the equivalence according to this concept has led to a modification of some tolerances. For example, the tolerance (0 %, +10 %) on the symmetrical value of the test current has been changed in IEC 62271-100:2008/AMD2:2017 to +10 % and −10 % in order to be able to adjust the last current loop amplitude and duration to the required values. For some cases, it may be necessary to decrease or increase these values from the rated symmetrical short-circuit current.

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With this procedure, depending on the actual test parameters, a specific test may cover several ratings if the applicable asymmetry criteria for each rating with their associated tolerances are met.

Annex A gives some guidance on how to use the asymmetry criteria.

13.5 Double earth fault

13.5.1 Basis for specification

This test requirement is limited to applications in non-effectively earthed systems.

In accordance with 6.108 of IEC 62271-100:2008, circuit-breakers applied in non-effectively earthed neutral systems shall be capable of clearing the short-circuit currents that may occur in the case of double earth faults i.e. earth faults on two different phases, one of which occurs on one side of the circuit-breaker and the other one on the other side.

Such a situation can occur if, after a single phase-to-earth fault, the two other phases stay energized long enough to allow another fault to earth to develop on another phase. This situation is unlikely to happen if the healthy phases are opened in a relatively short time after the occurrence of the initial fault. However, it may be provoked by the voltage elevation on healthy phases that is produced by the first fault to earth.

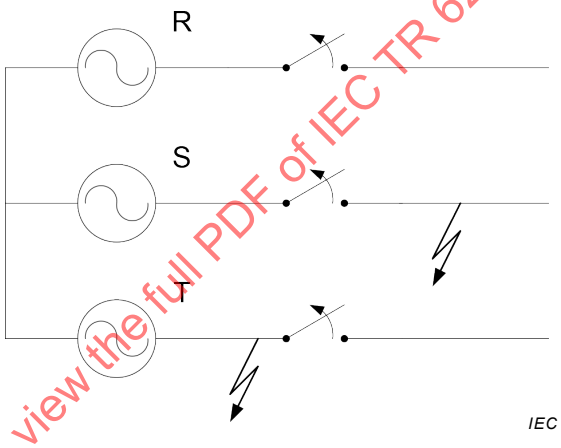

Figure 141 – Representation of a system with a double earth fault

Figure 141 illustrates the case where a fault is present in phase S. Due to the voltage increase on the healthy phases a fault develops on the other side of the circuit-breaker in phase T. The total fault current needs to be interrupted by pole S.

From Figure 141, it can be seen that one pole of the circuit-breaker is required to interrupt a short-circuit under phase-to-phase voltage. As the recovery voltage is higher than in other terminal fault test duties, this breaking condition could be more severe than a terminal fault T100 condition, but, as explained in 13.5.4, the short-circuit current is only 87 % of the rated short-circuit current.

This condition is not covered by test duty T100 and, since it has a low probability of occurrence, IEC 62271-100 requires only one breaking test to be performed. When this standard was established, it was considered that it is only necessary to test with the most severe condition of arcing time, i.e. with a long arcing time corresponding to a high energy content of the arc and with a moving contact position close to the fully open position.

13.5.2 Short-circuit current

The calculation of the short-circuit current is detailed in 13.5.4.

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A symmetrical current is specified in testing, as in test duty T100s, because a symmetrical condition leads to the highest TRV peak possible when compared to the value specified for test duty T100.

13.5.3 TRV

The RRRV is the same as for terminal fault test duty T100s. The voltage factor for the double earth fault is $\sqrt{3}$, since the full phase-to-phase voltage is applied to one pole, whereas it is 1,5 for terminal fault. The di/dt is obtained by multiplying the di/dt value of T100s by $\frac{\sqrt{3}}{2}$. It follows that the rate of rise of recovery voltage is equal to the values of T100s multiplied by $\frac{\sqrt{3}}{1{,}5} \times \frac{\sqrt{3}}{2} = 1$

Specified TRVs with two parameters and four-parameters are determined from the RRRV and a pole-to-clear factor of $\sqrt{3}$. They are given in Table 28 of IEC 62271-100:2008.

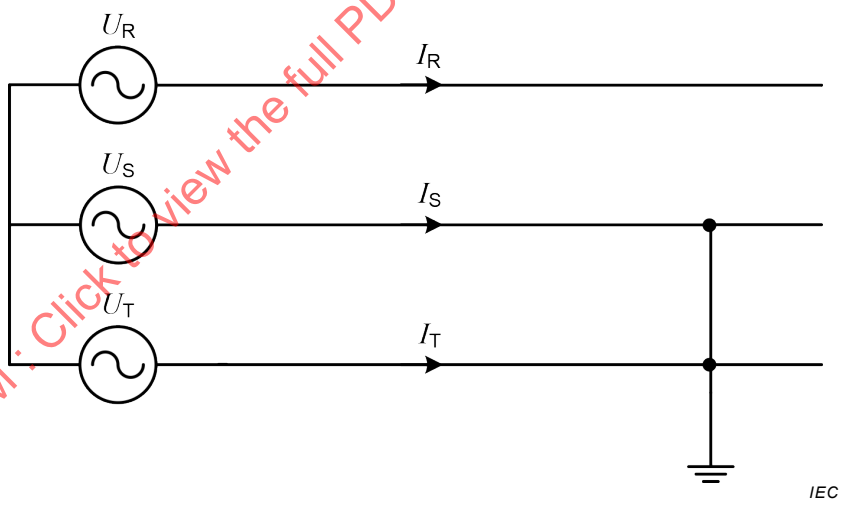
In the case of a two-parameter TRV, t_3 is derived from u_c and the RRRV.

In the case of a four-parameter TRV, u_1 and u_c are calculated on the basis of a pole-to-clear factor of $\sqrt{3}$, t_1 is derived from u_1 and the RRRV and $t_2 = 4 \times t_1$.

13.5.4 Determination of the short-circuit current in the case of a double-earth fault

Figure 142 shows a schematic representation of the fault case illustrated in Figure 141.

Phase supply voltage is U.



Key

U_R, U_S, U_T	Voltages in R, S and T-phase, respectively
I_R, I_S, I_T	Currents in R, S and T-phase, respectively

Figure 142 – Representation of circuit with double-earth fault

The circuit in Figure 142 is analysed using symmetrical components. The indices used are 0 for zero sequence component, 1 for the positive sequence component and 2 for the negative sequence component.

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$I_R = 0 \rightarrow \quad I_0 + I_1 + I_2 = 0$
$U_S = 0 \rightarrow \quad U_0 + a^2 U_1 + a U_2 = 0$
$U_T = 0 \rightarrow \quad U_0 + a U_1 + a^2 U_2 = 0$

with

$a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

$$U_1 = U - X_1 I_1 \tag{178}$$

$$U_2 = -X_2 I_2 \tag{179}$$

$$U_0 = -X_0 I_0 \tag{180}$$

this gives:

$-X_0 I_0 + a^2(U - X_1 I_1) - a X_2 I_2 = 0$
$-X_0 I_0 + a(U - X_1 I_1) - a^2 X_2 I_2 = 0$
$I_1 + I_2 + I_0 = 0$

or,

$$a^2 X_1 I_1 + a X_2 I_2 + X_0 I_0 = a^2 U \tag{181}$$

$$a X_1 I_1 + a^2 X_2 I_2 + X_0 I_0 = a U \tag{182}$$

$$I_1 + I_2 + I_0 = 0 \tag{183}$$

Multiplying Equation (182) with "a" and subtracting Equation (181) leads to:

$$(1 - a) X_2 I_2 + (a - 1) X_0 I_0 = 0 \Rightarrow X_2 I_2 = X_0 I_0 \tag{184}$$

Multiplying Equation (181) with "a" and subtracting Equation (180) leads to:

$$X_1 I_1 (1\text{-}a) + (a\text{-}1) X_0 I_0 = (1\text{-}a) U \rightarrow X_1 I_1 - X_0 I_0 = U \tag{185}$$

A system of 3 equations with 3 unknown is obtained:

$$I_1 + I_2 + I_0 = 0 \tag{186}$$

$$X_2 I_2 = X_0 I_0 \tag{187}$$

$$X_1 I_1 - X_0 I_0 = U \tag{188}$$

Resolution of Equations (186), (187) and (188):

$$I_1 + \frac{X_0 I_0}{X_2} + I_0 = 0$$

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$$I_0 \times \frac{X_2 + X_0}{X_2} = -I_1 \qquad I_0 = -\frac{I_1 X_2}{X_2 + X_0}$$

$$X_1 I_1 + \frac{X_0 X_2}{X_2 + X_0} \times I_1 = U \text{ , or } I_1\left(X_1 + \frac{X_0 X_2}{X_2 + X_0}\right) = U \Rightarrow I_1 = \frac{U}{X_1 + \frac{X_0 X_2}{X_2 + X_0}} \quad (189)$$

and

$$I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad (190)$$

$$I_2 = -I_1 - I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad (191)$$

The current in phase S is given by:

$I_S = I_0 + a^2 I_1 + a I_2$ with $a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

From Equations (190) and (191), and with the standard hypothesis $X_2 = X_1$:

$$I_S = -\frac{X_1 I_1}{X_1 + X_0} + a^2 I_1 - a\frac{X_0 I_1}{X_1 + X_0}$$

$$\frac{I_S}{I_1} = \frac{-X_1 + a^2 X_1 + a^2 X_0 - a X_0}{X_1 + X_0} = \frac{-X_1\left(3/2 + j\frac{\sqrt{3}}{2}\right) - jX_0\sqrt{3}}{X_1 + X_0}$$

Using the equation for I_1 given in Equation (188), the current for the double earth fault (I_{def}) is then:

$$I_{def} = I_S = \frac{-U\sqrt{3}}{X_1 + 2X_0}\left(\frac{\sqrt{3}}{2} + \frac{j}{2} + j\frac{X_0}{X_1}\right)$$

For non-effectively earthed networks $X_0 >> X_1$, which gives:

$$I_{def} = \frac{U\sqrt{3}}{X_1 + 2X_0} \times j\frac{X_0}{X_1} = -j\frac{U\sqrt{3}}{2X_1}$$

The three-phase short-circuit is given by $I_{sc} = U/X_1 \rightarrow I_{def} = -j\frac{\sqrt{3}}{2} I_{sc}$, or $|I_{def}| = 0{,}87|I_{sc}|$.

Fault currents relative to the three-phase short-circuit current are shown in Figure 143 for this case and for other fault cases.

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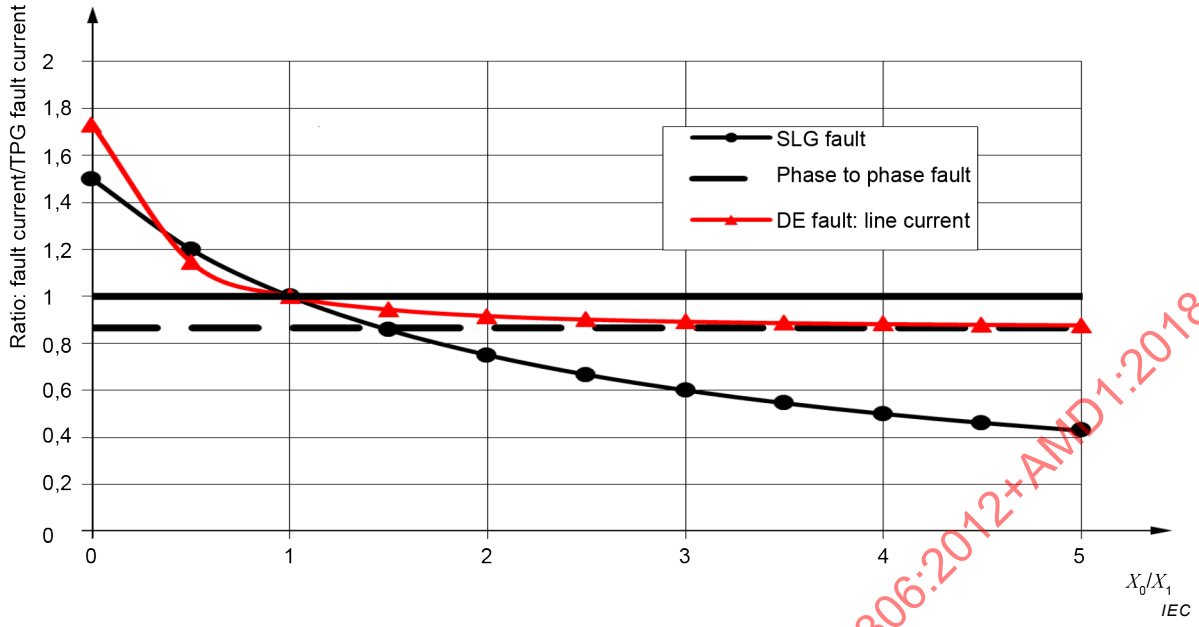

Key

SLG fault	Single-line to earth fault	TPG fault	Three-phase to earth fault
DE fault	Double earth fault	Solid line	Three-phase to earth current

Figure 143 – Fault currents relative to the three-phase short-circuit current

13.6 Break time

The break time of a circuit-breaker is the maximum interval between the instant of initialization of the opening operation (i.e. energizing of the trip circuit) and the instant of interruption of the current in all three phases during terminal fault test-duties T30, T60 and T100s under the following conditions:

– rated auxiliary supply voltage and frequency;

– rated pressures for operation, insulation and interruption;

– an ambient air temperature of (20 ± 5) °C.

The break time is defined based on the minimum arcing time because the longest recorded arcing time during the tests can be longer than under the actual field condition.

Terminal fault tests are carried out at the minimum auxiliary supply voltage and/or pressures for operation and/or interruption. For convenience of testing, the auxiliary supply voltage may be the rated or maximum value as long as it does not affect the making or breaking capability. (The operating times of some circuit-breakers may vary with the auxiliary supply voltage). In order to verify the break time during these test-duties, the maximum break time should be amended to take account of the lower auxiliary supply voltage and pressures as follows:

$$t_{\mathrm{bmax}} = t_{\mathrm{or}} + t_{\mathrm{am}} + t_{\mathrm{w}} - \frac{18^{\mathrm{o}}}{360^{\mathrm{o}}} \times T$$

where

t_{bmax} is the maximum determined break time;

t_{or} is the opening time under rated conditions (recorded during no-load operation at rated supply voltage and frequency of closing and opening devices and of auxiliary circuits, at rated pressure for operation and at a ambient temperature of 20 °C ± 5 °C)

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t_{am} is the longest of the recorded minimum arcing times during test-duties T30, T60 and T100s;

$\frac{18^o}{360^o} \times T$ takes the uncertainty in the determination of the minimum arcing time into account;

T is one period of power frequency (20 ms for 50 Hz, 16,7 ms for 60 Hz) and t_w is the necessary interrupting window expressed in ms:

– for single-phase tests in substitution for three-phase conditions
  - non-effectively earthed neutral systems: $t_{we} = 150 - d\alpha$
  - effectively earthed neutral systems: $t_{we} = 180 - d\alpha$
– for three-phase tests

  $t_{we} = 60 - d\alpha$

  t_{we} is expressed in electrical degrees

$$t_w = \frac{t_{we}}{360^o} \times T$$

$d\alpha$ is the tripping impulse step in the search for the minimum arcing time, it is equal to 18 electrical degrees.

If the maximum break time determined according to this procedure exceeds the break time, the test-duty that has given the longest break time may be repeated with auxiliary supply voltage and pressure for operation and interruption at their rated values.

NOTE The break time during a make-break operation may be longer than that of a single break operation for some circuit-breaker designs. Such longer break times may impact system protection strategy and stability if the delay is longer than the relay time. Users should advise the manufacturer of the maximum allowable break time during make-break operations.

14 ~~Double earth fault~~ Synthetic making and breaking tests

~~14.1 Basis for specification~~

~~This test requirement is limited to applications in non-effectively earthed systems.~~

~~In accordance with 6.108 of IEC 62271-100:2008, circuit-breakers applied in non-effectively earthed neutral systems shall be capable of clearing single-pole the short-circuit currents which may occur in case of double earth faults i.e. earth faults on two different phases, one of which occurs on one side of the circuit-breaker and the other one on the other side.~~

~~Such a situation can occur if, after a single phase-to-earth fault, the two other phases stay energized long enough to allow another fault to earth to develop on another phase. This situation is unlikely to happen if the healthy phases are opened in a relatively short time after the occurrence of the initial fault. However it may be provoked by the voltage elevation on healthy phases that is produced by the first fault to earth.~~

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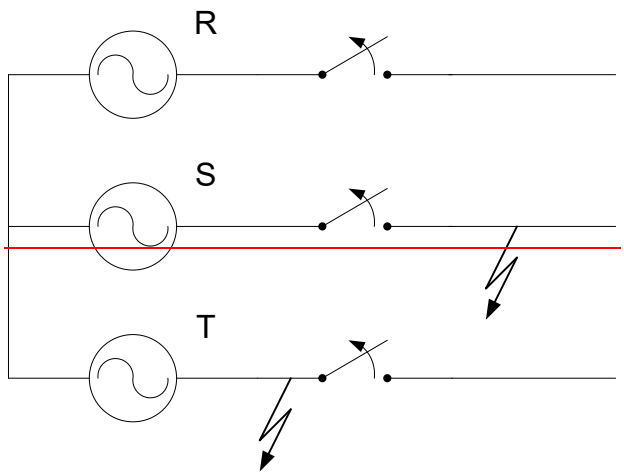

Figure 72 – Representation of a system with a double-earth fault

Figure 72 illustrates the case where a fault is present in phase S. Due to the voltage increase on the healthy phases a fault develops on the other side of the circuit-breaker in phase T. The total fault current needs to be interrupted by pole S.

From Figure 72 it can be seen that one pole of the circuit-breaker is required to interrupt a short-circuit under phase-to-phase voltage. As the recovery voltage is higher than in other terminal fault test duties, this breaking condition could be more severe than a terminal fault T100 condition, but, as explained in 14.4, the short-circuit current is only 87 % of the rated short-circuit current.

This condition is not covered by test duty T100 and, since it has a low probability of occurrence, IEC 62271-100 requires only one breaking test to be performed. When this standard was established it was considered that it is only necessary to test with the most severe condition of arcing time, i.e. with a long arcing time corresponding to a high energy content of the arc and with a moving contact position close to the fully open position.

14.2 Short-circuit current

The calculation of the short-circuit current is detailed in 14.4.

A symmetrical current is specified in testing, as in test duty T100s, because a symmetrical condition leads to the highest TRV peak possible when compared to the value specified for test duty T100.

14.3 TRV

The RRRV is the same as for terminal fault test duty T100s. The voltage factor for the double earth fault is √3, since the full phase-to-phase voltage is applied to one pole, whereas it is 1,5 for terminal fault. The di/dt is obtained by multiplying the T100s value by $\frac{\sqrt{3}}{2}$. It follows that the rate of rise of recovery voltage is equal to the values of T100s multiplied by $\frac{\sqrt{3}}{1,5} \times \frac{\sqrt{3}}{2} = 1$

Specified TRVs with two parameters (rated voltages less than 100 kV) and four-parameters (rated voltages equal or higher than 100 kV) are determined from the RRRV and a pole-to-clear factor of √3. They are given in Table 28 of IEC 62271-100:2008.

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In the case of a two-parameter TRV, t_3 is derived from u_c and the RRRV.

In the case of a four-parameter TRV, u_1 and u_c are calculated on the basis of a pole-to-clear factor of √3, t_1 is derived from u_1 and the RRRV and $t_2 = 4 \times t_1$.

14.4 Determination of the short-circuit current in the case of a double-earth fault

Figure 73 shows a schematic representation of the fault case illustrated in Figure 17.

Phase supply voltage is U.

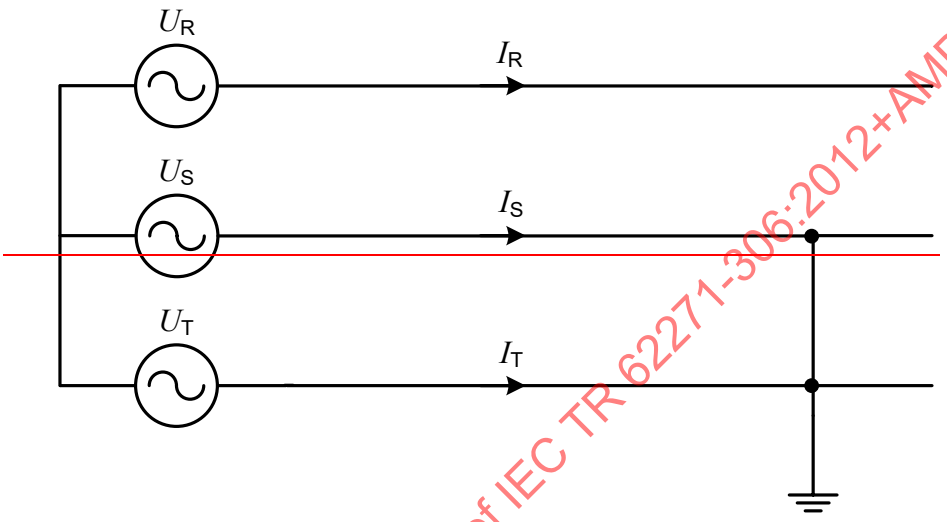

Figure 73 – Representation of circuit with double-earth fault

The use of symmetrical components leads to the following equations:

$I_R = 0 \quad \rightarrow \quad I_1 + I_2 + I_0 = 0$

$U_S = 0 \quad \rightarrow \quad U_0 + a^2 U_1 + a U_2 = 0$

$U_T = 0 \quad \rightarrow \quad U_0 + a U_1 + a^2 U_2 = 0$

with

$a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

$$U_1 = U - X_1 I_1 \qquad (82)$$

$$U_2 = -X_2 I_2 \qquad (83)$$

$$U_0 = -X_0 I_0 \qquad (84)$$

this gives:

$-X_0 I_0 + a^2 (U - X_1 I_1) - a X_2 I_2 = 0$

$-X_0 I_0 + a (U - X_1 I_1) - a^2 X_2 I_2 = 0$

$I_1 + I_2 + I_0 = 0$

or,

$$a^2 X_1 I_1 + a X_2 I_2 + X_0 I_0 = a^2 U \qquad (85)$$

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$$aX_1I_1 + a^2X_2I_2 + X_0I_0 = aU \quad (86)$$

$$I_1 + I_2 + I_0 = 0 \quad (87)$$

Multiplying Equation (86) with "a" and subtracting Equation (85) leads to:

$$(1 - a)X_2I_2 + (a - 1)X_0I_0 = 0 \Rightarrow X_2I_2 = X_0I_0 \quad (88)$$

Multiplying Equation (85) with "a" and subtracting Equation (84) leads to:

$$X_1I_1(1-a) + (a-1)X_0I_0 = (1-a)U \rightarrow X_1I_1 - X_0I_0 = U \quad (89)$$

A system of 3 equations with 3 unknown is obtained:

$$I_1 + I_2 + I_0 = 0 \quad (90)$$

$$X_2I_2 = X_0I_0 \quad (91)$$

$$X_1I_1 - X_0I_0 = U \quad (92)$$

Resolution of Equations (90), (91) and (92):

$$I_1 + \frac{X_0 I_0}{X_2} + I_0 = 0$$

$$I_0 \times \frac{X_2 + X_0}{X_2} = -I_1 \qquad I_0 = \frac{I_1 X_2}{X_2 + X_0}$$

$$X_1 I_1 + \frac{X_0 X_2}{X_2 + X_0} \times I_1 = U, \text{ or } I_1\left(X_1 + \frac{X_0 X_2}{X_2 + X_0}\right) = U \Rightarrow I_1 = \frac{U}{X_1 + \frac{X_0 X_2}{X_2 + X_0}} \quad (93)$$

and

$$I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad (94)$$

$$I_2 = -I_1 - I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad (95)$$

The current in phase S is given by:

$I_S = I_0 + a^2 I_1 + a I_2$ with $a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

From Equations (94) and (95), and with the standard hypothesis $X_2 = X_1$:

$$I_S = -\frac{X_1 I_1}{X_1 + X_0} + a^2 I_1 - a\frac{X_0 I_1}{X_1 + X_0}$$

$$\frac{I_S}{I_1} = \frac{-X_1 + a^2 X_1 + a^2 X_0 - aX_0}{X_1 + X_0} = \frac{-X_1\left(3/2 + j\frac{\sqrt{3}}{2}\right) - jX_0\sqrt{3}}{X_1 + X_0}$$

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~~Using the equation for I_1 given in Equation (93), the current for the double earth fault (I_{def}) is then:~~

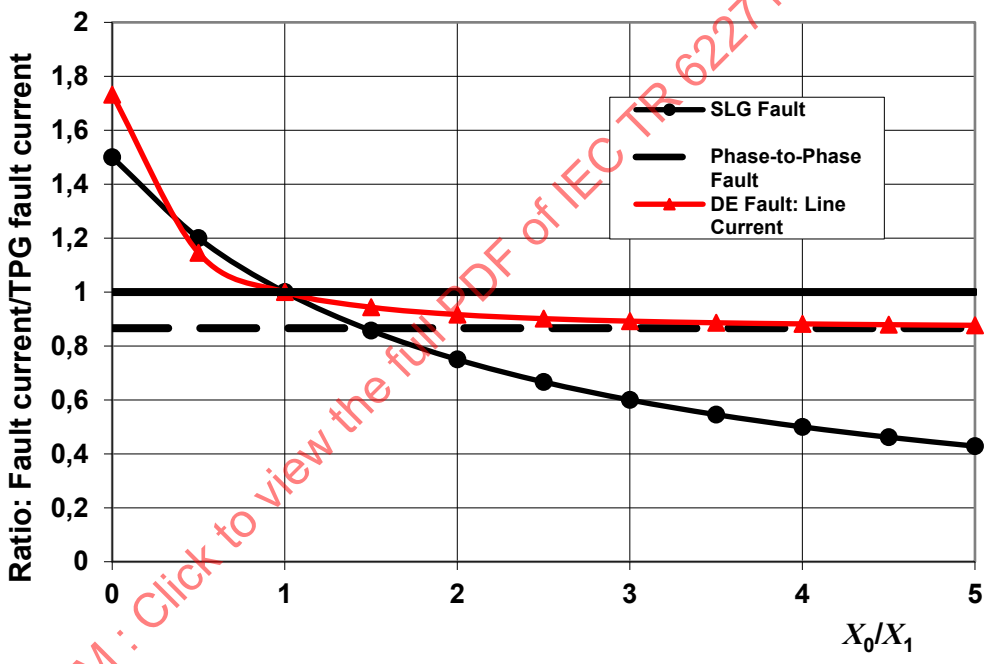
$$I_{def} = I_S = \frac{-U\sqrt{3}}{X_1 + 2X_0}\left(\frac{\sqrt{3}}{2} + \frac{j}{2} + j\frac{X_0}{X_1}\right)$$

~~For non-effectively earthed networks $X_0 >> X_1$, which gives:~~

$$I_{def} = -\frac{U\sqrt{3}}{X_1 + 2X_0} \times j\frac{X_0}{X_1} = -j\frac{U\sqrt{3}}{2X_1}$$

~~The three-phase short-circuit is given by $I_{sc} = U/X_1 \rightarrow I_{def} = -j\frac{\sqrt{3}}{2} I_{sc}$, or $|I_{def}| = 0{,}87|I_{sc}|$.~~

~~Fault currents relative to the three-phase short-circuit current are shown in Figure 74 for this case and for other fault cases.~~



~~Key~~

~~SLG fault~~	~~Single line to earth fault~~	~~TPG fault~~	~~Three phase to earth fault~~
~~DE fault~~	~~Double earth fault~~	~~Solid line~~	~~Three phase to earth current~~

~~Figure 74 – Fault currents relative to the three-phase short-circuit current~~

14.1 General

With the increasing voltage and current ratings of circuit-breakers, the total available short-circuit power of a high power laboratory has to be increased accordingly. The investments required to increase the short-circuit power are very high. In order to still be able to perform the correct type tests on circuit-breakers with the available short-circuit power, synthetic tests are performed.

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Requirements for synthetic testing and examples of synthetic circuits are given in IEC 62271-101.

Generally a synthetic test circuit consists of separate current and voltage circuits (see Figure 144). During the high-current interval, the short-circuit current will be fed from a current circuit (source providing the necessary current at a reduced voltage). This reduced voltage should have an amplitude of sufficient magnitude to prevent the arc voltage from distorting the short-circuit current in such a way that the circuit-breaker is not stressed in the same way as under system conditions. For tests that need less power (e.g. capacitive current switching tests), some synthetic test circuits using a single source can also be used.

When the current is interrupted by the circuit-breaker under test (TB in Figure 144), the voltage circuit will give the correct voltage stresses across the contact gap. An auxiliary circuit-breaker (AB in Figure 144) is used to separate the voltage circuit from the current circuit, thus avoiding that the high-voltage from the voltage circuit stresses the current circuit.

The principle used for the making operation is similar. The voltage circuit first provides the correct voltage stress during the closing operation and as soon as the pre-arcing occurs, the current circuit will then provide the correct short-circuit current.

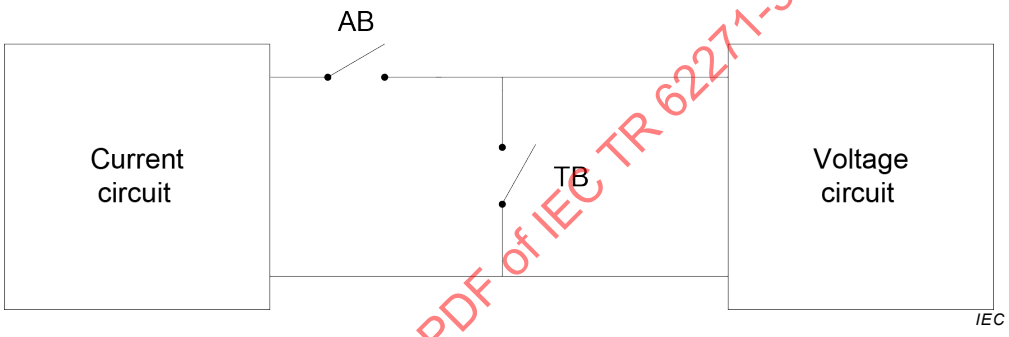

Figure 144 – Principle of synthetic testing

In order for a synthetic test to be valid, the following requirements should be met:

– the arc energy in the contact gap should be equal to that of a direct test;
– the di/dt at current zero should be in accordance with the current and frequency specified;
– the recovery voltage should appear immediately after current zero i.e. without delay;
– the prospective TRV should be at least equal to the required TRV;
– the voltage source should have a sufficient power to avoid excess damping of the transient process by the post arc current.

Synthetic testing allows in general testing at one particular arcing time per operation. In order to cover the full extinguishing window, it may be necessary to use re-ignition circuits.

14.2 Current injection methods

14.2.1 General

In a synthetic test circuit using current injection, the superposition of the currents takes place shortly before the zero of the power-frequency short-circuit current. A current of smaller amplitude but higher frequency, derived from the voltage circuit, is superimposed either in the test circuit-breaker or in the auxiliary circuit-breaker. The instant of switching in this injected current is selected by means of a current-dependent control circuit. This instant should be such that the character of the resulting current wave in the test circuit-breaker corresponds to that of the specified breaking current prior to the current zero during the interval of significant change of arc voltage.

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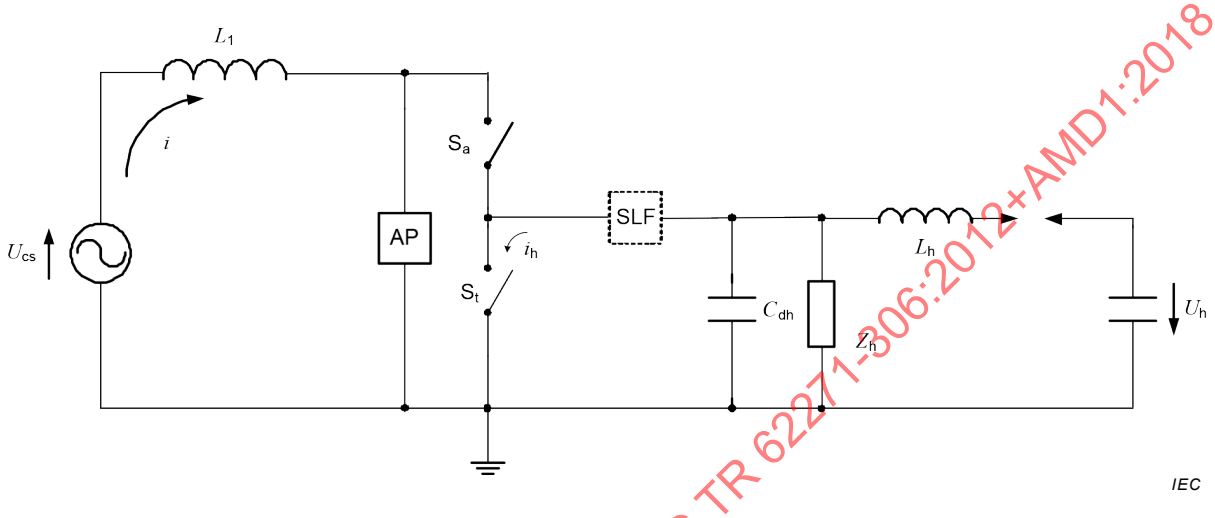
In this way, the circuit-breaker under test is automatically connected into the voltage circuit after the interruption of the current in the auxiliary circuit-breaker, so there will be no delay between the current stress and the application of the voltage stress.

14.2.2 Current injection circuit with the voltage circuit in parallel with the test circuit-breaker (parallel circuit)

Figure 145 shows the simplified circuit diagram of a current injection circuit with the voltage circuit connected in parallel with the test circuit-breaker.



Key

U_{cs}	voltage of current circuit	C_{dh}	capacitance for time delay of voltage circuit
L_1	inductance of current circuit	L_h	inductance of voltage circuit
AP	arc prolonging circuit	U_h	charging voltage of voltage circuit
S_a	auxiliary circuit-breaker	i	current of the current circuit
S_t	test circuit-breaker	i_h	injected current
Z_h	equivalent surge impedance of voltage circuit	SLF	short-line-fault circuit (for the corresponding tests)

Figure 145 – Typical current injection circuit with voltage circuit in parallel with the test circuit-breaker

The voltage circuit is switched in shortly before the zero of the power-frequency short-circuit current, prior to the interaction interval. At this time, the high-frequency oscillatory current i_h is superimposed on the power-frequency short-circuit current i, with the same polarity to give a resultant test current in the test circuit-breaker.

After the auxiliary circuit-breaker interrupts the power-frequency short-circuit current i, the test circuit-breaker is connected only to the voltage circuit and i_h is the only remaining current. The voltage circuit also provides the recovery voltage across the test circuit-breaker after the current is interrupted.

Figure 146 shows an example of injection timing. The two points of inflection typically indicate the start of the current injection in the test circuit-breaker and the interruption of the power-frequency short-circuit current by the auxiliary circuit-breaker. The waveshape of the transient recovery voltage can be adjusted by varying the values of Z_h and C_{dh} (Figure 145), to obtain compliance with the requirements of IEC 62271-100 (see 4.1.4 of IEC 62271-101:2012).

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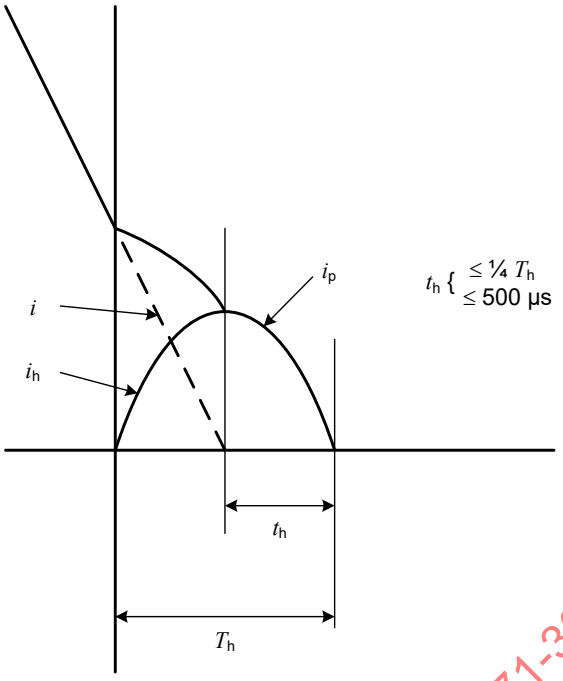

Key

i	current in the auxiliary circuit-breaker	T_h	duration of one period of the injected current
i_h	injected current	t_h	time during which the arc is fed only by the injected current
i_p	current in the test circuit-breaker		

Figure 146 – Injection timing for current injection scheme with the circuit given in Figure 145

14.2.3 Current injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker (series circuit)

As the series current injection method is not used by laboratories, it is no longer under consideration.

14.2.4 Determination of the interval of significant change of the arc voltage

To determine the interval of significant change of the arc voltage that occurs immediately prior to current zero, the following method may be applied, dependent on individual arc voltage characteristics.

The arc voltages of circuit-breakers vary considerably in general shape. In many cases, the arc voltage is not steady but fluctuates about a mean value. This mean value is obtained by drawing a smooth curve in the middle, between the maximum and minimum arc voltage levels (Figure 147). This curve can be used to identify significant changes. The shape of mean arc voltage characteristics may also vary widely.

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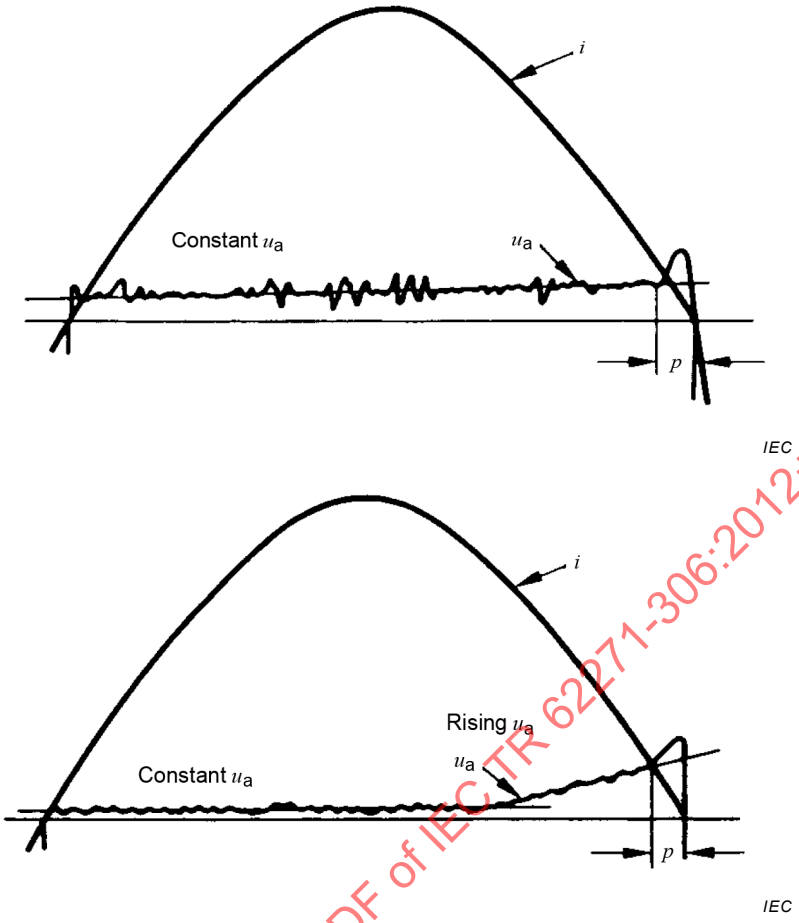

Key

i	current	p	interval of significant change of arc voltage
u_a	arc voltage		

Figure 147 – Examples of the determination of the interval of significant change of arc voltage from the oscillograms

Most circuit-breakers show a nearly constant or steadily rising arc voltage during the current loop, with an appreciable increase just prior to current zero. In such cases, it is not difficult to determine from the oscillogram the instant at which a significant change begins. For this purpose, it is preferable to use an oscillograph giving a relatively large deflection for the arc voltage and having a time scale that is fast enough to enable the interval of significant change of arc voltage to be measured accurately.

In some cases, it may be difficult to determine the interval of significant change of arc voltage because

a) the arc voltage remains nearly constant or steadily rises during the current loop almost to the instant of current zero,

b) changes in the arc voltage occur considerably before the current zero.

In these cases, an injection current frequency as low as possible should be used, taking account also of the requirements in 4.2.1 of IEC 62271-101:2012.

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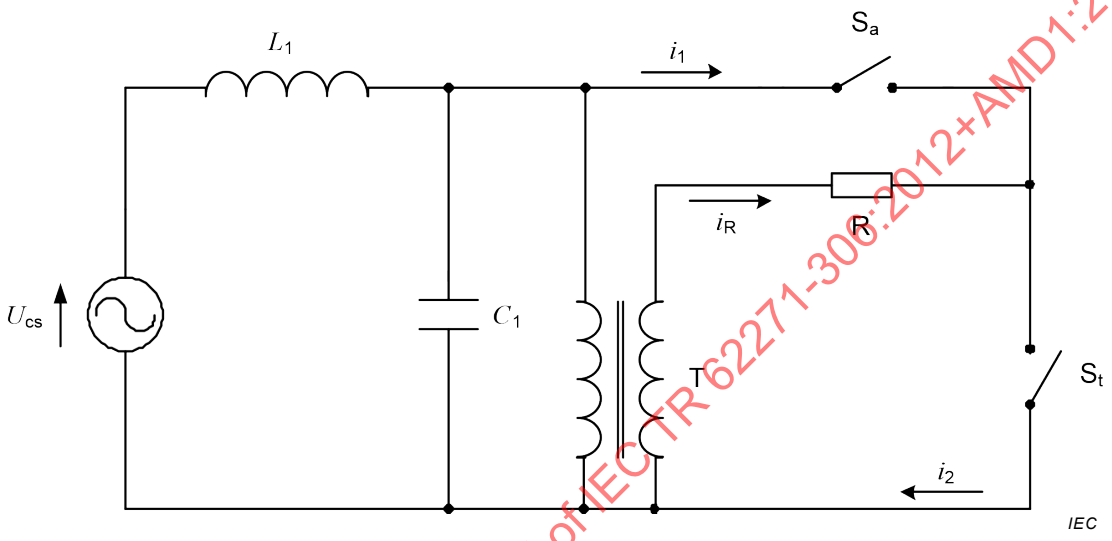
14.3 Duplicate transformer circuit

14.3.1 Principle of the method

In the duplicate test circuit (also known as the Skeats circuit), the current is supplied from a current circuit to the series combination of the auxiliary and the test circuit-breaker. The high voltage is applied to the test circuit-breaker via a resistance from a transformer (or auto-transformer), the primary of which is connected to the current circuit across the auxiliary and test circuit-breakers.

Figure 148 shows the principal layout of the circuit.



Key

U_{cs}	voltage of the current circuit	i_1	current through the auxiliary circuit-breaker
L_1	inductance of current circuit	i_2	current through the test circuit-breaker
C_1	capacitance of the current circuit which together with L_1 controls the first part of the TRV	i_R	current through resistor R
T	transformer	S_a	auxiliary circuit-breaker
R	phase-shifting resistor	S_t	test circuit-breaker

Figure 148 – Transformer or Skeats circuit

During the high-current interval, the arc voltages of the test and auxiliary circuit-breakers induce a current, i_R in the high-voltage circuit that adds to the current through the test circuit-breaker, $i_2 = i_1 + i_R$. The current in the auxiliary breaker will thus reach zero and interrupt before the test circuit-breaker. If the arc voltages are assumed nearly constant, the test circuit-breaker current will go through zero at a time Δt after the interruption of the auxiliary breaker approximately given by:

$$\Delta t = \frac{n(u_{aa} + u_{at}) - u_{at}}{n \times \hat{u}_{cs}} \times \frac{L_2}{R}$$

where

n is the transformer ratio;

u_{aa}, u_{at} are the arc voltages in S_a and S_t, respectively;

$\hat{u}_{cs}$ is the voltage peak of the current circuit;

L_2 = $n^2 L_1 + L_T$ (effective inductance in the high-voltage circuit);

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L_T is the leakage inductance of T.

During the interval Δt, the rate of change of the current through the test circuit-breaker di_2/dt will approximately attain the value:

$$\frac{di_2}{dt} = -\frac{n \times \hat{u}_{cs}}{L_2} = -\frac{n\,\hat{u}_{cs}}{n^2 L_1 + L_T}$$

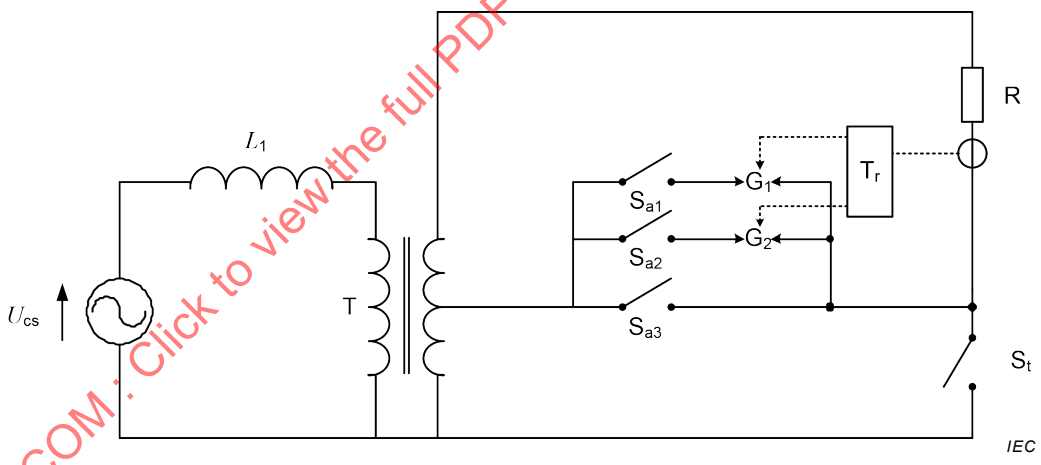
i.e. di_2/dt will be lower than the prospective uninfluenced value. This value is reduced by a factor of the same magnitude as the transformer ratio n.

By choosing the value R of the resistance R sufficiently large, the time interval Δt could be kept small. On the other hand, a high value will increase the damping of the TRV. For circuit-breakers with post-arc current, the value may be further restricted. Values of R in the range some kΩ are normally used, giving $\Delta t \leq 10$ μs.

The test circuit could be used when testing the dielectric recovery of a circuit-breaker. It could further be used for closing tests and could be extended to work with several full voltage applications.

14.3.2 Practical arrangement of the circuit

A practical circuit arrangement is shown in Figure 149. The circuit illustrated in Figure 149 can be used to apply full recovery voltage in three consecutive current zeros in an opening operation by opening the auxiliary circuit-breakers S_{a1}, S_{a2} and S_{a3} in turn. The spark gaps G_1 and G_2 are triggered to restore the current if the test circuit-breaker fails to interrupt in the first and second current zero respectively.



Key

U_{cs}	voltage of the current circuit	S_{a1}, S_{a2}, S_{a3}	auxiliary circuit-breakers
L_1	inductance of current circuit	S_t	test circuit-breaker
T	transformer	T_r	triggering circuit
R	phase-shifting resistor	G_1, G_2	triggered gaps

Figure 149 – Triggered transformer or Skeats circuit

Figure 149 can also apply full voltage stresses at both closing and opening in a CO operating cycle. The test circuit-breaker S_t closes against full voltage (S_{a1} is open) and, when it pre-strikes, one of the spark gaps, e.g. G_2, is triggered to make the current circuit (S_{a2} is closed). S_{a3} is closed before the opening of the test circuit-breaker and used as auxiliary

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circuit-breaker at the first current zero. If necessary, a second current zero could be tested by means of G_1 and S_{a1}.

In a similar manner the two opening operations in an auto-reclosing operation can be fully tested.

14.4 Voltage injection methods

14.4.1 General

In a synthetic test circuit using voltage injection, the current circuit provides the entire short-circuit current for the test circuit-breaker and also, after current zero, the first part of the transient recovery voltage.

By suitable choices of its voltage and natural frequency, the correct values of the power factor, current and first part of the TRV can be obtained.

About the time of the first peak of the transient recovery voltage of the current circuit, the voltage circuit is switched in by means of a voltage-dependent control circuit in such a way that the specified transient recovery voltage is continued and so that there will be no delay between the current stress and the voltage stress.

A voltage injection test circuit is not valid for tests where attention is paid to the short-line fault tests and terminal fault tests with ITRV, because

– the source-side impedance does not correspond to network (or direct test circuit) conditions during the interaction interval;
– the di/dt deviates from the prospective value during a (short) time interval just before current zero.

14.4.2 Voltage injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker (series circuit)

Figure 150 shows the simplified circuit diagram of a voltage injection circuit with the voltage circuit connected in parallel with the auxiliary circuit-breaker. The current circuit supplies the entire short-circuit current stress. A capacitor of suitable value is connected in parallel with the auxiliary circuit-breaker. After the current zero of the power-frequency short-circuit current, this capacitor transmits the entire transient recovery voltage of the current circuit to the test circuit-breaker, passing the necessary energy for the post-arc current.

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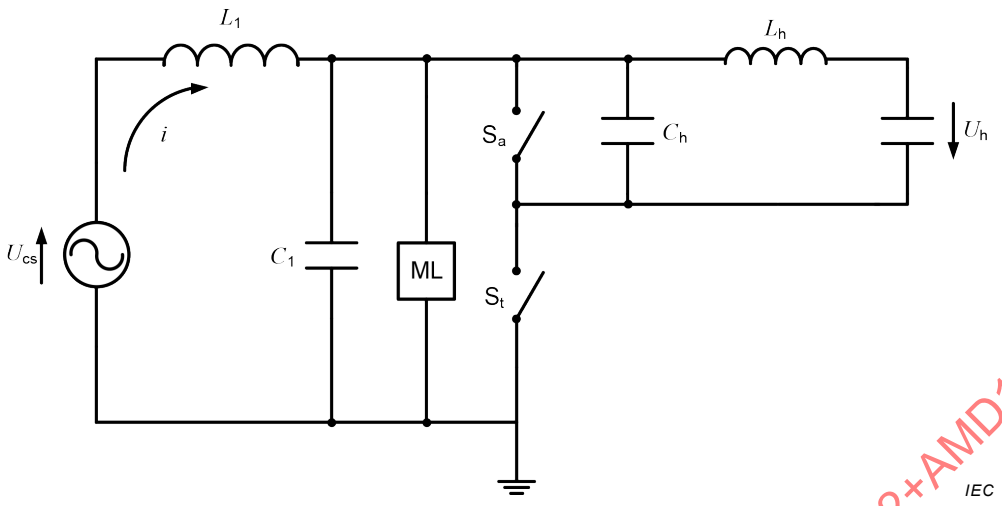

Key

U_{cs}	voltage of current circuit	S_t	test circuit-breaker
L_1	inductance of current circuit	C_h	capacitance of voltage circuit which together with L_h controls the major part of the TRV
C_1	capacitance of current circuit which together with L_1 controls the first part of the TRV	L_h	inductance of voltage circuit
ML	multi-loop reignition circuit	U_h	charging voltage of voltage circuit
S_a	auxiliary circuit-breaker	i	current of the current source

Figure 150 – Typical voltage injection circuit diagram with voltage circuit in parallel with the auxiliary circuit-breaker (simplified diagram)

About the time of the first peak of this transient voltage, the voltage circuit will be switched in and from this moment onwards the transient recovery voltages of both circuits are added together to form the transient recovery voltage across the test circuit-breaker.

Figure 151 shows the current in the test circuit-breaker and the waveshape of the voltage across the auxiliary circuit-breaker and test circuit-breaker. The auxiliary circuit-breaker is stressed only by the voltage of the voltage circuit. Both components of the voltage across the test circuit-breaker are superimposed to produce the transient recovery voltage, the waveshape of which can be adjusted by varying C_h and C_1 in conjunction with additional components – not shown in Figure 150 – to obtain compliance with the requirements of IEC 62271-100 (see 4.1.4 of IEC 62271-101:2012).

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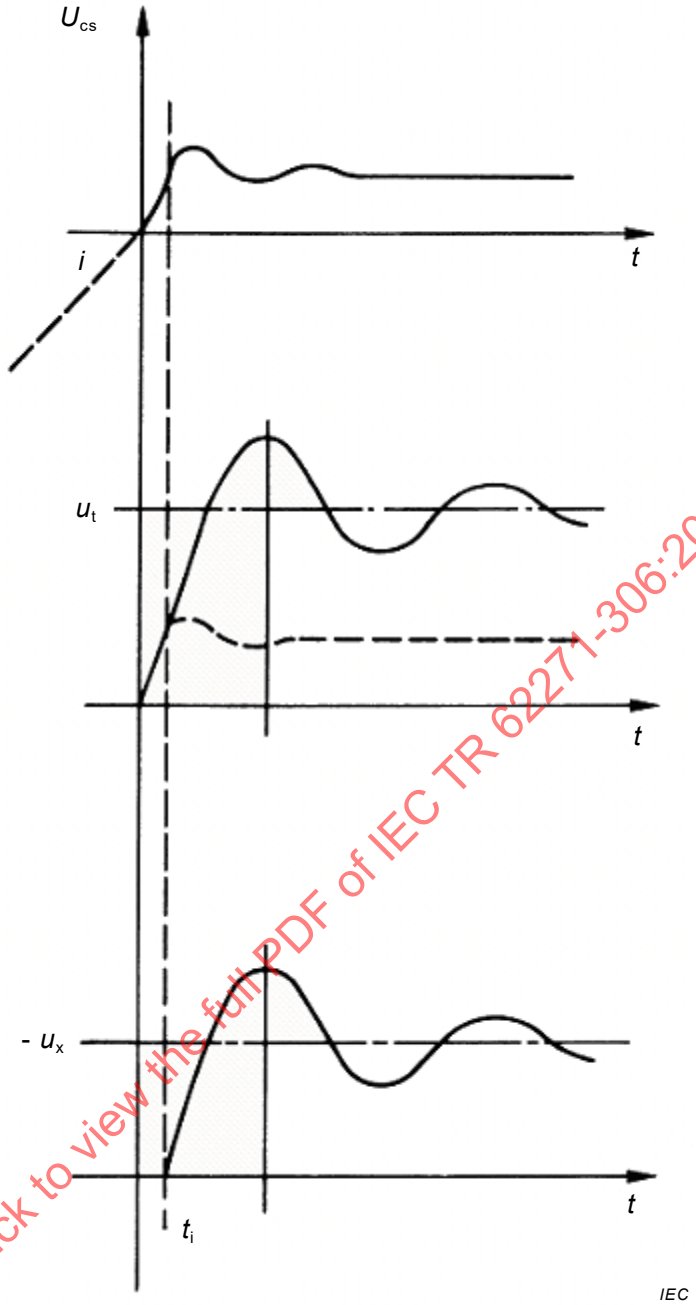

Key

i	power-frequency current in test and auxiliary circuit-breakers	u_t	voltage across test circuit-breaker
U_{cs}	TRV from current circuit	u_x	voltage across auxiliary circuit-breaker
		t_i	instant of voltage injection

Figure 151 – TRV waveshapes in a voltage injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker

14.4.3 Voltage injection circuit with the voltage circuit in parallel with the test circuit-breaker

This voltage injection circuit is similar to the one described above except that the voltage circuit is in parallel with the test circuit-breaker instead of the auxiliary circuit-breaker. It is not in common usage.

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14.5 Current distortion

14.5.1 General

Current distortion is a well-known factor that should be considered during synthetic testing. Subclauses 14.5.2, 14.5.3 and 14.5.4 give a basic analysis using simplified methods. In practice, digital calculations by computers may be more appropriate where various arc voltage waveshapes can be introduced.

14.5.2 Current distortion immediately prior to current zero

The interaction interval begins when the arc voltage starts to change significantly as the current approaches zero. The change of the arc voltage during this time influences the shape and the rate-of-change of the current immediately before current zero.

This deviation from the prospective current curve is caused by the distortion current, which mainly flows in the low time constant impedance, taking into account all parameters of the actual circuit.

The particular way in which the current approaches zero is responsible for the physical conditions of the medium between the arcing contacts of a circuit-breaker at current zero. The major interaction between circuit and circuit-breaker is caused by the arc voltage charging and discharging capacitances and influencing di/dt just before zero.

In a simplified circuit, as in Figure 152 representing a short-circuit in service or a direct test, the voltage u supplies an arc current i with the appropriate arc voltage u_a. Parallel to the arc is a capacitor C.

If it is assumed that the arc voltage $u_a = 0$, then a prospective short-circuit current i_p (see Figure 153) will flow through the arc, the magnitude and waveshape of this current being determined by the inductance L, the voltage u, the frequency of this voltage and the moment of current initiation.

If it is assumed that the supply voltage $u = 0$ and that an arc voltage exists, then the arc voltage will produce a current flow. This current i_d (see Figure 154) is the distortion current, which will flow partly as i_{dL} through the inductance L, and partly as i_{dC} through the capacitance C. For this condition, the following equations apply:

$$u_a - L \times \frac{d}{dt}(i_{dL}) = 0$$

and

$$C \frac{d}{dt}(u_a) - i_{dC} = 0$$

From these, the following equation for i_d can be obtained:

$$i_d = i_{dL} + i_{dC} = \frac{1}{L}\int u_a \, dt + C \times \frac{d}{dt}(u_a)$$

If both of the voltages, u and u_a are present (see Figure 155), then the resulting actual current is given by:

$$i = i_p - i_d$$

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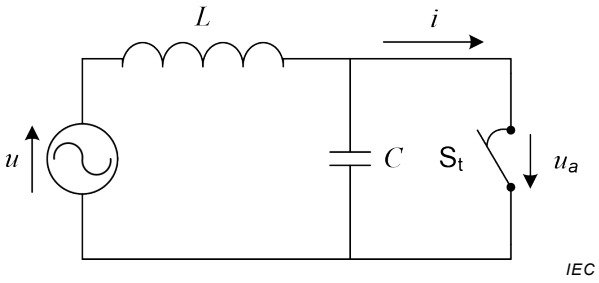

Figure 152 – Direct test circuit, simplified diagram

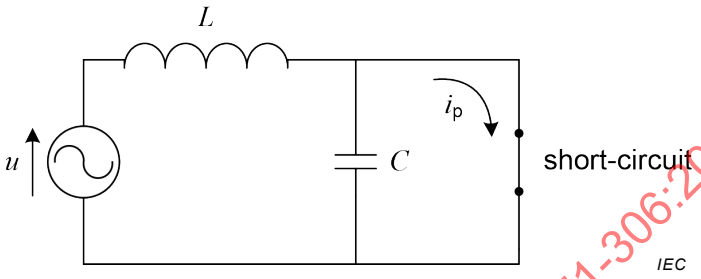

Figure 153 – Prospective short-circuit current flow

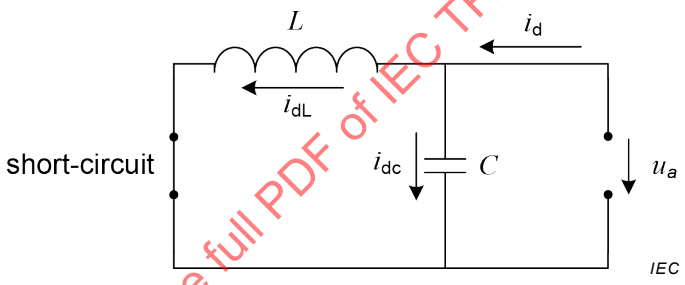

Figure 154 – Distortion current flow

Key to Figure 152, Figure 153 and Figure 154

u	voltage supplying the direct circuit	C	capacitance of the full power direct circuit, together with L controlling the transient recovery-voltage of the circuit
u_a	arc voltage of circuit-breaker	S_t	circuit-breaker
L	inductance of the full power direct circuit, together with u controlling the short-circuit current	i	actual current
i_p	prospective short-circuit current	i_{dL}	distortion current through L
i_{dc}	distortion current through C	i_d	total distortion current

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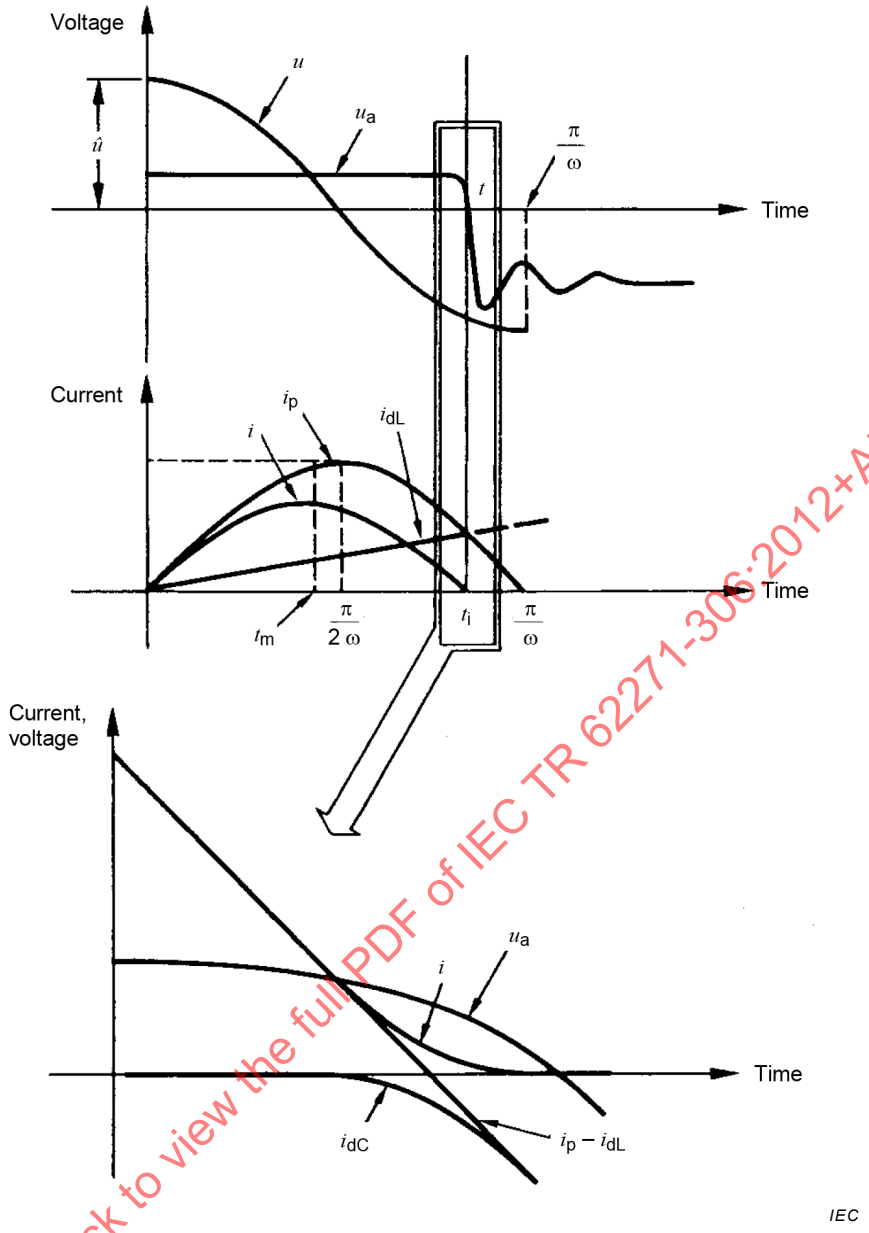

Key

u	voltage supplying the direct circuit	i_{dC}	distortion current through C
u_a	arc voltage of circuit-breaker	i	actual current
i_p	prospective short-circuit current	i_{dL}	distortion current through L
t_m	instant of peak value	t_i	duration of the actual current loop

Figure 155 – Distortion current

14.5.3 Current distortion during the high-current interval

14.5.3.1 General

During this interval, the arc voltage generates a distortion current i_d, in the circuit. i_d is superimposed on the total current.

By comparison with the prospective current, the resulting arc current exhibits distortion in four physical aspects: current amplitude, loop duration, arc-energy and di/dt.

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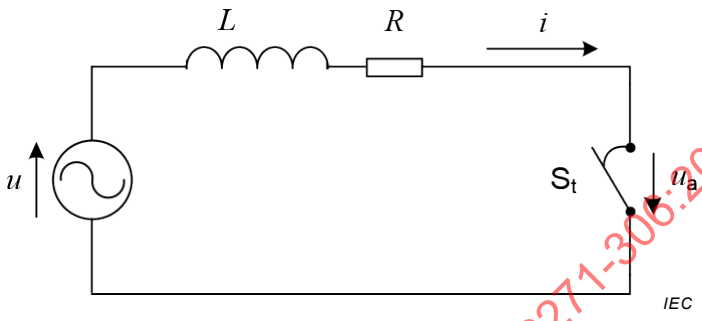
To evaluate the influence of the arc voltage, it is sufficient, in practice, to consider the current amplitude and the loop duration.

As a first approximation, two different arc voltage characteristics can be considered, namely:

a) a constant arc voltage $u_a = U_a$;

b) a linearly rising arc voltage $u_a = S \times t$, where S is the linear rate-of-rise of the arc voltage.

Since the current through the capacitor C (see Figure 152) will be small during this period of arcing, the simplified diagram of Figure 156 is adequate.



Key

u	voltage supplying the direct circuit	R	resistance of the direct circuit
u_a	arc voltage of circuit-breaker	i	actual current
L	inductance of the full power direct circuit, together with u controlling the short-circuit current		

Figure 156 – Simplified circuit diagram for high-current interval

14.5.3.2 Distortion during one loop of arcing related to a symmetrical current

The following equations are derived, where the resistance in Figure 156 is neglected since the effect of this during the single loop is negligible. Some results are given in Figure 157 and Figure 158.

Calculations are made based on the characteristics shown in Figure 157 and Figure 158.

$\hat{u} = \omega L \times \hat{i}_p$ peak value of voltage of current circuit

$\hat{i}_p$ peak value of prospective current

$\hat{i}$ peak value of actual current (reduced by arc voltage)

t_m instant of peak value $\hat{i}$

a) *Ratio of current amplitudes*

– for constant arc voltage:

$$\frac{\hat{i}}{\hat{i}_p} = \sin(\omega \times t_m) - \frac{U_a}{\hat{u}} \times \omega\, t_m$$

– for linearly rising arc voltage:

$$\frac{\hat{i}}{\hat{i}_p} = \sin(\omega \times t_m) - \frac{S\omega}{2\,\hat{u}}\, t_m^2$$

b) *Actual current loop duration* T_1 (reduced by arc voltage)

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– for constant arc voltage

$$\sin(\omega T)_1 = \frac{U_a\,\omega}{\hat{u}}\,T_1$$

– for linearly rising arc voltage:

$$\sin(\omega T)_1 = \frac{S\omega}{2\,\hat{u}}\,T_1^2$$

In Figure 159 and Figure 160, the relative reduction of current amplitude $\Delta i/\hat{\imath}_p$ and current loop duration $\Delta t/T_p$ are given as a function of ratio $U_a/\hat{u}$ for a constant arc voltage and of ratio $S\times T_a/2\times\hat{u}$ for a linearly rising arc voltage, respectively, where:

$\Delta i = \hat{\imath}_p - \hat{\imath}$,

$\Delta t = T_p - T_1$

T_p = prospective current loop duration

T_a = actual arcing time ($T_a = T_1$ for one loop of arcing, see Figure 157 and Figure 158).

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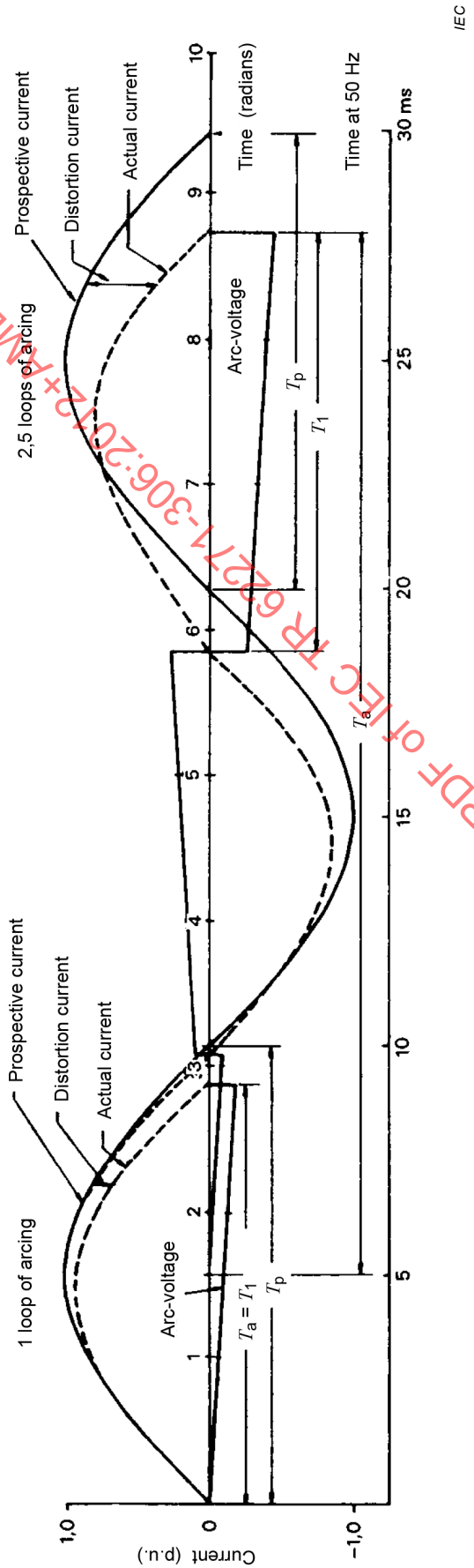

Key

T_a actual arcing time

T_p loop duration of the prospective current

T_1 loop duration of the actual current

Figure 157 – Current and arc voltage characteristics for symmetrical current and constant arc voltage

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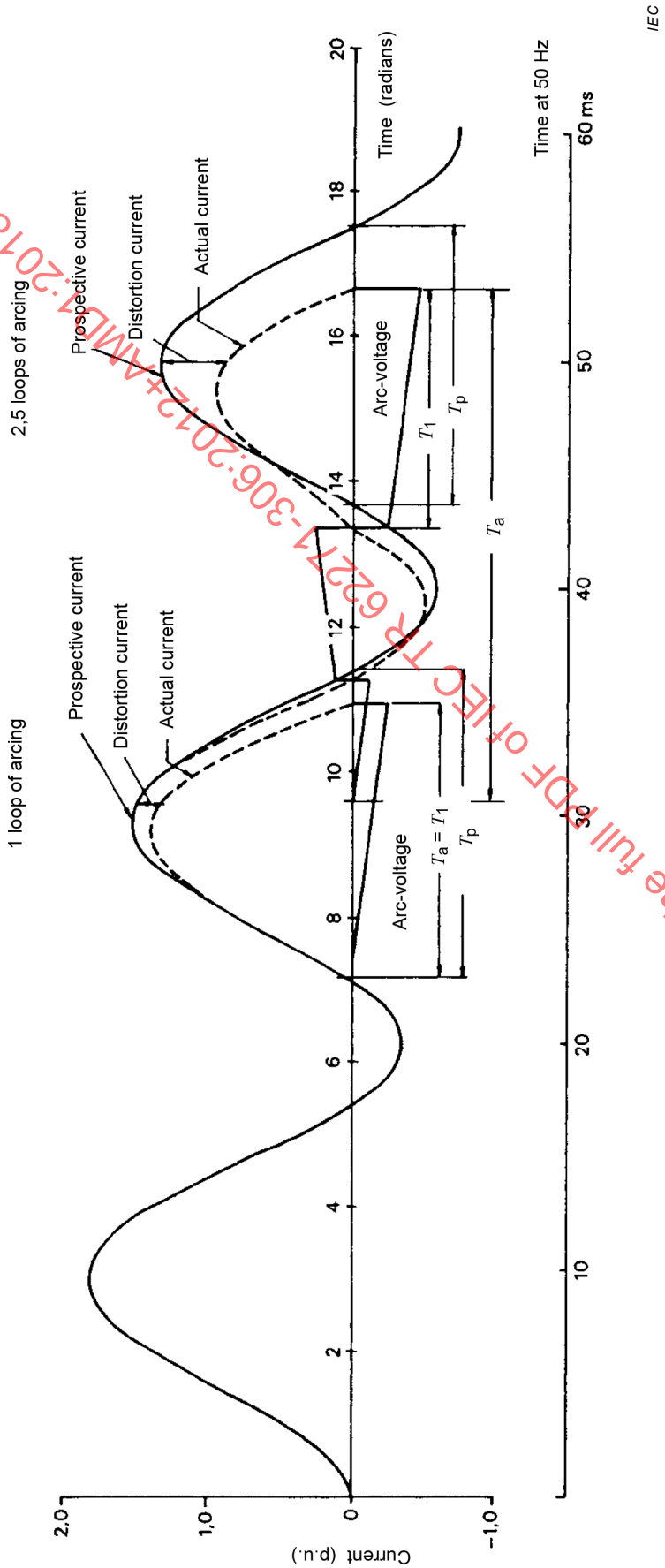

Key

T_a actual arcing time

T_p loop duration of the prospective current

T_1 loop duration of the actual current

Figure 158 – Current and arc voltage characteristics for asymmetrical current and constant arc voltage

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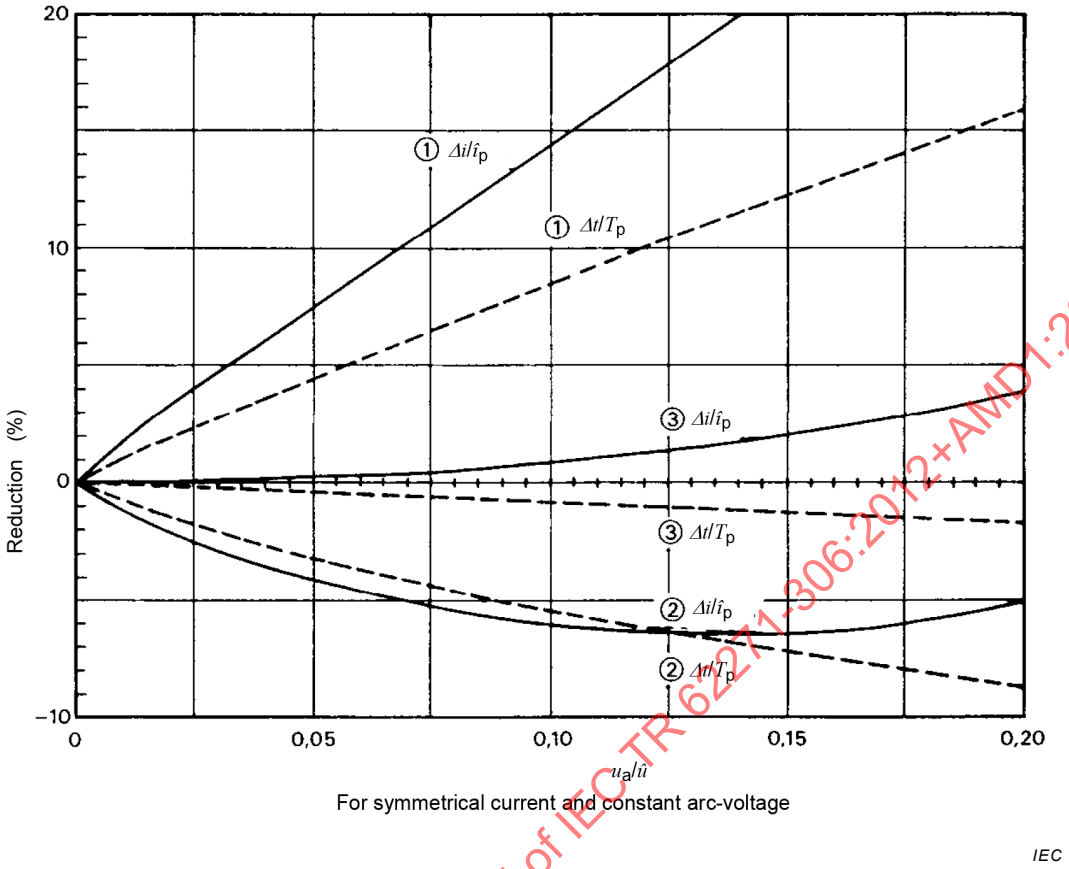

① 1 loop of arcing

② 2 loops of arcing

③ 2,5 loops of arcing

See Figure 157.

Key

$\Delta i/\hat{i}_p$ relative reduction of current amplitude

$\Delta t/T_p$ relative reduction of duration of current loop

$u_a/\hat{u}$ ratio of arc voltage to supply voltage

Figure 159 – Reduction of amplitude and duration of final current loop of arcing for symmetrical current and constant arc voltage

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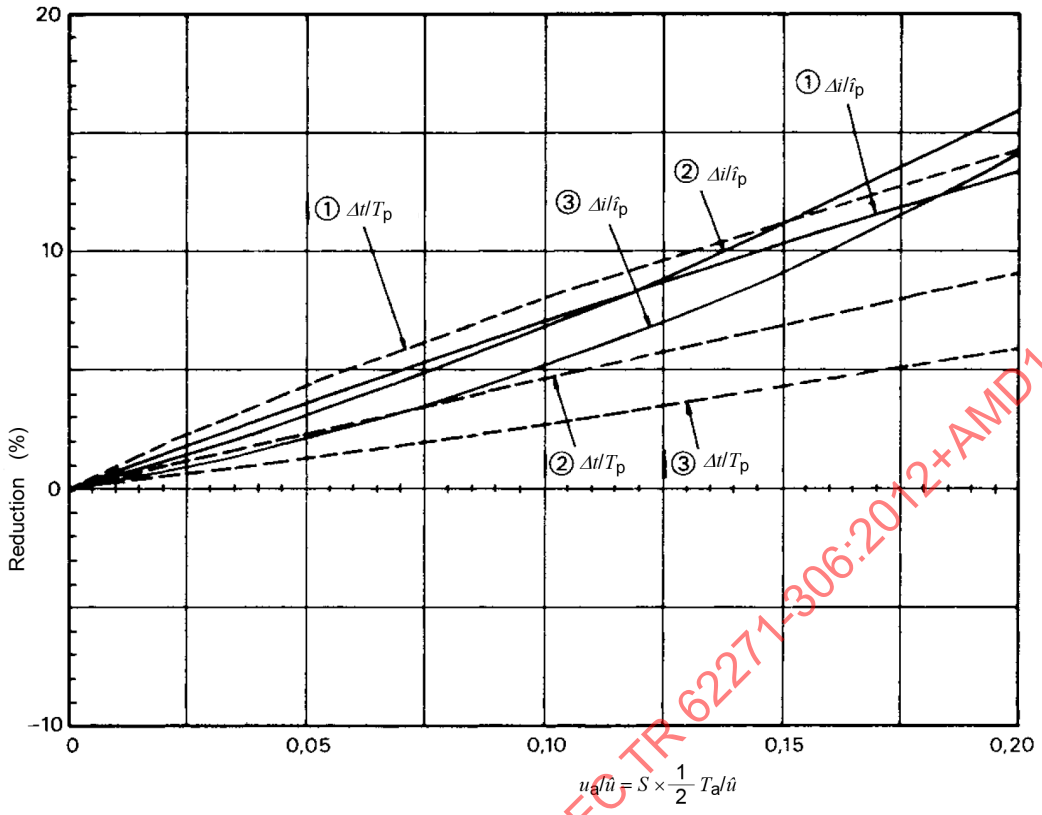

① 1 loop of arcing

② 2 loops of arcing

③ 2,5 loops of arcing

See Figure 157.

Key

$\Delta i/\hat{i}_p$ relative reduction of current amplitude

$\Delta t/T_p$ relative reduction of duration of current loop

$u_a/\hat{u}$ ratio of arc voltage to supply voltage

Figure 160 – Reduction of amplitude and duration of final current loop of arcing for symmetrical current and linearly rising arc voltage

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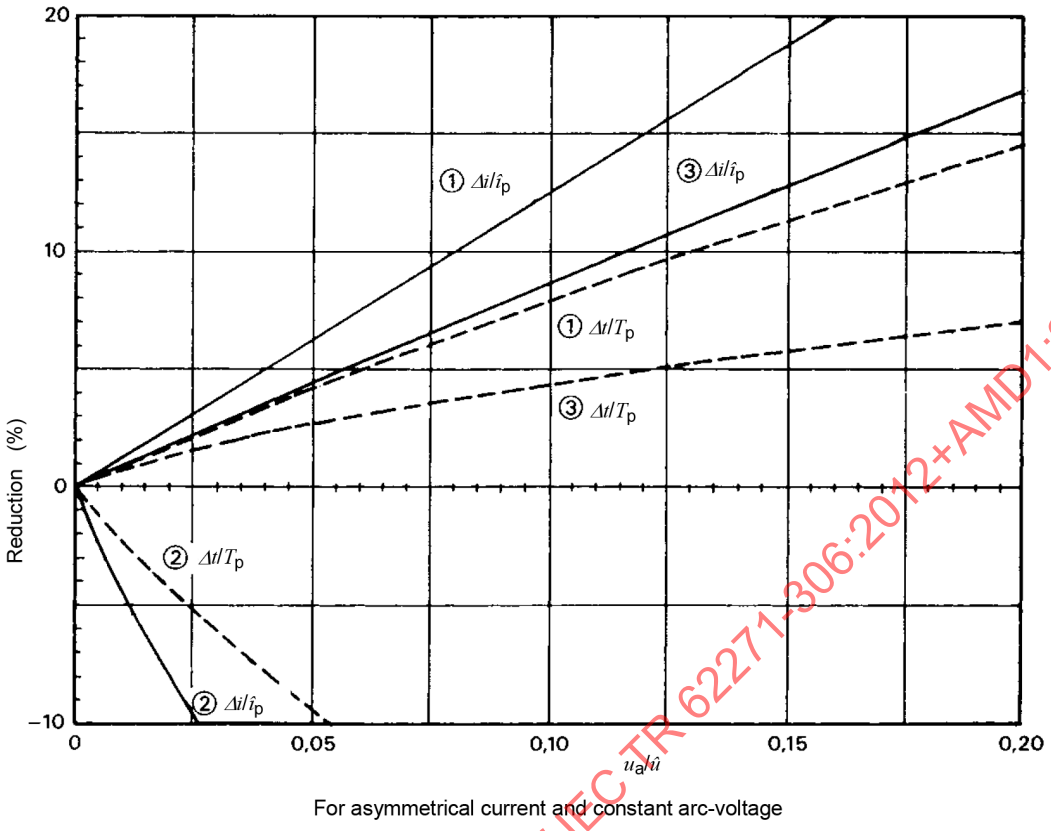

① 1 loop of arcing

② 2 loops of arcing

③ 2,5 loops of arcing

See Figure 158.

Key

$\Delta i/\hat{i}_p$	relative reduction of current amplitude	$u_a/\hat{u}$	ratio of arc voltage to supply voltage
$\Delta t/T_p$	relative reduction of duration of current loop		

Figure 161 – Reduction of amplitude and duration of final current loop of arcing for asymmetrical current and constant arc voltage

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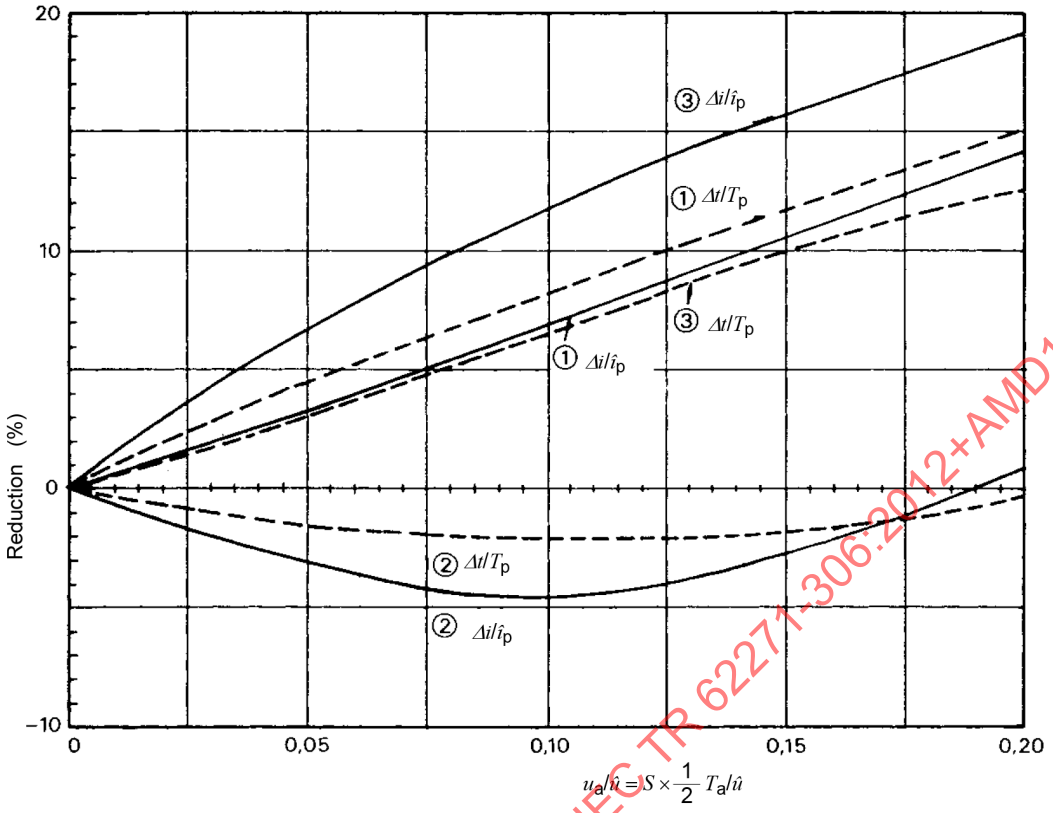

① 1 loop of arcing

② 2 loops of arcing

③ 2,5 loops of arcing

See Figure 158.

Key

$\Delta i/\hat{i}_p$	relative reduction of current amplitude	$u_a/\hat{u}$	ratio of arc voltage to supply voltage
$\Delta t/T_p$	relative reduction of duration of current loop		

Figure 162 – Reduction of amplitude and duration of final current loop of arcing for asymmetrical current and linearly rising arc voltage

14.5.3.3 Distortion in general case

The distortion currents in the case of both symmetrical and asymmetrical currents including more than one loop of arcing are obtained by the following equations which are applicable for the case of constant and linearly rising arc voltages. These calculations are based on a circuit as in Figure 156 where the L/R time constant of the supply impedance is introduced. The p.u. prospective current is given by:

$$i_p/\hat{i}_p = \sin(\omega t + \omega t_1 - \varphi) - \sin(\omega t_1 - \varphi) \times e^{-\frac{R}{L}t}$$

where

t is the time coordinate counting from the instant of current initiation;

t_1 is the time interval between the beginning of the positive voltage loop and current initiation;

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φ is the arctan $\frac{\omega L}{R}$ for symmetrical current $\varphi = \omega t_1$.

The per unit distortion currents are

$i_d/\hat{i}_p = C$ for the first loop of arcing,
$i_d/\hat{i}_p = D - E$ for the second loop of arcing,
$i_d/\hat{i}_p = D - F + G$ for the third loop of arcing,

where C, D, E, F and G are defined as follows:

a) *for constant arc voltage*:

$$C = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t_{cs})}\right]$$

$$D = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t'_0 - t_{cs})}\right] e^{-\frac{R}{L}(t - t'_0)}$$

$$E = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t'_0)}\right]$$

$$F = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t''_0 - t'_0)}\right] e^{-\frac{R}{L}(t - t''_0)}$$

$$G = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t''_0)}\right]$$

where

$M = \frac{U_a}{\hat{u}}$ = the ratio between the arc voltage and the peak value of the power-frequency voltage

$$\cos\varphi = \frac{R}{\sqrt{R^2 + (\omega L)^2}}$$

where

t_{cs} is the instant of contact separation

t_0', t_0'' is the instants at the end of each current loop

b) *for linearly rising arc voltage:*

$$C = \frac{M}{\cos\varphi}\left[(t - t_{cs}) - \frac{L}{R}\left(1 - e^{-\frac{R}{L}(t - t_{cs})}\right)\right]$$

$$D = \frac{M}{\cos\varphi}\left[(t'_0 - t_{cs}) - \frac{L}{R}\left(1 - e^{-\frac{R}{L}(t'_0 - t_{cs})}\right)\right] e^{-\frac{R}{L}(t - t'_0)}$$

$$E = \frac{M}{\cos\varphi}\left[(t - t'_0) - \frac{L}{R}\left(1 - e^{-\frac{R}{L}(t - t'_0)}\right) + (t'_0 - t_{cs}) \times \left(1 - e^{-\frac{R}{L}(t - t'_0)}\right)\right]$$

$$F = \frac{M}{\cos\varphi}\left[(t''_0 - t'_0) - \frac{L}{R}\left(1 - e^{-\frac{R}{L}(t''_0 - t'_0)}\right) + (t'_0 - t_{cs}) \times \left(1 - e^{-\frac{R}{L}(t''_0 - t'_0)}\right)\right] e^{-\frac{R}{L}(t - t''_0)}$$

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$$G = \frac{M}{\cos\varphi}\left[(t - t_0'') - \frac{L}{R}(1 - e^{-\frac{R}{L}(t - t_0'')}) + (t_0'' - t_{cs}) \times (1 - e^{-\frac{R}{L}(t - t_0'')})\right]$$

where

$$M = \frac{S \times T_a}{2\,\hat{u}}$$

Relative reductions of current amplitudes and loop durations related to the last arcing loop for some typical cases are given in Figure 159 to Figure 162.

For symmetrical current, values are given for constant arc voltage as a function of ratio $U_a/\hat{u}$ in Figure 159 and for linearly rising arc voltage as a function of the ratio $S \times T_a/2\hat{u}$ in Figure 160. For asymmetrical current, the corresponding results are given in Figure 161 and Figure 162.

For arcing times, three typical values, i.e. for 1, 2 and 2,5 loops, are introduced. In the case of asymmetrical current contact parting positions have been selected starting about 1,5 cycles after current initiation.

The modifying of arc voltage is much dependent on not only arc voltage but also arcing time and current asymmetry, therefore an exact evaluation for each case is necessary.

NOTE In order to be able to compare the curves relevant to either type of arcing, suitable values have been chosen for the arc voltages: the value at the last current zero for linearly rising arc voltage is twice the value U_a for the constant arc voltage.

14.5.4 Examples of estimation of the parameters of the distorted current

14.5.4.1 General

In the following, some examples of application of the methods of evaluation of the distorted current shown in 14.5.2 and 14.5.3 are given for the single pole test of a 123 kV circuit-breaker.

For the synthetic test examples, equal arc voltages and contact parting positions of both the test and the auxiliary circuit-breaker are assumed.

14.5.4.2 Symmetrical current test

14.5.4.2.1 Constant arc voltage

Direct test

Rated voltage $U_r = 123$ kV

Single pole test voltage $U_t = \frac{123 \times 1{,}3}{\sqrt{3}} = 92$ kV

Mean value of constant arc voltage (last loop) $U_a = 1$ kV

Therefore: $\frac{U_a}{\hat{u}} = \frac{1}{92 \times \sqrt{2}} = 0{,}007\,7$

by calculation for one loop of arcing (see 14.5.3): $\frac{\Delta i}{\hat{i}_p} = -1{,}2\,\%$

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and $\frac{\Delta t}{T_p} = -0{,}7\ \%$

Synthetic test

Current circuit voltage U_1 = 31 kV

Mean value of constant arc voltage (test and auxiliary circuit-breaker, last loop) $U_{as} = 2U_a$ = 2 kV

therefore: $\frac{U_{as}}{\hat{u}} = \frac{2}{31 \times \sqrt{2}} = 0{,}046$

from Figure 159 for one loop of arcing $\frac{\Delta i}{\hat{i}_p} = -7\ \%$

and: $\frac{\Delta t}{T_p} = -4{,}5\ \%$

14.5.4.2.2 Linearly rising arc voltage

Direct test

Single pole test voltage U_t = 92 kV as above

Linearly rising arc voltage $\frac{S \times T_a}{2} = 3\ \text{kV}$

therefore: $\frac{S \times T_a}{2\hat{u}} = \frac{3}{92\sqrt{2}} = 0{,}023$

from Figure 160 for one loop of arcing $\frac{\Delta i}{\hat{i}_p} = -1{,}7\ \%$

and $\frac{\Delta t}{T_p} = -2{,}2\ \%$

Synthetic test

Current circuit voltage U_1 = 31 kV as above

Linearly rising arc voltage (test and auxiliary circuit-breaker) $\frac{S \times T_a}{2} = 2 \times 3 = 6\ \text{kV}$

therefore: $\frac{S \times T_a}{2\hat{u}} = \frac{6}{31\sqrt{2}} = 0{,}137$

from Figure 160 for one loop of arcing $\frac{\Delta i}{\hat{i}_p} = -10\ \%$

and $\frac{\Delta t}{T_p} = -11{,}2\ \%$

In the first example, the tolerances on the amplitude and the duration of the power-frequency current loop, in accordance with 4.1 of IEC 62271-101:2012, should not be exceeded during

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the actual synthetic test. This depends, however, on the decrement of the AC component of the current being negligible.

In the second example, the current circuit voltage has to be increased or other measures as described in 4.1 of IEC 62271-101:2012 have to be taken because the tolerance on the loop duration is exceeded. Whilst tolerance on the current amplitude is apparently not exceeded, it might be exceeded in practice where there is likely to be some decrement of the AC component of the prospective current.

14.5.5 Asymmetrical current test

If the arc voltage is approximately constant or linearly rising, the curves in Figure 161 and Figure 162 can be used. The method of evaluation is similar to the one outlined for the symmetrical case. For example in case of constant arc voltage:

Direct test

Single pole test voltage $U_t = \frac{123 \times 1,3}{\sqrt{3}} = 92\,\text{kV}$ (as above)

Constant arc voltage U_a = 1 kV

therefore: $\frac{U_a}{\hat{u}} = \frac{1}{92 \times \sqrt{2}} = 0,0077$

for contact parting at around 1,5 cycles after current initiation and one loop of arcing $\frac{\Delta i}{\hat{i}_p} = -1\%$

and: $\frac{\Delta t}{T_p} = -0,6\,\%$ (Figure 161)

Synthetic test

Current circuit voltage U_1 = 14,2 kV

Constant arc voltage (test and auxiliary circuit-breakers) U_a = 2 kV

therefore: $\frac{U_a}{\hat{u}} = \frac{2}{14,2 \times \sqrt{2}} = 0,10$

for the same situation as above: $\frac{\Delta i}{\hat{i}_p} = -12,6\,\%$

and $\frac{\Delta t}{T_p} = -8,0\,\%$ (Figure 161)

The actual arc voltage may not follow one of the simplified characteristics. In such a case, the current reduction during the synthetic test can be measured from actual oscillograms or calculated. The actual current of the direct test that is required to establish the synthetic test driving voltage can only be calculated.

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For circuit-breakers having relatively low arc voltage (e.g. u_a = 2 % U_1), the modifying effect of the arc voltage on the current in the system or in the direct circuit is negligible. Therefore the specified prospective current is assumed as reference current.

NOTE If the opening of the auxiliary circuit-breaker is delayed in relation to the opening of the test circuit-breaker, or if an auxiliary circuit-breaker with a lower arc voltage is used, then its influence on the breaking current will be smaller than that of the test circuit-breaker.

14.6 Step-by-step method to prolong arcing

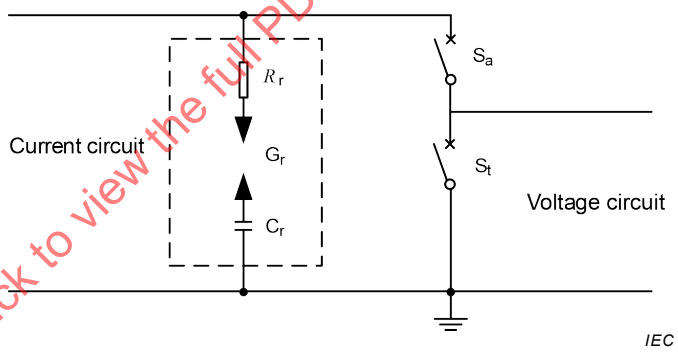
With this method, only one voltage source is used. The test circuit-breaker is artificially re-ignited by a special re-ignition circuit, or other means, in order to prolong arcing up to the current zero at which the voltage source is to be applied.

a) Method with a separate re-ignition circuit

A separate re-ignition circuit provides a rapidly rising pulse of current, of opposite polarity to that of the power-frequency current, approximately 10 µs before current zero. The current through the circuit-breaker is thus rapidly reversed and conduction in the arc gap is maintained for a further loop of power-frequency current. As an example, a re-ignition circuit is indicated in Figure 163. The corresponding current and voltage for a symmetrical current breaking tests is shown in Figure 164. Several such circuits may be used for prolonging the arcing through several loops of current. The re-ignition circuit can in principle be applied to re-ignite both test and auxiliary circuit-breaker. However, the need to re-ignite both circuit-breakers is usually avoided by suitably delaying the separation of the auxiliary circuit-breaker contacts.

b) Method with increased power-frequency circuit severity

In some cases, the arcing of the test circuit-breaker may be prolonged by increasing the rate-of-rise of the transient recovery voltage in the power-frequency current circuit. Whether this is effective or not depends upon the characteristics of the power-frequency current circuit and of the circuit-breaker under test.



Key

S_t	test circuit-breaker	C_r	capacitor for re-ignition circuit
S_a	auxiliary circuit-breaker	G_r	spark gap for closing re-ignition circuit
R	resistor for re-ignition circuit		

Figure 163 – Typical re-ignition circuit diagram for prolonging arc-duration

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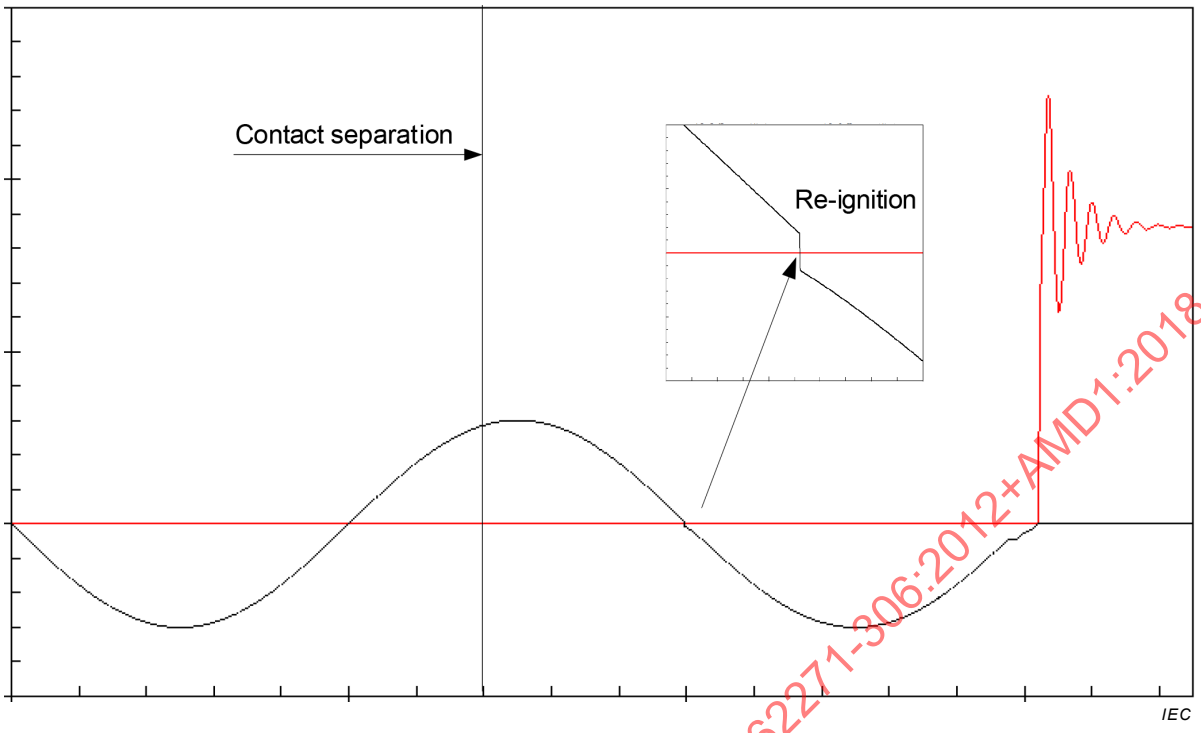

Figure 164 – Typical waveshapes obtained during a symmetrical test using the circuit in Figure 163

14.7 Examples of the application of the tolerances on the last current loop based on 4.1.2 and 6.109 of IEC 62271-101:2012

A few examples are given to show how the tolerances given in Annex B of IEC 62271-100:2008 are applied to the last current loop of test-duties T60, T100a and L90.

– T60, with a short-circuit rated current of 40 kA, with a rated frequency of 50 Hz:

  3) Final loop minimum amplitude: 0,9 × 0,6 × 40 × √2 = 30,5 kA;

  4) Final loop minimum duration: 0,9 × 10 = 9 ms.

– T100a, with a short-circuit rated current of 40 kA, with a rated frequency of 50 Hz, k_{pp} = 1,5, time constant of 45 ms, minimum clearing time between 27 ms and 47,5 ms, first-pole-to-clear:

  5) Final loop minimum amplitude: 0,9 × 1,33 × 40 × √2 = 67,7 kA;

  6) Final loop maximum amplitude: 1,1 × 1,33 × 40 × √2 = 82,8 kA;

  7) Final loop minimum duration: 0,9 × 12,2 = 11 ms;

  8) Final loop maximum duration: 1,1 × 12,2 = 13,4 ms.

– L90, with a short-circuit rated current of 40 kA, with a rated frequency of 50 Hz:

  9) Minimum value of (Final loop amplitude) × (final loop duration): 0,95 × (0,9 × 40 × √2) × 10 = 483,7 As;

  10) Final loop minimum amplitude: 0,95 × 0,9 × 40 × √2 = 48,4 kA;

  11) Final loop maximum amplitude: 1,1 × 0,9 × 40 × √2 = 56 kA;

  12) Final loop minimum duration: 0,9 × 10 = 9 ms.

There are no additional tolerances that can be applied.

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15 Transport, storage, installation, operation and maintenance

15.1 General

The purpose of this clause is to provide additional information to assist in ensuring that the circuit-breaker is transported, stored, installed, operated and maintained in a manner that maximises reliability and availability for the life of the equipment.

The circuit-breaker should have been routine tested before transportation to prove that it is of suitable quality and considered by the manufacturer to be suitable for use on a high-voltage network. It must then be transported, stored, installed, operated and maintained in accordance with the instructions given by the manufacturer. These instructions should be provided before the delivery of the equipment. Ideally they should be available at the time of purchase or technical assessment for purchase.

The recommended approach to the management of the circuit-breaker asset evolves during the life of the equipment from the basis of the initial recommendations of the manufacturer. This initial program can be optimised using the experience of the user and the manufacturer. The development of management strategies for circuit-breakers is outside the scope of IEC 62271-100. CIGRE provides important reference documents covering reliability [28], condition monitoring [29] and life management [30] of circuit-breakers.

15.2 Transport and storage

A circuit-breaker that has met all factory testing and inspection requirements is considered to be correctly manufactured and suitable for use on a high-voltage network. It is therefore important to ensure the circuit-breaker is transported and stored in a manner that does not cause damage to the equipment.

IEC 62271-1 emphasises the need for protection from damage caused by moisture and vibration during transport and storage. Appropriate instructions must be provided by the manufacturer and should include packing units, packaging description, dimensions, weights and storage requirements.

Consideration may also be necessary for any special conditions that may be imposed by the circumstances of the project when determining transport and storage options. This includes any environmental changes that are likely to be experienced during transportation and storage, for example ambient temperature, pressure, humidity and pollution especially from salt (sea/coastal) environments. A particular consideration may be whether the packed equipment should be capable of being stored outdoors for a defined period without being damaged. Equipment should also be packed or crated in a manner suitable for stacking and for handling by forklift or other appropriate means and arranged so that complete items of plant may be delivered to separate sites independently. Packing of switchgear and controlgear with insulation other than ceramic insulation should be suitably protected against invasion by vermin.

Each packing case should contain a list detailing the contents of the case. There should be clear indication of any special handling conditions, which should preferably be repeated on the container. Shock indicators are a useful method of determining whether the equipment has been subjected to high impacts during transportation.

Any valves or other fittings liable to damage during shipment should have covers or shall be replaced by plugs.

A power supply may also be required for connection to the anti-condensation heaters during storage. Clear instructions must be provided to ensure safe connection of such supplies and potential damage to sub-components adjacent to the heaters.

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The requirements for the packing and storage of spare parts need to be considered to ensure they can be appropriately stored, identified and handled.

Any damage or doubts regarding the condition of the circuit-breaker should be referred to the manufacturer.

15.3 Installation

Subclauses 10.2.1 to 10.2.4 of IEC 62271-1:2007 describe the unpacking, lifting, assembly, mounting and connections to the circuit-breaker. Connections include the high-voltage and current connections, auxiliary circuits, liquid or gas systems and earthing.

It is important that the required information is provided for the safe and effective unpacking, lifting and assembly of the circuit-breaker on the appropriate foundations.

Responsibilities for installation and commissioning of the circuit-breakers need to be defined before these activities are commenced. It is important to ensure that the installation and commissioning staff are competent and there is adequate expert supervision. Involvement of the manufacturer should be considered and there may be a need for qualification of staff in the installation and commissioning of each type of circuit-breaker. Responsibility should also be defined for the supply of SF_6, other gases, and hydraulic oil where appropriate, for filling to operational pressure.

Confirmation should be made that correct gas transport pressures have been maintained and subsequent filling is to the correct pressure. The use of recycled gas complying with IEC 60480 is encouraged provided there is agreement with the manufacturer. The manufacturer is to state any requirements for the use of recycled gas. All necessary testing to prove the quality of the gas is recommended.

Within the bounds of practicality there is to be no discharge of SF_6 due to the impact of SF_6 on the environment and potential health and safety implications. SF_6 should not be released imprudently to the atmosphere. Any unwanted or waste SF_6 should be recovered for recycling. More information regarding recovery and equipment for recovery of SF_6 is provided in IEC 62271-4 [7].

Confirmation should be made of all connections including high-voltage, secondary and earthing connections. The high-voltage terminal connectors should be installed as designed to ensure terminal loading forces and support bending moments are not exceeded for all environmental, operational, fault and seismic conditions. This requirement is important for adjacent equipment as well as the circuit-breaker.

Checks should include correct assembly, avoidance of damage, correct gas pressures and correct earthing.

15.4 Commissioning

Commissioning tests are recommended to be performed following installation. The purpose of these tests is to confirm the following:

– transport and storage have not damaged the circuit-breaker;
– separate units are compatible;
– assembly has been performed correctly;
– the circuit-breaker will operate correctly.

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Commissioning tests are particularly important when a large part of the assembly and/or adjustment is performed on site.

Repetition of the full program of routine tests already performed in the factory should be avoided.

If major sub-assemblies are combined at site, without previous tests on the complete circuit-breaker, then a minimum of 50 no-load operations are to be performed on site. Deferred routine tests may be included in the 50 operations because both site routine tests and commissioning tests confirm the correct operation of the circuit-breaker.

The manufacturer should provide instructions for inspection and tests that should be made after installation and all connections have been made. The results should be provided in a commissioning test report. The commissioning test program should be based on the manufacturer's recommendations and should be agreed before the program is commenced.

Subclause 10.2.101 of IEC 62271-100:2008 contains guidance for commissioning tests. A commissioning test program is required that may include but not be limited to the tests included in the guide. The nominated tests are comprehensive but it may be appropriate to exclude some tests or include additional tests as appropriate. The selection of tests should consider the type and construction of the circuit-breaker as well as the conditions of transportation, storage and installation. Subclause 10.2.101 of IEC 62271-100:2008 includes tests and checks in the following categories:

- general checks including assembly, tightness, external insulation, paint, corrosion protection, operating devices, earth connection and operations counter;
- checks of electrical circuits including wiring, position indication, alarms, lockouts, heating and lighting;
- checks of the insulation including filing pressure and quality (in accordance with IEC 60376, IEC 60480 and IEC 62271-4 for SF_6);
- checks on operating fluids including levels, filling pressure and purity;
- site operations;
- insulating and interrupting fluid alarm and lockout pressures on rising and falling pressures;
- characteristic rising and falling operating pressures for hydraulic and pneumatic systems including lockout, low pressure alarm, safety valve and pumping device cut-in and cut-out;
- power consumption during operations;
- verification of the operating sequence;
- closing and opening times of each pole including control and auxiliary contacts;
- recharging time of the operating mechanism;
- mechanical travel characteristics where the circuit-breaker has been assembled as a complete circuit-breaker for the first time or where all or part of the routine tests have been performed on site;

  These mechanical travel characteristics may be used as a reference for future maintenance. Due to differences in the measurement equipment, the results may differ from the information provided by the manufacturer;
- opening, closing and auto reclosing at the minimal functional pressure for operation;
- the time during which the circuit-breaker remains closed during a CO operation including an anti-pumping check;
- behaviour of the circuit-breaker on a closing command while an opening command is already present;
- the application of an opening command on both releases simultaneously;

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- protection against pole discrepancy;
- dielectric tests on auxiliary circuits taking care not to damage vulnerable sub components;
- measurement of the resistance of the main circuit.

Procedures need to be included in the instructions for any adjustments that may be needed for correct operation.

Recommendations shall also be provided for any relevant measurements that should be made and recorded to assist with future maintenance decisions.

The instructions need to be sufficient for final inspection and putting into service.

15.5 Operation

The manufacturer needs to provide suitable instructions and the user needs to have suitable understanding of the equipment characteristics and principles of operation. This must include the relevant safety requirements and the actions that must be taken for operation, isolation, earthing, maintenance and testing. These instructions should preferably be agreed and understood by the user prior to installation and ideally at the time of purchase.

15.6 Maintenance

The manufacturer should provide a maintenance manual that includes the extent and frequency of the recommended maintenance and a description of the maintenance work. Suitable drawings should clearly identify assembles, sub-assemblies and significant spare parts necessary for the maintenance and repair of the equipment. Measurement values and tolerances should be included which may require corrective action. Specifications should also be included for any materials and tools needed during maintenance. The manufacturer should also be prepared to state their policy for the continued supply and availability of spares. The maintenance manual and any training must adequately cover the various hazards that may create: a risk to personal safety; a risk to the environment; or damage to the circuit-breaker. These hazards may include electrical, mechanical, thermal, operational and chemical aspects.

The user needs to ensure maintenance staff are suitably competent for the task. The user should also ensure suitable records are kept of the history of service, maintenance, failures and measurements taken.

It is important that suitable information is exchanged between the manufacturer and user during the life of the equipment. This should include failure information, special instructions and refinements to the recommended maintenance procedures. It is important that both parties provide information.

Further tools and techniques are available to optimise the performance of the equipment and effectiveness of the maintenance effort. On-line condition monitoring and Reliability Centred Maintenance (RCM) are examples of emerging strategies that can be applied to circuit-breakers. Information gained by the use of such techniques should be shared with the manufacturer. CIGRE provides comprehensive analysis of the strategies available in these areas [29, 30].

15.7 Corrosion: Information regarding service conditions and recommended test requirements

15.7.1 General

The minimum requirement for switchgear and controlgear with regard to corrosion is that the function of the equipment should not be affected during the service life by corrosion under the conditions specified by the user. All bolted or screwed parts of the main circuit and of the enclosure should remain easy to disassemble, as applicable. In particular, galvanic corrosion

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of materials in contact should be considered because, for example, it may lead to the loss of tightness or increased contact resistance.

Corrosion might not only occur due to oxidizing gases, but also due to material incompatibility. An example is a connection made between bare aluminium or an aluminium alloy part and a silver coated part of the main circuit. Reference is made to [143] in the bibliography.

Due to the many variables involved, for example, design of equipment, service conditions, user maintenance practices, and the expected life of the equipment; standardized requirements and verification testing is left to agreement between the user and the manufacturer. In either case, however, the following guidelines should be followed.

Corrosion stresses are strongly dependant on the installation. The atmospheric conditions are important, but the installation should consider the solar and temperature variation, the air flow, etc.

NOTE When a surface becomes and remains wet, the two main factors involved in atmospheric corrosion are sodium chloride, mainly in marine environments, and sulphur dioxide, mainly in industrial environments. Occasionally, both of these factors apply at the same time.

15.7.2 Recommendation for minimum requirements

The basic function of switchgear and controlgear to be considered should include, but not be limited to, the following:

– the ability to withstand normal system voltage and carry rated continuous current;
– the continuity of earthing circuits;
– the ability to access or disassemble equipment as required to perform routine inspection and maintenance;
– the ability to provide minimum security against unauthorized access;
– the ability to provide for the safety of the user or the public as appropriate.

15.7.3 Recommended test requirements

The tests and test methods are related to the material used in the equipment and are recommended when required by the relevant equipment standard or by agreement between the user and the manufacturer.

Specific corrosion and humidity tests should be performed according to the relevant IEC standard, reference is made to IEC 60068-1 [132].

15.8 Electromagnetic compatibility on site

EMC site measurements are not type tests but may be performed in special situations:

– where it is deemed necessary to verify that actual stresses are covered by the EMC severity class of the auxiliary and control circuits, or
– in order to evaluate the electromagnetic environment, in order to apply proper mitigation methods, if necessary,
– to record the electromagnetically induced voltages in auxiliary and control circuits, due to switching operations both in the main circuit and in the auxiliary and control circuits. It is not considered necessary to test all auxiliary and control circuits in a substation under consideration. A typical configuration should be chosen.

Measurement of the induced voltages should be made at representative ports in the interface between the auxiliary and control circuits and the surrounding network, for example, at the input terminals of control cubicles, without disconnection of the system. The extension of the

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auxiliary and control circuits is described in 5.19 of IEC 62271-1:2007. Instrumentation for recording induced voltages should be connected as outlined in IEC 60816 [133].

Switching operations should be carried out at normal operating voltage, both in the main circuit and in the auxiliary and control circuits. Induced voltages will vary statistically and thus a representative number of both making and breaking operations should be chosen, with random operating instants.

The switching operations in the main circuit are to be made under no-load conditions. The tests will thus include the switching of parts of the substation but no switching of load currents and no fault currents.

The making operations in the main circuit should be performed with trapped charge on the load side corresponding to normal operating voltage. This condition may be difficult to obtain at testing, and, as an alternative, the test procedure may be as follows:

– discharge the load side before the making operation, to assure that the trapped charge is zero;
– multiply recorded voltage values at the making operation by 2, in order to simulate the case with trapped charge on the load side.

The switching device in the primary system should be operated at rated pressure and auxiliary voltage.

NOTE 1 The most severe cases, with regard to induced voltages, will normally occur when only a small part of a substation is switched.

NOTE 2 The most severe electromagnetic disturbances are expected to occur at disconnector switching, especially for GIS installations.

The recorded or calculated peak value of induced common-mode voltage, due to switching in the main circuit, should not exceed 1,6 kV for interfaces of the auxiliary and control circuits.

The note to 5.19 of IEC 62271-1:2007 gives guidelines for improvement of electromagnetic compatibility.

16 Inductive load switching

16.1 General

Inductive load switching covers the following cases:

- shunt reactor switching;
- motor switching;
- unloaded transformer switching.

IEC 62271-110 covers requirements and testing for motor and shunt reactor switching.

Circuit-breakers in general have no difficulty interrupting small inductive currents, the current in fact is usually forced to a premature zero by a phenomenon known as current chopping. However, the resultant chopping overvoltages and those due to subsequent re-ignition (in the circuit-breaker), the magnitude of which are dependent on both the characteristics of the circuit-breaker and the circuit, can be of such significance as to require some form of limitation (e.g. surge arresters and controlled switching – point on wave switching). The duty is thus very interactive and due diligence should be exercised in selecting a circuit-breaker for this purpose.

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The general theory of inductive current switching is essentially common to all of the above-noted switching cases. On this basis, shunt reactor switching is considered in detail and unloaded transformer and motor switching as extensions to that case.

16.2 Shunt reactor switching

16.2.1 General

The three shunt reactor switching cases to be considered are:

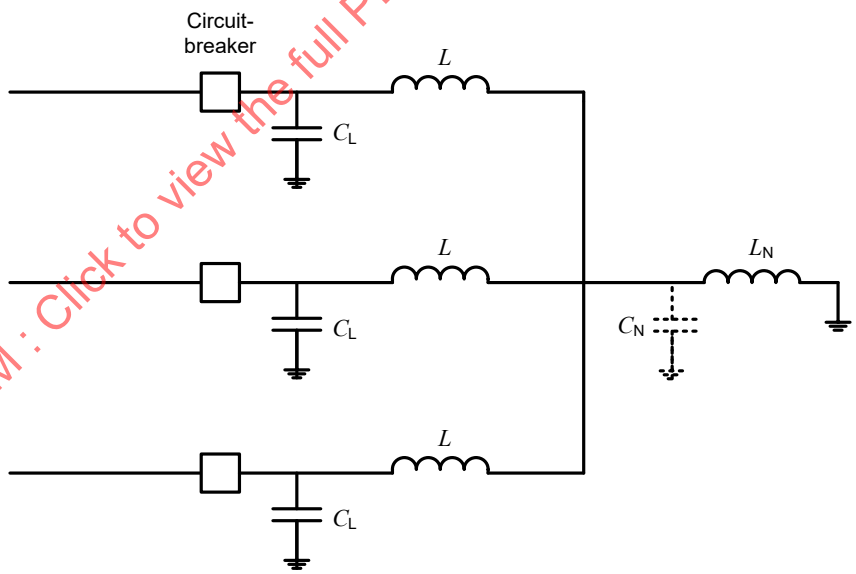
- solidly earthed shunt reactors usually applied at HV (72,5 kV ≤ U_r ≤ 245 kV, where U_r is the rated voltage) and EHV (300 kV ≤ U_r ≤ 800 kV);
- neutral reactor earthed shunt reactors usually applied at EHV;
- unearthed shunt reactors usually applied at U_r ≤ 52 kV but also up to 170 kV in some countries.

All three cases can be readily analysed by first considering the general case of the neutral reactor earthed shunt reactor and extending it to the other two cases.

Typical shunt reactor characteristics are provided in 16.5 and related system and station characteristics in 16.6.

16.2.2 Chopping overvoltages

The general case is shown in Figure 75 where the shunt reactor is represented by its inductance L and capacitance C_L and the neutral reactor correspondingly by L_N and C_N. C_L includes the inherent capacitance of the shunt reactor and the capacitance of all components between the circuit-breaker and the shunt reactor. C_N is the inherent capacitance of the neutral reactor but does not influence first-pole-to-clear considerations and can be ignored.



Key

C_L	Load side capacitance of the shunt reactor	C_N	Inherent capacitance of the neutral reactor
L	Single-phase shunt reactor inductance	L_N	Inductance of the neutral reactor

Figure 75 – General case for shunt reactor switching

After contact parting as the current goes towards zero, an unstable interaction occurs between the arc and the capacitance in parallel with the circuit-breaker (refer to 16.7). This interaction results in a negatively damped oscillation in the current which eventually crosses

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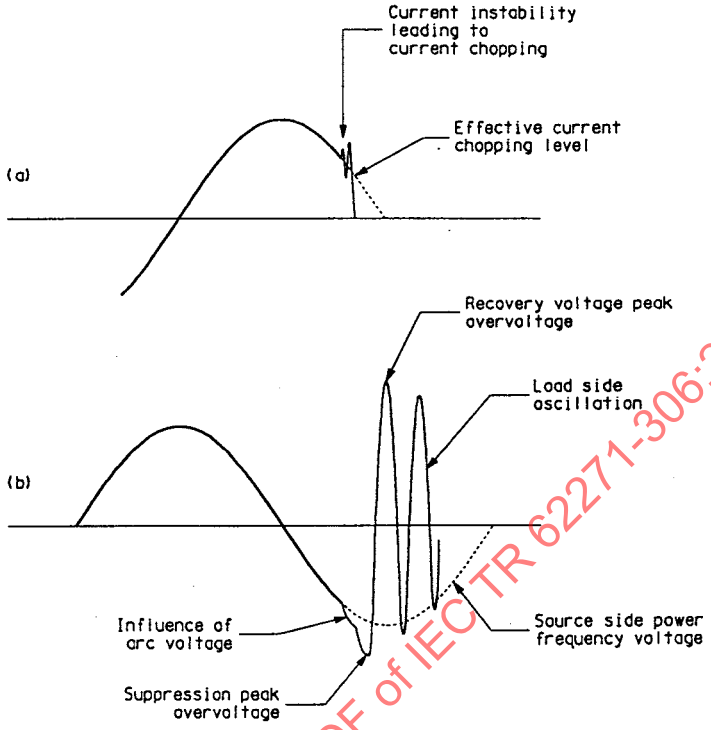
the zero line thus chopping the current prior to the power frequency zero crossing as shown in Figure 76. The chopping of the current leaves stored energy in the shunt reactor resulting in an overvoltage referred to as the suppression peak overvoltage. The task now is to calculate the magnitude of this overvoltage and apply it to the first-pole-to-clear case for the circuit-breaker. The highest suppression peak overvoltage may actually occur on the second or third pole to clear due to higher current chopping at the associated longer arcing times.



(a) Current through circuit-breaker

(b) Voltage across shunt reactor

Figure 76 – Current chopping phenomena

The first-pole-to-clear representation for the general case (Figure 75) is shown in Figure 77. i_c is the chopped current in the first-pole-to-clear and the second and third poles are considered to be earthed through an infinite bus.

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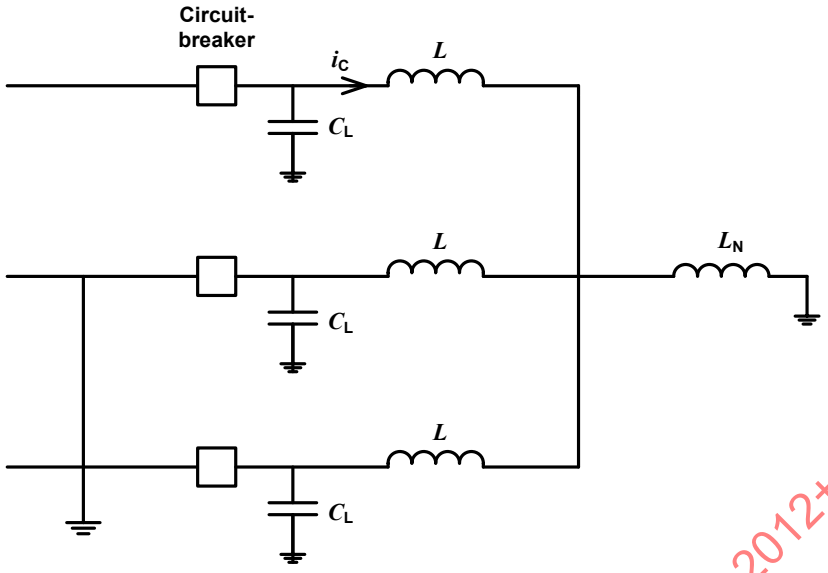

Key

i_c	Chopped current	C_L	Load side capacitance of the shunt reactor
L	Single-phase shunt reactor inductance	L_N	Inductance of the neutral reactor

Figure 77 – General case first-pole-to-clear representation

The single-phase equivalent circuit for the first-pole-to-clear is derived from Figure 77 and shown in Figure 78.

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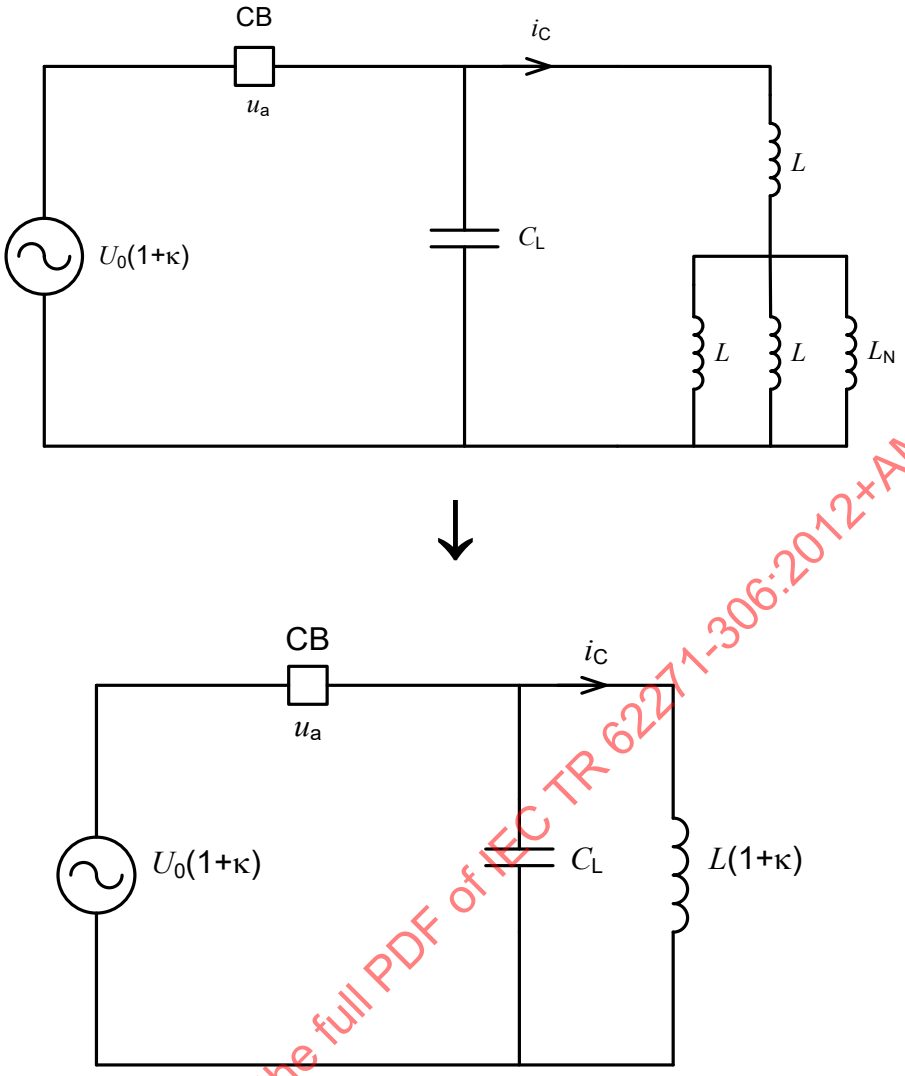

Key

U_0	Power frequency crest voltage to earth at the instant of current interruption	u_a	Arc voltage
i_c	Chopped current	C_L	Load side capacitance of the shunt reactor
L	Single-phase shunt reactor inductance	L_N	Inductance of the neutral reactor
κ	Neutral shift factor	CB	Circuit-breaker

Figure 78 – Single phase equivalent circuit for the first-pole-to-clear

κ is defined by considering the total load inductance L' as follows:

$$L' = L\left[1 + \frac{1}{2 + L/L_N}\right] = L[1+\kappa] \qquad (96)$$

For solidly earthed shunt reactors, $L_N = 0$, $\kappa = 0$ and $L' = L$; for non-effectively earthed shunt reactors $L_N = \infty$; $\kappa = 0{,}5$ and $L' = 1{,}5\ L$.

U_0 is the peak voltage at the reactor at the associated load current and is the 1 p.u. voltage. u_a is the arc voltage (see Figure 79) and the voltage at C_L just prior to current chopping is $U_0 + u_a$ since the arc voltage is in phase with the current and of opposite polarity to U_0. $U_0 + u_a$ is referred to as the initial voltage and is expressed as k_{in} in p.u. as shown in Figure 79.

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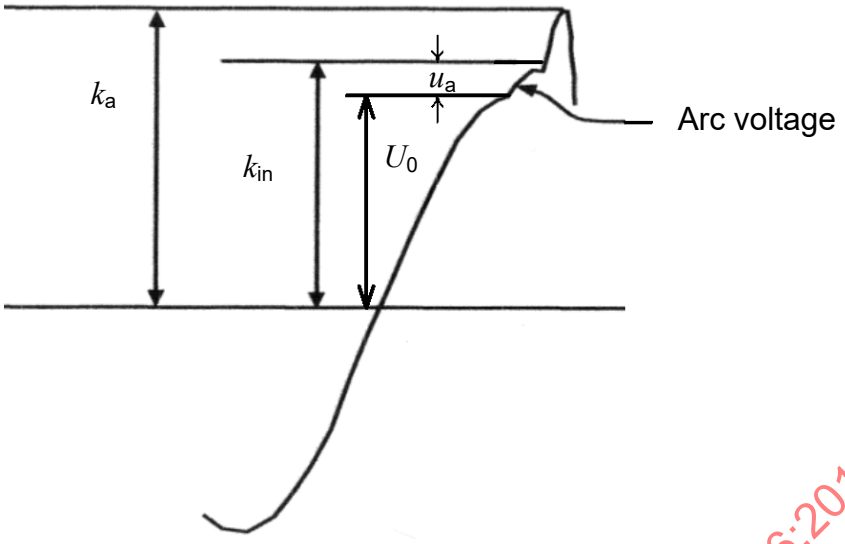

Key

U_0	Power frequency crest voltage to earth at the instant of current chopping	k_a	Suppression peak overvoltage
u_a	Arc voltage	k_{in}	Initial voltage (U_0 + u_a)

Figure 79 – Voltage conditions at and after current interruption

$$k_{in} = \frac{U_0 + u_a}{U_0} = 1 + \frac{u_a}{U_0}$$

$$u_a = U_0(k_{in} - 1)$$

Referring to Figure 77 for the first-pole-to-clear, the energy stored E_c in the capacitance C_L at the instant of current chopping is given by:

$$E_C = \frac{1}{2} C_L [U_0(1+\kappa) + u_a]^2 = \frac{1}{2} C_L [U_0(1+\kappa) + U_0(k_{in} - 1)]^2 = \frac{1}{2} C_L [U_0(k_{in} + \kappa)]^2$$

Similarly, the energy E_L stored in the inductance $L(1 + \kappa)$ is given by

$$E_L = \frac{1}{2} L(1+\kappa) i_c^2$$

The maximum voltage U_m, actually an overvoltage occurs when the total available energy E_T is stored capacitively in C_L:

$$E_T = E_C + E_L = \frac{1}{2} C_L [U_0(k_{in} + \kappa)]^2 + \frac{1}{2} L(1+\kappa) i_c^2 = \frac{1}{2} C_L U_m^2$$

$$\frac{U_m}{U_0} = \sqrt{(k_{in} + \kappa)^2 + \left(\frac{i_c}{U_0}\right)^2 \frac{L}{C_L}(1+\kappa)} = k_b \text{ in p.u.}$$

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k_b is the overvoltage with respect to the shifted neutral (Figure 80) and the so-called suppression peak with respect to earth k_a in p.u. is given by:

$$k_a = k_b - \kappa = \sqrt{(k_{in} + \kappa)^2 + \left(\frac{i_c}{U_0}\right)^2 \frac{L}{C_L}(1+\kappa)} - \kappa \quad (97)$$

Equation (97) is the general equation for k_a and is directly applicable to the neutral reactor earthed reactor case. For the solidly earthed neutral case, $\kappa = 0$ and Equation (97) becomes

$$k_a = \sqrt{k_{in}^2 + \left(\frac{i_c}{U_0}\right)^2 \frac{L}{C_L}} \quad (98)$$

and for the non-effectively earthed neutral case, $\kappa = 0{,}5$ giving

$$k_a = \sqrt{\left(k_{in}^2 + 0{,}5\right) + \left(\frac{i_c}{U_0}\right)^2 \frac{1{,}5L}{C}} - 0{,}5 \qquad k_a = \sqrt{(k_{in} + 0{,}5)^2 + \left(\frac{i_c}{U_0}\right)^2 \frac{1{,}5L}{C}} - 0{,}5 \quad (99)$$

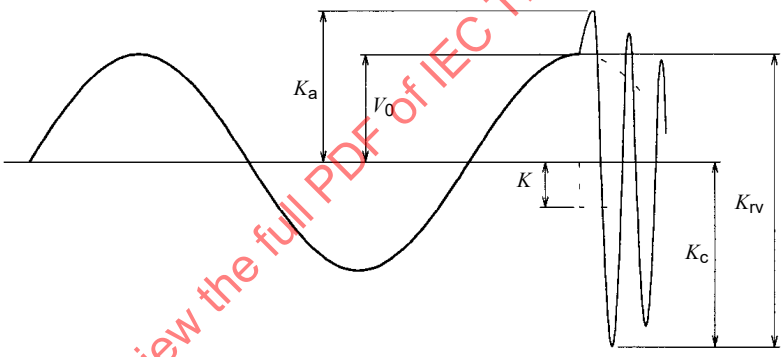

Figure 80 – Shunt reactor voltage at current interruption

With regard to Equation (99), especially for high current reactors (low values of L), the second term under the root sign may be insignificant and k_a is dependent only on the arc voltage.

The value of the chopped current is dependent on the capacitance C_t seen from the circuit-breaker terminals including the source side capacitance C_S, the grading capacitor capacitance C_p, the number N of interrupters in series per pole and the so-called chopping number λ for a single interrupter, which is a characteristic value of the circuit-breaker. The chopping current level is given by:

$$i_{ch} = \lambda\sqrt{NC_t} \quad (100)$$

where $$C_t = C_p + \frac{C_s C_L}{C_s + C_L}$$

The chopping number approach can be applied for all current circuit-breaker types except vacuum circuit-breakers, where the basic Equation (97) must be used. The approach is valid provided that the circuit as seen by the circuit-breaker can be considered as an equivalent

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parallel capacitance in the relevant range of frequencies. Where this is not the case a computational approach using EMTP or other method is required [31].

Typical chopping numbers are given in Table 29. For gas circuit-breakers in particular, current chopping increases with arcing time and likewise the chopping number.

Table 29 – Circuit-breaker chopping numbers

Circuit-breaker type	Chopping number λ $AF^{-0,5}$
Minimum oil	$5{,}8 \times 10^4$ to 10×10^4
Air blast	15×10^4 to 20×10^4
SF_6 puffer	4×10^4 to 19×10^4
SF_6 self-blast	3×10^4 to 10×10^4
SF_6 rotating arc	$0{,}39 \times 10^4$ to $0{,}77 \times 10^4$

The maximum value of C_t leading to the highest chopping level and subsequent highest suppression peak overvoltage occurs when $C_s >> C_L$ and C_t is given by:

$$C_t = C_P + C_L \tag{101}$$

Substituting for i_{ch} (from Equations (100) and (101)) in Equation (99) gives k_a on a chopping number basis:

~~$k_a = (1+\kappa)\sqrt{1+\frac{NL}{(1+\kappa)}\left(\frac{\lambda}{U_0}\right)^2\left(\frac{C_P}{C_L}+1\right)} - \kappa$~~ $k_a = \sqrt{(k_{in}+\kappa)^2 + NL(1+\kappa)\left(\frac{\lambda}{U_0}\right)^2\left(\frac{C_P}{C_L}+1\right)} - \kappa$ (102)

A more useful variation of Equation (102) based on the shunt reactor rating Q in var and taking U_0 as the peak value of the system voltage to earth is:

~~$k_a = (1+\kappa)\sqrt{1+\left(\frac{1{,}5}{1+\kappa}\right)\left(\frac{N\lambda^2}{\omega Q}\right)\left(\frac{C_P}{C_L}+1\right)} - \kappa$~~ $k_a = \sqrt{(k_{in}+\kappa)^2 + \frac{1{,}5\,N\lambda^2(1+\kappa)}{\omega Q}\left(\frac{C_P}{C_L}+1\right)} - \kappa$ (103)

For solidly earthed shunt reactors, $\kappa = 0$ and k_a is given by:

~~$k_a = \sqrt{1+\frac{1{,}5N\lambda^2}{\omega Q}\left(\frac{C_P}{C_L}+1\right)}$~~ $k_a = \sqrt{k_{in}{}^2 + \frac{1{,}5N\lambda^2}{\omega Q}\left(\frac{C_P}{C_L}+1\right)}$ (104)

For non-effectively earthed shunt reactors, $\kappa = 0{,}5$, $N = 1$, C_P is negligible compared to C_L and k_a is given by:

$$k_a = \sqrt{(k_{in}+0{,}5)^2 + \frac{2{,}25\lambda^2 N}{\omega Q}\left(\frac{C_P}{C_L}+1\right)} - 0{,}5 \tag{105}$$

k_a and the subsequent recovery voltage peak overvoltage k_c stress the shunt reactor, the latter being given by (refer to Figure 80):

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$$k_c = 2\kappa + k_a \tag{106}$$

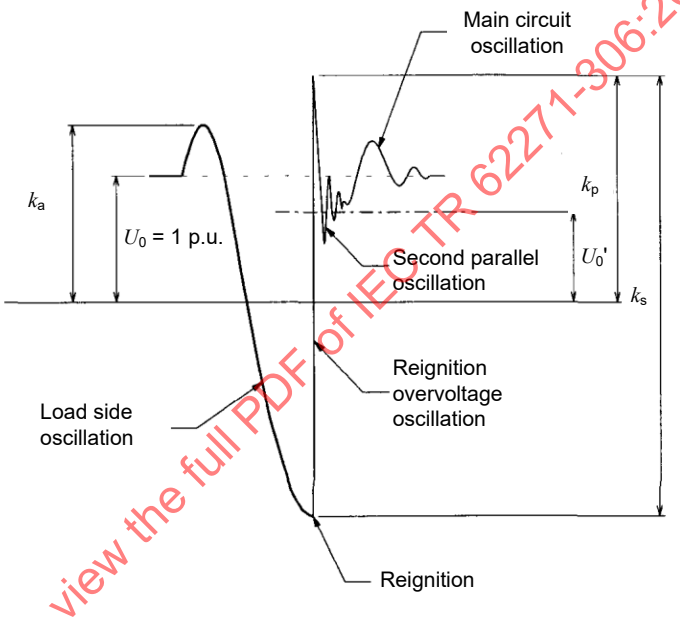
The transient recovery voltage peak imposed on the circuit-breaker is k_{rv} (refer to Figure 80) given by:

$$k_{rv} = 1 + 2\kappa + k_a \tag{107}$$

The influence of the earthing arrangement is reflected in the 2κ factor, the multiplier of 2 being due to the fact that the oscillation is about the shifted neutral point.

16.2.3 Re-ignition overvoltages

When a re-ignition occurs in the circuit-breaker the load side voltage rapidly tends to the source side voltage but overshoots producing a re-ignition overvoltage as shown in Figure 81.



U_0 Power frequency crest voltage to earth at instant of current interruption

k_a Suppression peak overvoltage in p.u. of U_0

k_p Re-ignition overvoltage peak to earth in p.u. of U_0

k_s Re-ignition overvoltage excursion in p.u. of U_0

$$\frac{U'_0}{U_0} = \frac{C_s}{C_s + C_L}\left(1 - k_a \frac{C_L}{C_s}\right)$$

Figure 81 – Re-ignition at recovery voltage peak for a circuit with low supply side capacitance

Figure 81 shows the case for a circuit where $C_s > C_L$.The re-ignition overvoltage in the worst case occurs when $C_s << C_L$ and its magnitude k_p in p.u. to earth assuming damping (β) is given by:

$$k_p = 1 + \beta(1 + 2\kappa + k_a) \tag{108}$$

The damping factor β is usually taken as 0,5 based on actual field experience.

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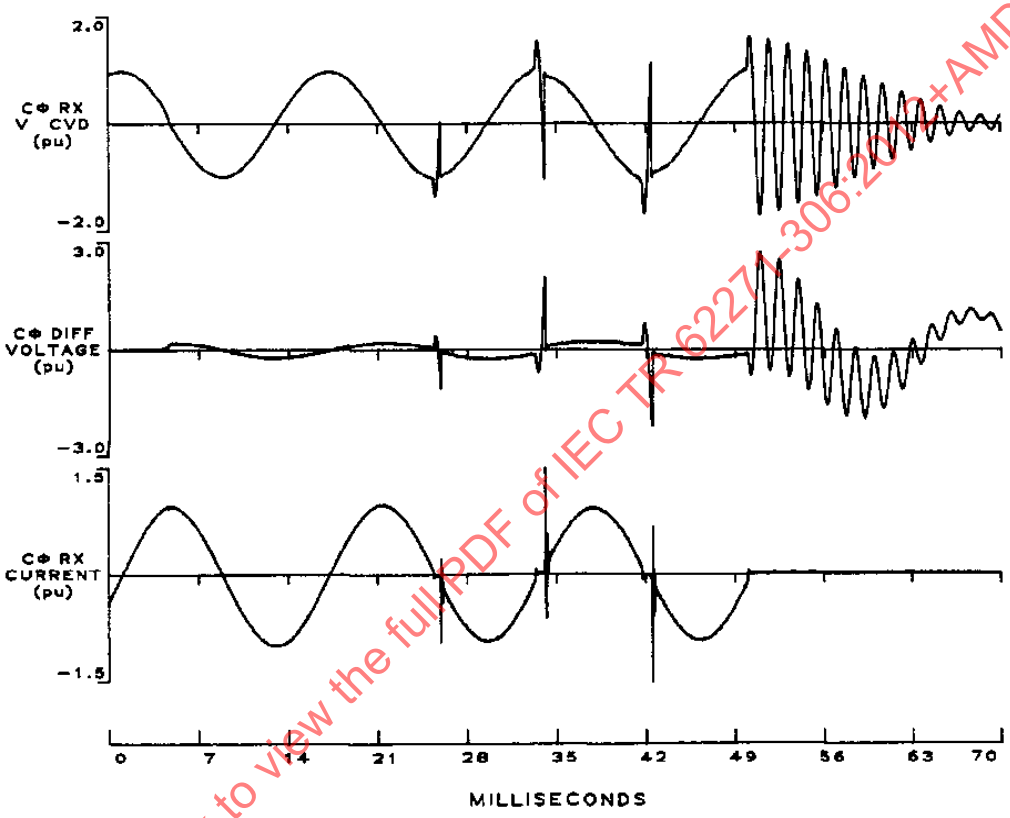
The excursion of the re-ignition transient k_s in p.u. is given by:

$$k_s = (1+\beta)(1+2\kappa+k_a) \quad (109)$$

Re-ignitions are normal occurrences but may be harmful to the interrupters [32] and also to the shunt reactor windings particularly at voltages of 245 kV and above (see Annex B of IEEE C57.21 – 2006 [33]).

Figure 82 shows an actual 500 kV shunt reactor switching event illustrating chopping and re-ignition overvoltages. The circuit-breaker in this case exhibits an extraordinary number of re-ignitions as compared to the typical case of re-ignition at one zero crossing only.



Upper trace	Voltage to earth at shunt reactor
Middle trace	Voltage across circuit-breaker
Lower trace	Shunt reactor current

Figure 82 – Field oscillogram of switching out a 500 kV 135 Mvar solidly earthed shunt reactor

16.2.4 Oscillation circuits

16.2.4.1 General

Four oscillation circuits play a role in shunt reactor switching and can be generally described by considering the solidly earthed shunt reactor case (refer to Figure 82). The first oscillation circuit relates to current interruption and the other three circuits to the re-ignition process.

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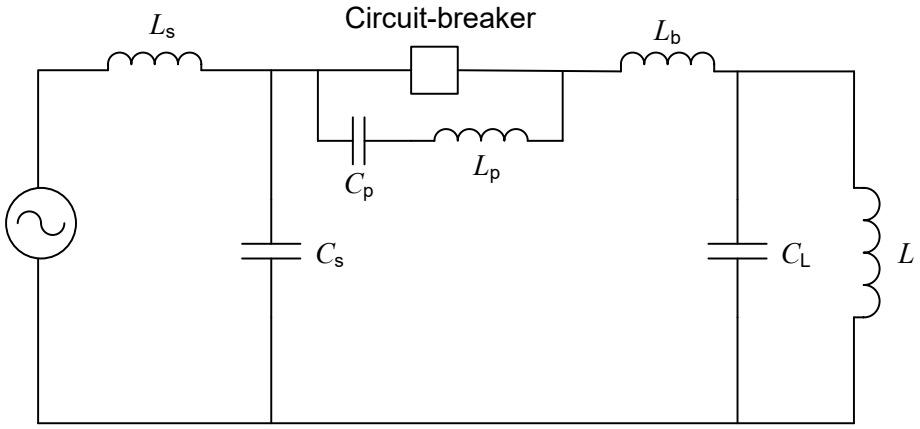

Key

L_s	Source inductance	L_b	Connection series inductance
C_s	Source side capacitance	C_L	Load side capacitance
L_p, C_p	First parallel circuit inductance and capacitance	L	Reactor inductance

Figure 83 – Single-phase equivalent circuit

16.2.4.2 Load side oscillation

A successful shunt reactor current interruption results in a decaying load side oscillation with the trapped energy oscillating between the inductance L and the capacitance C_L (Figure 83). The frequency of this oscillation is:

$$f_L = \frac{1}{2\pi\sqrt{LC_L}} \tag{110}$$

and is typically in the range 1 kHz to 5 kHz for EHV and HV shunt reactors and up to 30 kHz for MV shunt reactors. f_L is the frequency of the circuit-breaker transient recovery voltage whose peak value is given by Equation (107).

16.2.4.3 First parallel oscillation

When a re-ignition occurs in the circuit-breaker, a first parallel oscillation occurs due to the discharge of capacitance C_P through the circuit-breaker (Figure 81 and Figure 83). The frequency of this oscillation is given by:

$$f_{p1} = \frac{1}{2\pi\sqrt{L_P C_P}} \tag{111}$$

and is typically in the range 1 MHz to 10 MHz. The circuit-breaker will not interrupt the current associated with this oscillation and therefore it has no significance with respect to overvoltages.

16.2.4.4 Second parallel oscillation

The second parallel oscillation follows the first parallel oscillation involving C_s, C_L and L_b and results in equalization of the voltages on C_s and C_L (Figure 83). The frequency of this oscillation is given by:

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$$f_{p2} = \frac{1}{2\pi\sqrt{L_b\left(\frac{C_s C_L}{C_s + C_L}\right)}} \quad (112)$$

and is typically in the range of 50 kHz to 1 MHz. This transient voltage is steep and may be unevenly distributed across the shunt reactor winding, stressing in particular the entrance turns of the winding. The re-ignition itself is particularly hazardous to the entrance turns.

16.2.4.5 Main circuit oscillation

Under certain circumstances (C_s and C_L of the same order of magnitude), a main circuit oscillation follows the second parallel oscillation (Figure 83). This oscillation is complex and its frequency in its simplest form is given by:

$$f_m = \frac{1}{2\pi}\sqrt{\frac{L_s + L}{L_s L(C_s + C_L)}} \quad (113)$$

and is in the range 5 kHz to 20 kHz.

16.2.5 Overvoltage limitation

Some method of overvoltage limitation is usually applied in all shunt reactor switching cases. The various methods and their relative effectiveness are reviewed in Table 30.

Table 30 – Chopping and re-ignition overvoltage limitation method evaluation for shunt reactor switching

Overvoltage limitation method	How does the method work?	Advantage	Disadvantage
Opening resistor	Resistor causes phase shift of current with respect to voltage resulting in current interruption by resistor switch at lower point on voltage halfwave thus reducing k_a and consequently k_{rv} significantly.	Very effective on circuit-breakers with very high chopping numbers, i.e. air-blast and dual pressure SF_6 circuit-breakers.	Adds significantly to mechanical complexity and maintenance requirements of the circuit-breaker; not viable – technically or economically – on single pressure SF_6 circuit-breakers; re-ignitions can still occur.
Surge arresters to earth at shunt reactor	Limits overvoltage to earth (k_a) at shunt reactor.	Passive.	Effective only for circuit-breakers producing suppression peak overvoltages in excess of the surge arrester protective level; re-ignition overvoltages still occur at up to twice the protective level of the surge arrester with no reduction in the re-ignition overvoltage excursion frequency.

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Overvoltage limitation method	How does the method work?	Advantage	Disadvantage
Metal oxide varistor (MOV) across circuit-breaker [34]	Limits the recovery voltage (k_{rv}) across the circuit-breaker to the protective level of the varistor and subsequent re-ignition overvoltages to maximum $1+\beta k_{arv}$ where k_{arv} is the protective level of the arrester in p.u. of V_o.	Passive; effective for all circuit-breaker types; particularly suitable for use on circuit-breakers at ≤ 52 kV; magnitude and probability of re-ignitions significantly reduced; energy absorbed by surge arrester is minimal.	Adds to complexity of circuit-breaker; surge arresters must be able to withstand forces associated with circuit-breaker operation; some re-ignitions will still occur albeit at low voltage levels.
Surge capacitor	Decreases frequency and thereby rate of rise of the load side oscillation; decreases frequency of re-ignition overvoltage excursion.	May reduce probability of re-ignitions; reduces frequency of the voltage excursion imposed on the shunt reactor winding; may reduce value of k_a for vacuum breakers where chopping current is dependent mainly on contact material.	Does not influence k_a for circuit-breakers other than vacuum type; leads to increased chopping current but not necessarily increased suppression peak overvoltages; does not eliminate re-ignitions; may have the effect of reducing the minimum arcing time such that probability of re-ignitions is unchanged; require space.
Controlled switching	Ensures contact parting with respect to current wave such that interruption occurs at the first subsequent current zero.	Eliminates re-ignitions.	Suitable only for mechanically consistent circuit-breakers with appropriate minimum arcing times; requires independent pole operation.

16.2.6 Circuit-breaker specification and selection

16.2.6.1 General

Shunt reactor switching is a very unique switching duty and requires diligent specification and selection of the circuit-breaker. The intent should be to specify the circuit-breakers in terms under the control of the manufacturer and to select the circuit-breaker to perform the duty while minimizing the overvoltage impact on the application which is under the control of the user.

16.2.6.2 Circuit-breaker specification

On the basis that the dedicated purpose of the circuit-breaker is to switch a shunt reactor only, the following characteristics should be specified. If short-circuit current interruption capability is required then this duty must also be specified.

- dielectric withstand requirements;
- rated short-time and peak withstand currents (assumes no fault clearing);
- shunt reactor rating;
- shunt reactor current;
- load side characteristics: Inductance L of the shunt reactor and C_L the total effective capacitance of the load side circuit including the shunt reactor and all connected equipment;

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- overvoltage limitation: The suppression peak overvoltage (k_a) should be stated; a k_a value of 2 p.u. is recommended for applications at or above 72,5 kV and 2,5 p.u. for applications at ≤ 52 kV. Note that no limitation for re-ignition overvoltages should be stated since these overvoltages are very circuit dependent;
- earthing arrangement whether solidly earthed, non-effectively earthed or neutral reactor earthed. In the latter case, the inductance of the neutral reactor should be stated;
- mechanical endurance: Shunt reactor circuit-breakers are usually subject to frequent operation and class M2 should be specified.

16.2.6.3 Circuit-breaker selection

Overvoltages can be limited either by proper selection of the circuit-breaker or by suitable protection schemes (e.g. surge arresters and controlled switching – point-on-wave switching). For HV circuit-breakers, by reference to Equation (104), a degree of control of overvoltage levels can be exercised by considering the quantities N, λ and C_P as follows [35]:

N: k_{rv} can be reduced by minimizing the number of interrupters in series on the circuit-breaker.

λ: Choose a circuit-breaker with a low chopping number. For gas circuit-breakers, the chopping number tends to increase with arcing time and therefore the minimum arcing time should be as short as possible.

C_P: The grading capacitance value should be as low as possible.

For vacuum circuit-breakers, where the chopping number approach is not applicable, reference is made to Equation (99) and 16.6. The only circuit-breaker characteristic in the equation is the chopped current level i_c. To provide some overvoltage level control, the choice is to select a vacuum circuit-breaker with contact material that minimizes current chopping [36].

The selection of circuit-breakers for non-effectively earthed shunt reactor switching at voltages ≤ 52 kV differs from that of the HV and EHV cases. At these voltages the current magnitudes are in the range of hundreds to thousands of Amperes (refer to 16.5) and arc voltage rather than current chopping is the consideration. Each application should be related to the TRV requirements for T10/T30 in Table 13 of IEC 62271-100:2008. ~~The procedure to be followed is as follows:~~ From Equation (105) the second term under the root sign will be negligible and k_a can be taken as equal to k_{in}.

~~a) Calculate the frequency of the load side oscillation:~~

~~$$f_L = \frac{1}{2\pi\sqrt{1{,}5LC_L}}$$~~

~~b) Calculate k_a from Equation (105). Note that the second term under the square root will usually be negligible and k_a can thus be taken as equal to k_{in}.~~

~~c) Calculate k_{rv} from Equation (107):~~

~~$$k_{rv} = 2 + k_{in}$$~~

~~d) Calculate the time to peak t_p of the recovery voltage oscillation:~~

~~$$t_p = \frac{1}{2f_L}$$~~

~~e) Calculate the t_3 value:~~

~~$$t_3 = 0{,}87 \times t_p$$~~

~~f) Calculate the rate of rise of the recovery voltage RRRV:~~

~~$$\text{RRRV} = \frac{U_r\sqrt{2}}{\sqrt{3}} \times k_{rv} / t_3$$~~

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~~g) Select the circuit-breaker rating from the above-noted table where both the recovery voltage peak and the rate of rise of recovery voltage equal or exceed the T10/T30 TRV values in the table.~~

16.2.7 Testing

EHV and HV circuit-breaker shunt reactor switching tests are normally unit tests in single phase circuits. The representation of the shunt reactor side circuit is of the essence. The test should be carried out using a directly connected HV shunt reactor and not a transformer coupled shunt reactor. This ensures that the load side oscillation is single frequency (as it should be), that the load side effective capacitance (C_L) can be exactly defined and that the proper interaction between the circuit-breaker and the circuit occurs. The exact definition of the load side effective capacitance, which includes the stray capacitances in the circuit and the circuit-breaker grading capacitance, is mandatory in order to determine the true chopping member of the circuit-breaker.

By reference to Equation (99), the worst case for suppression peak overvoltage generation is at minimum current giving the highest inductance value (L). The purpose of the testing is not so much to demonstrate interrupting capability – the current is after all forced to a premature zero – but rather to establish that the circuit-breaker meets certain performance criteria and to derive its chopping current and chopping number characteristics. These characteristics are dependent on arcing time for most circuit-breaker types and a large number of test shots are required in order to provide confidence in the results. In a typical test, the required number of test shots are applied over the expected range of arcing time and the suppression peak overvoltages are measured. Equation (99) is used to calculate i_c (κ = 0) and then Equation (100) to calculate λ. A regression analysis is required to derive the chopping number characteristic and, once derived, the characteristic can be used to predict actual performance in the field [37].

To be judged as suitable for shunt reactor switching, a circuit-breaker must meet the following two performance criteria:

a) the circuit-breaker shall interrupt the current with at most one re-ignition leading to conduction of another loop of power frequency current. This criterion applies to all three circuit-breaker poles in three-phase tests;

NOTE Multiple high frequency re-ignitions in any one current zero crossing are counted as one re-ignition.

b) all re-ignitions should occur between the arcing contacts.

The application of laboratory test results to actual shunt reactor applications is described in 16.8. Statistical equations associated with 16.8 are given in 16.9.

~~No testing is required for circuit-breakers used in unearthed shunt reactor switching applications. These applications lack the commonality of the chopping number approach and it would be impossible for any laboratory to carry the range of reactor sizes required for the purpose. However, because the applications can be related to the T10/T30 values as described above, these tests constitute proof of the breaker capability for the application.~~

The individual test circuits and TRV parameters for all possible system and shunt reactor application and earthing conditions are given in 6.114 of IEC 62271-110:2012.

16.3 Motor switching

16.3.1 General

High-voltage AC motors are typically in the range 2 kV to 14 kV and 100 kW to 40 MW and can be classified as follows [38]:

- asynchronous squirrel-cage motors, direct starting, starting current 6 to 7 times rated motor current, power factor 0,1 to 0,2;

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- asynchronous slip-ring motors, starting current generally less than 6 times rated motor current;
- synchronous motors, often started by means of a squirrel-cage rotor, starting current 3 to 5 times motor rated current, power factor 0,25 to 0,3.

From a circuit-breaker (or contactor) perspective, the direct started asynchronous motor is the most important category. The characteristics of this application are [38]:

a) Starting current
   - high current (I = 6…7 × motor rated current);
   - low power factor (cos $\varphi \approx$ 0,1…0,2);
   - infrequent operation;
   - due to the higher interrupted current the chopping current can attain higher values;
   - the arcing time for some switching devices may be longer than when the motor is running;
   - according to practical experience the overvoltages when breaking the starting current are usually higher than when breaking no-load or load-current. In addition to possible higher chopping currents, overvoltages are also caused by re-ignitions, which usually are much more numerous when starting current is interrupted.

b) No-load current
   - the no-load current of a small HV motor may be lower than the chopping current level of the circuit-breaker;
   - the power-frequency recovery-voltage is very small compared to the case of breaking the starting current. As the rotor is running a voltage is induced in the stator with a frequency equal to the power frequency during the first periods;
   - re-ignitions are not likely as the recovery voltage is low;
   - low power factor (cos $\varphi \approx$ 0,1).

c) Load current
   - high power factor (cos φ = 0,7 – 0,9);
   - power-frequency recovery voltage is low;
   - low overvoltages, no re-ignitions.

With regard to breaking capability and overvoltage generation, it is clear that the breaking of starting current is the most severe case. This case is discussed in the following based on the CIGRE motor switching equivalent circuit approach.

16.3.2 Chopping and re-ignition overvoltages

The motor switching equivalent circuit is shown in Figure 84.

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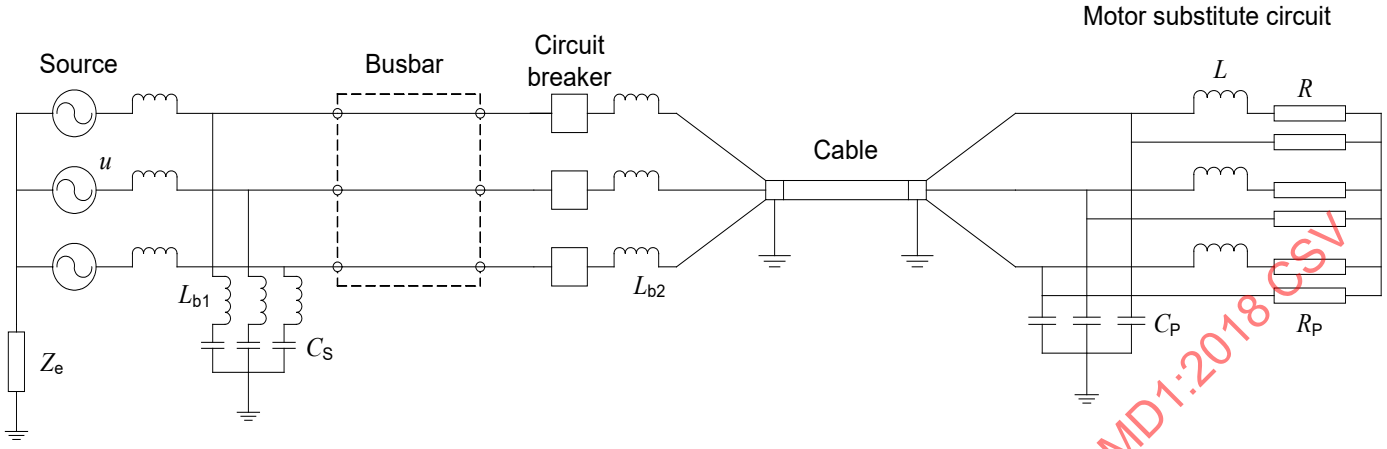

Key

u	Rated voltage	R_P	Motor substitute parallel resistance
Z_e	Earthing impedance	L_{b2}	Inductance of connections
L_s	Source side inductance	L	Motor substitute inductance
C_s	Supply side capacitance	R	Motor substitute resistance
L_{b1}	Inductance of capacitors and connections	C_P	Motor substitute parallel capacitance

Figure 84 – Motor switching equivalent circuit

Motor switching is analogous to the non-effectively earthed shunt reactor switching case and the equations for this case as shown in 16.6 can be applied with the following qualifications:

a) C_L is the total motor and cable capacitance per phase. The cable is treated as a lumped capacitance;

b) the equations for k_p and k_s are applicable for the single re-ignition case shown in Figure 81, i.e. no voltage escalation. Voltage escalation is discussed in 16.3.3 below;

c) the chopping number approach is not applicable to vacuum circuit-breakers or contactors.

16.3.3 Voltage escalation

A characteristic of vacuum circuit-breakers or contactors is their ability to interrupt high frequency currents. This can lead to repeated prestriking and interruption during a closing operation and repeated re-ignition and interruption during an opening operation. In both cases this can result in a phenomenon referred to as voltage escalation [39 – 43]. Voltage escalation occurs when successive re-ignitions and interruptions result in increasing values of the initial voltage for the load side oscillations and hence increasing TRV values across the circuit-breaker.

Voltage escalation is hazardous to the motor due to the high stress imposed on the turn-to-turn winding insulation by the steep fronted re-ignition overvoltage excursions. However, voltage escalation can be suppressed by RC dampers or by gapped metal oxide surge suppressors on the load side of the motor [44 – 46].

16.3.4 Virtual current chopping

Virtual current chopping is the suppression of one current (power frequency load current) by the superposition of another (induced high frequency current). The chopping is caused by the coupling of a re-ignition in one phase to one or two of the other phases. This mutual coupling is the reason for the inclusion of an open busbar section in the test circuit shown in Figure 83 [49]. The occurrence of virtual current chopping is limited to small motors (20 kW to 100 kW) operating at the higher voltages of 6,6 kV or 11 kV [46, 47].

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16.3.5 Overvoltage limitation

Some method of overvoltage limitation is applied in all motor circuits with the intent of protecting the motor insulation against steep front re-ignition overvoltage transients. The various methods and their effectiveness are reviewed in Table 31. The re-ignition circuit is that equivalent to the second parallel oscillation circuit described in 16.2.4.4.

Table 31 – Re-ignition overvoltage limitation method evaluation for motor switching

Overvoltage limitation method	How does the method work?	Advantage	Disadvantage
Surge arresters to earth at motor terminals [46, 47]	Limits overvoltage to earth at the motor.	Passive.	Effective only for circuit-breakers producing suppression peak overvoltages in excess of the surge arrester protective level; re-ignitions can still occur at up to twice the above protective level with no reduction in the re-ignition overvoltage excursion frequency; has little or no influence on multiple re-ignitions associated with vacuum circuit-breakers.
Surge suppressors at circuit-breaker terminals [43, 44]	Limits overvoltage to earth at the motor.	Passive; more effective than surge arrester given that it consists of a metal oxide varistor (MOV) in series with gap thereby resulting in a lower protective level.	Similar to that for surge arresters but more effective in limiting multiple re-ignitions.
Surge capacitors at motor terminals [46, 47]	Decreases frequency of the motor circuit recovery voltage and also frequency of the re-ignition overvoltage excursion.	Effective for circuit-breaker types other than vacuum circuit-breakers; may reduce k_a for vacuum circuit-breakers where the chopping current is dependent mainly on contact material	Multiple re-ignitions will still occur with vacuum circuit-breakers; single re-ignitions will still occur with other circuit-breaker types.
RC damper at motor terminals [41, 42, 43]	Introduces losses into the re-ignition circuit; high frequency re-ignition current damped and becomes exponentially decaying current with no zero crossing.	Properly selected can eliminate multiple re-ignitions, voltage escalation and virtual current chopping in adjacent phases.	Cost of losses in resistor; each installation may have to be treated as unique thereby restricting use of standard components; no waveshaping effect of capacitor; fast surges up to 3 p.u. still possible.
Zinc oxide (ZnO) RC-damper at motor terminals [47]	ZnO surge arrester is applied across the resistor and operates when the re-ignition overvoltage exceeds ≤ 1,5 p.u. inserting the capacitor.	Offers the advantages of both surge capacitors and RC-dampers; overvoltages can be limited to 2 p.u.	Cost of losses in resistor; each installation may be unique.

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Overvoltage limitation method	How does the method work?	Advantage	Disadvantage
Series reactors [45]	Applied in series with the circuit-breaker provides damping of the high frequency re-ignition currents.	Damps the high frequency re-ignition currents and limits the voltage escalation process; reduces the steepness of the surges imposed on the motor windings.	Does not eliminate multiple re-ignitions and voltage escalation; not in common use having been applied only in Japan at voltages up to 6,6 kV; cost of losses; noise.
MOV across circuit-breaker [48]	Limits the voltage across the circuit-breaker at which re-ignitions can occur to the protective level of the varistor.	Magnitude and probability of re-ignitions are reduced; multiple re-ignitions and voltage escalation are suppressed.	Does not eliminate multiple re-ignitions and voltage escalation; steep surges can still be imposed on motor even though the magnitude of the overvoltages may be limited.

16.3.6 Circuit-breaker specification and selection

16.3.6.1 General

The specification and selection of circuit-breakers (or contactors) for motor switching is simpler than for the case of shunt reactors. While shunt reactor switching devices are often customized, off-the-shelf devices are generally used for motor switching. This is enabled by the application of overvoltage limitation measures as appropriate to the type of switching device.

16.3.6.2 Circuit-breaker specification

The following characteristics should be specified:

- dielectric withstand requirements;
- motor rating;
- motor starting, load and no-load currents;
- load side characteristics: motor starting equivalent inductance and the total effective capacitance including the connecting cable;
- mechanical endurance: class M1 or M2 in accordance with expected frequency of operation.

16.3.6.3 Circuit-breaker selection

The two predominant circuit-breaker technologies in use for motor switching today at medium voltage are SF_6 based on self-extinguishing and vacuum. While both technologies offer equal or relative performance with regard to application characteristics, both are well-suited for motor switching [48]. The choice of technology will in most cases be based on the installed cost of the circuit-breaker and associated overvoltage limitation measures.

16.3.7 Testing

The circuit-breaker should be tested in accordance with the requirements of IEC 62271-110.

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16.4 Unloaded transformer switching

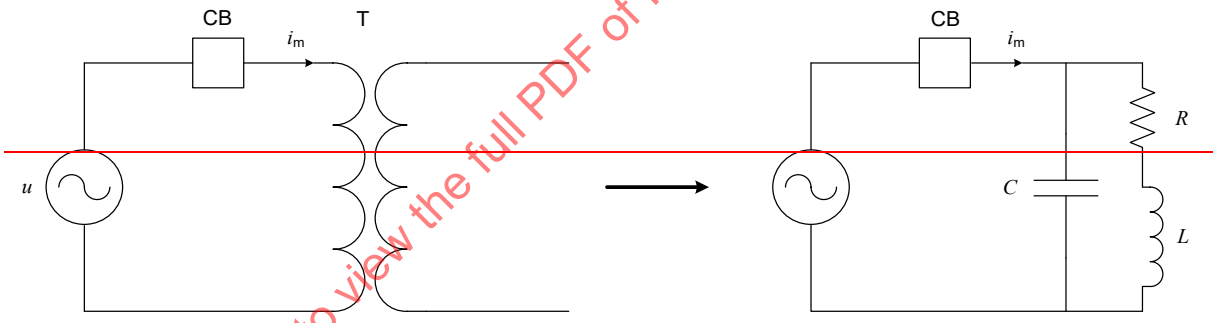
16.4.1 General

Due to the enormous variations in transformer ratings and the non-linear behaviour of the core, it is not possible to model the switching of no-load transformers using linear components in a test laboratory. A test on an available transformer would only be valid for that transformer at the particular level of excitation used and would not be representative for other excitation levels on the same transformer and certainly not for other transformers. In summary, type testing for no-load transformers is not required for two reasons. Firstly, the duty is less severe than any other switching duty and secondly, the duty cannot in any case be correctly modelled in a test laboratory.

In exceptional cases at voltages of 52 kV and below where there is an agreement with the manufacturer and the user to test a specific combination of circuit-breaker and transformer, reference can be made to the French National Standard[8] for unloaded transformer switching tests for circuit-breakers rated at 1 kV to 36 kV.

16.4.2 Oil-filled transformers

The switching of no-load oil-filled transformers from the high-voltage side using high-voltage circuit-breakers is not considered onerous or to deserve particular attention. The reason for this is that the stresses imposed on the circuit-breakers are very much less severe than for any other switching duty. The magnitude of the current is negligible, generally less than 1 A for modern low-loss transformers. The load side TRV is an under-damped oscillation whose circuit parameters can be derived from the factory core measurements and impulse test circuit. The equivalent circuit for the unloaded transformer is as shown in Figure 85. An example of an actual unloaded transformer TRV field measurement is shown in Figure 86.



Key

u	Source voltage	i_m	Magnetizing current of the transformer
CB	Circuit-breaker	L, R, C	Components representing transformer
T	Transformer		

Figure 85 – Unloaded transformer representation for TRV calculation

[8] UTE C64-115, February 1990.

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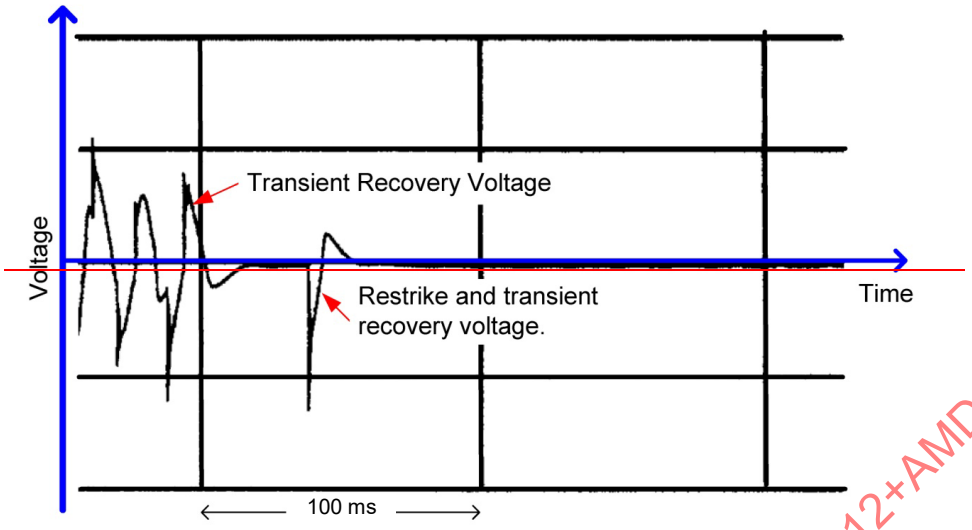

Figure 86 – TRV on switching out an unloaded 500 kV, 300 MVA transformer bank

16.4.3 Dry type transformers

16.4.3.1 General

In systems at ≤ 52 kV the use of dry type transformers is common. Such transformers are often switched with vacuum circuit-breakers. This case has certain similarities to motor switching including the fact that there is usually a length of cable between the circuit-breaker and the transformer [50]. The transformers can be treated, as for both shunt reactors and motors, as a capacitance in parallel with an inductance. The effective capacitance is much lower than for oil-filled transformers and is in the order of 200 pF to 500 pF. The inductance is the magnetizing inductance of the transformer and the magnetizing currents are typically in the range 1 % to 3 % of rated full load current. For example, a 13,8 kV, 5 MVA transformer with 3 % magnetizing current would have a natural frequency of 3,8 kHz (C = 500 pF, L = 3,52 H) assuming that the core losses are insignificant.

16.4.3.2 Overvoltages

Overvoltages are not an issue when switching out high-voltage transformers using SF_6 gas circuit-breakers. However, vacuum circuit-breakers are now used up to 145 kV but no information is available on how they perform in this regard. In any case, transformers are always protected by a surge arrester for other reasons.

Studies have shown that the overvoltage level on switching unloaded dry-type transformers is dependent on the length of cable between the circuit-breaker and the transformer [39]. The results indicate that the longer the cable the lower the overvoltage level, but the overvoltage level tends to increase with increasing MVA for constant cable length. The highest overvoltages occur on multiple re-ignitions and voltage escalation to as high as 3,5 p.u.; interruption of inrush current can result in overvoltages in excess of 5 p.u. [49].

16.4.3.3 Overvoltage limitation

Overvoltage limitation is considered by reference to that for motor switching as discussed in Table 31.

Surge arresters: studies indicate that surge arresters applied at the transformer terminals are effective in limiting overvoltages to earth for transformers.

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~~**Surge capacitors:** surge capacitors have the effect of reducing the surge impedance of the load and thereby the overvoltage levels [39].~~

~~**RC dampers:** effectiveness similar to that described for motor switching applications, i.e. will prevent multiple re-ignitions in vacuum circuit-breakers [50].~~

~~**ZnO-RC dampers:** effectiveness similar to that described for motor switching. Whether such devices have been applied in this context is unknown.~~

~~Series reactors and controlled switching are not viewed as being applicable to this switching duty.~~

~~**16.4.3.4 Circuit-breaker specification and selection**~~

~~In most cases, circuit-breakers rated at 52 kV and below are specified and selected according to requirements other than unloaded transformer switching. The reason for this is that the circuit-breakers are taken to inherently have this capability with due regard to possible overvoltage limitation.~~

16.4.1 General

Unloaded transformer switching is an insignificant duty for circuit-breakers. The current to be interrupted is magnetizing current in the order of a few A at most and the associated transient recovery voltage is minimal as discussed below.

Owing to the enormous variations in transformer ratings and the non-linear behaviour of the core, it is not possible to model the switching of no-load transformers using linear components in a test laboratory. A test on an available transformer would only be valid for that transformer at the particular level of excitation used and would not be representative for other excitation levels on the same transformer, and certainly not for other transformers.

In summary, type testing for no-load transformers is not required for two reasons:

– the duty is less severe than any other switching duty;
– the duty cannot be correctly modelled in a test laboratory.

16.4.2 Transient recovery voltage calculation

Transformers can be oil-filled, dry-type or SF_6 gas filled. The basis for calculation of the transient recovery voltage for the unloaded switching case follows.

Circuit representation for unloaded transformer switching is shown in Figure 165.

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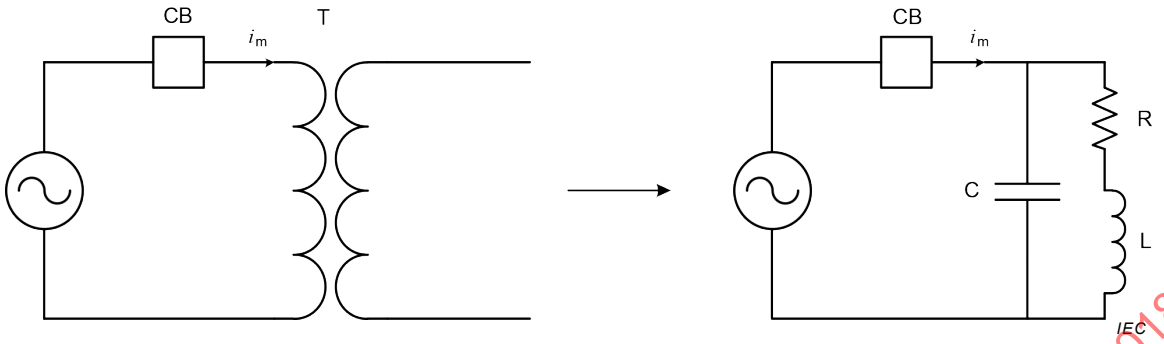

Key

i_m	magnetising current
CB	circuit-breaker
T	transformer
R, L, C	equivalent circuit of the transformer

Figure 165 – Unloaded transformer switching circuit representation

The transformer can be represented as a source-free series RLC circuit. At current interruption, a voltage U remains on the capacitor, which then rings down to zero. The associated oscillation is underdamped with an amplitude factor usually not exceeding 1,3 p.u. at a frequency of a few hundred Hz as illustrated in Figure 166. The transient recovery voltage seen by the circuit-breaker is thus the difference between the source and transformer voltages and tends to be dominated by the former voltage due to the relative peaks not necessarily coinciding.

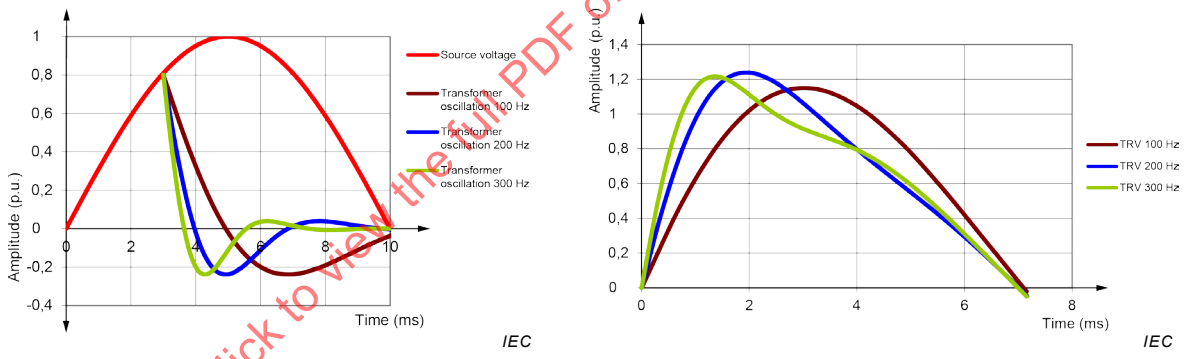

Figure 166 – Transformer side oscillation (left) and circuit-breaker transient recovery voltage (right)

The transformer side oscillation is described by the equation:

$$\upsilon = Ue^{-d_s t_g}\left(\cos\sqrt{1-d_s^2}\ t_g + \frac{d_s}{\sqrt{1-d_s^2}}\sin\sqrt{1-d_s^2}\ t_g\right) \quad (192)$$

where U is the initial voltage, d_s is the degree of damping in the circuit given by $d_s = R\Big/2\sqrt{\frac{L}{C}}$ and t_g is generic time in radians given by $t_g = t/\sqrt{LC}$, t being real time in s [134].

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The parameters for the RLC circuit transformer representation can be approximated from the factory core loss measurements (R and L) and impulse voltage tests (C). The core losses P_o are given by:

$$P_o = U_o I_o \cos\phi \tag{193}$$

where P_o is in W, U_o is the r.m.s. applied voltage in V and I_o is the r.m.s. value of the magnetizing current in A. All three quantities being known, we can write

$$\cos\phi = \frac{P_o}{U_o I_o} \tag{194}$$

and

$$Z = R + \mathrm{j}\omega L = \frac{U_o}{I_o}(\cos\phi + \mathrm{j}\sin\phi) \tag{195}$$

giving

$$R = \frac{U_o}{I_o}\cos\phi \text{ and } L = \frac{U_o}{\omega I_o}\sin\phi \tag{196}$$

The value of C is calculated from the lightning impulse test wave shape time to peak T:

$$T = 2{,}5 \times R_s C_T \tag{197}$$

where R_s is the series resistance in the lightning impulse test circuit and C_T is the total load capacitance including any external front capacitors. If no front capacitors are used, $C_T = C$. As an alternative, the value of C may also be estimated from transformer winding dissipation factor measurements.

The frequency of the transformer side oscillation is given by:

$$f_{tfr} = \frac{1}{2\pi\sqrt{LC}} \tag{198}$$

When an unloaded transformer is de-energised by a circuit-breaker on the high-voltage side, it is very unlikely that any re-ignitions will occur. The re-ignition circuit loop involves the source side capacitance C_s, C and the combined inductance of the circuit-breaker, buswork and earth connections as shown in Figure 167.

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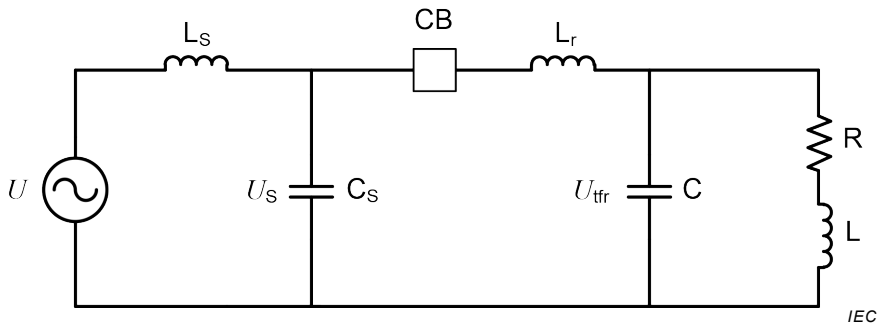

Key

U	System voltage	CB	Circuit-breaker
L_s	Short-circuit inductance	L_r	Bus inductance
U_s	Source voltage	U_{tfr}	Voltage across the transformer
C_s	Source capacitance	C, R, L	Equivalent circuit of the transformer

Figure 167 – Re-ignition loop circuit

Re-ignitions take place in two stages. The re-ignition occurs at a certain voltage difference $U_s - U_{tfr}$ across the circuit-breaker (Figure 167). Initially the two voltages will equalize at a voltage U_e dependent on the ratio C_s/C and then is followed by a second voltage excursion as the equalization voltage adjusts to the source voltage by way of an overvoltage transient U_{ov}. The magnitude of this transient is given by:

$$U_{ov} = U_s + \beta\left(\frac{U_s - U_{tfr}}{1 + C_s/C}\right) \tag{199}$$

where β is the damping factor of value < 1.

In reality, the value of U_{ov} can approach 3 p.u. with respect to earth at a low frequency dependent on the source inductance L_s and the ratio C_S/C.

The transient that causes difficulties for transformers is the equalization transient. While not high in terms of magnitude, its frequency is high given by:

$$f_e = \frac{1}{2\pi\sqrt{L_r\left(\frac{C_S C}{C_S + C}\right)}} \tag{200}$$

This frequency may coincide with the frequency of a possible internal resonance circuit within the transformer which, if triggered, may result in failure of the transformer. IEEE Std. C57.142 [135] contains more information about the interaction of the circuit-breaker, transformer and system.

In systems at ≤ 52 kV the use of dry type transformers is common. Such transformers are often switched with vacuum circuit-breakers. This case has certain similarities to motor switching including the fact that there is usually a length of cable between the circuit-breaker and the transformer [136]. The transformers can be treated, as for both shunt reactors and motors, as a capacitance in parallel with an inductance. The effective capacitance is much lower than for oil-filled transformers and is in the order of 200 pF to 500 pF. The inductance is the magnetizing inductance of the transformer and the magnetizing currents are typically in

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the range 1 % to 3 % of rated full load current. For example, a 13,8 kV, 5 MVA transformer with 3 % magnetizing current would have a natural frequency of 3,8 kHz (C = 500 pF, L = 3,52 H) assuming that the core losses are insignificant.

16.4.3 Overvoltages

Overvoltages are not an issue when switching out high-voltage transformers using SF_6 gas circuit-breakers. However, vacuum circuit-breakers are now used up to 145 kV but no information is available on how they perform in this regard. In any case, transformers are always protected by a surge arrester for other reasons.

Studies have shown that the overvoltage level on switching unloaded dry-type transformers is dependent on the length of cable between the circuit-breaker and the transformer [137]. The results indicate that the longer the cable the lower the overvoltage level, but the overvoltage level tends to increase with increasing MVA for constant cable length. The highest overvoltages occur on multiple re-ignitions and voltage escalation to as high as 3,5 p.u.; interruption of inrush current can result in overvoltages in excess of 5 p.u. [138].

16.4.4 Overvoltage limitation

Overvoltage limitation is considered by reference to that for motor switching as discussed in 16.3.5.

Surge arresters: studies indicate that surge arresters applied at the transformer terminals are effective in limiting overvoltages to earth for transformers.

Surge capacitors: surge capacitors have the effect of reducing the surge impedance of the load and thereby the overvoltage levels [137].

RC dampers: effectiveness similar to that described for motor switching applications, i.e. will prevent multiple re-ignitions in vacuum circuit-breakers [136].

ZnO-RC dampers: effectiveness similar to that described for motor switching. Whether such devices have been applied in this context is unknown.

16.4.5 Circuit-breaker specification and selection

In most cases, circuit-breakers rated at 52 kV and below are specified and selected according to requirements other than unloaded transformer switching. The reason for this is that the circuit-breakers are taken to inherently have this capability with due regard to possible overvoltage limitation.

16.5 Shunt reactor characteristics

16.5.1 General

At 72,5 kV and above, shunt reactors are generally directly connected to station busbars or to transmission line terminations and are solidly earthed or through a neutral reactor (sometimes referred to as a four-reactor scheme). At voltages below 72,5 kV, reactors are commonly connected to system transformer tertiary windings and are usually unearthed

16.5.2 Shunt reactors rated 72,5 kV and above

The majority of the installed shunt reactors at 72,5 kV and above are in the 30 Mvar to 300 Mvar (three-phase) range. The largest single-phase units have a rating of 400 Mvar as a three-phase group.

The characteristics of shunt reactors depend to a great extent on the design, which can be:

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- three-legged gapped iron-core;
- five-legged gapped iron-core;
- shell-type gapped iron-core;
- coreless (air-cored).

Table 32 gives some typical shunt reactor characteristics.

Table 32 – Typical shunt reactor electrical characteristics

Applied voltage kV	Rating Mvar	Power frequency Hz	Rated current A	Inductance H	Capacitance nF	Natural frequency kHz
765	150 – 300	60	113 – 226	5,17 – 10,35	1,7 – 4,0	1,1 – 1,7
735	330	60	259	4,34	1	2,4
525	135	60	148	5,43	1,8 – 4,0	1,1 – 1,6
400	120 – 200	50	173 – 289	2,55 – 4,25	1,9 – 3,2	1,4 – 2,3
236	125	60	306	1,18	2,1	3,2
132	55	50	240	1,0	1,3	4,4
115	25	60	126	1,4	2,9	2,5
60	20	60	190	0,48	2,0	5,1
36	35 – 100	50/60	560 – 1 600	98 – 34	0,8 – 2 [a]	9 – 16 [b]
24	35 – 100	50/60	840 – 2 400	44 – 15	0,8 – 2 [a]	14 – 24 [b]
17,5	40 – 80	50/60	1 400 – 2 600	20 – 10	0,8 – 2 [a]	21 – 29 [b]
12	40 – 75	50/60	1 900 – 3 600	10 – 5	0,8 – 2 [a]	29 – 41 [b]

[a] Oil-filled reactor capacitance phase-to-earth ignoring internal capacitive coupling between phases.

[b] Applicable to first-pole-to-clear.

In the range 72,5 kV to 245 kV, reactors are most commonly oil-filled and have three-legged gapped cores with layer, continuous disc or interleaved disc windings. Air-cored dry type reactors in the range 69 kV to 145 kV are in use.

At 300 kV to 550 kV, reactors are single-phase or three-phase units with three-legged, five-legged or shell-type cores (with the wound core legs gapped). The windings are of the layer, continuous disc or interleaved disc type.

At 735 kV and 765 kV, reactors are almost exclusively banks of single-phase units with similar constructions as for 550 kV single-phase units.

The effective capacitance values of the reactors are dependent on the design and construction. For oil-filled units, the capacitance is composed of bushing capacitance, winding series capacitance and winding capacitances to earth or to shields. Bushing capacitances range from 500 pF to 800 pF.

Effective winding capacitances vary from a minimum of about 1 200 pF to a maximum of about 3 500 pF, layer windings having the lowest values and interleaved disc windings the highest values. For dry coil units, no bushings are involved and capacitance is that due to windings to earth and winding series capacitance. Both of these values are low, the latter so

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because of the large number of turns inherent in such coils, and the effective capacitance is in the range 300 pF to 500 pF.

For general reactor switching application and laboratory testing purposes, oil-filled reactors can reasonably be assumed to have an effective capacitance of at least 2 000 pF. This will give natural frequencies of 1 kHz to 5 kHz for reactors rated 72,5 kV to 800 kV, the lower frequencies being applicable at the higher voltages and vice versa.

16.5.3 Shunt reactors rated below 72,5 kV

Shunt reactors rated below 72,5 kV are either oil-filled, three-legged iron-core units or dry coil units. Table 32 gives some typical shunt reactor characteristics in this range.

Table 32 illustrates the wide range of current and natural frequency applicable in this voltage range. For dry-coil reactor units, the capacitance to earth is in the range 300 pF to 500 pF and the corresponding natural frequencies will be two to three times those given in the above table.

16.6 System and station characteristics

16.6.1 General

System (source) and station characteristics interact with the circuit-breaker during the switching of shunt reactors and must be considered in the application of circuit-breakers for this purpose.

16.6.2 System characteristics

The system characteristics which impact on reactor switching are the source inductance and the source side capacitance. The source inductance can be derived from the prevailing short-circuit level at the station. The source side capacitance is in general very much greater than the load side capacitance. For circuit-breaker type testing purposes, the former capacitance is assumed to be at least 10 times greater than the latter.

16.6.3 Station characteristics

Directly connected shunt reactors are connected either to station busbars or to overhead lines. A worldwide survey has shown that connection to busbars is three times more common than that to transmission lines. The characteristics which are of relevance are the inductance of the connecting busbar or line and any capacitances in addition to that of the reactor. Typical values are given in Table 33.

Table 33 – Connection characteristics for shunt reactor installations

Connection	Inductance μH/m	Capacitance pF/m
Busbar/line	1	10
Cable	0,2 – 0,5	200 – 400
GIS	0,2	60

The inductance of even the longest connection lengths (150 m to 200 m) is not significant compared to the inductance of high-voltage reactors, but does influence the re-ignition process. The capacitance of long connecting busbar/line lengths (up to 170 m reported), and relatively short cable or busbars in gas insulated substations (GIS) lengths is significant compared to that of the reactor and must be considered. Additionally, other connected equipment between the circuit-breaker and the reactor will also contribute to the overall load

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side capacitance and may also require consideration. Capacitance values for such equipment are given in Table 34.

Table 34 – Capacitance values of various station equipment

Equipment	Capacitance[a] nF
Capacitive voltage transformers	2 – 16
Current transformers	0,15 – 1,2
Voltage transformers	0,15 – 0,45
Surge arresters	0,08 – 0,12
Switch disconnectors	0,06 – 0,20
Busbar support insulators	0,05
GIS air entrance bushings	
- SF_6[b]	0,03 – 0,15
- Capacitor[c]	0,10 – 1
- Epoxy[d]	0,10 – 1

[a] Variation is with voltage rating.
[b] Without capacitive voltage grading.
[c] Oil-filled with capacitive voltage grading.
[d] Resin impregnated with capacitive voltage grading.

16.7 Current chopping level calculation

When interrupting small inductive currents, circuit-breakers will force the current to zero prior to the natural current zero. This phenomenon is referred to as current chopping, the degree of which and associated resultant overvoltages, depends on the type of circuit-breaker and the circuit involved.

Current chopping is caused by an unstable interaction between the arc and the circuit. Arc instability is defined as any abrupt change in the conductivity of the arc occurring away from the natural zero in the current loop and having its origin in the arc characteristic and/or the arc cooling mechanism. In the early 1960s Rizk showed for arcs in gases and oil that, following a rapid change of arc current, the arc voltage will approach a new stationary value through an exponential curve, which is characterized by a time constant [51, 52]. Assuming initial static arc conditions of a current I_a giving an arc voltage of U_a, the response to a step current change of δI is:

$$U(t) = U_a + R_i \delta I + (R_a - R_i)\delta I e^{-t/\theta},$$

where $R_i = \left(\frac{dU}{dI}\right)_{I=I_a}$ i.e. the incremental or dynamic arc resistance, which is negative for low current arcs (see Figure 87),

$R_a = \frac{U_a}{I_a}$ is the static arc resistance;

and θ is the thermal time constant of the arc. θ is proportional to the current and is dependent on the circuit-breaker cooling mechanism [51, 52].

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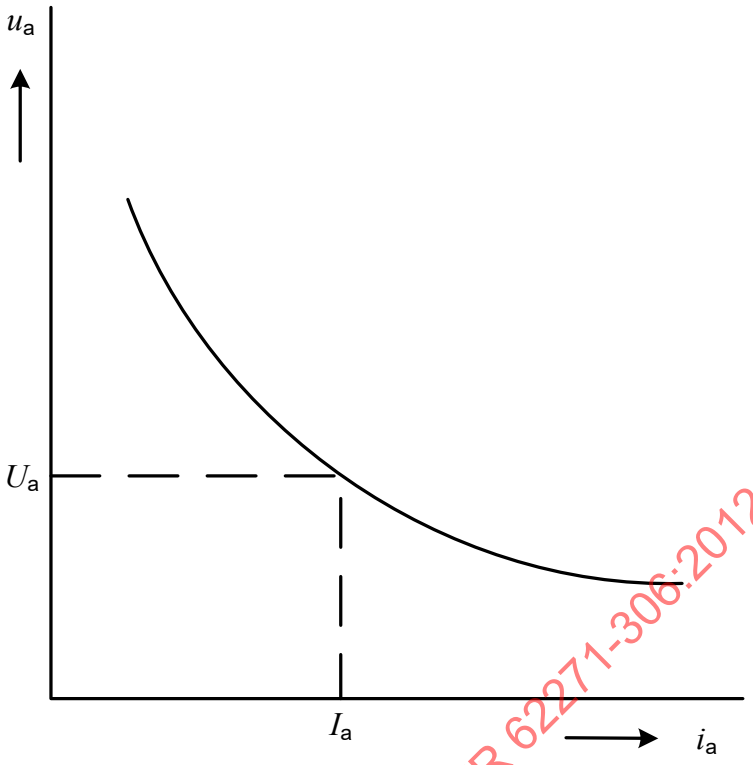

Figure 87 – Arc characteristic

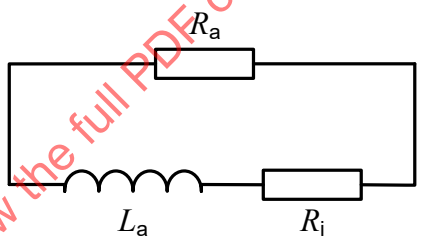

Figure 88 – Rizk's equivalent circuit for small current deviations from steady state

Rizk recognized that the above behaviour could be represented by means of an equivalent circuit assuming that the static characteristic of the arc is given by the equation:

$$u_a i_a^{\alpha} = n \tag{114}$$

where u_a is the arc voltage, i_a the arc current, α a constant and n a statistically random variable.

The equivalent circuit for the arc is shown in Figure 88.

In the equivalent circuit, R_a is as defined above and

$$R_i = -\frac{\alpha R_a}{1+\alpha} \tag{115}$$

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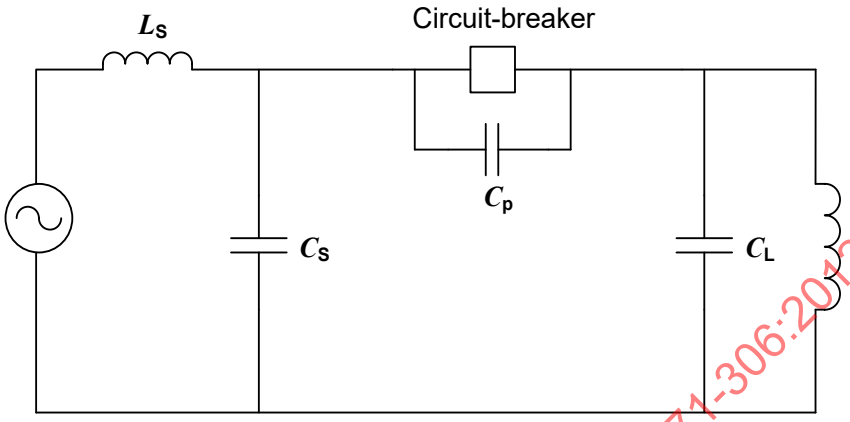
and

$$L_a = \frac{\theta R_a}{1+\alpha} \tag{116}$$

The single-phase equivalent circuit for inductive current switching is shown in Figure 89.



Key

L_s	Source side inductance
L	Load inductance
C_s	Source side capacitance
C_L	Load side capacitance
C_p	Capacitance across the circuit-breaker

Figure 89 – Single phase equivalent circuit

L_s and L are large enough to prevent rapid current changes and local bus inductance is assumed small enough to be neglected. Therefore, the external circuit which interacts with the arc is C_p (grading or stray capacitance) in parallel with C_s and C_L in series and designated as C in the following.

The combined arc/external-circuit circuit that can be used to calculate the instability limit is as shown in Figure 90.

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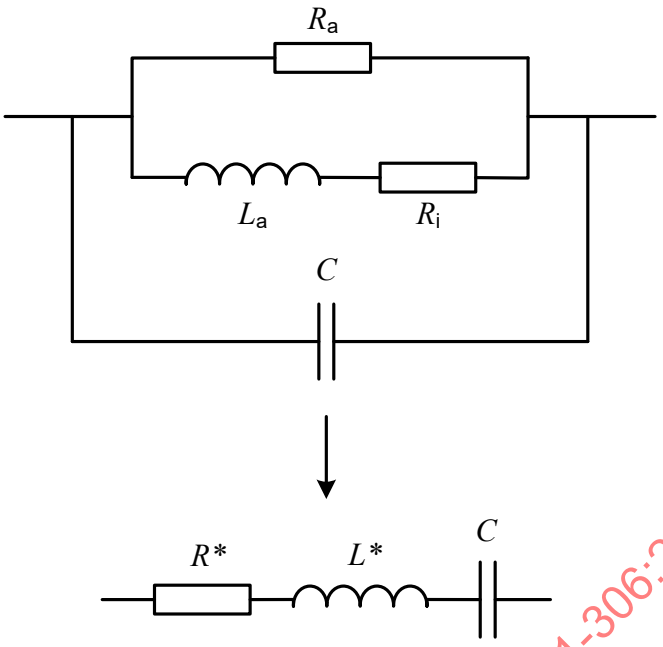

Figure 90 – Circuit for calculation of arc instability

The impedance Z of the circuit is:

$$Z = \frac{R_a(R_i + j\omega L_a)}{R_a + R_i + j\omega L_a} + \frac{1}{j\omega C} \quad (117)$$

or

$$Z = R^* + j\left(\omega L^* - \frac{1}{\omega C}\right) \quad (118)$$

where

$$R^* = \frac{R_a R_i(R_a + R_i) + \omega^2 R_a L_a^2}{(R_a + R_i)^2 + \omega^2 L_a^2} \quad (119)$$

and

$$L^* = \frac{L_a R_a}{(R_a + R_i)^2 + \omega^2 L_a^2} \quad (120)$$

The circuit becomes unstable when the real part of Z, i.e. R^*, becomes negative resulting in negative damping. This occurs, then, at an angular frequency of ω_i (the instability limit) when

$$R_a R_i(R_a + R_i) + \omega_i^2 R_a L_a^2 < 0 \quad (121)$$

Substituting for R_i and L_a (Equations (119) and (120)) in Equation (121) gives

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$$\omega_i < \frac{\sqrt{\alpha}}{\theta} \tag{122}$$

At ω_i, the arc behaves like a pure inductance

$$L^*_{\omega i} = \frac{L_a R_a}{(R_a + R_i) + \omega_i^2 L_a^2}$$

Again substituting for R_i and L_a, this gives

$$L^*_{\omega i} = \theta R_a \tag{123}$$

Now,

$$\omega_i^2 = \frac{1}{L^*_{\omega i} C} = \frac{1}{\theta R_a C} = \frac{\alpha}{\theta^2}$$

or

$$\alpha R_a C = \theta \tag{124}$$

The circuit will become instable and chop the current when Equation (124) is fulfilled. If I_c is the chopped current, then at chopping

$$R_a = \frac{U_{ac}}{I_c}$$

but $U_{ac} = nI_c^{-\alpha}$ giving

$$R_a = nI_c^{-\alpha-1} \tag{125}$$

Substituting for R_a in Equation (124)

$$\alpha n I_c^{-\alpha-1} C = \theta$$

or

$$I_c = \left(\frac{\alpha n}{\theta} \times C\right)^{\frac{1}{\alpha+1}} \tag{126}$$

Laboratory tests have shown that α is approximately 1 and thus

$$I_c = \sqrt{\frac{n}{\theta} C} \tag{127}$$

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or

$$I_c = \lambda\sqrt{C} \tag{128}$$

Equation (130) has been shown to be valid for air-blast [53, 54], minimum oil [54, 55] and SF_6 circuit-breakers [54, 56, 57]. The frequency of the instability oscillation is high and chopping can be considered to be instantaneous.

16.8 Application of laboratory test results to actual shunt reactor installations

16.8.1 General

The purpose of this subclause is to describe the procedure, based on laboratory test results, to be followed to estimate the overvoltage levels that will occur in actual shunt reactor installations and to determine the suitability of a particular circuit-breaker for the purpose.

The procedure described applies principally to shunt reactor installations with solidly earthed neutrals. The procedure may however be applied with suitable adaptation to the unearthed and neutral reactor earthed cases. Due to the statistical nature of overvoltage generation, it is necessary to apply statistical methods to estimate the risk for overvoltages at or above certain levels. Applicable statistical equations are given in 16.9 for convenience.

16.8.2 Overvoltage estimation procedures

16.8.2.1 Chopping number of one interrupter

The main characteristic evaluated in the laboratory test is the chopping number (λ). The chopping number is an inherent characteristic of the circuit-breaker and is usually independent of the circuit. The chopping number can therefore be used to estimate the behaviour of the circuit-breaker in other circuits than the test circuit.

The chopping number varies statistically and must be expressed in terms of:

- a mean value;
- a standard deviation;
- dependence on arcing time (if applicable).

The chopping number for a single interrupter circuit-breaker is defined by:

$$\lambda = i_{ch} / \sqrt{C_t} \tag{129}$$

where

i_{ch} is the chopped current value; and

C_t is the total capacitance in parallel with the circuit-breaker.

The value of chopped current should, if possible, be directly measured for each test and current zero at which interruption is attempted or achieved.

If actual measurement is not possible, then i_{ch} can be calculated for *solidly earthed reactors* using Equation (130):

$$i_{ch} = U_0\sqrt{\frac{C_L}{L}\left(k_a^2 - k_{in}^2\right)} \tag{130}$$

λ is then calculated using Equation (129).

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Equation (130) is restricted to single-phase reactors or solidly earthed reactors. The determination of the chopping number is usually made in single-phase tests.

If only three-phase tests with *unearthed reactors* are available for estimation of the chopping number, Equation (131) can be used.

$$i_{ch} = U_0 \sqrt{\frac{C_L}{1{,}5L}\left[(k_a + 0{,}5)^2 - (k_{in} + 0{,}5)^2\right]} \tag{131}$$

If C_L is not explicitly known, it can be calculated from the load oscillation frequency since the effective inductance can be assumed equal to the power frequency value, L, which is always known. Refer to 16.2.4.

The values of i_{ch} and λ will vary statistically from test to test. If the values show no clear dependence on the arcing time, the statistical variation is usually a normal distribution. On this basis, the mean value, λ_{mean}, and the standard deviation s are calculated according to 16.9.

In the event that i_{ch} and λ exhibit a clear dependence on arcing time, a linear relationship can be assumed as a first approximation:

$$\lambda_{mean} = A + Bt_a \tag{132}$$

where t_a is the arcing time. The constants A and B can be derived by performing a linear regression. The dispersion around the regression line will probably be wide and therefore it is also necessary to derive the standard deviation of the regression line (generally referred to as the standard error of estimate). Refer to 16.8.3 and 16.9.

16.8.2.2 Estimation of chopping overvoltages in shunt reactor installations

For the first case, where the chopping number is independent of the arcing time, the maximum chopping number for one interrupter is given by:

$$\lambda_{max} = \lambda_{mean} + 2\sigma \tag{133}$$

Statistically, this is the 2 % value, i.e. the value that will be exceeded in less than 2 % of the switching operations.

To estimate the maximum suppression peak overvoltage to earth for a circuit-breaker with N interrupters in series, the applicable value of λ_{max} is inserted in Equation (102) or its derivative Equations (103) or (104).

For the second case, where the chopping number is dependent on arcing time, the maximum chopping number will occur at the maximum arcing time, $t_{a\ max}$. The maximum chopping number (2 % value) for a single interrupter is given by:

$$\lambda_{max} = (A + Bt_{a\ max} + 2S_e) \tag{134}$$

where S_e is the standard error of estimate defined in 16.9.

The maximum suppression peak overvoltage is calculated using Equation (136).

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16.8.2.3 Estimation of re-ignition overvoltages in shunt reactor installations

It is important to note that overvoltages occurring in laboratory tests due to re-ignitions have no relevance for the estimation of re-ignition overvoltages in actual shunt reactor installations. Estimated re-ignition overvoltage levels are derived on the basis described in 16.2.3.

For the case where the chopping number is independent of arcing time, re-ignition overvoltages k_p and k_s are given by Equations (108) and (109), respectively.

For circuit-breakers, whose chopping numbers vary with arcing time, the applicable k_a value is that obtained at the longest arcing time (t_{ar}) resulting in a re-ignition. The value t_{ar} can generally be considered as the longest arcing time, $t_{a\ max}$, less one half-cycle. The applicable maximum chopping number is thus:

$$\lambda_{max\ r} = A + Bt_{ar} + 2\ S_e \quad (135)$$

This value is then used in Equations (102) or (135) to derive the actual value of $k_{a\ max\ r}$. Finally, $k_{p\ max}$ and $k_{s\ max}$ are derived using equations (108) and (109), respectively.

16.8.2.4 Evaluation of recovery voltage stress across circuit-breaker

The maximum recovery voltage across the circuit-breaker ($k_{r\ max}$) in per unit value is given by the following:

- for solidly earthed reactors:

$$k_{r\ max} = 1 + k_{a\ max} \quad (136)$$

- for unearthed reactors:

$$k_{r\ max} = 2 + k_{a\ max} = 1{,}5 + k_{b\ max} \quad (137)$$

- for neutral reactor earthed reactors:

$$k_{r\ max} = 1 + 2\ \kappa + k_{a\ max} \quad (138)$$

16.8.3 Case studies

16.8.3.1 General

Laboratory tests were carried out at 141 kV on a single interrupter SF_6 circuit-breaker in a single-phase circuit as shown in Figure 89. The details of the test circuit are given in Table 35.

Table 35 – Laboratory test parameters

Parameter	Load circuit 1	Load circuit 2
Current (A r.m.s.)	337	84
L (H)	1,125	4.5
C_S (nF)	20	10
C_L (nF)	2	1

As required by IEC 62271-110, the initial voltage (k_{in} p.u.), the suppression peak overvoltage (k_a p.u.) and the associated arcing times were measured.

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The measured values of k_{in} and k_a are shown in Figure 91 and Figure 92, respectively. The chopped current values are calculated using Equation (131) and the chopping numbers using Equation (129) and shown in Figure 93 and Figure 94, respectively.

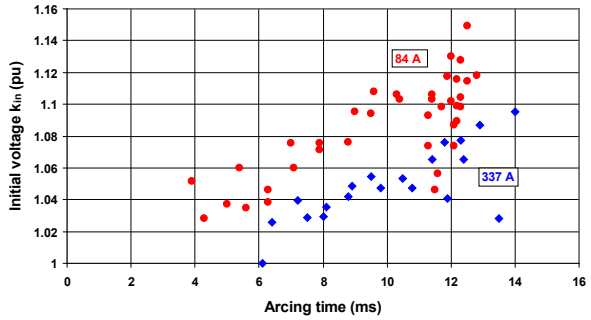

Figure 91 – Initial voltage versus arcing time

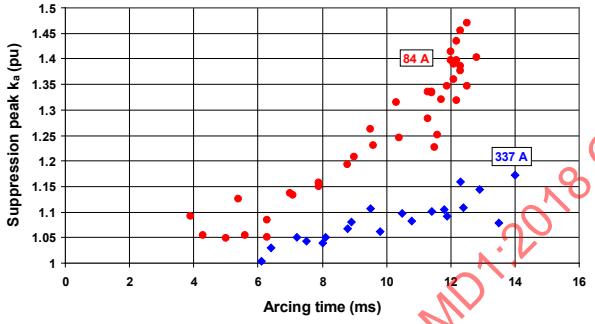

Figure 92 – Suppression peak overvoltage versus arcing time

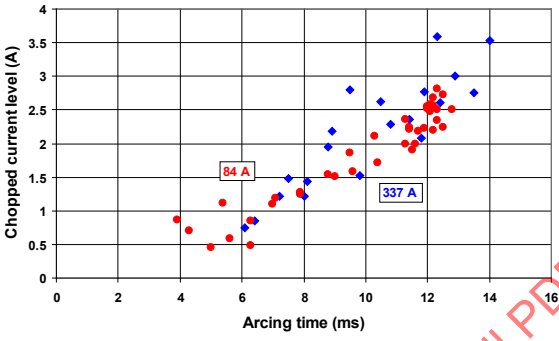

Figure 93 – Calculated chopped current levels versus arcing time

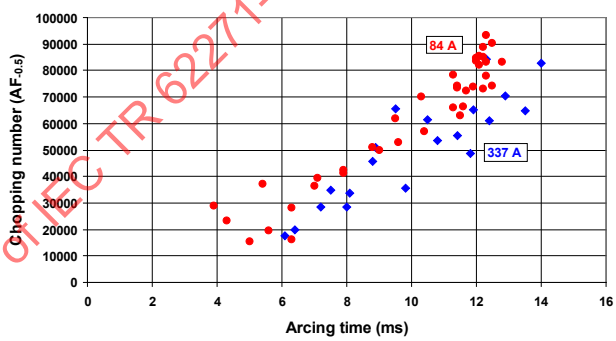

Figure 94 – Calculated chopping numbers versus arcing time

Figure 95 shows the linear regression of all test points using the equations given in 16.8:

$\lambda_{mean} = 7\,755\ t_a - 19\,859$ and $\lambda_{max} = 7\,755\ t_a - 196$

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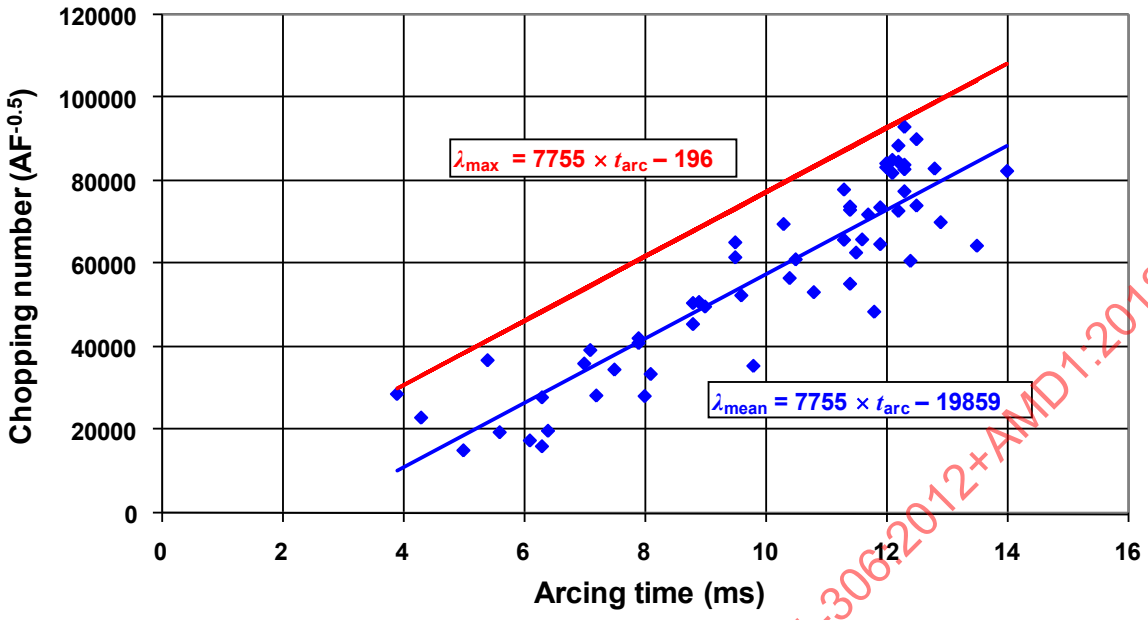

Figure 95 – Linear regression for all test points

The results are now applied to a two-interrupter 500 kV circuit-breaker switching a 525 kV, 135 Mvar shunt reactor at 50 Hz. 1 p.u. voltage = $525\sqrt{2}/\sqrt{3}$ = 428 kV.

16.8.3.2 Case 1, solidly earthed shunt reactor C_P/C_L << 1 and no overvoltage limitation applied

t_a = 13 ms

λ_{max} = 100 619 $AF^{-0,5}$

k_{in} = 1,13 p.u.

From Equation (104):

$$k_{a\,max} = \sqrt{1{,}13^2 + \frac{1{,}5 \times 100\,619^2 \times 2}{314 \times 135 \times 10^6}} = 1{,}4 \text{ p.u.}$$

From Equation (136):

$k_{r\,max}$ = 2,4 p.u. (1 027 kV)

16.8.3.3 Case 2: As for Case 1 except C_P/C_L = 0,5

$k_{r\,max}$ = 2,53 p.u. (1 084 kV)

16.8.3.4 Case 3: As for Case 1 except controlled switching applied at t_a = 8 ms

λ_{max} = 61 844 $AF^{-0,5}$

k_{in} = 1,08 p.u.

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$$k_{a\,max} = \sqrt{1{,}08^2 + \frac{1{,}5 \times 61\,844^2 \times 2}{314 \times 135 \times 10^6}} = 1{,}2 \text{ p.u.}$$

$k_{r\,max}$ = 2,2 p.u. (942 kV)

16.8.3.5 Case 4: As for Case 2 except controlled switching applied at t_a = 8 ms

$k_{r\,max}$ = 2,25 p.u. (963 kV)

16.8.3.6 Case 5 As for Case 1 except reactor neutral earthed through 1 600 Ω reactor (κ = 0,3)

From Equation (103):

$$k_{a\,max} = \sqrt{1{,}43^2 + \frac{1{,}5 \times 1{,}3 \times 100\,619^2 \times 2}{314 \times 135 \times 10^6}} - 0{,}3 = 1{,}42 \text{ p.u.}$$

From Equation (138)

$k_{r\,max}$ = 3,02 p.u. (1 292 kV)

16.8.3.7 Case 6: As for Case 2 except reactor neutral earthed through 1 600 Ω reactor (κ = 0,3)

$k_{r\,max}$ = 3,16 p.u. (1 352 kV)

16.8.3.8 Case 7: As for Case 5 except controlled switching applied at t_a = 8 ms

λ_{max} = 61 844 $AF^{-0,5}$

k_{in} = 1,08 p.u.

$$k_{a\,max} = \sqrt{1{,}38^2 + \frac{1{,}5 \times 1{,}3 \times 61\,844^2 \times 2}{314 \times 135 \times 10^6}} - 0{,}3 = 1{,}2 \text{ p.u.}$$

$k_{r\,max}$ = 2,8 p.u. (1 198 kV)

16.8.3.9 Case 8: As for Case 6 except controlled switching applied at t_a = 8 ms

$k_{r\,max}$ = 2,86 p.u. (1 224 kV)

16.8.3.10 Summary of cases 1 through 8

The calculated transient recovery voltage values are summarized in Table 36.

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Table 36 – 500 kV circuit-breaker TRVs

Case	Reactor	C_P/C_L	Controlled switching (Y/N)	$k_{r\,max}$ kV_{peak}
1	Solidly earthed	0	N	1 027
2		0,5	N	1 084
3		0	Y	942
4		0,5	Y	963
5	Neutral reactor earthed	0	N	1 292
6		0,5	N	1 352
7		0	Y	1 198
8		0,5	Y	1 224

Comments on the $k_{r\,max}$ values in Table 36:

a) For solidly earthed reactors, controlled switching is usually applied without except and results in a limiting of the transient recovery voltage across the circuit-breaker. However, the circuit-breaker should be capable of successful current interruption at the maximum arcing time and associated higher transient recovery voltage;

b) For applications where the reactor is earthed through a neutral reactor, it is common practice to earth the neutral point using a single-pole disconnector prior to switching out the reactor. The benefit to the circuit-breaker transient recovery voltage requirements is obvious from Table 36.

For comparison, the test results applied to a 1 000 kV, 330 Mvar reactor using a four interrupter circuit-breaker, and assuming that neutral is always solidly earthed prior to switching, are shown in Table 37.

Table 37 – 1 000 kV circuit-breaker transient recovery voltages

C_P/C_L	Controlled switching (Y/N)	$k_{r\,max}$ kV_{peak}
0	N	1 925
0,5	N	2 015
0	Y	1 779
0,5	Y	1 811

For the cases where controlled switching is not applied, re-ignitions are a possibility. For the 500 kV circuit-breaker cases, the maximum values of k_p and k_s (derived using Equations (107) and (108)) are shown in Table 38.

Table 38 – 500 kV circuit-breaker: maximum re-ignition overvoltage values

Case	Reactor	C_P/C_L	$k_{p\,max}$ kV_{peak}	$k_{s\,max}$ kV_{peak}
1	Solidly earthed	0	942	1 540
2		0,5	970	1 626
5	Neutral reactor earthed	0	1 074	1 938
6		0,5	1 104	2 028

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16.9 Statistical equations for derivation of chopping and re-ignition overvoltages

16.9.1 General

The purpose of this subclause is to provide, for convenience, the statistical equations used in the derivation of chopping and re-ignition overvoltages.

16.9.2 Chopping number independent of arcing time

With reference to Equation (132):

$$\lambda_{\text{mean}} = \frac{1}{n}\sum_{i=1}^{n}\lambda_{\text{i}} \tag{139}$$

and

$$\sigma^2 = \frac{n\sum_{i=1}^{n}\lambda_{\text{i}}^2 - \left(\sum_{i=1}^{n}\lambda_{\text{i}}\right)^2}{n(n-1)} \tag{140}$$

where

n is the number of test shots;

λ_{i} chopping number corresponding to the i^{th} test shot.

16.9.3 Chopping number dependent on arcing time

Calculate values for S_{xx}, S_{yy} and S_{xy} as follows:

$$S_{\text{xx}} = n\sum_{i=1}^{n}t_{\text{ai}}^2 - \left(\sum_{i=1}^{n}t_{\text{ai}}\right)^2$$

$$S_{\text{yy}} = n\sum_{i=1}^{n}\lambda_{\text{i}}^2 - \left(\sum_{i=1}^{n}\lambda_{\text{i}}\right)^2$$

$$S_{\text{xy}} = n\sum_{i=1}^{n}t_{\text{ai}}\lambda_{\text{i}} - \left(\sum_{i=1}^{n}t_{\text{ai}}\right)\left(\sum_{i=1}^{n}\lambda_{\text{i}}\right)$$

where n and λ_{i} are as noted above and t_{ai} is the arcing time corresponding to the i^{th} test shot.

With reference to Equation (132):

$$B = \frac{S_{\text{xy}}}{S_{\text{xx}}} \tag{141}$$

$$A = \frac{1}{n}\sum_{i=1}^{n}\lambda_{\text{i}} - \frac{B}{n}\sum_{i=1}^{n}t_{\text{ai}} \tag{142}$$

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$$S_e^2 = \frac{1}{n(n-2)}\left(S_{yy} - B^2 S_{xx}\right) \quad (143)$$

17 Information and technical requirements relevant for enquiries, tenders and orders

17.1 General

This clause provides a list of useful technical information items in a tabular form to be considered for possible exchange between user and supplier during contracting stage.

When in the table "supplier information" is mentioned, this means that only the supplier needs to deliver this information.

Attention should be paid to the fact that such table should be complemented with information and characteristics relevant for the type of switchgear and controlgear considered; see product standards.

17.2 Normal and special service conditions (refer to Clause 2 of IEC 62271-1:2007)

		User requirements	Supplier proposals
Service condition	Indoor or Outdoor		
Ambient air temperature: Minimum Maximum	 °C °C		
Solar radiation	W/m^2		
Altitude	m		
Pollution	Class		
Excessive dust or salt			
Ice coating	mm		
Wind	m/s		
Humidity	%		
Condensation or precipitation			
Vibration	Class		
Induced electromagnetic disturbance in auxiliary and control circuits	kV		

17.3 Ratings and other system parameters (refer to Clause 4 IEC 62271-1:2007)

		User requirements	Supplier proposals
Nominal voltage of system	kV		
Highest voltage of system	kV		
Rated voltage for equipment (U_r)	kV		
Rated insulation levels phase to earth and between phases Rated short-duration power-frequency withstand voltage (U_d) Rated switching impulse withstand voltage (U_s) – phase to earth	 kV kV kV		

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		User requirements	Supplier proposals
– between phases Rated lightning impulse withstand voltage (U_p)	kV kV		
Rated frequency (f_r)	Hz		
Rated continuous current (I_r)	A	According single line	
Rated short-time withstand current (I_k)	kA		
Rated peak withstand current (I_p)	kA		
Rated duration of short circuit (t_k)	s		
Rated supply voltage of closing and opening devices and of auxiliary and control circuits (U_a)	V		
Rated supply frequency of closing and opening devices and of auxiliary circuits	Hz	DC or 50 or 60	
Type of system neutral earthing		Effectively or non-effectively	

17.4 Design and construction (refer to Clause 5 of IEC 62271-1:2007)

As required by the relevant standards.

		User requirements	Supplier proposals
Number of phases	Three- or single-phase encapsulation		
Mass of the heaviest transport unit			
Mounting provisions			
Type of gas-pressure or liquid-pressure system			
Overall dimensions of the installation			
Description by name and category of the various compartments			
Rated filling level and minimum functional level			
Low- and high-pressure interlocking and monitoring devices			
Interlocking devices			
Degrees of protection			
Arrangement of the external connections			
Accessible sides			
Volume of liquid or mass of gas or liquid for the different compartments			
Facilities for transport and mounting			
Instructions for operation and maintenance			
Specification of gas or liquid condition			

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17.5 Documentation for enquiries and tenders

		User requirements	Supplier proposals
Scope of supply (training, technical and layout studies and requirements for co-operating cycle with other parties)			
Single-line diagram			
General arrangement drawings of substation layout			
Provisions for transport and mounting to be given by the user			
Foundation loading		Supplier information	
Gas schematic diagrams		Supplier information	
List of type test reports		Supplier information	
List of recommended spare parts		Supplier information	

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Annex A
(informative)

Consideration of DC time constant of the rated short-circuit current in the application of high-voltage circuit-breakers

A.1 General

A time constant of 45 ms is generally adequate on systems rated 800 kV and below. For 1 100 kV and 1 200 kV systems, the standardized d.c. time constant has been defined as 120 ms mainly because the use of multi-conductor bundles on transmission lines. Alternative special case d.c. time constants, related to the rated voltage of the circuit-breaker, should cover cases where the standard d.c. time constant 45 ms is not sufficient. This may apply, for example, to systems with very high rated voltage (for example 800 kV systems having higher d.c. time constant for lines e.g. when multi-conductor bundles are used), to some medium voltage systems with radial structure or to any systems with particular system structure or line characteristics. Alternative special case d.c. time constants have been defined in subclause 4.101.2 of IEC 62271-100:2008 taking into account the results of the survey by CIGRE WG13.04 [58].

When specifying an alternative special case d.c. time constant, the following considerations should be taken into account:

a) The d.c. time constants referred to in IEC 62271-100 are only valid for three-phase fault currents. The single-phase to earth short-circuit d.c. time constant is generally lower than that for three-phase fault currents.

b) For maximum asymmetrical current, the initiation of the short-circuit current has to take place at system voltage zero in at least one phase.

c) The d.c. time constant is related to the maximum rated short-circuit current of the circuit-breaker. If, for example, higher d.c. time constants than 45 ms are expected but with a short-circuit current lower than rated, such a case may be covered by the asymmetrical rated short-circuit current test using a 45 ms time constant (see following paragraphs for equivalency examples).

d) The d.c. time constant of a complete system is a time-dependent parameter considered to be an equivalent constant derived from the decay of the short-circuit currents in the various branches of that system and is not a real, single and unique d.c. time constant value.

e) Various methods for the calculation of the d.c. time constant are in use, the results of which may differ considerably. Caution should be taken in choosing the right method.

f) When choosing an alternative special case d.c. time constant, it has to be kept in mind, that the circuit-breaker is stressed by the asymmetrical current after contact separation. The instant of contact separation corresponds to the sum of the opening time of the circuit-breaker and the reaction time of the protection relay. In IEC 62271-100, this relay time is defined as one half-cycle of power frequency. If the protection time is longer this should be taken into account.

g) The choice of a single special case value of the d.c. time constant minimises the number of tests required to demonstrate the capability of the equipment.

For example, a test carried out on a circuit-breaker at 63 kA with a d.c. time constant of 45 ms does not automatically cover the performance of a circuit-breaker having a rating of 50 kA with a d.c. time constant of 75 ms, actual test parameters should be known in order to determine if the equivalency can be made.

Some general important aspects need to be considered. In order to state the equivalency of a certain circuit-breaker for another fault current rating and d.c. time constant, the following parameters have to be examined carefully in relation to the interrupting technology used:

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1) amplitude of the last current loop before interruption;

2) duration of the last current loop before interruption;

3) arcing time window;

4) arc energy;

5) di/dt at current interruption;

6) TRV peak voltage u_c and first reference voltage u_1, as applicable.

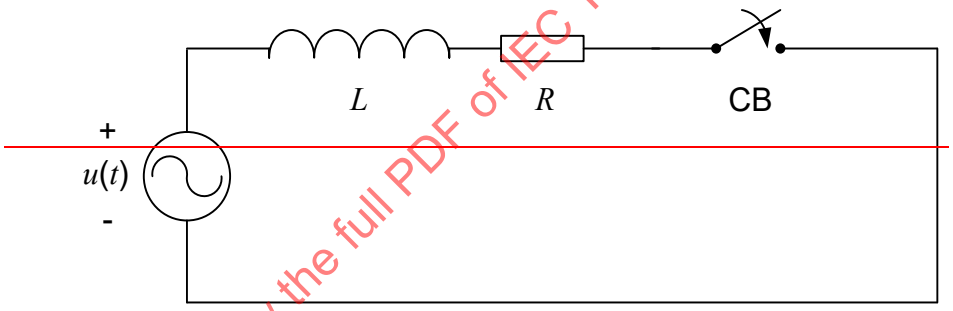
A.2 Basic theory

One of the duty that a circuit-breaker has to perform is to interrupt all short-circuit currents up to its rated short-circuit current. The short-circuit current may be symmetrical, partly asymmetrical or fully asymmetrical depending on the instant where the fault was initiated.

Asymmetrical occur in all type of inductive circuits and the level of asymmetry depends on the instant of fault initiation and the d.c. time constant (τ) of the circuit under evaluation.

NOTE The d.c. time constant of a circuit is sometimes expressed as the X/R ratio of a circuit, where $X = 2\pi f \times \tau$, where f is the power frequency in Hz and R represent the losses (Ω) in the circuit.

The simplified single-phase circuit shown in Figure A.1 illustrates the studied case.



Key

$u(t)$	Source voltage, $u(t) = U\sin(\omega t + \alpha)$	R	Losses in the circuit
L	Source inductance	CB	Circuit-breaker

Figure A.1 – Simplified single-phase circuit

In case of power systems ωL is generally $>> R$.

By using differential equations, the resulting current is:

$$I(t) = \frac{U}{Z} \times \left[\sin(\omega t + \alpha - \varphi) - e^{-t/\tau} \times \sin(\alpha - \varphi) \right] \quad \text{(A.1)}$$

where

U is the peak of the applied voltage $u(t)$;

Z is the circuit impedance: $Z = \sqrt{R^2 + \omega^2 L^2}$;

ω is the angular frequency: $2\pi f$;

α is the fault making angle (instant) on the applied sinusoidal voltage;

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φ is the phase angle of the circuit impedance $\varphi = \tan^{-1}\left(\frac{\omega L}{R}\right) = \tan^{-1}\left(\frac{X}{R}\right)$

τ is the d.c. time constant (L/R) of the circuit.

The resulting fault current has two components, the first part of the equation being the sinusoidal part and the second being the exponential decaying d.c. component.

From Equation (A.1), the d.c. component will be maximum when $\sin(\alpha - \phi) = 1$ or $\alpha - \phi = \pi/2$.

$$I(t)_{max} = I\left[\sin\left(\omega t + \pi/2\right) e^{-t/\tau}\right] \quad \text{(A.2)}$$

The peak value of the current will occur when $\sin(\omega t + \pi/2) = -1$ or $\omega t = \pi$ giving

$$I_{pk} = I\left(1 + e^{-t/\tau}\right) \quad \text{(A.3)}$$

Equations (A.2) and (A.3) are for the negative d.c. component case and, to obtain the positive d.c. component case, multiply the right side by –1. I = U/Z and further equal to $\sqrt{2}$ times the symmetrical r.m.s. interrupting current rating of the circuit-breaker under consideration. The maximum peak current occurs when the circuit is made at a voltage zero crossing.

For the standardized d.c. time constants (45 ms and 120 ms) and the alternative special case d.c. time constants given in IEC 62271-100 (60 ms, 75 ms and 120 ms), the d.c. components in p.u. of the peak symmetrical current are shown in Figure A.2.

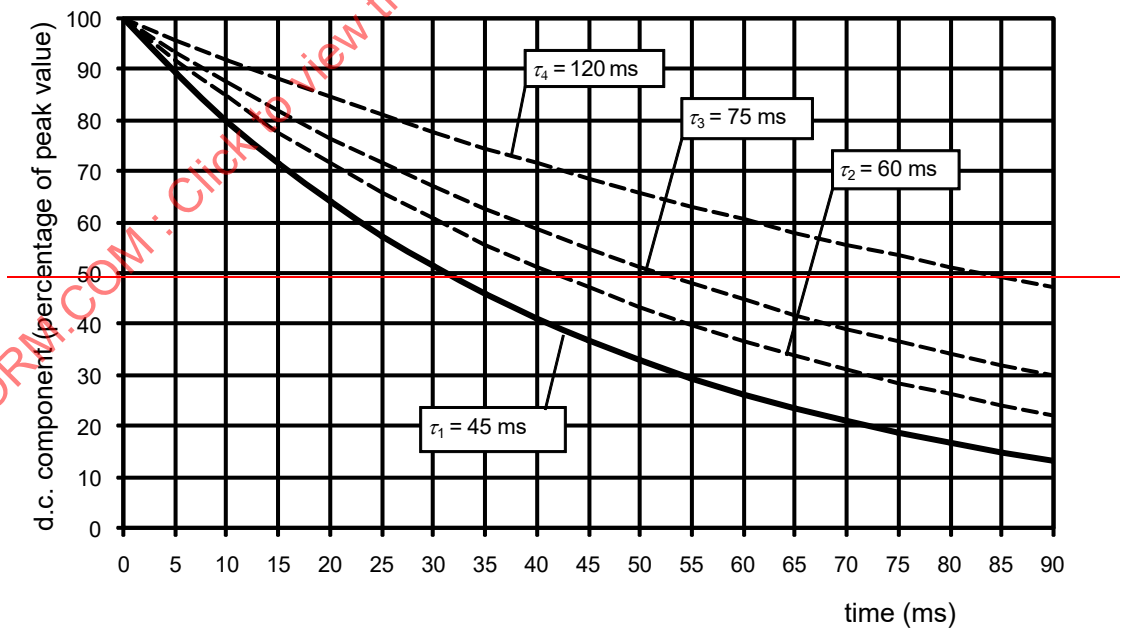

Figure A.2 – Percentage d.c. component in relation to the time interval from the initiation of the short-circuit for the standard time constants and for the alternative special case time constants (from IEC 62271-100)

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Asymmetrical current related values of X/R and I_{peak} are power frequency dependent as summarized in Tables A.1 and A.2. The I_{peak} values in brackets are the recommended values used for standardization purposes in IEC 62271-100.

Table A.1 – X/R values

$\tau = L/R$	50 Hz		60 Hz	
ms	X/R	$\tan^{-1} X/R$	X/R	$\tan^{-1} X/R$
45	14	85,9	17	86,6
60	19	86,9	22,6	87,4
75	23,5	87,5	28,3	87,9
120	37,7	88,5	45,2	88,7

Table A.2 – I_{peak} values

$\tau = L/R$	I_{peak} (p.u.)	
ms	50 Hz	60 Hz
45	2,55 (2,5)	2,59 (2,6)
60	2,61 (2,7)	2,65 (2,7)
75	2,65 (2,7)	2,68 (2,7)
120	2,72 (2,7)	2,73 (2,7)

For a three-phase fault initiated simultaneously in the three phases, the asymmetry level at fault initiation of the most asymmetrical phase is always ranging from 87 % to 100 % whatever instant the fault is initiated on the applied voltage.

The current equations for a three-phase fault initiated simultaneously on the three phases are:

$$I_{\varphi A}(t) = \frac{U}{Z} \times \left[\sin(\omega t + \alpha - \varphi) - e^{-t/\tau} \times \sin(\alpha - \varphi) \right] \quad \text{(A.4)}$$

$$I_{\varphi B}(t) = \frac{U}{Z} \times \left[\sin\left(\omega t + \alpha - \varphi - 2\pi/3\right) - e^{-t/\tau} \times \sin(\alpha - \varphi - 2\pi/3) \right] \quad \text{(A.5)}$$

$$I_{\varphi C}(t) = \frac{U}{Z} \times \left[\sin\left(\omega t + \alpha - \varphi + 2\pi/3\right) - e^{-t/\tau} \times \sin(\alpha - \varphi + 2\pi/3) \right] \quad \text{(A.6)}$$

In the first edition of IEC 62271-100 (and earlier editions of IEC 60056), the concept of d.c. component of the rated short-circuit current was used together with the asymmetry level at contact separation. At that time, a single unified standardized d.c. time constant of 45 ms was specified. With the introduction of new alternative special cases d.c. time constants, the concept of defining asymmetry level at contact separation has been changed to the concept of last current loop parameters since this is the important aspect to consider for arc energy and di/dt prior to interruption. This concept also allows performing tests on a circuit-breaker with a test circuit having a different time constant than the rated one and does also permit to validate more than one rating from the results obtained from a single T100a test series.

The considerations given in this section are based on the assigned ratings of the circuit-breaker and on the actual test parameters measured during the T100a test-duty.

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The purpose of this subclause is to give guidance how to use test results for validating other ratings with other d.c. time constants from a single test series results and to give guidance on how to modify the test parameters in order to obtain the required last current loop parameters. However, in doing this, the scope of this section is limited since the amplitude, duration and the di/dt at current zero all change as the d.c. time constant changes. A higher asymmetry results in a lower du/dt and peak value of the TRV, reducing the stress during the recovery process. This fact has been disregarded in the subclause dealing with equivalency and therefore the results can be considered conservative when the results obtained from a test series validating a lower d.c. time constant are used to validate an higher d.c. time constant rating. On the contrary, care should be exercised on the TRV parameters when the results obtained from a test series validating an higher d.c. time constant are used to validate a lower d.c. time constant rating. Annex P of IEC 62271-100:2008 gives the methodology for calculating TRV parameters during asymmetrical fault condition.

IEC 62271-100 introduces tolerances for testing purposes during the last current loop of arcing interval prior to interruption. A ±10 % tolerance is specified on both last current loop amplitude and duration. There is an additional allowance if the tolerances on current amplitude or current loop duration cannot be fulfilled then the product "$I \times t$", "I" being the peak value of the last current loop and "t" being the duration of the last current loop, is between 81 % and 121 % of the required values.

The application of generator circuit-breakers with delayed current zeros is beyond the scope of this section and this specific case is covered in Annex B.

A.3 Network reduction

The rate of decay of the d.c. component is usually expressed as the d.c. time constant of the short-circuit current.

It should be noted that the d.c. time constant of the short-circuit current at the point of the fault is not the simple ratio of L/R typically obtained by network reduction short-circuit programs because each component of the network has its own d.c. time constant. Experience has shown that using the R and L values obtained by the typical network reduction short-circuit program will give the correct short-circuit current. However, the d.c. time constant based on the ratio of these values will generally be less than the correct value.

Transient calculation programs need to be used in order to obtain the correct d.c. time constant of a particular network location.

A.4 Special case time constants

With the publication of the first edition of IEC 62271-100 the concept of a circuit-breaker being able to deal with d.c. time constants other than the standard time constant of 45 ms was introduced for the first time. IEC 62271-100 specifies additional "special cases time constants" of 60 ms, 75 ms and 120 ms in 4.101.2. In 4.101.2 b) of IEC 62271-100:2008 the following insight is provided:

– 120 ms for rated voltages up to and including 52 kV;

– 60 ms for rated voltages from 72,5 kV up to and including 420 kV;

– 75 ms for rated voltages 550 kV and 800 kV.

Moreover, Amendment 1 of the second edition of IEC 62271-100 introduces a second standardized d.c. time constant of the rated short-circuit current of 120 ms for circuit-breakers rated above 800 kV.

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For application of circuit-breakers on power systems, IEC 62271-100 calls attention to the fact that not all applications fall within the confines of existing standard. This is a logical extension for the following reasons:

– the lower voltage circuit-breakers will frequently be applied close to generation or step down transformers or current limiting reactors which exposes the circuit-breakers in such locations to the much longer d.c. time constants;

– at the higher system voltages, bundled conductors may be used on transmission lines and the circuit-breaker again may be close to transformers. The bundled conductors and the transformer reactance will contribute to the higher d.c. time constant.

For the circuit-breaker application engineer this raises the question of how to evaluate the individual applications. This clause tries to provide some guidance.

A.5 Guidance for selecting a circuit-breaker

A.5.1 General

To evaluate the effect of different d.c. time constants some general observations can be made. For cases in which the actual short-circuit current is less but the d.c. time constant is greater the di/dt of the current at current zero and the amplitude of both current loops will be less than the rated values. The arc energy represented by the area under the major current loop is probably one of the most important consideration. The amplitude and duration of the major current loop are directly related to the d.c. time constant of the short-circuit current.

In an effort to evaluate the effect of different d.c. time constants, the standardized d.c. time constants of 45 ms and 120 ms, and special case d.c. time constants of 60 ms, 75 ms, 90 ms and 120 ms were examined.

IEC 62271-100 specifies criteria on the last current loop amplitude and duration. The important parameter to be considered is the arc energy from contact separation to interruption and the last current loop is of prime importance because generally most of the arc energy is within that last current loop, at least for modern circuit-breakers. The exact result would have been to compare the integral of the current waveshape from contact separation to current zero but this type of calculation is not practical in test laboratories. It is not all test laboratories having proper digital data acquisition systems or sufficient calculation tools to perform such calculation. Instead IEC 62271-100 asks to compare the parameters of the last current loop (I_{peak}, loop duration and product "$I \times t$"). Such measurements are easy to perform and can be done in all test laboratories without any specific constraints.

The methodology to evaluate the effect of different time constants is as follows:

a) Determine the last current loop parameters (amplitude and duration) obtained during T100a test series (last loops (minor and major if tested single phase) or major and extended major current loop amplitudes and durations if tested three-phase.

b) Use Equation (A.1) to find the current waveshape of the specific case to be studied. Use an "α" of 0 rad in order to obtain the full asymmetrical offset.

c) Determine where the interruption will take place. The time sequence events in the operation of a circuit-breaker that always precede the actual interruption and tend to establish the most likely time for interruption are:

   – relay time;

   – circuit-breaker minimum opening time;

   – minimum arcing time;

   – The sum of the above times is defined in IEC 62271-100 as the minimum clearing time. The next full major current loop found is the earliest full major loop or extended major current loop that the circuit-breaker can see in service.

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IEC 62271-100 has tabulated the last loop current parameters for standardized and alternative special cases d.c. time constants for both 50 Hz and 60 Hz systems. Equation (A.1) can also be used to find the exact (non-rounded) current loop parameters.

Some assumptions have been taken:

a) The arc voltage is constant during the period of arcing. This allows the arc energy of the last current loop to be represented by the "$I \times t$" product;

– A smaller symmetrical fault current with a longer d.c. time constant (compared with the rated short-circuit current and the standard time constant) has a larger percentage of d.c. component and the resultant di/dt is always less than the one associated with the highest rated short-circuit current. In such case, the circuit-breaker should still be able interrupt at the normal current zero if it has met all other criteria (see NOTE);

b) If the arc energy represented by the "$I \times t$" product is less than 121 % of the standard wave, the interruption will be generally successful (see NOTE);

c) If the energy represented by the "$I \times t$" product is greater than 121 % of that of the standard interruption, the interruption could be unsuccessful.

NOTE Some circuit-breaker technologies use the arc energy as the main source of energy for current interruption. For such technologies, a lower arc energy may result in longer arcing times and the ability of interrupting lower current should be carefully evaluated. Care should be exercised in the evaluation of the minimum arcing time. The arc energy associated with minor current loops are lower for higher d.c. time constants which may result in a longer minimum arcing time and thus in a longer maximum and medium arcing times.

The determination of the area X under the current curve may be obtained by solving Equation (A.5). This equation is the exact calculation method.

$$X = \int_{t_1}^{t_2} i(t)\mathrm{d}t \qquad \text{(A.7)}$$

where

$i(t)$ is the total current i_{total} as given in Equation (A.1);

t_1 is the time of contact separation;

t_2 is the time of current zero where interruption could occur.

As said before, this method cannot be easily used in test laboratories because it necessitates digital data acquisition systems with proper software which are not always available. Instead, the comparison of the last current loop arcing energy by using the current loop parameters "$I \times t$" is a quite reasonable approximation (within 5 %) of the last current loop integral (see A.5.5).

The general guidance is to de-rate a circuit-breaker one class or approximately 80 % to deal with greater d.c. time constants. The question that must be answered is whether this is sufficient. For test purposes IEC 62271-100 gives the following asymmetry criteria to be fulfilled when performing T100a:

– last current loop amplitude;

– last current loop duration;

– arc energy during the last current loop (product "$I \times t$")

– asymmetry level at current zero.

Using the above methodology the following cases were examined.

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A.5.2 Case 1

Assumptions: Circuit-breaker ratings: I: 63 kA, τ = 45 ms and f = 60 Hz.

– Relay time 8,33 ms;

– Minimum opening time 17 ms;

– Minimum arcing time (interruption after minor loop) 8 ms;

– Frequency 60 Hz;

– Time constant 45 ms;

– Specific tests parameters recorded during T100a test-duty were exactly those associated with the rated values.

Table A.3 shows a comparison of the last major loop parameters for case 1.

Table A.3 – Comparison of last major current loop parameters, case 1

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	63	45	124,5	10,55	1 314
2	50	60	106,1/85,2	11,15/105,7	1 183/90,0
3	50	75	111,3/89,4	11,6/110,0	1 291/98,3
4	50	120	120,7/96,9	12,55/119,0	1 515/115,3

Particular points of Table A.3:

It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (63 kA and τ = 45 ms) had last current loop parameters equal to 100 % of the rated values as shown in the last three columns of row 1.

a) Row 1 provides the reference values for a 63 kA rating with τ = 45 ms as obtained during test duty T100a;

b) The 2nd row shows the requirements for a 50 kA rating with τ = 60 ms. The product "$I \times t$" of the last current loop is in accordance with the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

c) In row 3, the rating is still 50 kA but the time constant has been increased to 75 ms. As for the second row, the product "$I \times t$" of the last current loop is in accordance with the criteria defined in IEC 62271-100;

d) In row 4, the rating is still 50 kA but the time constant has been further increased to 120 ms. The "$I \times t$" product of the last major current loop has increased even more. This is still satisfactory because the product "$I \times t$" of the last current loop is in accordance with the criteria defined in IEC 62271-100.

The equivalence shown before should be carefully studied with the actual waveform of the last current loop parameters used during tests for the demonstration of the reference rating (63 kA and τ = 45 ms). According to IEC 62271-100 and IEC 62271-101 (in case of synthetic testing), it is permissible to have the amplitude and the duration of the last current loop reduced by

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10 % from the rated values. In such case, the last current loop parameters as shown in Table A.4 are obtained.

Table A.4 – Comparison of last major current loop parameters, case 1: test parameters used for the reference case set at the minimum permissible values

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	63	45	112,5 [a]	9,5 [b]	1 060
2	50	60	106,1/94,3	11,15/117,4	1 183/110,7
3	50	75	111,3/98,9	11,6/122,1	1 291/120,8
4	50	120	120,7/107,3	12,55/132,1	1 515/141,7
5	40	120	96,6/85,9	12,55/132,1	1 212/113,4

[a] Last current loop amplitude equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

[b] Last current loop duration equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

Particular points of Table A.4:

It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (63 kA and τ = 45 ms) had a last current loop parameters equal to 90 % of the rated values.

a) Row 1 provides the minimum permissible (90 %) reference values for a 63 kA rating with τ = 45 ms;

b) The 2nd row shows the requirements for a 50 kA rating with τ = 60 ms. The product "$I \times t$" of the last current loop is in accordance with the criteria defined in IEC 62271-100 thus assuring a satisfactory application;

c) The 3rd row shows the equivalence for a 50 kA rating with τ = 75 ms. The product "$I \times t$" of the last current loop is close to the upper maximum limit of the "$I \times t$" criteria defined in IEC 62271-100;

d) As for the case shown in row 3, the rating is still 50 kA but the time constant has been increased to 120 ms. Here the "$I \times t$" product exceeds the upper tolerance stated in IEC 62271-100 and the reference rating does not demonstrate the performance of the circuit-breaker for this fault current (50 kA) and a time constant of 120 ms;

e) The last row shows the requirements for a 40 kA rating with τ = 120 ms. The product "$I \times t$" of the last current loop is in accordance with the criteria defined in IEC 62271-100 thus assuring a satisfactory application.

From the above examples, it can be shown that the actual test parameters obtained during tests are of major importance to determine to which extent the reference test can be used to demonstrate the circuit-breaker ability to interrupt other fault currents with different d.c. time constants. From these examples, it has been shown that the one or two de-rating steps from the R10 series may be needed to cover lower short-circuit currents with higher d.c. time constants.

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Finally, the comparison with the last major current loop parameters may be not enough to state if a particular circuit-breaker may be used for lower rated short-circuit current and higher d.c. time constant values. Some circuit-breaker technologies use the arc energy as the main source of energy for current interruption. For such cases, the "$I \times t$" product of the last minor loop will always be much less than 81 % of the rated values (see Table A.3). Careful evaluation of the minimum arcing time needs to be done. Comparison of minimum arcing times obtained during T10, T30, T60 and T100s can be used as a tool to evaluate the increase of the minimum arcing time due to the reduced arc energy on the minor current loop. If the minimum arcing times found during T10, T30 and T60 are not greater by more than a ¼ cycle from that measured in T100s, then it can be considered that a similar minimum arcing time on the minor loop than the reference case would be obtained. If this is the case, comparison of the last major current loop parameters to access circuit-breaker capabilities is sufficient. If not, additional tests may need to be performed to ensure that the minimum arcing time will not be significantly longer than the reference case.

Table A.5 – Comparison of last minor current loop parameters, case 1

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last minor current loop kA_{peak}/% of the reference case	Duration of the last minor current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	63	45	46,3	5,5	254,7
2	50	60	30,4/65,7	5,0/90,9	152,0/59,7
3	50	75	25,5/55,1	4,5/81,8	114,8/45,1
4	50	120	17,0/36,7	4,0/72,7	68,0/26,7
5	40	120	13,6/29,3	4,0/72,7	54,4/21,4

A.5.3 Case 2

Assumptions: Circuit-breaker ratings: I = 20 kA, τ = 45 ms and f = 50 Hz.

- Relay time 10 ms;
- Minimum opening time 22 ms;
- Minimum arcing time (interruption after minor loop) 8 ms;
- Frequency 50 Hz;
- Time constant 45 ms.

A comparison of the last loop parameters is shown in Table A.6.

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Table A.6 – Comparison of last major current loop parameters, case 2

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	20	45	37,6	12,15	456,8
2	16	60	32,6/86,7	12,9/106,2	420,5/92,1
3	16	75	34,2/90,9	13,5/111,0	461,7/101,1
4	16	120	37,6/100	14,6/120,2	549,0/120,2
5	12,5	120	29,3/78,0	14,6/120,2	427,8/93,6

Particular points of Table A.6:

As mentioned in Table A.1, it should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (20 kA and τ = 45 ms) had a last current loop parameters equal to 100 % of the rated values as shown in the last three columns of row 1 of Table A.6.

a) Row 1 contains the reference values for 50 Hz, 20 kA rating;

b) In rows 2 to 5 it can be seen that a reduction of one step in the R 10 series will cover all cases for τ = 60, 75, 90 and 120 ms. For all these cases, the product "$I \times t$" of the last major current loop is in accordance with the criteria defined in IEC 62271-100 thus assuring a satisfactory application.

As also mentioned for case 1, the applicability of a reference case to other fault currents and different d.c. time constants depends on the actual test parameters measured for the reference case. As an extreme case, if we consider that the last major current loop parameters during the reference test were at the minimum tolerance stated by IEC 62271-100 and IEC 62271-101 then the current loop parameters of Table A.7 are obtained.

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Table A.7 – Comparison of last major current loop parameters, case 2: test parameters used for the reference case set at the minimum permissible values

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	20	45	33,9 [a]	10,94 [b]	370,9
2	16	60	32,6/96,2	12,9/117,9	420,5/113,4
3	16	75	34,2/100,9	13,5/123,4	461,7/124,4
4	16	120	37,6/110,9	14,6/133,5	549,0/148,0
5	12,5	120	29,3/86,4	14,6/133,5	427,8/115,3

[a] Last current loop amplitude equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

[b] Last current loop duration equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

Particular points of Table A.7:

It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (20 kA and τ = 45 ms) had a last current loop parameters equal to 90 % of the rated values.

a) Row 1 provides the minimum permissible (90 %) reference values for a 20 kA rating with τ = 45 ms;

b) The 2nd row shows the requirements for a 16 kA rating with τ = 60 ms. The product "$I \times t$" of the last current loop is in accordance with the criteria defined in IEC 62271-100 thus assuring a satisfactory application;

c) The 3rd and the 4th rows show the equivalence for a 16 kA rating with τ = 75 ms and 120 ms. For these cases, the resulting "$I \times t$" products exceed the upper tolerance stated in IEC 62271-100 and the reference rating does not demonstrate the performance of the circuit-breaker for these cases;

d) The last row shows the requirements for a 12,5 kA rating with τ = 120 ms. The product "$I \times t$" of the last current loop is in accordance with the criteria defined in IEC 62271-100 thus assuring a satisfactory application.

From the above examples, it can be shown, as for case 1, that the actual test parameters obtained during tests are again of crucial importance to determine to which extent the reference test can be used to demonstrate the circuit-breaker ability to interrupt other fault currents with different d.c. time constants. From these examples, it has been shown that the one or two de-rating steps from the R10 series may be needed to cover lower short-circuit currents with higher d.c. time constants.

A.5.4 Case 3

The examples given in A.5.2 and A.5.3 were based on single-phase tests. For three-phase tests on medium voltage circuit-breakers, very short minimum arcing times may be observed in particular for vacuum circuit-breakers. As an extreme example, Figure A.3 shows the resulting current curves for a circuit-breaker having a minimum arcing time of 1 ms.

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For the first valid operation, the interruption occurs on phase A for which the asymmetry criteria is met.

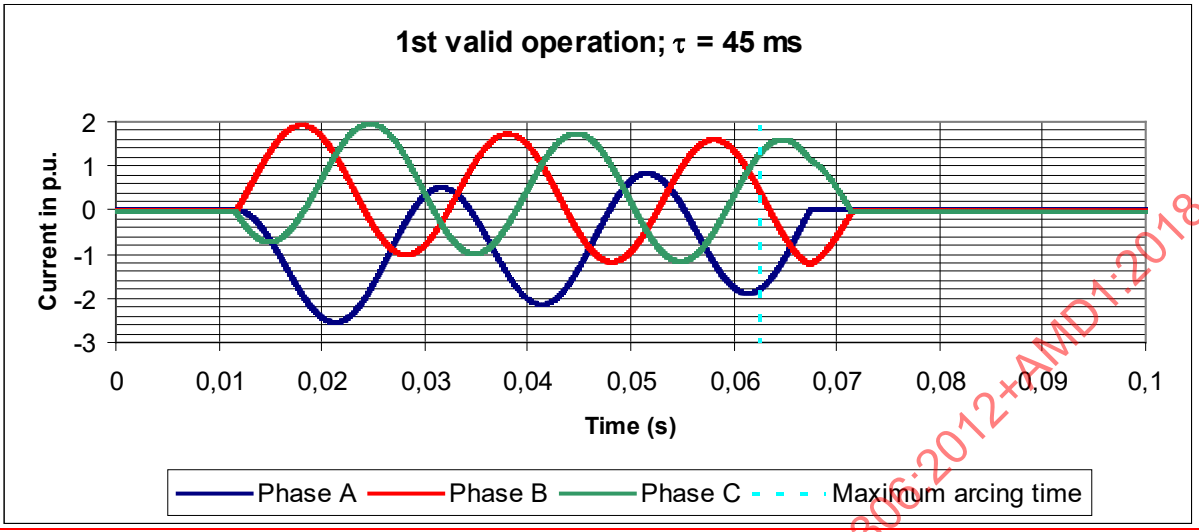

Figure A.3 – First valid operation in case of three-phase test (τ = 45 ms) on a circuit-breaker exhibiting a very short minimum arcing time

This example shows that the maximum possible arcing time on the asymmetrical phase is less than half of the major loop duration. The actual arcing time represents only 40 % of the major loop duration.

For the second test, the procedure given in IEC 62271-100 has been followed and the current oscillogram shown in Figure A.4 is obtained.

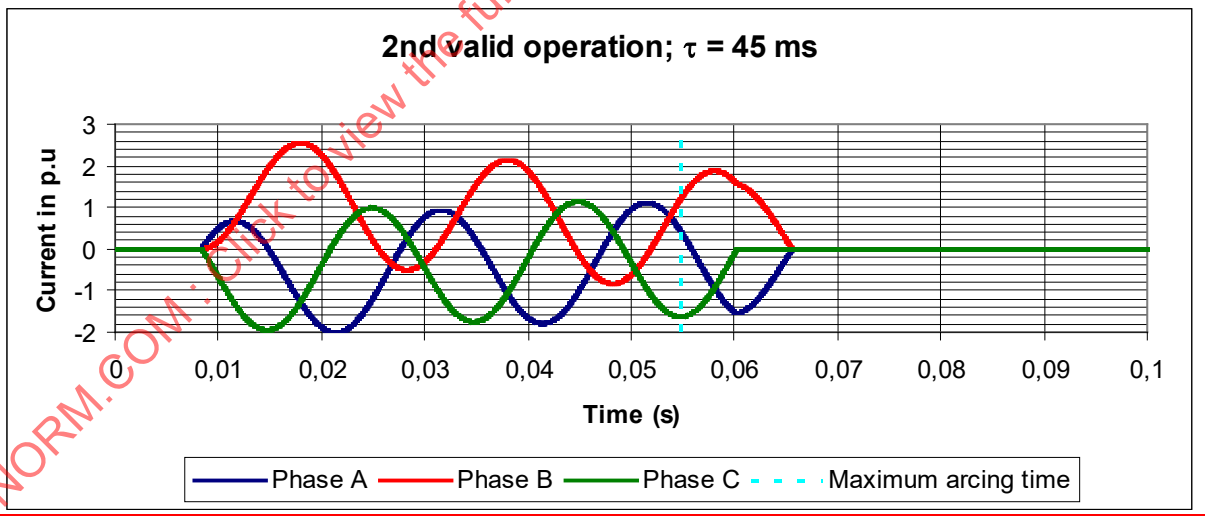

Figure A.4 – Second valid operation in case of three-phase test on a circuit-breaker exhibiting a very short minimum arcing time

The interruption occurs on phase B on an extended major current loop. This example shows that the maximum possible arcing time on the extended major loop is slightly less than the extended major loop duration. The actual arcing time represents 86 % of the extended major loop duration.

Finally, for the third valid operation, the curves of Figure A.5 are obtained:

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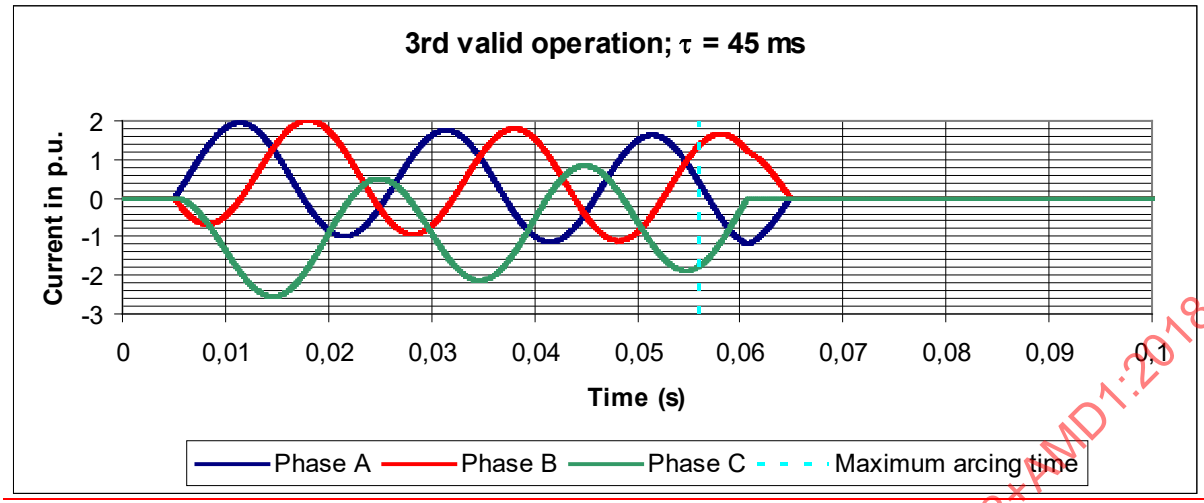

Figure A.5 – Third valid operation in case of three-phase test on a circuit-breaker exhibiting a very short minimum arcing time

The interruption occurs on phase C on a major current loop. Here also, as the first valid operation, the maximum possible arcing time on the asymmetrical phase is less than half of the major loop duration. The actual arcing time represents 46 % of the major loop duration.

The fact that this type of circuit-breakers exhibiting very short minimum arcing time do not see the full major and extended major loop, this raises the question if the "$I \times t$" method stated in IEC 62271-100 is still valid for such circuit-breakers. For the case shown before, the arc energy for the interruption on the major current loop will be not more than 50 % of the one calculated for the full major current loop. For the extended major loop, energy calculation has shown that 89 % of the relative full extended loop energy will be seen by the circuit-breaker.

Similar calculations have been done with a d.c. time constant of 120 ms and the results are very similar, mainly regarding the relative arc energy associated with the major extended current loop. For that particular case, the energy associated with the maximum possible arcing time represents 88 % of the total prospective arc energy of that current loop. For the other valid operations on the major current loop, the maximum arcing time window is slightly less than the 45 ms case (less than 40 % of the loop duration).

Because the relative arc energy associated with the extended major loop is quite close to 100 %, it is reasonable to use the same equivalency criteria ("$I \times t$" product) for circuit-breakers tested three-phase and exhibiting short minimum arcing times (e.g. < 3 ms).

A.5.5 Validity of the equivalence method prescribed by IEC 62271-100

IEC 62271-100 recommends a simple and practical way for the evaluation of the arc energy of the last current loop prior to interruption. It suggests multiplying the loop amplitude by the loop duration to obtain a representative loop area ("$I \times t$" product) for comparison.

Table A.8 gives the results of the relative arc energy calculations for the different 60 Hz currents and d.c. time constants for interruption at the end of a major loop.

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Table A.8 – 60 Hz comparison between the integral method and the method prescribed by IEC 62271-100

Row	Current rating kA r.m.s. symmetrical	Time constant ms	Area of the last major loop by the exact integral method As	Peak of last major loop I kA peak	Last loop duration ms	$I \times t$ As	Ratio: area of major loop	Ratio: product $I \times t$	Difference to integral method %
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
1	63	45	805,8	124,5	10,55	1 314	1	1	–
2	50	60	718,2	106,1	11,15	1 183	0,891 3	0,900 3	1,01
3	50	75	777,8	111,3	11,60	1 291	0,965 3	0,982 5	1,78
4	50	120	890,5	120,7	12,55	1 515	1,105 1	1,153 0	4,33
5	40	120	712,4	96,6	12,55	1 212	0,884 1	0,922 4	4,33
The ratio area of column (8) is derived from column 4 divided by 805,8 and the ratio area of column (9) from division of column (7) by 1314.									

Similarly, Table A.9 gives the results of the relative arc energy calculation for the different 50 Hz currents and d.c. time constants for interruption at the end of a major loop.

Table A.9 – 50 Hz comparison between the integral method and the method prescribed by IEC 62271-100

Row	Current rating kA r.m.s. symmetrical	Time constant ms	Area of the last major loop by the exact integral method As	Peak of last major loop I kA peak	Last loop duration ms	$I \times t$ As	Ratio: area of major loop	Ratio: product $I \times t$	Difference to integral method %
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
1	63	45	893,2	118,5	12,15	1 440	1	1	
2	50	60	802,0	101,5	12,90	1 309	0,897 9	0,909 0	1,24
3	50	75	875,2	107,1	13,50	1 446	0,979 8	1,004 2	2,49
4	50	120	1 019,2	117,4	14,60	1 714	1,141 1	1,190 3	4,31
5	40	120	815,3	93,9	14,60	1 371	0,912 8	0,952 1	4,31
The ratio area of column (8) is derived from column 4 divided by 893,2 and the ratio area of column (9) from division of column (7) by 1 440.									

Particular points of Tables A.8 and A.9:

a) Row 1 is the reference case;

b) In rows 2 through 5 the IEC 62271-100 the "$I \times t$" method is compared to the exact integral method for determining the relative arc energy of the last major current loop prior to interruption;

c) Rows 2 through 5 show that the relative difference between the two methods remains below 5 %.

With a difference of less than 5 % for a d.c. time constant variation from 45 ms to 120 ms it is shown that the "$I \times t$" method as stated in IEC 62271-100 is fully adequate for adjustment of test circuit parameters as well as to extend test results for another current and d.c. time

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constant ratings. The integral method should be considered as the exact method to calculate the equivalent arc energy during the last current loop and also during the whole arcing period but cannot be implemented in all test laboratories because of the different capabilities of measuring system used. Therefore, the "$I \times t$" method was proposed to ease and speed up the result analysis after a test.

A.6 Discussion regarding equivalency

The method of analysis described for demonstrating the equivalency is not difficult to perform but access to the actual test results for the reference case is necessary. It must also be recognized that this investigation is only addressing a simultaneous three-phase fault case where one of the phases has always an offset ranging from 87 % to 100 % of the full d.c. offset depending on the point-on-wave initiation. It is the resulting current from that fully asymmetrical phase that has been compared. The fault currents that circulate in the other two phases will have significant reduced d.c. components and the ability of the circuit-breaker to interrupt these currents is not considered more difficult than those of all other test-duties defined by IEC 62271-100.

This investigation supports the recommendation that if d.c. time constants greater than 45 ms are encountered on a system, the selection of a circuit-breaker rated one or two steps up (depending on actual test parameters for the reference case) in the R10 series above the expected system fault current for d.c. time constants up to 120 ms should be satisfactory. While the number of cases investigated is limited the method can be applied to almost any combinations of three-phase fault currents and related d.c. time constants as a predictor of the maximum amount of energy involved.

Figure A.6 and Figure A.7 show selected plots for Case 1 and Case 2 of the currents with different d.c. time constants for both 60 Hz and 50 Hz respectively. An examination of the figures suggests that it is possible to use this method to evaluate different test combinations. For example one could use it to evaluate a test current at 50 Hz to show equivalence to a test current at 60 Hz. Since most such tests will be done using synthetic circuits the di/dt can be adjusted to the correct value at the time of interruption. By varying the amplitude of the current, the arc energy can be adjusted to be equivalent. For the manufacturer and/or user that knows the interrupting characteristics of a circuit-breaker, the outlined method is a useful tool for the evaluation of different interrupting capabilities under asymmetrical fault conditions.

IEC 62271-100 recognizes the problems associated with testing circuit-breakers with different d.c. time constants. It is fundamental that the circuit-breaker sees the correct prospective di/dt and at the time of interruption. As mentioned earlier, if synthetic test are conducted this can be adjusted to the correct value. If direct tests are used, the current level is adjusted to have the correct di/dt at the time of interruption. One fundamental consideration that must be accounted for is the d.c. time constant of the test station whether direct or synthetic test are used. The effective arc energy level under the last current loop can be adjusted by selecting the initiation instant of the short-circuit current (e.g. asymmetry level) or by adjusting the current level or a combination of both to obtain the correct last current loop parameters (amplitude and duration). Clause A.7 gives examples of waveshape adjustments during testing.

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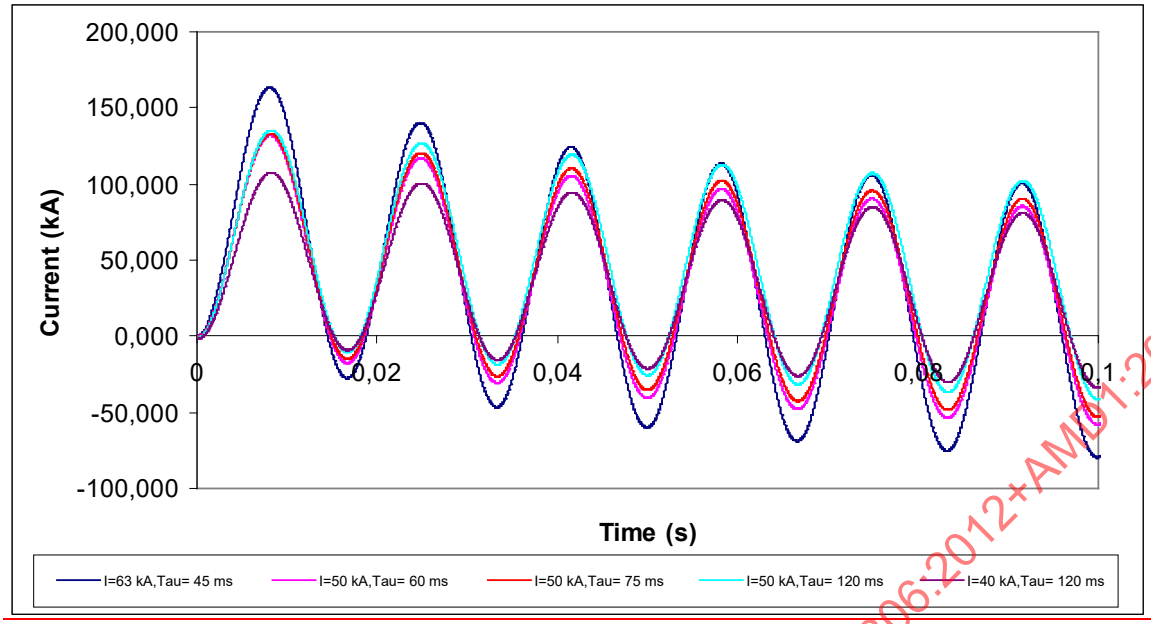

Figure A.6 – Plot of 60 Hz currents with indicated d.c. time constants

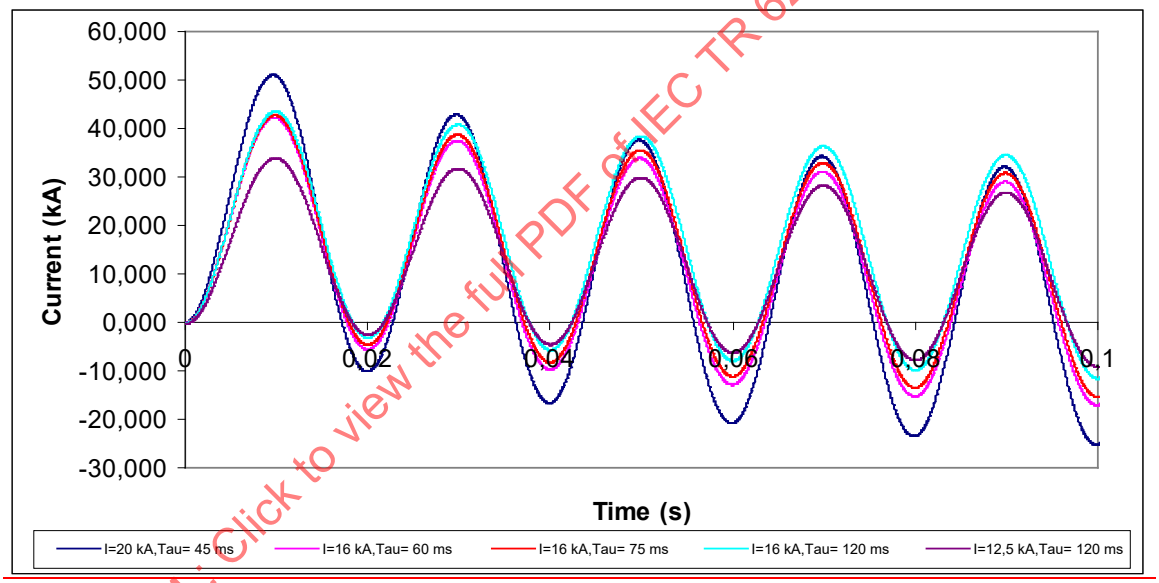

Figure A.7 – Plot of 50 Hz currents with indicated d.c. time constants

A.7 Current and TRV waveform adjustments during tests

A.7.1 General

The examples given in this clause are based on standardized cases and give guidelines how to use the asymmetry criteria defined in 6.106.6 of IEC 62271-100:2008 in an actual test. It is usual that the rated d.c. time constant of the circuit-breaker is different than the d.c. time constant of the test circuit and some adjustments on the test parameters are necessary. Three different cases are given covering the major cases that may occur in test laboratories.

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A.7.2 Three-phase testing of a circuit-breaker with a rated d.c. time constant of the rated short-circuit breaking current constant longer than the test circuit time constant

Rated voltage of the circuit-breaker:	24 kV
First-pole-to-clear factor:	1,5
Rated d.c. time constant of the rated short-circuit breaking current:	120 ms
Test circuit time constant:	60 ms
Minimum arcing time:	7,5 ms
Minimum opening time:	32,5 ms
DC component at contact separation:	70,2 %
Minimum clearing time:	40 ms
Frequency:	50 Hz

The time constant of the test circuit differs from the rated d.c. time constant of the rated short-circuit breaking current. The adjustment method chosen in order to reach the required data is the pre-tripping method together with controlled closing.

NOTE 1 Controlled closing means the initiation of the test current at a chosen instant on the applied voltage in order to vary the initial d.c. component of the test current.

Table A.10 – Example showing the test parameters obtained during a three-phase test when the d.c. time constant of the test circuit is shorter than the rated d.c. time constant of the rated short-circuit current

Parameters	Requirements (calculated values, rounded values are given in Table 18 of IEC 62271-100:2008)		Test data when using pre-tripping and controlled closing methods		Deviation between required values and test values %
	Major loop with first clearing pole	Second pole-to-clear major/minor loop [a]	Major loop with first clearing pole	Second pole-to-clear major/minor loop [a]	
D.C. component at current interruption (%)	62,1		54,2		-13
di/dt at current interruption (%)	80,1		86,9		+8
Peak of the last current loop (p.u.)	1,66	1,34/0,72	1,61	1,32/0,76	-3 -1,5/+5,6 [b]
Duration of the last current loop (ms)	14,5	13,2/7,65	14,4	13,05/7,8	-2 -1/+2 [b]
Δt (ms) [c]		3		3,3	+10
$\gamma \times t$ (p.u. ms)	24,07		23,18		-3,7

[a] Values calculated for a non-effectively earthed neutral system using a network calculation program (see NOTE 2).

[b] Second-pole-to-clear.

[c] Δt is the time interval between the first-pole-to-clear and the last-pole-to-clear.

Result: It is possible to fulfil the requirements by using the pre-tripping and controlled closing options. The TRV and di/dt values will be higher than required, but still within the given tolerances. The arcing time for the second clearing pole will be slightly longer than the required one. The test data cover the required values. Tighter tolerances may be achieved by

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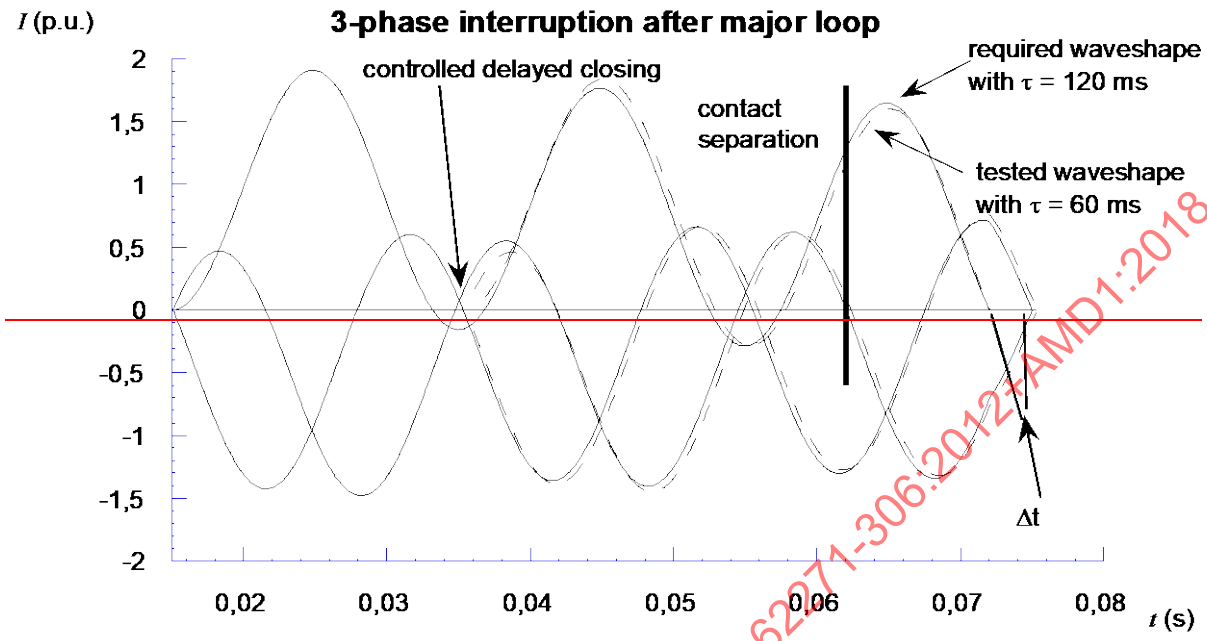
changing test current and/or the TRV amplitude factor. The results are illustrated in Figure A.8.



NOTE Due to the shorter time constant of the test circuit the short-circuit current is initiated later (pre-tripping method, see NOTE 1 of 6.106.6.3 of IEC 62271-100:2008) and to choose the closing angle in a way to achieve the required d.c. component at current zero (controlled closing).

Figure A.8 – Three-phase testing of a circuit-breaker with a rated d.c. time constant of the rated short-circuit breaking current longer than the test circuit time constant

As seen in Table A.10, the ratings of the circuit-breaker given in A.7.2 are fully covered by the test data. Attention should be paid to the fact that the percentage of asymmetry at current zero is lower than the rating given by the manufacturer at contact separation. This difference is normal because the value assigned by the manufacturer is based on the specified d.c. time constant of the rated short-circuit breaking current of 120 ms, it does not take into account the arcing time and the d.c. time constant of the test circuit. The test parameters to be fulfilled are those described for the last current loop as defined in 6.106.6 of IEC 62271-100:2008.

NOTE 2 The easiest way to calculate the required three phase or single phase waveshape characteristics is by a network calculation program such as EMTP, MATHLAB, etc. The waveshape characteristics can also be calculated by hand from the fundamental three phase or single phase short-circuit current equations.

A.7.3 Single phase testing of a circuit-breaker with a rated d.c. time constant of the rated short-circuit breaking current shorter than the test circuit time constant

Rated voltage of the circuit-breaker:	550 kV
First-pole-to-clear factor:	1,3
Rated d.c. time constant of the rated short-circuit breaking current:	45 ms
Test circuit time constant:	60 ms
Minimum arcing time:	7,5 ms
Minimum opening time	32,5 ms
DC component at contact separation	38,9 %
Minimum clearing time:	40 ms
Frequency:	50 Hz

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The time constant of the test circuit differs from the rated d.c. time constant of the rated short-circuit breaking current. The adjustment method chosen to reach the required data is the controlled closing method.

Table A.11 – Example showing the test parameters obtained during a single-phase test when the d.c. time constant of the test circuit is longer than the rated d.c. time constant of the rated short-circuit current

Parameters	Requirements (calculated values, rounded values are given in Table 15 of IEC 62271-100:2008)		Test data when using controlled closing method		Deviation between required values and test values %
	Major loop with longest possible arcing time	Minor loop with shortest possible arcing time	Major loop	Minor loop	
D.C. component at current interruption (%)	28,9	37,9	28,6	40,2	-1,0 +6,1 [b]
di/dt at current interruption [a] (%)	97,8	89,9	97,3	89,6	+0,5 -0,6 [b]
Peak of the last current loop (p.u.)	1,33	0,59	1,32	0,57	-0,8 -3,4 [b]
Duration of the last current loop (ms)	12,3	7,35	12,15	7,35	-1,2 0 [b]
u_1 [a]	96,5 %	91,9 %	96,0 %	91,3 %	-0,5 -0,7 [b]
u_c [a]	92,3 %	97,9 %	91,9 %	97,1 %	-0,4 -0,9 [b]
$I \times t$ (p.u. ms)	16,36	4,34	16,04	4,19	-2,0 -3,5 [b]
[a] In case of synthetic testing it is possible to control these values independent from the time constant. [b] Minor loop.					

Result: All test requirements can be fulfilled by using the controlled closing method. All values obtained are very close to the required values. Tighter tolerances may be achieved by changing the test current amplitude and/or the TRV amplitude factor of the TRV shaping circuit. The values for u_1 and u_c have been derived from the equations of Annex P of IEC 62271-100:2008. The results are illustrated in Figure A.9.

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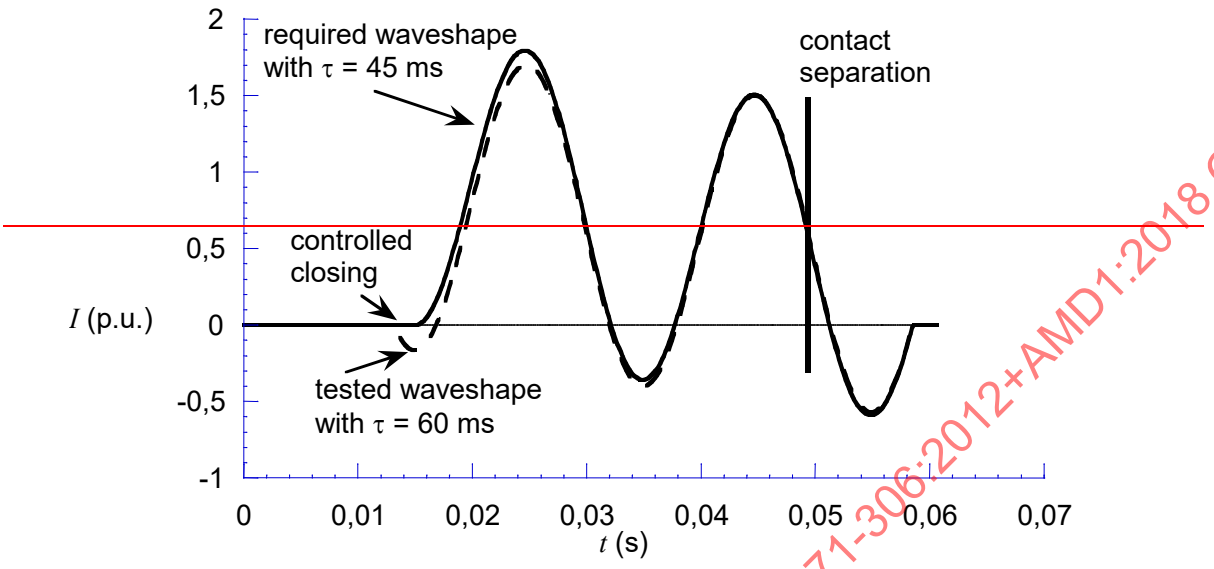

Figure A9a – Interruption in a current zero following a minor loop

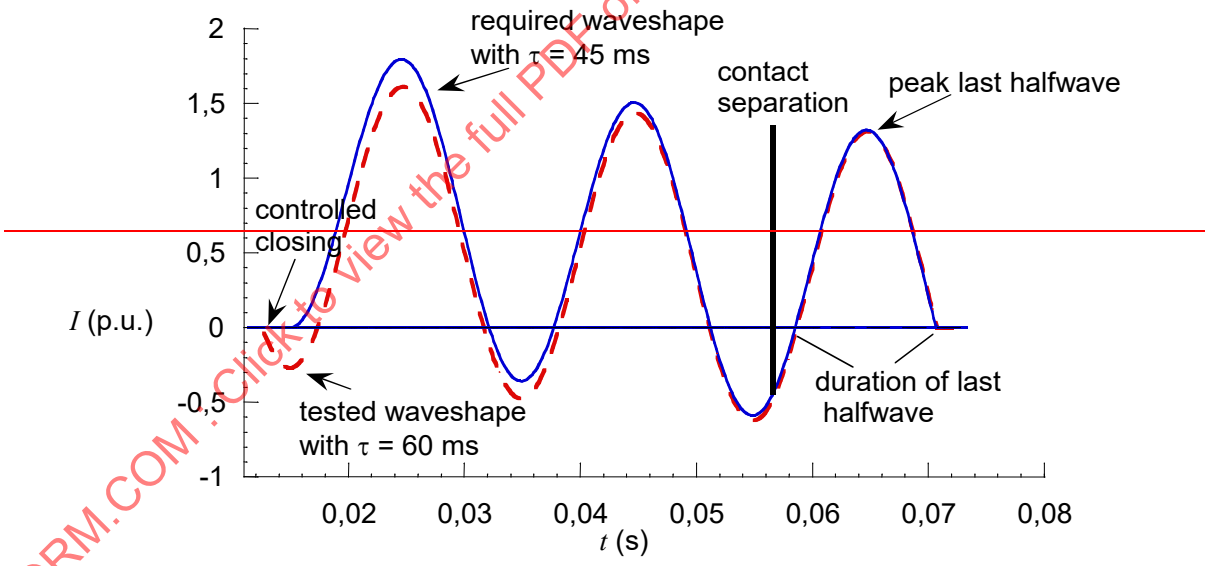

Figure A.9b – Interruption in a current zero following a major loop

Figure A.9 – Single phase testing of a circuit-breaker with a rated d.c. time constant of the rated short-circuit breaking current shorter than the test circuit time constant

As seen in Table A.11, the ratings of the circuit-breaker given in A.7.2 are fully covered by the test data. Attention should be paid to the fact that the percentage of asymmetry at current zero is lower than the rating given by the manufacturer at contact separation. This difference is normal because the value assigned by the manufacturer is based on the specified d.c. time constant of the rated short-circuit breaking current of 45 ms, it does not take into account the arcing time and the d.c. time constant of the test circuit. The test parameters to be fulfilled are those described for the last current loop as defined in 6.106.6 of IEC 62271-100:2008.

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A.7.4 Single-phase testing of a circuit-breaker with a rated d.c. time constant of the rated short-circuit breaking current longer than the test circuit time constant

Rated voltage of the circuit-breaker:	550 kV
First-pole-to-clear factor:	1,3
Rated d.c. time constant of the rated short-circuit breaking current:	75 ms
Test circuit time constant:	60 ms
Minimum arcing time:	7,5 ms
Minimum opening time	32,5 ms
DC component at contact separation	56,7 %
Minimum clearing time:	40 ms
Frequency:	50 Hz

The time constant of the test circuit differs from the rated d.c. time constant of the rated short-circuit breaking current. The adjustment method chosen in order to reach the required data was the controlled closing method.

Table A.12 – Example showing the test parameters obtained during a single-phase test when the d.c. time constant of the test circuit is shorter than the rated d.c. time constant of the rated short-circuit current

Parameters	Requirements (calculated values, rounded values are given in Table 16 of IEC 62271-100:2008)		Test data when using controlled closing method		Deviation between required values and test values %
	Major loop with longest possible arcing time	Minor loop with shortest possible arcing time	Major loop	minor loop	
D.c. component at current interruption (%)	47,2	56,4	39,2	48,6	-20 -16,6 [b]
di/dt at current interruption* (%)	90,2	80,2	94,1	84,9	+4,3 +5,8 [b]
Peak of the last current loop (p.u.)	1,51	0,41	1,44	0,44	-4,6 +7,3 [b]
Duration of the last current loop (ms)	13,65	6,15	13,5	6,75	1,1 +9,8 [b]
u_1 [a]	88,1 %	82,8 %	92,3 %	82,1 %	+4,8 +5,2 [b]
u_c [a]	81,3 %	90,9 %	86,6 %	94 %	+6,5 +3,4 [b]
$t_1 \times f$ (p.u. ms)	20,61	2,52	19,44	2,97	-5,7 +17,9 [b]

[a] In case of synthetic testing it is possible to control these values independent from the time constant.

[b] Minor loop.

Result: All test requirements can be fulfilled by using the controlled closing method. All values, except the d.c. component, are very close to the required values. In this case additional pre-tripping is necessary to achieve the allowed tolerances (-5 % +10 %). Tighter tolerances may be achieved by changing the test current amplitude and/or the TRV amplitude factor of the TRV shaping circuit. The values for u_1 and u_c have been derived from the equations of Annex P of IEC 62271-100:2008. The results are illustrated in Figure A.10.

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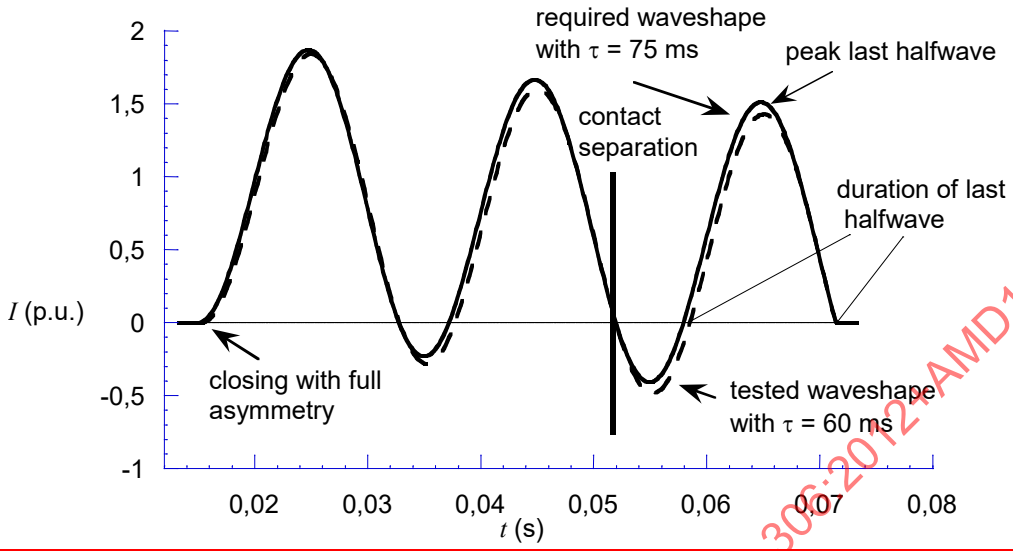

Figure A.10a – Interruption in a current zero following a major loop

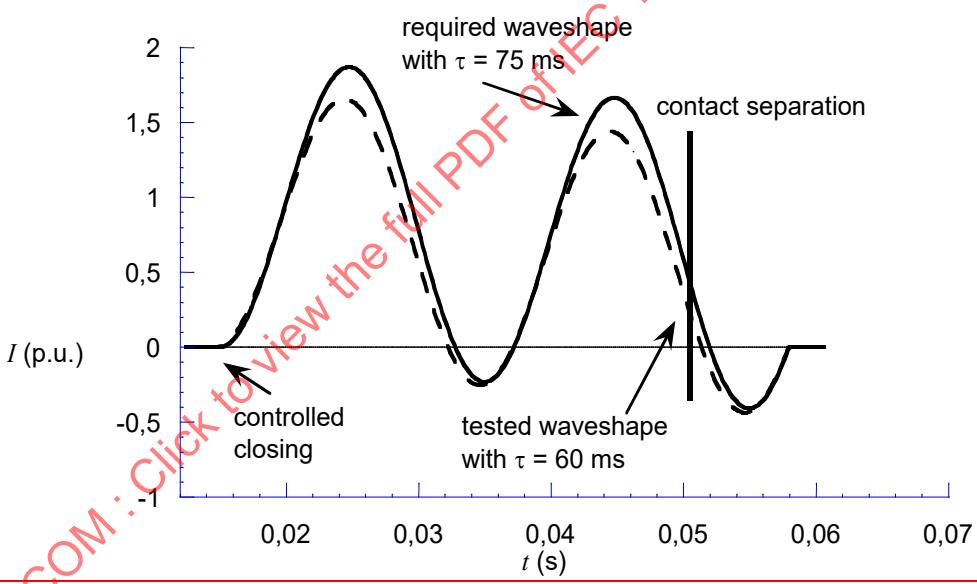

Figure A.10b – Interruption in a current zero following a minor loop

Figure A.10 – Single-phase testing of a circuit-breaker with a rated d.c. time constant of the rated short-circuit breaking current longer than the test circuit time constant

As seen in Table A.12, the ratings of the circuit-breaker given are fully covered by the test data. Attention should be paid to the fact that the percentage of asymmetry at current zero is lower than the rating given by the manufacturer at contact separation. This difference is normal because the value assigned by the manufacturer is based on the specified d.c. time constant of the rated short-circuit breaking current of 75 ms, it does not take into account the arcing time and the d.c. time constant of the test circuit. The test parameters to be fulfilled are those described for the last current loop as defined in 6.106.6 of IEC 62271-100:2008.

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~~**A.8 Conclusions**~~

~~a) Based on this work, a circuit-breaker applied at an interrupting current level one or two steps below the circuit-breaker rating in the R10 series may be satisfactory for d.c. time constants above the standard test value of 45 ms;~~

~~b) This evaluation showed, for the limited cases studied, that the one step reduction in the R10 series may cover applications up through a d.c. time constant of 120 ms depending on the last current loop parameters obtained during tests for the reference ratings of the circuit-breaker;~~

~~c) The "$I \times t$" product method defined in IEC 62271-100 can be used to evaluate equivalence of tests done at 50 Hz or 60 Hz at one d.c. time constant to cover applications at 50 Hz or 60 Hz with different d.c. time constants;~~

~~d) The "$I \times t$" method defined in IEC 62271-100 is the only method that can be used to check tolerance last current loop parameters during test-duty T100a;~~

~~e) The application engineer needs to determine the actual expected fault current including its d.c. time constant at the system point of interest to determine the required circuit-breaker rating.~~

A.1 General

A time constant of 45 ms is generally adequate on systems rated 800 kV and below. For 1 100 kV and 1 200 kV systems, the standardized DC time constant has been defined as 120 ms mainly because the use of multi-conductor bundles on transmission lines. Alternative special case DC time constants, related to the rated voltage of the circuit-breaker, should cover cases where the standard DC time constant 45 ms is not sufficient. This may apply, for example, to systems with very high rated voltage (for example 800 kV systems having higher DC time constant for lines e.g. when multi-conductor bundles are used), to some medium voltage systems with radial structure or to any systems with particular system structure or line characteristics. Alternative special case DC time constants have been defined in 4.101.2 of IEC 62271-100:2008/AMD2:2017 of taking into account the results of the survey by CIGRE WG13.04 [139].

The choice of a single special case value of the DC time constant minimises the number of tests required to demonstrate the capability of the equipment.

For example, a test carried out on a circuit-breaker at 63 kA with a DC time constant of 45 ms does not automatically cover the performance of a circuit-breaker having a rating of 50 kA with a DC time constant of 75 ms, actual test parameters should be known in order to determine if the equivalency can be made.

Some general important aspects need to be considered. In order to state the equivalency of a certain circuit-breaker for another fault current rating and DC time constant, the following parameters have to be examined carefully in relation to the interrupting technology used:

a) amplitude of the last current loop before interruption;

b) duration of the last current loop before interruption;

c) arcing time window;

d) arc energy;

e) di/dt at current interruption;

f) TRV peak voltage u_c and first reference voltage u_1, as applicable.

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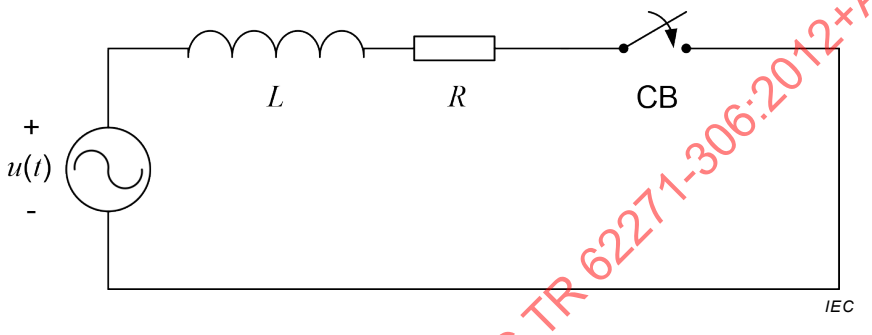
A.2 Basic theory

One of the duties that a circuit-breaker has to perform is to interrupt all short-circuit currents up to its rated short-circuit current. The short-circuit current may be symmetrical, partly asymmetrical or fully asymmetrical depending on the instant where the fault was initiated.

Asymmetrical currents occur in all type of inductive circuits and the level of asymmetry depends on the instant of fault initiation and the DC time constant (τ) of the circuit under evaluation.

NOTE The DC time constant of a circuit is sometimes expressed as the X/R ratio of a circuit, where $X = 2\pi f \times L$, where f is the power frequency in Hz and R represent the losses (Ω) in the circuit.

The simplified single-phase circuit shown in Figure A.1 illustrates the studied case.



Key

$u(t)$	Source voltage, $u(t) = U\sin(\omega t + \alpha)$	R	Losses in the circuit
L	Source inductance	CB	Circuit-breaker

Figure A.1 – Simplified single-phase circuit

In case of power systems ωL is generally $>> R$.

By using differential equations, the resulting current is:

$$I(t) = \frac{U}{Z} \times \left[\sin(\omega t + \alpha - \varphi) - e^{-t/\tau} \times \sin(\alpha - \varphi) \right] \quad \text{(A.1)}$$

where

U is the peak of the applied voltage $u(t)$;

Z is the circuit impedance: $Z = \sqrt{R^2 + \omega^2 L^2}$;

ω is the angular frequency: $2\pi f$;

α is the fault making angle (instant) on the applied sinusoidal voltage;

φ is the phase angle of the circuit impedance $\varphi = \tan^{-1}\left(\frac{\omega L}{R}\right) = \tan^{-1}\left(\frac{X}{R}\right)$;

τ is the DC time constant (L/R) of the circuit.

The resulting fault current has two components, the first part of the equation being the sinusoidal part and the second being the exponential decaying DC component.

From Equation (A.1), the DC component will be maximum when $\sin(\alpha - \phi) = 1$ or $\alpha - \phi = \pi/2$.

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$$I(t)_{\text{max}} = I\left[\sin\left(\omega t + \pi/2\right) - e^{-t/\tau}\right] \quad \text{(A.2)}$$

The peak value of the current will occur when $\sin(\omega t + \pi/2) = -1$ or $\omega t = \pi$ giving

$$I_{\text{pk}} = -I\left(1 + e^{-t/\tau}\right) \quad \text{(A.3)}$$

where $t = \pi/\omega$.

The maximum asymmetrical peak current is always obtained when the circuit-breaker is closed at 0° of the applied voltage (α= 0), which is not necessarily giving the maximum DC component. Equations (A.2) and (A.3) are approximate since the peak of the asymmetrical current does not occur exactly after π radians. However, the equations are accurate to at least two decimal places if the phase angle between the current peak and the zero of the applied voltage is less than 4° and therefore is suitable for the purpose.

Equations (A.2) and (A.3) are for the negative DC component case and, to obtain the positive DC component case, multiply the right side by –1. $I = U/Z$ and further equal to $\sqrt{2}$ times the symmetrical r.m.s. interrupting current rating of the circuit-breaker under consideration. The maximum peak current occurs when the circuit is made at a voltage zero crossing.

For the standardized DC time constants (45 ms and 120 ms) and the alternative special case DC time constants given in IEC 62271-100 (60 ms, 75 ms and 120 ms), the DC components in p.u. of the peak symmetrical current are shown in Figure A.2.

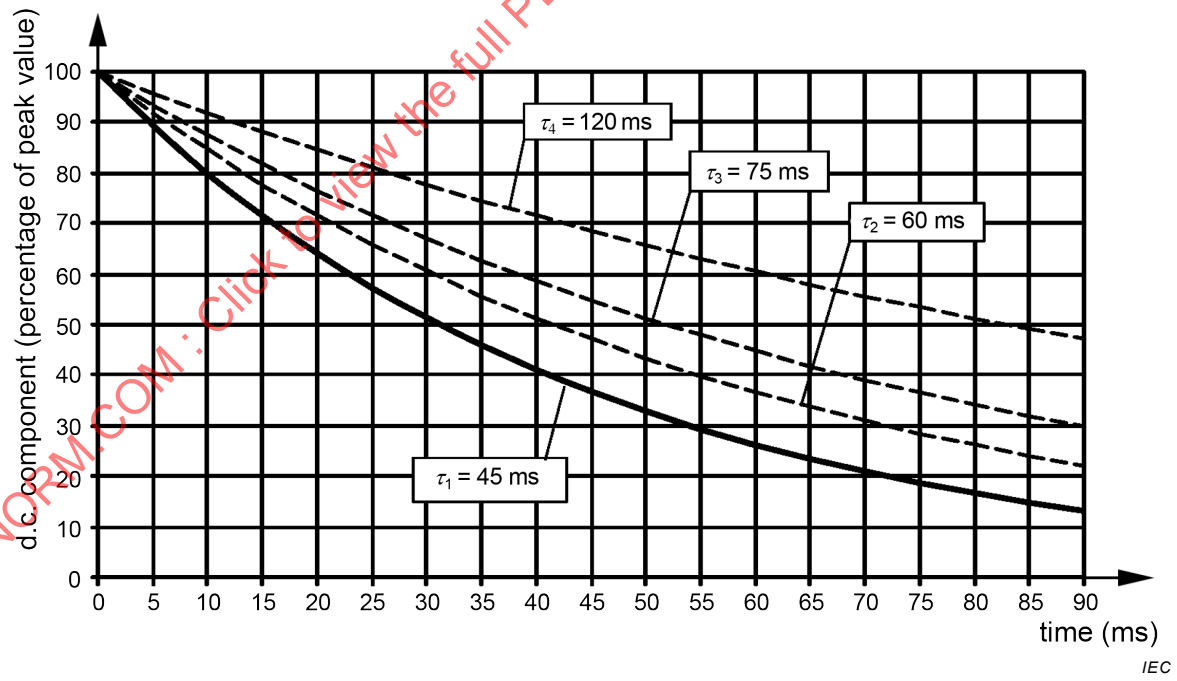

Figure A.2 – Percentage DC component in relation to the time interval from the initiation of the short-circuit for the standard time constants and for the alternative special case time constants (from IEC 62271-100)

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Asymmetrical current related values of X/R and I_{peak} are power frequency dependent as summarized in Tables A.1 and A.2. The I_{peak} values in brackets are the recommended values used for standardization purposes in IEC 62271-100.

Table A.1 – X/R values

$\tau = L/R$	50 Hz		60 Hz	
ms	X/R	$\tan^{-1} X/R$	X/R	$\tan^{-1} X/R$
45	14	85,9	17	86,6
60	19	86,9	22,6	87,4
75	23,5	87,5	28,3	87,9
120	37,7	88,5	45,2	88,7

Table A.2 – I_{peak} values

$\tau = L/R$	I_{peak} (p.u.)	
ms	50 Hz	60 Hz
45	2,55 (2,5)	2,59 (2,6)
60	2,61 (2,7)	2,65 (2,7)
75	2,65 (2,7)	2,68 (2,7)
120	2,72 (2,7)	2,73 (2,7)

For a three-phase fault initiated simultaneously in the three phases, the DC component of the fault current at fault initiation of the most asymmetrical phase is always ranging from 87 % to 100 % whatever instant the fault is initiated on the applied voltage. This DC component range leads to an asymmetrical current peak ranging from 93,5 % to 100 % whatever instant the fault is initiated on the applied voltage.

The current equations for a three-phase fault initiated simultaneously on the three phases are:

$$I_{\varphi A}(t) = \frac{U}{Z} \times \left[\sin(\omega t + \alpha - \varphi) - e^{-t/\tau} \times \sin(\alpha - \varphi) \right] \quad \text{(A.4)}$$

$$I_{\varphi B}(t) = \frac{U}{Z} \times \left[\sin\left(\omega t + \alpha - \varphi - 2\pi/3\right) - e^{-t/\tau} \times \sin(\alpha - \varphi - 2\pi/3) \right] \quad \text{(A.5)}$$

$$I_{\varphi C}(t) = \frac{U}{Z} \times \left[\sin\left(\omega t + \alpha - \varphi + 2\pi/3\right) - e^{-t/\tau} \times \sin(\alpha - \varphi + 2\pi/3) \right] \quad \text{(A.6)}$$

In the first edition of IEC 62271-100 (and earlier editions of IEC 60056), the concept of DC component of the rated short-circuit current was used together with the asymmetry level at contact separation. At that time, a single unified standardized DC time constant of 45 ms was specified. With the introduction of new alternative special cases DC time constants, the concept of defining asymmetry level at contact separation has been changed to the concept of last current loop parameters since this is the important aspect to consider for arc energy and di/dt prior to interruption. This concept also allows performing tests on a circuit-breaker with a test circuit having a different time constant than the rated one and does also permit to validate more than one rating from the results obtained from a single T100a test series.

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The considerations given in this subclause are based on the assigned ratings of the circuit-breaker and on the actual test parameters measured during the T100a test-duty.

The purpose of this subclause is to give guidance on how to use test results for validating other ratings with other DC time constants from a single test series results and to give guidance on how to modify the test parameters in order to obtain the required last current loop parameters. However, in doing this, the scope of this subclause is limited since the amplitude, duration and the di/dt at current zero all change as the DC time constant changes. A higher asymmetry results in a lower du/dt and peak value of the TRV, reducing the stress during the recovery process. This fact has been disregarded in the subclause dealing with equivalency and therefore the results can be considered conservative when the results obtained from a test series validating a lower DC time constant are used to validate an higher DC time constant rating. On the contrary, care should be exercised on the TRV parameters when the results obtained from a test series validating an higher DC time constant are used to validate a lower DC time constant rating. Annex I of IEC 62271-101:2012/AMD1:2017 gives the methodology for calculating TRV parameters during asymmetrical fault condition.

IEC 62271-100:2008/AMD1:2012 of introduces tolerances for testing purposes during the last current loop of arcing interval prior to interruption. A ±10 % tolerance is specified on both last current loop amplitude and duration. Then, the resulting product "$I \times t$", "I" being the peak value of the last current loop and "t" being the duration of the last current loop, will range between 81 % and 121 % of the required values.

The application of generator circuit-breakers breaking currents with delayed current zeros is beyond the scope of this document; this specific case is covered in IEC 62271-37-013 [145].

A.3 Network reduction

The rate of decay of the DC component is usually expressed as the DC time constant of the short-circuit current.

It should be noted that the DC time constant of the short-circuit current at the point of the fault is not the simple ratio of L/R typically obtained by network reduction short-circuit programs because each component of the network has its own DC time constant. Experience has shown that using the R and L values obtained by the typical network reduction short-circuit program will give the correct short-circuit current. However, the DC time constant based on the ratio of these values will generally be less than the correct value.

Transient calculation programs need to be used in order to obtain the correct DC time constant of a particular network location.

A.4 Special case time constants

With the publication of the first edition of IEC 62271-100 the concept of a circuit-breaker being able to deal with DC time constants other than the standard time constant of 45 ms was introduced for the first time. IEC 62271-100:2008 specifies additional "special cases time constants" of 60 ms, 75 ms and 120 ms in 4.101.2. In 4.101.2 b) of IEC 62271-100:2008/AMD1:2012 and IEC 62271-100:2008/AMD2:2017, the following insight is provided:

– 120 ms for rated voltages up to and including 52 kV;
– 60 ms for rated voltages from 72,5 kV up to and including 420 kV;
– 75 ms for rated voltages 550 kV and 800 kV.

Moreover, IEC 62271-100:2008/AMD1:2012 introduces a second standardized DC time constant of the rated short-circuit current of 120 ms for circuit-breakers rated above 800 kV.

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For application of circuit-breakers on power systems, IEC 62271-100 calls attention to the fact that not all applications fall within the confines of existing standards. The introduction of a special DC time constant value is a logical extension for the following reasons:

– the lower voltage circuit-breakers will frequently be applied close to generation or step down transformers or current limiting reactors which exposes the circuit-breakers in such locations to the much longer DC time constants;
– at the higher system voltages, bundled conductors may be used on transmission lines and the circuit-breaker again may be close to transformers. The bundled conductors and the transformer reactance will contribute to the higher DC time constant.

For the circuit-breaker application engineer, this raises the question of how to evaluate the individual applications. This annex tries to provide some guidance.

A.5 Guidance for selecting a circuit-breaker

A.5.1 General

To evaluate the effect of different DC time constants, some general observations can be made. For cases in which the actual short-circuit current is less but the DC time constant is greater, the di/dt of the current at current zero and the amplitude of current loops will be less than the rated values. The arc energy represented by the area under the major and the major extended current loop is probably one of the most important considerations. The amplitude and duration of the major and the major extended current loops are directly related to the DC time constant of the short-circuit current.

In an effort to evaluate the effect of different DC time constants, the standardized DC time constants of 45 ms and 120 ms, and special case DC time constants of 60 ms, 75 ms, 90 ms and 120 ms were examined.

IEC 62271-100:2008/AMD2:2017 introduces major changes for demonstration of arcing times during test-duty T100a. Both three-phase tests and single-phase tests in substitution of three-phase tests have been harmonized and are based on a three-phase fault condition. Tests on the minor current loop during single-phase test are not anymore required. Minimum clearing time ranges have been re-calculated based on the minimum clearing time (including relay time) and the zero crossings on the intermediate asymmetrical phase for which the minimum arcing time is defined. For practical reasons and because the DC component of the intermediate asymmetrical phase is relatively low, the minimum arcing time on the intermediate asymmetrical phase is considered to be the same as obtained during T100s and does not need to be re-demonstrated during T100a. It is acknowledged that for some circuit-breaker technologies the minimum arcing time obtained during T100s will be different that the one that would be obtained on the intermediate asymmetrical phase during T100a. For such cases, the required arcing times may not be obtained and additional tests up to a maximum of 6 tests are specified in order to demonstrate the required maximum arcing times.

IEC 62271-100 specifies criteria on the last current loop amplitude and duration. The important parameter to be considered is the arc energy from contact separation to interruption and the last current loop is of prime importance because generally most of the arc energy is within that last current loop, at least for modern circuit-breakers. The exact result would have been to compare the integral of the current waveshape from contact separation to current zero, but this type of calculation is not practical in test laboratories. Not all test laboratories have proper digital data acquisition systems or sufficient calculation tools to perform such calculation. Instead IEC 62271-100 asks to compare the parameters of the last current loop (I_{peak} and loop duration). Such measurements are easy to perform and can be done in all test laboratories without any specific constraints.

The methodology to evaluate the effect of different time constants is as follows:

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a) Determine the last current loop parameters (amplitude and duration) obtained during T100a test series (last loops (major if tested single phase) or major and extended major current loop amplitudes and durations if tested three-phase.

b) Use Equations (A.4), (A.5) and (A.6) to find the current waveshapes of the specific case to be studied. Use an "α" of 0 rad. in order to obtain the full asymmetrical offset on one phase and resultant intermediate asymmetries on the two other phases.

c) Determine where the interruption will take place. The time sequence events in the operation of a circuit-breaker that always precede the actual interruption and tend to establish the most likely time for interruption are:

   – relay time;

   – circuit-breaker minimum opening time;

   – minimum arcing time on the minor current loop of the intermediate asymmetrical phase starting with a minor current loop (as mentioned earlier, the minimum arcing time on the minor current loop of the intermediate asymmetrical phase is considered to be equal to the one found during T100s);

   – The sum of the above times is defined in IEC 62271-100:2008/AMD2:2017 as the minimum clearing time. The major current loop of the full asymmetrical phase at a time after current initiation corresponding the end of the minimum clearing time range defined in Table 41 of IEC 62271-100:2008/AMD2:2017 for which the calculated minimum clearing time falls in is the current loop parameters for which the circuit-breaker should be able to interrupt.

Table 39 of IEC 62271-100:2008/AMD2:2017 has tabulated the last loop current parameters for standardized and alternative special cases DC time constants for both 50 Hz and 60 Hz systems.

Some assumptions have been taken:

a) The tolerance of ±10 % defined for both current amplitude and current loop duration is resulting in an allowable arc energy range during the arcing period. The arc voltage is assumed to be constant during the period of arcing. This allows the arc energy of the last current loop to be represented by the "$I \times t$" product;

   A smaller symmetrical fault current with a longer DC time constant (compared with the rated short-circuit-current and the standard time constant) has a larger percentage of DC component and the resultant di/dt is always less than the one associated with the highest rated short-circuit current. In such a case, the circuit-breaker should still be able interrupt at the normal current zero if it has met all other criteria;

b) If the arc energy represented by the "$I \times t$" product is less than 121 % of the standard wave, the interruption will be generally successful;

c) If the arc energy represented by the "$I \times t$" product is greater than 121 % of that of the standard interruption, the interruption could be unsuccessful.

Some circuit-breaker technologies use the arc energy as the main source of energy for current interruption. For such technologies, a lower arc energy may result in longer arcing times and the ability of interrupting lower current should be carefully evaluated. Care should be exercised in the evaluation of the minimum arcing time. The arc energy associated with minor current loops are lower for higher DC time constants that may result in a longer minimum arcing time and thus in a longer maximum arcing time.

The determination of the area X under the current curve may be obtained by solving Equation (A.7). This equation is the exact calculation method.

$$X = \int_{t_1}^{t_2} i(t)\mathrm{d}t \qquad \text{(A.7)}$$

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where

$i(t)$ is the fully asymmetrical current $I_{\varphi A}(t)$ as given in Equation (A.4) for a making angle α = 0 rad;

t_1 is the time of contact separation;

t_2 is the time of current zero where interruption could occur.

As said before, this method cannot be easily used in test laboratories because it necessitates digital data acquisition systems with proper software, which are not always available. Instead, the comparison of the last current loop arcing energy by using the current loop parameters "$I \times t$" is a quite reasonable approximation (within 5 %) of the last current loop integral (see A.5.5).

The general guidance is to de-rate a circuit-breaker one class or approximately 80 % to deal with greater DC time constants. The question that should be answered is whether this is sufficient. For test purposes, IEC 62271-100 gives the following asymmetry criteria to be fulfilled when performing T100a:

– last current loop amplitude;

– last current loop duration;

Using the above methodology, the following cases were examined.

A.5.2 Case 1

Assumptions: Circuit-breaker ratings: I: 63 kA, τ = 45 ms and f = 60 Hz.

– relay time: 8,33 ms;

– minimum opening time: 17 ms;

– minimum arcing time (interruption on the minor loop of the intermediate asymmetrical phase starting with a minor loop): 8 ms;

– specific tests parameters recorded during T100a test-duty were exactly those associated with the rated values.

Table A.3 shows a comparison of the last major loop parameters for case 1 and for the first-pole-to-clear.

Table A.3 – Comparison of last major current loop parameters for the first-pole-to-clear, case 1

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	63	45	124,7	10,5	1 309
2	50	60	106,1/85,1	11,1/105,7	1 177/89,9
3	50	75	111,0/89,0	11,6/110,5	1 288/98,4
4	50	120	120,9/97,0	12,5/119,0	1 511/115,5

Particular points of Table A.3:

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It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (63 kA and τ = 45 ms) had last current loop parameters equal to 100 % of the rated values as shown in the last three columns of row 1.

a) Row 1 provides the reference values for a 63 kA rating with τ = 45 ms as obtained during test duty T100a;

b) The 2nd row shows the requirements for a 50 kA rating with τ = 60 ms. The current amplitude is less than 90 % of the test current obtained at 63 kA. The current loop duration is within the tolerance given. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

c) In row 3, the rating is still 50 kA but the time constant has been increased to 75 ms. As for the second row, the current amplitude is slightly less than 90 % of the test current obtained at 63 kA. The current loop duration is within the tolerance given. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

d) In row 4, the rating is still 50 kA but the time constant has been further increased to 120 ms. Both current amplitude and current loop duration are with the tolerances prescribed by IEC 62271-100. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application.

The equivalence shown before should be carefully studied with the actual waveshape of the last current loop parameters used during tests for the demonstration of the reference rating (63 kA and τ = 45 ms). In accordance with IEC 62271-100 and IEC 62271-101 (in the case of synthetic testing), it is permissible to have the amplitude and the duration of the last current loop reduced by 10 % from the rated values. In such a case, the last current loop parameters for the first-pole-to-clear as shown in Table A.4 are obtained.

Table A.4 – Comparison of last major current loop parameters for the first-pole-to-clear, case 1: test parameters used for the reference case set at the minimum permissible values

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values and minimum tolerances	63	45	112,2 [a]	9,5 [b]	1 066
2	50	60	106,1/94,6	11,1/116,8	1 178/110,5
3	50	75	111,0/98,9	11,6/122,1	1 288/120,8
4	50	120	120,9/107,8	12,5/131,6	1 511/141,8
5	40	120	96,7/86,2	12,5/131,6	1 209/113,4

[a] Last current loop amplitude equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

[b] Last current loop duration equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

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Particular points of Table A.4:

It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (63 kA and τ = 45 ms) had a last current loop parameters equal to 90 % of the rated values.

a) Row 1 provides the minimum permissible (90 %) reference values for a 63 kA rating with τ = 45 ms;

b) The 2nd row shows the requirements for a 50 kA rating with τ = 60 ms. The current amplitude is within the tolerance given. The current loop duration is more than 110 % of the current loop duration obtained at 63 kA. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

c) The 3rd row shows the equivalence for a 50 kA rating with τ = 75 ms. The current amplitude is within the tolerance given. The current loop duration is more than 110 % of the current loop duration obtained at 63 kA. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

d) As for the case shown in row 4, the rating is still 50 kA but the time constant has been increased to 120 ms. The current amplitude is still within the tolerance given. The current loop duration is significantly higher than 110 % of the current loop duration obtained at 63 kA. The product "$I \times t$" calculated from the last current loop parameters exceeds the resulting tolerance derived from the criteria defined in IEC 62271-100, thus the interrupting capability cannot be assessed by the test done at 63 kA;

e) The last row shows the requirements for a 40 kA rating with τ = 120 ms. The current amplitude is lower than 90 % of the current obtained during the test at 63 kA. The current loop duration is more than 110 % of the current loop duration obtained at 63 kA. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application.

From the above examples, it can be shown that the actual test parameters obtained during tests are of major importance to determine to which extent the reference test can be used to demonstrate the circuit-breaker ability to interrupt other fault currents with different DC time constants. From these examples, it has been shown that the one or two de-rating steps from the R10 series may be needed to cover lower short-circuit currents with higher DC time constants.

Finally, the comparison with the last major current loop parameters may be not enough to state if a particular circuit-breaker may be used for lower rated short-circuit current and higher DC time constant values. Some circuit-breaker technologies use the arc energy as the main source of energy for current interruption. Careful evaluation of the minimum arcing time needs to be done. Comparison of minimum arcing times obtained during T10, T30, T60 and T100s can be used as a tool to evaluate the increase of the minimum arcing time due to the reduced arc energy. If the minimum arcing times found during T10, T30 and T60 are not greater by more than a ¼ cycle from that measured in T100s, then it can be considered that a similar minimum arcing time on the minor loop than the reference case would be obtained. If this is the case, comparison of the last major current loop parameters to access circuit-breaker capabilities is sufficient. If not, additional tests may need to be performed to ensure that the minimum arcing time will not be significantly longer than the reference case.

A.5.3 Case 2

Assumptions: Circuit-breaker ratings: I = 20 kA, τ = 45 ms and f = 50 Hz.

– Relay time: 10 ms;

– Minimum opening time: 22 ms;

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– Minimum arcing time (interruption after on the minor loop of the intermediate asymmetrical phase starting with a minor loop): 8 ms.

A comparison of the last loop parameters for the first-pole-to-clear is shown in Table A.5.

Table A.5 – Comparison of last major current loop parameters of the first-pole-to-clear, case 2

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values	20	45	37,6	12,2	458,7
2	16	60	32,6/86,7	12,9/105,7	420,5/91,7
3	16	75	34,2/90,9	13,4/109,8	458,3/99,9
4	16	120	37,6/100	14,6/119,7	549,0/119,8
5	12,5	120	29,3/78,0	14,6/119,7	427,8/93,2

Particular points of Table A.5:

As mentioned in Table A.1, it should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (20 kA and τ = 45 ms) had a last current loop parameters equal to 100 % of the rated values as shown in the last three columns of row 1 of Table A.5.

a) Row 1 contains the reference values for 50 Hz, 20 kA rating;

b) In rows 2 to 5, it can be seen that a reduction of one step in the R 10 series will cover all cases for τ = 60 ms, 75 ms, 90 ms and 120 ms. For all these cases, the product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application.

As also mentioned for case 1, the applicability of a reference case to other fault currents and different DC time constants depends on the actual test parameters measured for the reference case. As an extreme case, if we consider that the last major current loop parameters during the reference test were at the minimum tolerance stated by IEC 62271-100 and IEC 62271-101, then the current loop parameters for the first-pole-to-clear of Table A.6 are obtained.

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Table A.6 – Comparison of last major current loop parameters for the first-pole-to-clear, case 2: test parameters used for the reference case set at the minimum permissible values

Row	Symmetrical current rating kA r.m.s.	Time constant ms	Amplitude of the last major current loop kA_{peak}/% of the reference case	Duration of the last major current loop ms/% of the reference case	Product "$I \times t$" As/% of the reference case
1 Reference case associated with test values equal to the rated values and minimum tolerances	20	45	33,8 [a]	11,0 [b]	371,8
2	16	60	32,6/96,2	12,9/117,3	420,5/113,1
3	16	75	34,2/100,9	13,4/121,8	458,3/123,3
4	16	120	37,6/110,9	14,6/132,7	549,0/147,6
5	12,5	120	29,3/86,4	14,6/132,7	427,8/115,1

[a] Last current loop amplitude equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

[b] Last current loop duration equal to 90 % of the rated value as permitted by IEC 62271-100 and IEC 62271-101.

Particular points of Table A.6:

It should be noted that the conclusions given below are only valid if the test performed to validate the reference rating (20 kA and τ = 45 ms) had a last current loop parameters equal to 90 % of the rated values.

a) Row 1 provides the minimum permissible (90 %) reference values for a 20 kA rating with τ = 45 ms;

b) The 2nd row shows the requirements for a 16 kA rating with τ = 60 ms. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application;

c) The 3rd and the 4th rows show the equivalence for a 16 kA rating with τ = 75 ms and 120 ms. For these cases, the "$I \times t$" products calculated from the last current loop parameters exceed the resulting tolerance derived from the criteria defined in IEC 62271-100, and the reference rating does not demonstrate the performance of the circuit-breaker for these specific cases;

d) The last row shows the requirements for a 12,5 kA rating with τ = 120 ms. The product "$I \times t$" calculated from the last current loop parameters is in accordance with the resulting tolerance derived from the criteria defined in IEC 62271-100, thus assuring a satisfactory application.

From the above examples, it can be shown, as for case 1, that the actual test parameters obtained during tests are again of crucial importance to determine to which extent the reference test can be used to demonstrate the circuit-breaker ability to interrupt other fault currents with different DC time constants. From these examples, it has been shown that the one or two de-rating steps from the R10 series may be needed to cover lower short-circuit currents with higher DC time constants.

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A.5.4 Case 3

The examples given in A.5.2 and A.5.3 were based on single-phase tests or for the first-pole-to-clear loop parameters during three-phase tests. For three-phase tests on medium voltage circuit-breakers, very short minimum arcing times may be observed in particular for vacuum circuit-breakers. As an extreme example, Figure A.3 shows the resulting current curves for a circuit-breaker having a minimum arcing time of 1 ms.

For the first valid operation, the interruption occurs on phase A for which the asymmetry criteria is met.

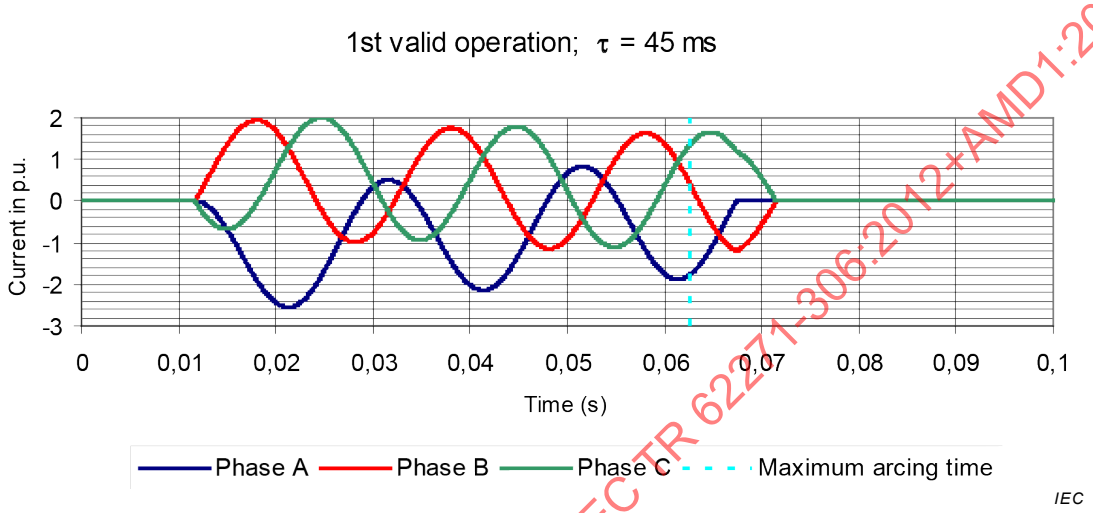

Figure A.3 – First valid operation in case of three-phase test (τ = 45 ms) on a circuit-breaker exhibiting a very short minimum arcing time

This example shows that the maximum possible arcing time on the asymmetrical phase is less than half of the major loop duration. The actual arcing time represents only 40 % of the major loop duration.

For the second test, the procedure given in IEC 62271-100 has been followed and the current oscillogram shown in Figure A.4 is obtained.

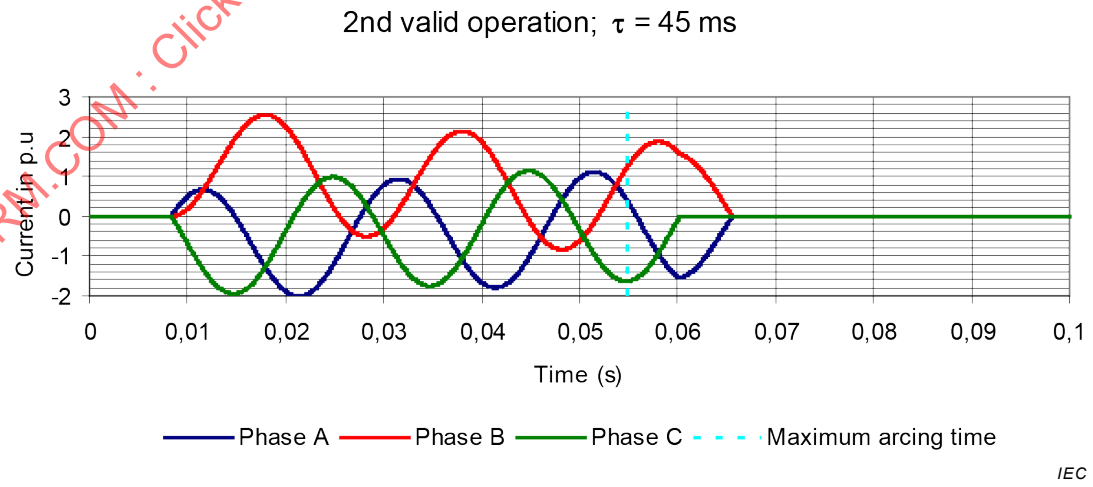

Figure A.4 – Second valid operation in case of three-phase test on a circuit-breaker exhibiting a very short minimum arcing time

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The interruption occurs on phase B on an extended major current loop. This example shows that the maximum possible arcing time on the extended major loop is slightly less than the extended major loop duration. The actual arcing time represents 86 % of the extended major loop duration.

Finally, for the third valid operation, the curves of Figure A.5 are obtained:

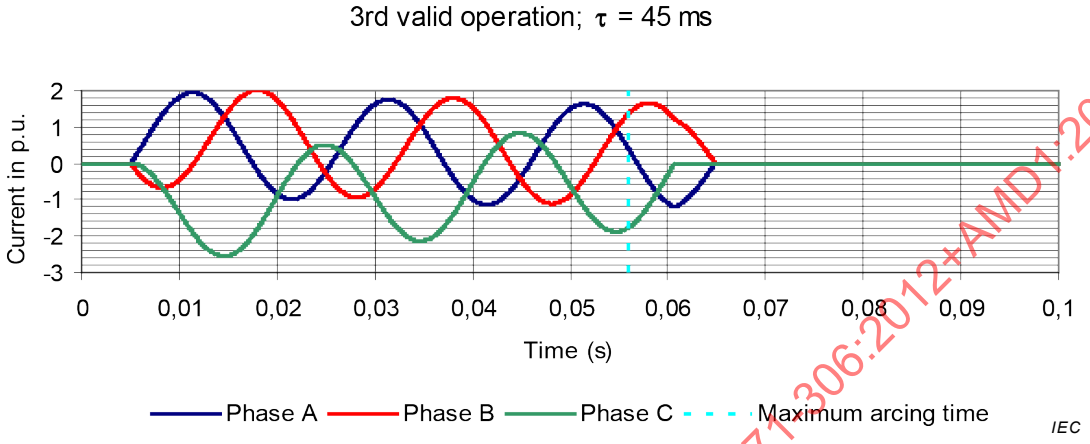

Figure A.5 – Third valid operation in case of three-phase test on a circuit-breaker exhibiting a very short minimum arcing time

The interruption occurs on phase C on a major current loop. Here also, as the first valid operation, the maximum possible arcing time on the asymmetrical phase is less than half of the major loop duration. The actual arcing time represents 46 % of the major loop duration.

The fact that this type of circuit-breaker exhibiting very short minimum arcing time does not see the full major and extended major loop, this raises the question if the "$I \times t$" method is still valid for such circuit-breakers. For the case shown before, the arc energy for the interruption on the major current loop will be not more than 50 % of the one calculated for the full major current loop. For the extended major loop, energy calculation has shown that 89 % of the relative full extended loop energy will be seen by the circuit-breaker.

Similar calculations have been done with a DC time constant of 120 ms and the results are very similar, mainly regarding the relative arc energy associated with the major extended current loop. For that particular case, the energy associated with the maximum possible arcing time represents 88 % of the total prospective arc energy of that current loop. For the other valid operations on the major current loop, the maximum arcing time window is slightly less than the 45 ms case (less than 40 % of the loop duration).

Because the relative arc energy associated with the extended major loop is quite close to 100 %, it is reasonable to use the same equivalency criteria ("$I \times t$" product) for circuit-breakers tested three-phase and exhibiting short minimum arcing times (e.g. < 3 ms).

A.5.5 Validity of the equivalence method prescribed by IEC 62271-100

IEC 62271-100 recommends a simple and practical way for the evaluation of the last loop parameters e.g. last loop current amplitude and last loop current duration. The resultant arc energy of the last current loop prior to interruption can be calculated by multiplying the loop amplitude by the loop duration to obtain a representative loop area ("$I \times t$" product) for comparison.

Table A.7 gives the results of the relative arc energy calculations for the different 60 Hz currents and DC time constants for interruption at the end of a major loop.

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Table A.7 – 60 Hz comparison between the integral method and the "$I \times t$" product method

Row	Current rating kA r.m.s. symmetrical	Time constant ms	Area of the last major loop by the exact integral method As	Peak of last major loop I kA	Last loop duration ms	$I \times t$ As	Ratio: area of major loop	Ratio: product $I \times t$	Difference to integral method %
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
1	63	45	805,8	124,7	10,55	1 309	1	1	–
2	50	60	718,2	106,1	11,1	1 177	0,89	0,90	1,01
3	50	75	777,8	111,0	11,6	1 288	0,96	0,98	2,08
4	50	120	890,5	120,9	12,5	1 511	1,10	1,15	4,55
5	40	120	712,4	96,7	12,5	1 209	0,88	0,92	4,55
The ratio area of column (8) is derived from column 4 divided by 805,8 and the ratio area of column (9) from division of column (7) by 1 309.									

Similarly, Table A.8 gives the results of the relative arc energy calculation for the different 50 Hz currents and DC time constants for interruption at the end of a major loop.

Table A.8 – 50 Hz comparison between the integral method and the "$I \times t$" product method

Row	Current rating kA r.m.s. symmetrical	Time constant ms	Area of the last major loop by the exact integral method As	Peak of last major loop I kA	Last loop duration ms	$I \times t$ As	Ratio: area of major loop	Ratio: product $I \times t$	Difference to integral method %
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
1	63	45	893,2	118,5	12,2	1 446	1	1	
2	50	60	802,0	101,8	12,9	1 313	0,90	0,91	1,11
3	50	75	875,2	106,8	13,4	1 431	0,98	0,99	1,02
4	50	120	1 019,2	117,4	14,6	1 714	1,14	1,19	4,38
5	40	120	815,3	93,9	14,6	1 371	0,91	0,95	4,40
The ratio area of column (8) is derived from column 4 divided by 893,2 and the ratio area of column (9) from division of column (7) by 1 446.									

Particular points of Tables A.7 and A.8:

a) Row 1 is the reference case;

b) In rows 2 to 5, the "$I \times t$" method is compared to the exact integral method for determining the relative arc energy of the last major current loop prior to interruption;

c) Rows 2 to 5 show that the relative difference between the two methods remains below 5 %.

With a difference of less than 5 % for a DC time constant variation from 45 ms to 120 ms, it is shown that the "$I \times t$" method is fully adequate to extend test results for another current and DC time constant ratings. The integral method should be considered as the exact method to calculate the equivalent arc energy during the last current loop and also during the whole

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arcing period but cannot be implemented in all test laboratories because of the different capabilities of the measuring system used. Therefore, the "$I \times t$" method was proposed to ease and speed up the result analysis after a test. "$I \times t$" is considered a reasonable approximation of the energy in the last major loop.

A.6 Discussion regarding equivalency

The method of analysis described for demonstrating the equivalency is not difficult to perform but access to the actual test results for the reference case is necessary. It should also be recognized that this investigation is only addressing a simultaneous three-phase fault case where one of the phases has always an offset ranging from 87 % to 100 % of the full DC offset depending on the point-on-wave initiation. It is the resulting current from that fully asymmetrical phase that has been compared. The fault currents that circulate in the other two phases will have significant reduced DC components and the ability of the circuit-breaker to interrupt these currents is not considered more difficult than those of all other test duties defined by IEC 62271-100.

This investigation supports the recommendation that if DC time constants greater than 45 ms are encountered on a system, the selection of a circuit-breaker rated one or two steps up (depending on actual test parameters for the reference case) in the R10 series above the expected system fault current for DC time constants up to 120 ms should be satisfactory. While the number of cases investigated is limited, the method can be applied to almost any combinations of three-phase fault currents and related DC time constants as a predictor of the maximum amount of energy involved.

Figure A.6 and Figure A.7 show selected plots for Case 1 and Case 2 of the currents with different DC time constants for both 60 Hz and 50 Hz respectively. An examination of the figures suggests that it is possible to use this method to evaluate different test combinations. For example one could use it to evaluate a test current at 50 Hz to show equivalence to a test current at 60 Hz. Since most such tests on high-voltage circuit-breakers will be done using synthetic circuits, the di/dt can be adjusted to the correct value at the time of interruption. By varying the amplitude of the current, the arc energy can be adjusted to be equivalent. For the manufacturer and/or user that knows the interrupting characteristics of a circuit-breaker, the outlined method is a useful tool for the evaluation of different interrupting capabilities under asymmetrical fault conditions.

IEC 62271-100 recognizes the problems associated with testing circuit-breakers with different DC time constants. It is fundamental that the circuit-breaker sees the correct prospective di/dt and at the time of interruption. As mentioned earlier, if synthetic tests are conducted, this can be adjusted to the correct value. If direct tests are used, the current level is adjusted within the prescribed tolerance to have the associated di/dt at the time of interruption. One fundamental consideration that should be accounted for is the DC time constant of the test station whether direct or synthetic test are used. The effective arc energy level under the last current loop can be adjusted by selecting the initiation instant of the short-circuit current (e.g. asymmetry level) or by adjusting the current level or a combination of both to obtain the correct last current loop parameters (amplitude and duration). Clause A.7 gives examples of waveshape adjustments during testing.

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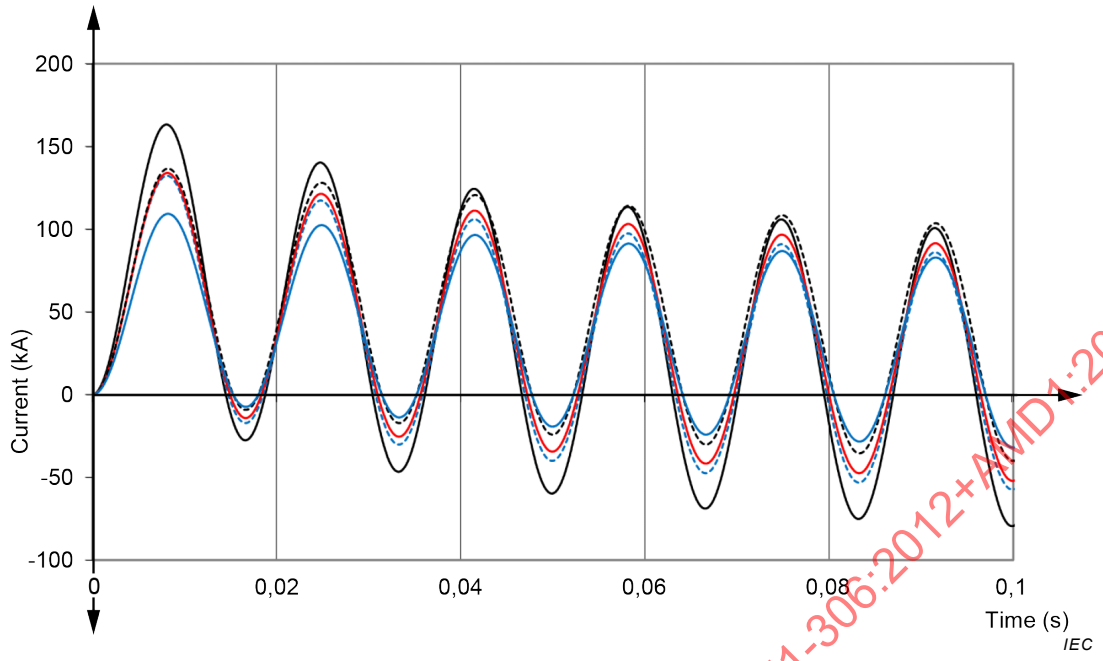
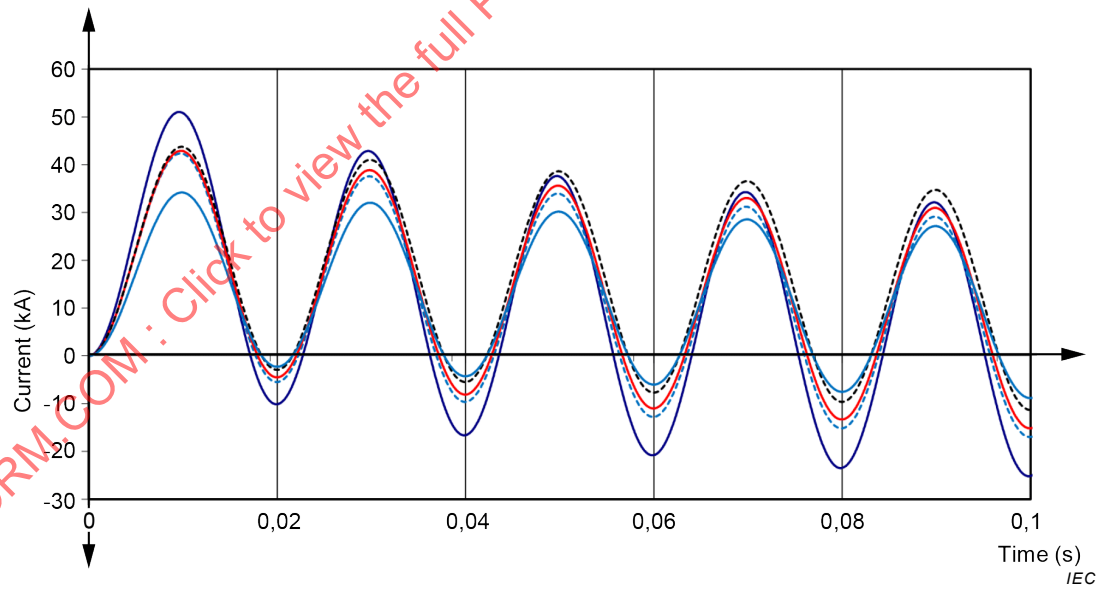


Key

Black, solid	63 kA, τ = 45 ms
Blue, dashed	50 kA, τ = 60 ms
Red	50 kA, τ = 75 ms
Black, dashed	50 kA, τ = 120 ms
Blue, solid	40 kA, τ = 120 ms

Figure A.6 – Plot of 60 Hz currents with indicated DC time constants



Key

Dark blue, solid	20 kA, τ = 45 ms
Blue, dashed	16 kA, τ = 60 ms
Red	16 kA, τ = 75 ms
Black, dashed	16 kA, τ = 120 ms
Blue, solid	12,5 kA, τ = 120 ms

Figure A.7 – Plot of 50 Hz currents with indicated DC time constants

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A.7 Current and TRV waveshape adjustments during tests

A.7.1 General

The examples given in this clause are based on standardized cases and give guidelines how to use the asymmetry criteria defined in IEC 62271-100:2008 in an actual test. It is usual that the DC time constant of the circuit-breaker is different than the DC time constant of the test circuit and some adjustments on the test parameters are necessary. Three different cases are given covering the major cases that may occur in test laboratories.

A.7.2 Three-phase testing of a circuit-breaker with a DC time constant of the rated short-circuit breaking current constant longer than the test circuit time constant

Rated voltage of the circuit-breaker:	24 kV
First-pole-to-clear factor:	1,5
DC time constant of the rated short-circuit breaking current:	120 ms
Test circuit time constant:	60 ms
Minimum arcing time during T100s:	7,5 ms
Minimum opening time:	32,5 ms
DC component at contact separation:	70,2 %
Minimum clearing time:	50 ms
Frequency:	50 Hz

The time constant of the test circuit differs from the DC time constant of the rated short-circuit breaking current. The adjustment method chosen in order to reach the required data is the pre-tripping method together with controlled closing.

NOTE 1 Controlled closing means the initiation of the test current at a chosen instant on the applied voltage in order to vary the initial DC component of the test current.

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Table A.9 – Example showing the test parameters obtained during a three-phase test when the DC time constant of the test circuit is shorter than the DC time constant of the rated short-circuit current

Parameters	Requirements (calculated values)		Test data when using pre-tripping and controlled closing methods		Deviation between required values and test values %
	Major loop with first clearing pole	Last-poles-to-clear major/minor loop [a]	Major loop with first clearing pole	Last-poles-to-clear major/minor loop [a]	
DC component at current interruption (%)	62,1		50,1		-19,3
di/dt at current interruption (%)	80,0		89,2		+11,5
Peak of the last current loop (p.u.)	1,56	1,28/0,75	1,56	1,48/0,95	0 +15,6/26,6[b]
Duration of the last current loop (ms)	13,8	12,7/7,45	13,8	14,1/8,8	0 +11/+17,8 [b]
Δt (ms) [c]		3,3		4,0	+21
I x t (p.u. ms)	21,53		21,53		0

[a] Values calculated for a non-effectively earthed neutral system using a network calculation program (see NOTE 2).

[b] Last-poles-to-clear.

[c] Δt is the time interval between the first-pole-to-clear and the last-poles-to-clear.

Result: It is possible to fulfil the requirements by using the pre-tripping and controlled closing options. In this particular case, the current initiation has been delayed by 2 cycles and the making angle has been moved from 0° to 22,5°. The TRV and di/dt values will be approximately 12 % higher than required. The arcing time for the last clearing poles will be slightly longer than the required one. The test data cover the required values. Tighter tolerances on the di/dt and on the TRV peak may be achieved by lowering test current and/or the TRV amplitude factor. The results are illustrated in Figure A.8.

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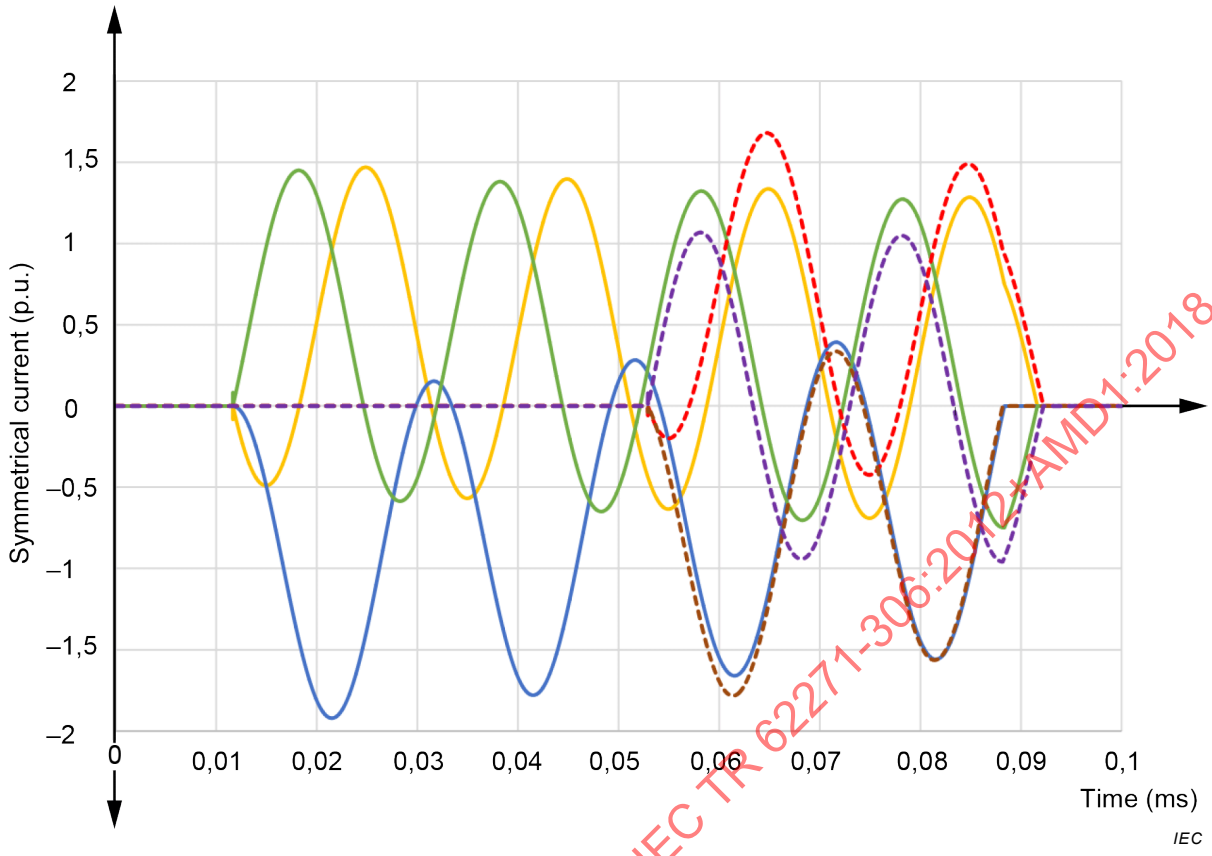

Key

Solid yellow line	Required current in A-phase
Solid blue line	Required current in B-phase
Solid green line	Required current in C-phase
Dotted red line	Test circuit A-phase
Dotted brown line	Test circuit B-phase
Dotted purple line	Test circuit C-phase

NOTE Owing to the shorter time constant of the test circuit, the short-circuit current is initiated later (pre-tripping method and to choose the closing angle in a way to achieve the required DC component at current zero (controlled closing).

Figure A.8 – Three-phase testing of a circuit-breaker with a DC time constant of the rated short-circuit breaking current longer than the test circuit time constant

As seen in Table A.9, the ratings of the circuit-breaker given in A.7.2 are fully covered by the test data. Attention should be paid to the fact that the percentage of asymmetry at current zero is lower than the rating given by the manufacturer at contact separation. This difference is normal because the value assigned by the manufacturer is based on the specified DC time constant of the rated short-circuit breaking current of 120 ms, it does not take into account the arcing time and the DC time constant of the test circuit. The test parameters to be fulfilled are those described for the last current loop.

NOTE 2 The easiest way to calculate the required three-phase or single-phase waveshape characteristics is by a network calculation program such as EMTP, MATHLAB, etc. The waveshape characteristics can also be calculated by hand from the fundamental three-phase or single-phase short-circuit current equations.

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A.7.3 Single phase testing of a circuit-breaker with a DC time constant of the rated short-circuit breaking current shorter than the test circuit time constant

Rated voltage of the circuit-breaker:	550 kV
First-pole-to-clear factor:	1,3
DC time constant of the rated short-circuit breaking current:	45 ms
Test circuit time constant:	60 ms
Minimum arcing time:	7,5 ms
Minimum opening time	32,5 ms
DC component at contact separation	38,9 %
Minimum clearing time:	50 ms
Frequency:	50 Hz

The time constant of the test circuit differs from the rated DC time constant of the rated short-circuit breaking current. The adjustment method chosen to reach the required data is the controlled closing method.

Table A.10 – Example showing the test parameters obtained during a single-phase test when the DC time constant of the test circuit is longer than the DC time constant of the rated short-circuit current

Parameters	Requirements (calculated values)	Test data when using controlled closing method	Deviation between required values and test values %
	Major loop	Major loop	
DC component at current interruption (%)	18,7	19,8	+5,9
di/dt at current interruption [a] (%)	99,6	99,1	-0,5
Peak of the last current loop (p.u.)	1,21	1,22	+0,8
Duration of the last current loop (ms)	11,4	11,4	0
u_1 [a]	98,9 %	98,4 %	-0,5
u_c [a]	95,8%	95,1 %	-0,7
$I \times t$ (p.u. ms)	13,79	13,91	+0,9
[a] In case of synthetic testing, it is possible to control these values independently of the time constant.			

Result: All test requirements can be fulfilled by using the controlled closing method. A making angle of 45° has been used. All values obtained are very close to the required values. Tighter tolerances may be achieved by changing the test current amplitude and/or the TRV amplitude factor of the TRV shaping circuit. The values for u_1 and u_c have been derived from the equations of Annex I of IEC 62271-101:2012/AMD1:2017. The results are illustrated in Figure A.9.

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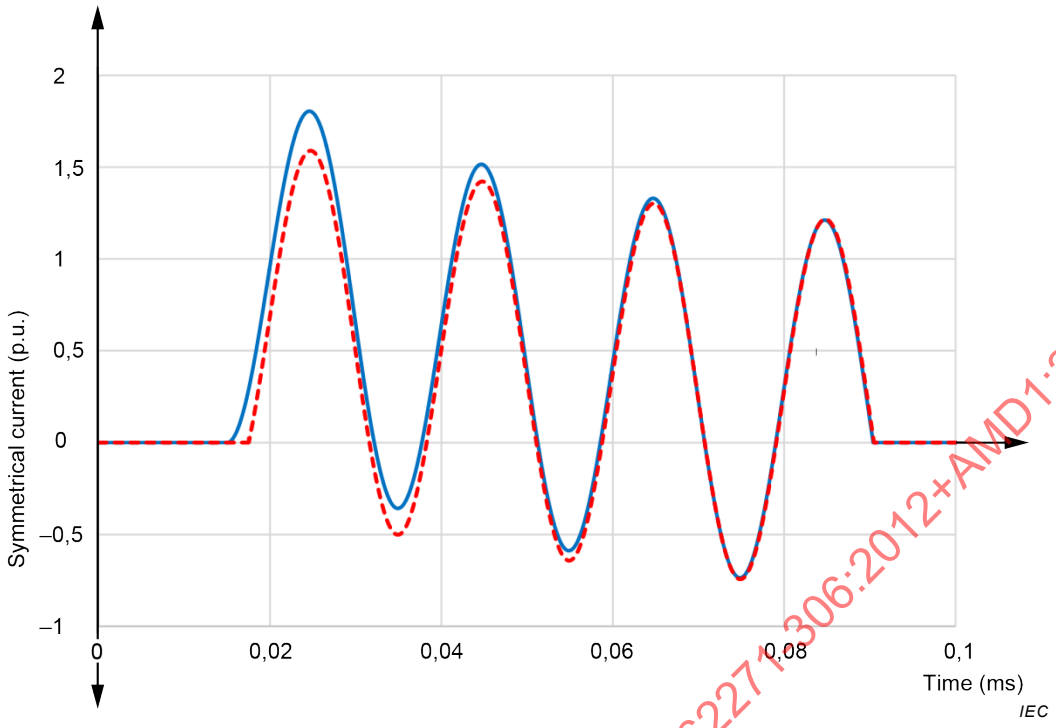

Key

Solid blue line	Required current
Dotted red line	Test circuit

Figure A.9 – Single phase testing of a circuit-breaker with a DC time constant of the rated short-circuit breaking current shorter than the test circuit time constant

As seen in Table A.10, the ratings of the circuit-breaker given in A.7.2 are fully covered by the test data. Attention should be paid to the fact that the percentage of asymmetry at current zero is lower than the rating given by the manufacturer at contact separation. This difference is normal because the value assigned by the manufacturer is based on the specified DC time constant of the rated short-circuit breaking current of 45 ms, it does not take into account the arcing time and the DC time constant of the test circuit. The test parameters to be fulfilled are those described for the last current loop.

A.7.4 Single-phase testing of a circuit-breaker with a DC time constant of the rated short-circuit breaking current longer than the test circuit time constant

Rated voltage of the circuit-breaker:	550 kV
First-pole-to-clear factor:	1,3
DC time constant of the rated short-circuit breaking current:	75 ms
Test circuit time constant:	60 ms
Minimum arcing time found during T100s:	7,5 ms
Minimum opening time	32,5 ms
DC component at contact separation	56,7 %
Minimum clearing time:	50 ms
Frequency:	50 Hz

The time constant of the test circuit differs from the rated DC time constant of the rated short-circuit breaking current. The adjustment method chosen in order to reach the required data was a combination of the pre-tripping method and the controlled closing method.

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Table A.11 – Example showing the test parameters obtained during a single-phase test when the DC time constant of the test circuit is shorter than the DC time constant of the rated short-circuit current

Parameters	Requirements (calculated values)	Test data when using controlled closing method	Deviation between required values and test values %
	Major loop	Major loop	
DC component at current interruption (%)	36,2	35,5	-1,9
di/dt at current interruption [a] (%)	94,8	95,4	+0,6
Peak of the last current loop (p.u.)	1,39	1,39	0
Duration of the last current loop (ms)	12,6	12,6	0
u_1 [a]	93,5 %	94,1 %	+0,6
u_c [a]	87,5 %	88,2 %	+0,8
$I \times t$ (p.u. ms)	17,5	17,5	0
[a] In case of synthetic testing it is possible to control these values independent from the time constant			

Result: All test requirements can be fulfilled by combining the controlled closing method and the pre tripping method. In this particular case, the current initiation has been delayed by 1 cycle and the making angle has been moved from 0° to 25°. All values are very close to the required values. The values for u_1 and u_c have been derived from the equations of Annex I of IEC 62271-101:2012/AMD1:2017. The results are illustrated in Figure A.10.

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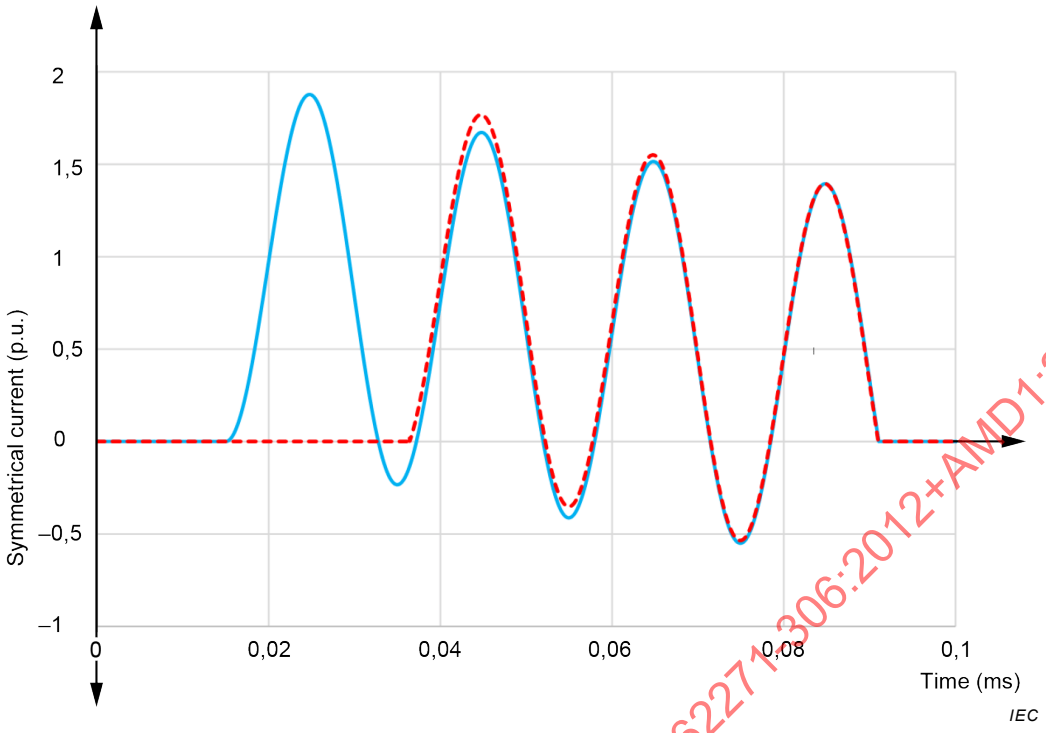

Key

Solid blue line	Required current
Dotted red line	Test circuit

Figure A.10 – Single-phase testing of a circuit-breaker with a DC time constant of the rated short-circuit breaking current longer than the test circuit time constant

As seen in Table A.11, the ratings of the circuit-breaker given are fully covered by the test data. Attention should be paid to the fact that the percentage of asymmetry at current zero is lower than the rating given by the manufacturer at contact separation. This difference is normal because the value assigned by the manufacturer is based on the specified DC time constant of the rated short-circuit breaking current of 75 ms, it does not take into account the arcing time and the DC time constant of the test circuit. The test parameters to be fulfilled are those described for the last current loop.

A.8 Conclusions

a) Based on this work, a circuit-breaker applied at an interrupting current level one or two steps below the circuit-breaker rating in the R10 series may be satisfactory for DC time constants above the standard test value of 45 ms;

b) This evaluation shows, for the limited cases studied, that the one step reduction in the R10 series may cover applications up through a DC time constant of 120 ms depending on the last current loop parameters obtained during tests for the reference ratings of the circuit-breaker;

c) The "$I \times t$" product method can be used to evaluate equivalence of tests done at 50 Hz or 60 Hz at one DC time constant to cover applications at 50 Hz or 60 Hz with different DC time constants;

d) The "$I \times t$" method is the most convenient and appropriate method that can be used to check tolerance last current loop parameters during test-duty T100a;

e) The application engineer needs to determine the actual expected fault current including its DC time constant at the system point of interest to determine the required circuit-breaker rating.

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Annex B
(informative)

Interruption of currents with delayed zero crossings

B.1 General

This technical report does not cover generator circuit-breakers as they are not in the scope of IEC 62271-100. The circuit-breakers referred to in this annex are either located on the high-voltage side of the step-up transformer (e.g. as shown in Figure B.1) but close to generation, or controlling networks with a high density of generation and large motor loads (e.g. as shown in Figure B.13).

An example is the high-voltage circuit-breaker in the connection between a power plant and the high-voltage network (circuit-breaker CB1 in Figure B.1). Examples of the latter can be found on off-shore oil platforms, in the auxiliary networks of large power plants, or in certain industrial sites.

The intention of this annex is to show that it can be determined by calculation whether a circuit-breaker can interrupt currents with delayed zero crossings under given circumstances provided that the performance of that circuit-breaker has been tested in a circuit with currents of more than 100 % asymmetry.

B.2 Faults close to major generation

B.2.1 Overview

All circuit-breakers manufactured today are alternating current circuit-breakers, i.e. circuit-breakers that need current zeros to interrupt. However, there are occasions when the fault current does not have current zeros how can today's SF_6 circuit-breakers manage such situations?

B.2.2 General

Under certain conditions faults occurring close to a power station may lead to the generator currents not passing through zero. Since circuit-breakers can only clear at a current zero this means that such currents could not be interrupted immediately and interruption would be delayed until current zeros occurred due to the d.c. component's decay. In actual fact, however, an arc is drawn between the opening circuit-breaker contacts with the effect that the d.c. components decay much more quickly. Considerable significance is therefore attached to the magnitude and variation of the arc voltage, the intensity of the gas flow and the design of the arc quenching arrangement. The arc drawn between the opening contacts may be regarded as a non-linear resistance which adds to the ohmic resistances of the other circuit elements and which contributes to the reduction of the d.c. time constant of the fault current, whereas the a.c. component remains unaffected.

With regard to the degree of fault current asymmetry the theoretical worst case condition is a non-simultaneous unearthed fault. As an example this fault can be a line-to-line short-circuit at voltage zero across two phases which after 90° becomes a three-phase fault at line-to-earth zero voltage in the third phase. This non-simultaneous fault inception produces the theoretically highest d.c. component of 136,6 %, i.e. it is 36,6 % higher than that of a simultaneous three-phase fault at line-to-earth voltage zero.

B.2.3 Fault location

The conditions for the occurrence of fully asymmetrical fault currents are closely linked to the resulting time constant of the d.c. component $\tau = L/R$, i.e. mainly to the ohmic resistance of

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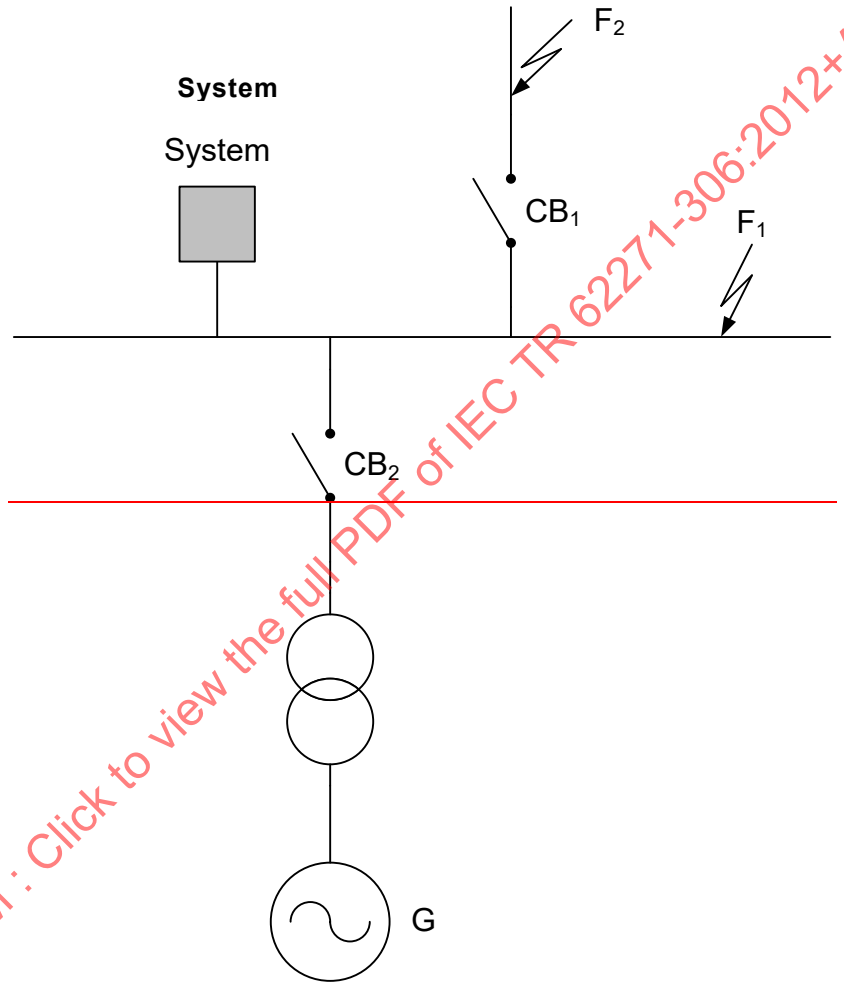
~~the short-circuit path. Therefore, to be able to assess the interrupting capability of circuit-breakers in this particular case, only fault currents supplied by generators which – together with their transformers – account for the smallest X/R ratios, should be taken into consideration.~~

~~In case of a fault which is being fed from a generator and also from the network via a transmission line the total fault current is not likely to be fully asymmetric because of the relatively high ohmic resistance of the line.~~

~~In the basic circuit diagram in Figure B.1 only faults at location F_1, which circuit-breaker CB_1 has to interrupt, should therefore be taken into account. Fault currents at location F_2 with its circuit-breaker CB_2 are subject to normal current zeros.~~



~~Key~~

~~F_1, F_2: Fault locations~~

~~CB_1, CB_2: Circuit-breakers~~

~~G: Generator~~

~~**Figure B.1 – Single line diagram of a power plant substation**~~

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B.2.4 Effect of the generator operating conditions

B.2.4.1 Underexcited operation of the generator

With respect to current asymmetry the maximum stress on the circuit-breaker is determined by the generator loading as well as by the particular instant of fault inception. In underexcited operation, when the generator produces active power and consumes reactive power, not only does the initial value of the d.c. component becomes larger than that of the a.c. component, but the time constants and reactances of the generator transverse axis, which are more unfavourable than those of the longitudinal axis, also affect the variation of the a.c. component.

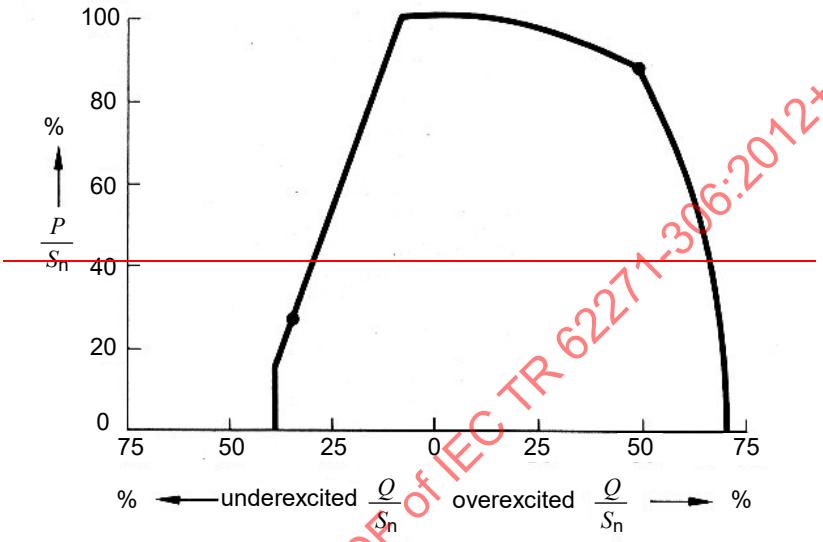
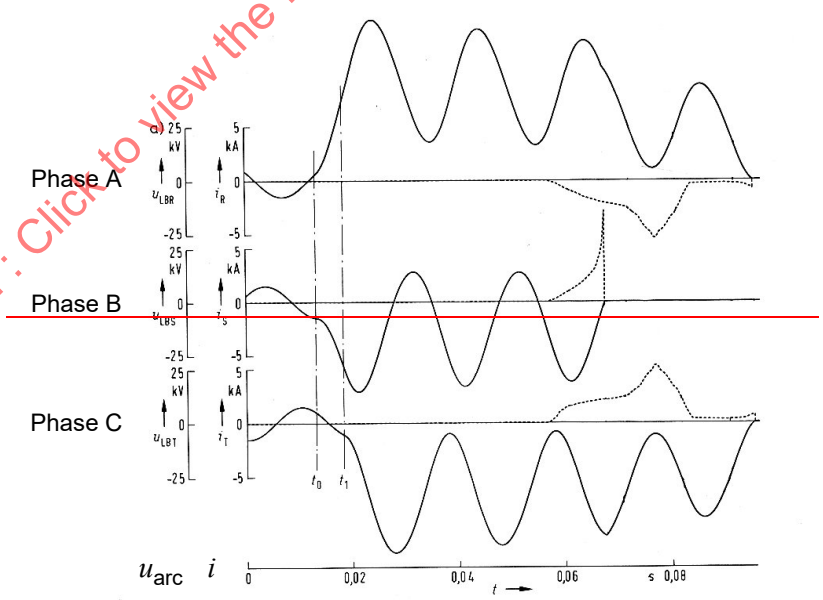


Figure B.2 – Performance chart (power characteristic) of a large generator



Key

t_0: Two-phase fault at phase-to-phase voltage zero

t_1: transition to three-phase fault at third phase voltage zero

Figure B.3 – Circuit-breaker currents i and arc voltages u_{arc} in case of a three-phase fault following underexcited operation: Non-simultaneous fault inception

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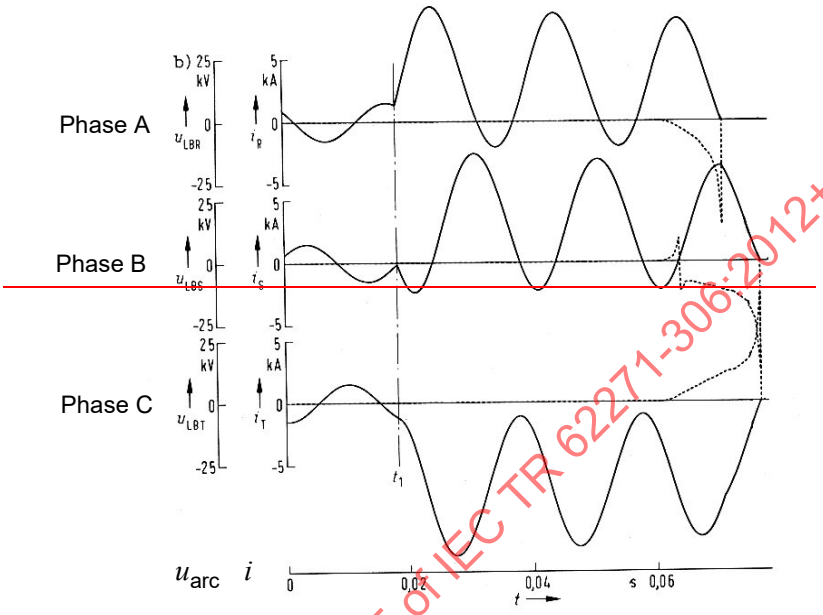
~~For a generator taken as an example an initial load of P = 30 % and Q = –35 % in accordance with the performance chart in Figure B.2 was found to be particularly critical.~~

~~Calculated currents and arc-voltages for non-simultaneous and simultaneous unearthed fault inception under these conditions are shown in Figure B.4 and Figure B.5. As there is no arc voltage involved during the first 55 ms these currents (at 50 Hz) can be considered inherent for the initial 55 ms.~~



~~Figure B.4 – Circuit-breaker currents i and arc voltages u_{arc} in case of a three-phase fault following underexcited operation: Simultaneous fault inception at third phase voltage zero~~

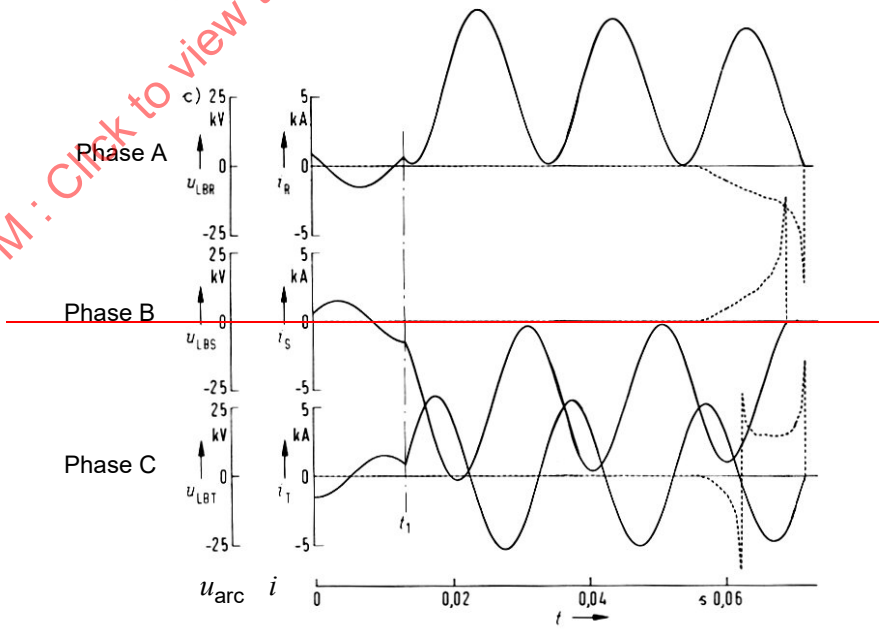


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Figure B.5 – Circuit-breaker currents *i* and arc voltages u_{arc} in case of a three-phase fault following underexcited operation: Simultaneous fault inception at third phase voltage crest

In Figure B.3 the initially two-phase fault occurred across the upper two phases at time t_0. The third phase was subjected to the now three-phase fault at time t_1. It can be seen that a further d.c. component is added in the first phase to the d.c. component of the two-phase fault current resulting in an asymmetry of the current in this phase of more than 100 %.

In the second phase current zeros continue to occur, while the d.c. component in the third phase is, also, above 100 %, but not as high as in the first phase.

For a given SF_6 circuit-breaker, the arc voltage of which has been determined experimentally, it has been assumed that an effective arc voltage appears between the opening contacts 55 ms after fault inception. This takes into account the time until contact separation and some milliseconds for the development of the full gas flow. The current in the second phase is interrupted at the next current zero. Consequently, a phase shift takes place in the a.c. and in the d.c. components in the other phases: the d.c. component in the first phase decreases, while it increases in the third phase there leading to an even higher current offset. However, due to the effect of the arc voltage, which acts as an additional resistance R_a and thus reduces the momentary value of the d.c. time constant to $\tau = L/(R + R_a)$, the currents are forced through zero in the first and third phase, as well, and are interrupted.

Figure B.4 and Figure B.5 show simultaneous unearthed faults which occur at time t_1. The d.c. components are less pronounced and the interruption takes a similar course as described for Figure B.3.

The arc voltage will also cause the fault currents to pass through zero in the event of a generator transformer fault (Figure B.6) but with the conditions otherwise the same as in Figure B.3.

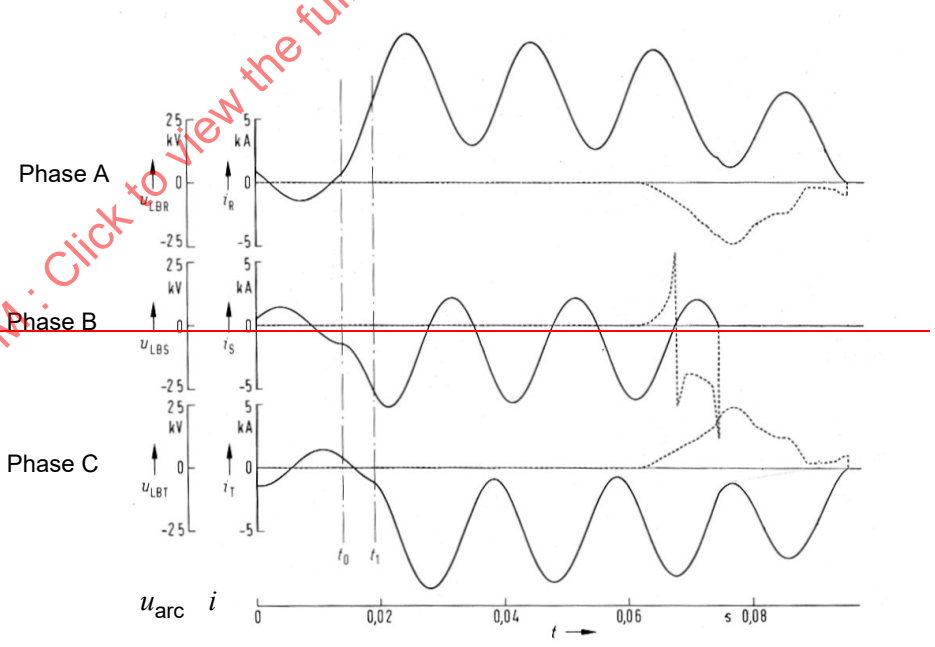

Figure B.6 – Circuit-breaker currents *i* and arc voltages u_{arc} under conditions of a non-simultaneous three-phase fault, underexcited operation and failure of a generator transformer

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B.2.4.2 Overexcited operation of the generator

Fault clearance following overexcited loading of the generator, i.e. active-power and reactive-power output, subjects the circuit-breaker to lower stresses (Figure B.7). The maximum displacement of the currents from the zero line under fault conditions following full load operation is much smaller than that of the currents due to underexcited operation (Figure B.3).

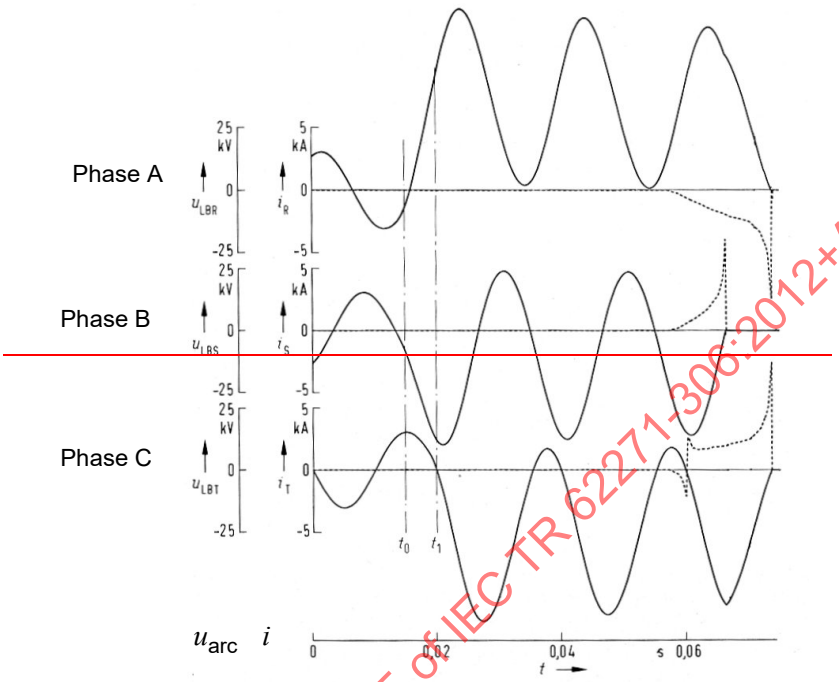

Figure B.7 – Circuit-breaker currents i and arc voltages u_{arc} under conditions of a non-simultaneous three-phase fault following full load operation

B.2.4.3 No-load operation of the generator

The calculated currents and arc voltages due to a non-simultaneous fault developing from no-load operation of the generator are shown in Figure B.8. As in case of a fault following full load operation (Figure B.7) the displacement of the currents from the zero line is smaller than for underexcited operation.

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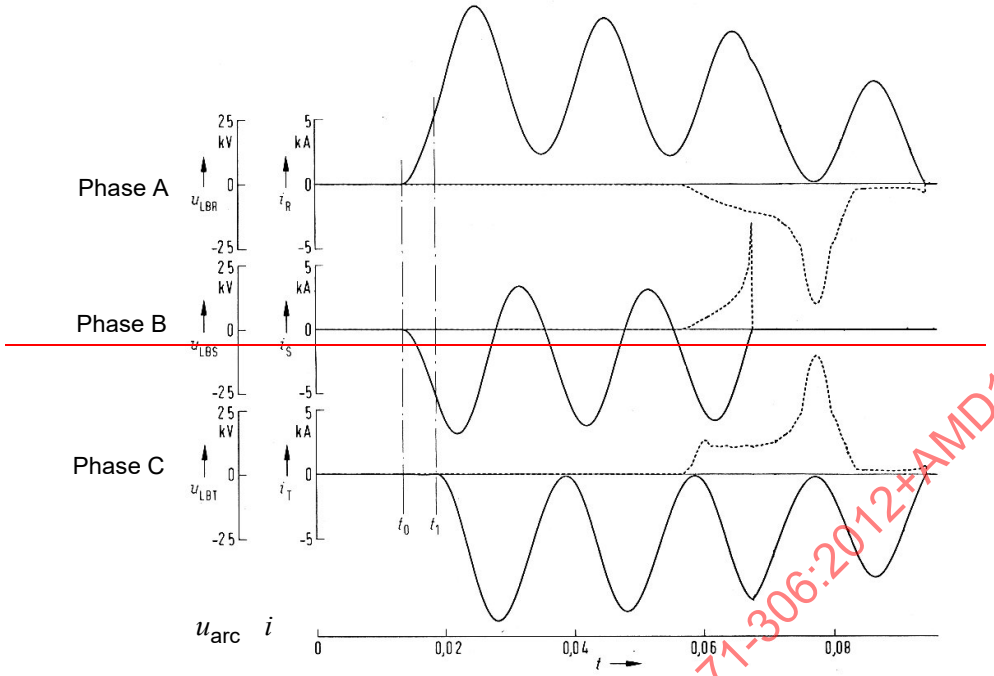

Figure B.8 – Circuit-breaker currents *i* and arc voltages u_{arc} under conditions of a non-simultaneous three-phase fault following no-load operation

B.2.5 Unsynchronized closing

It can be seen from Figure B.9 that not only fault conditions but also attempting to synchronize at an unsuitable differential angle may cause the current zeros to be delayed. Owing to the mean electrical moment which thereby occurs and the resulting speed variation the currents can be constricted to such an extent that they may no longer pass through zero in any of the phases. However, this does not occur until after a prolonged period because of the much higher mechanical time constants. Should the circuit-breaker operate in this constriction range it still can interrupt the current due to the higher arc voltage as shown in Figure B.9.

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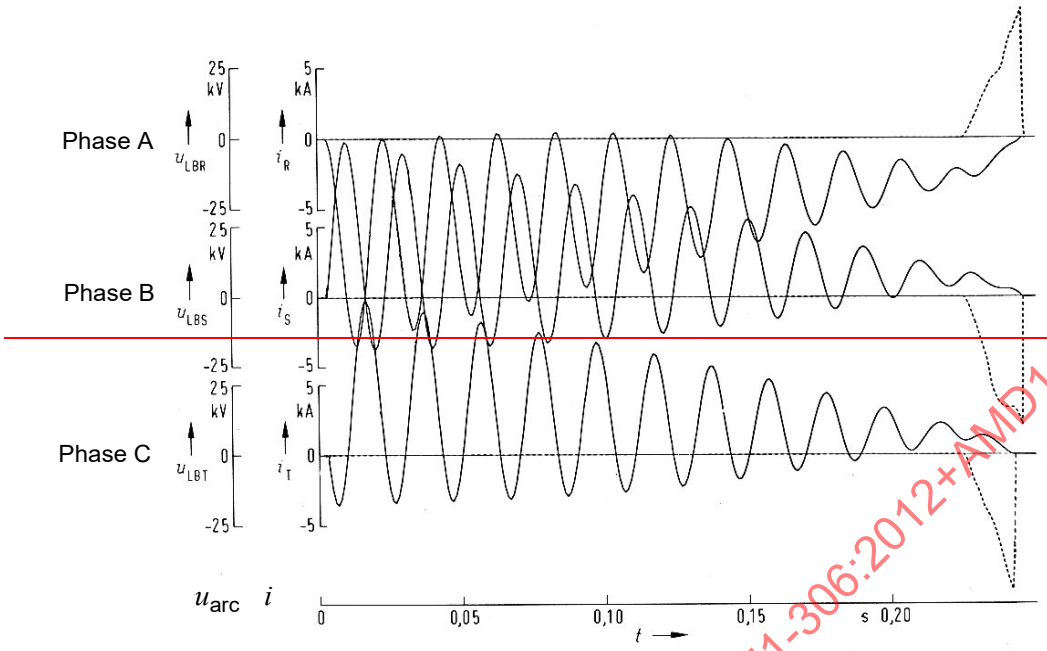

Figure B.9 – Circuit-breaker currents *i* and arc voltages u_{arc} under conditions of unsynchronized closing with 90° differential angle

B.2.6 Proof of performance

B.2.6.1 Testing

Normally, testing of a high-voltage circuit-breaker under these conditions can, only, be carried out single-phase, i.e. on the circuit-breaker pole with the highest d.c. component. To produce d.c. components greater than 100 % for several cycles the test circuit must have a high X/R ratio giving a d.c. time constant τ of possibly several hundred ms. The test voltage must be at least as high as the rated phase voltage or in case of unit testing as high as the rated voltage across the most highly stressed interrupter for the first-pole-to-clear in an unearthed fault or the last phase-to-clear in an earthed system. The a.c. component of the test current has to cover the a.c. component of the short-circuit current of the generator considering the conditions stated in B.2.2 and B.2.3.

In practice the test procedure in order to subject one pole to a short-circuit current with delayed current zeros is as follows (Figure B.10, Phase A).

In most cases the tests are made single-pole on one interrupter unit. The first two phases of the test circuit are switched in by a make-switch when their phase-to-phase voltage passes through zero. The third phase is switched in a quarter cycle later. By varying the delay of the making in the third phase the amount of asymmetry of the short-circuit current can be adjusted. Figure B.10 shows the oscillogram of the current not affected by the arc, i.e. the inherent current of the test circuit. It can be seen that at the transition to the three-phase circuit a further d.c. component is added to the d.c. component of the two phase current with the effect that the current in phase A is displaced by more than 100 %. The short-circuit generators should not be superexcited to delay the current zero by several cycles due to the decaying a.c. component.

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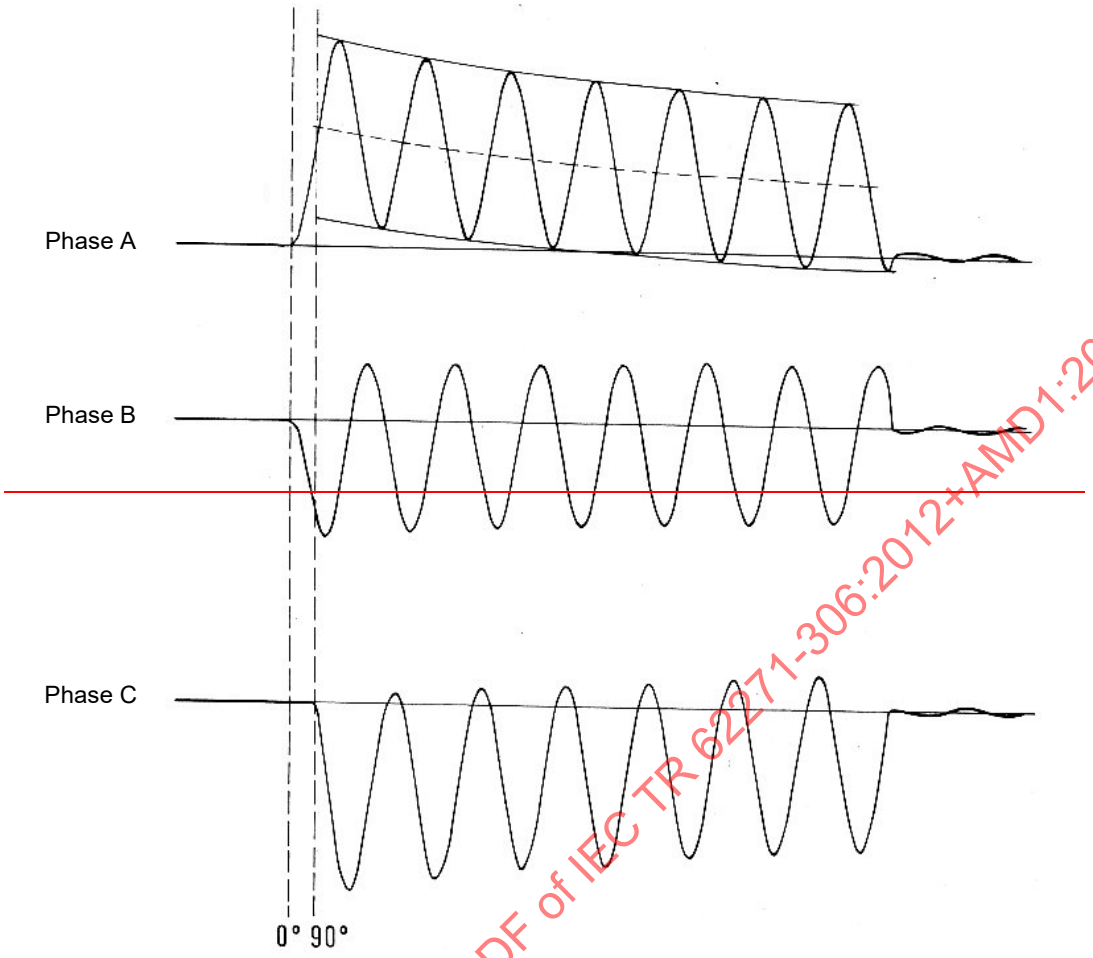

~~Example:~~

~~Test voltage: 70 kV~~ ~~1st current minimum: 850 A~~

~~Test current: a.c. component: 2,63 kA r.m.s.~~ ~~2nd current minimum: 450 A~~

~~Current peak: 8,5 kA~~ ~~3rd current minimum: 260 A~~

~~Figure B.10 – Prospective (inherent) current~~

~~The contacts of the test breaker should be set to part about 1 ms after the initial inception of the current flow. Thus, the test circuit-breaker is subjected to the maximum asymmetrical current after contact separation. The arcing time is then varied systematically in order to determine the minimum and maximum times for each a.c. current and voltage step.~~

~~B.2.6.2 Calculation of the performance of a circuit-breaker~~

~~The arc characteristics measured during the tests are converted into a mathematical model in order to obtain details about the interrupting capability of the circuit-breaker in other situations or under the varied fault conditions, respectively. The model must be a true representation of the arc voltage variation from contact separation until arc extinction. The instantaneous values of the currents and corresponding arc voltages, which were taken from actual test oscillograms, produce the distribution of dots shown in Figure B.11 together with the mean tolerance band. The wide variation of the readings results from the instable and rather inconsistent arc behaviour.~~

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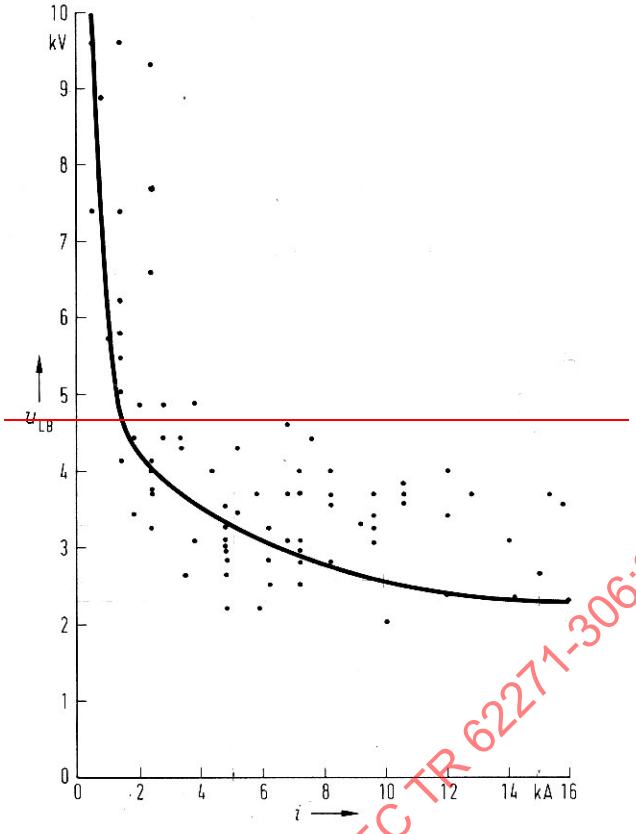

Figure B.11 – Arc voltage-current characteristic for a SF_6 puffer type interrupter

In addition to the voltage-current characteristic of the arc, the variation of the gas pressure in the arcing chamber, the extension of the arc by the gas flow and the contact distance which rises with the arcing time must be taken into account. These circuit-breaker characteristics can be expressed mathematically by a standardized assessment function $e(t)$ with a maximum value of 1 (Figure B.12). Strictly speaking this function has no physical significance.

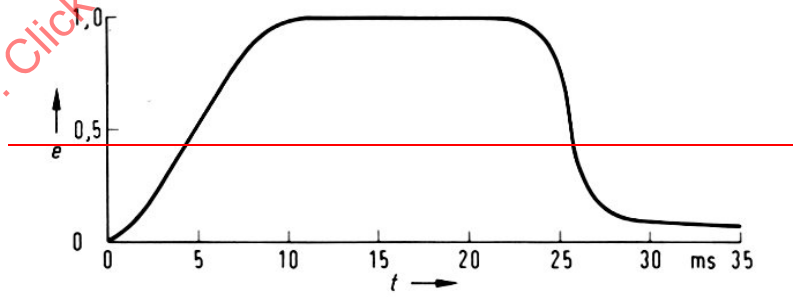

Figure B.12 – Assessment function $e(t)$

The total function of the arc voltage – as a function of time, the circuit-breaker characteristics and the instantaneous current value – is obtained by multiplying the individual functions shown in Figure B.11 and Figure B.12.

$$u_{arc}(t, i) = u_{arc}(i) \times e(t)$$

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Using this total arc voltage function u_{arc} the arc drawn between the opening contacts may be regarded as a non-linear ohmic resistance which mainly reduces the d.c. time constant of the fault current, while the a.c. component remains unaffected.

Other methods of calculation have also been developed to compare testing and simulation [59] and [60].

B.2.7 Distributed generation and large motors

In distribution voltage systems fault currents with delayed zero crossings may occur either in the proximity of a concentration of generation or when switching off large high-voltage motors or in a combination of both. Even vacuum circuit-breakers with their relatively low arc voltage may be well suited to clear under these conditions, provided they are designed to withstand the high current peak values associated with such faults. Also, their contact configuration must be able to withstand prolonged arcing. In any case it will be necessary to investigate the conditions of the particular application to determine the actual stress upon the circuit-breaker.

B.2.8 Conditions for fault currents with delayed zeros

In distribution voltage networks with an extremely large concentration of generation and motor load, the probability that short-circuit currents with a d.c. component well above 100 % will occur is even higher than in high-voltage systems. The d.c. time constant τ may be in the order of some hundreds of milliseconds. This means the current in at least one phase will have no current zeros for several cycles.

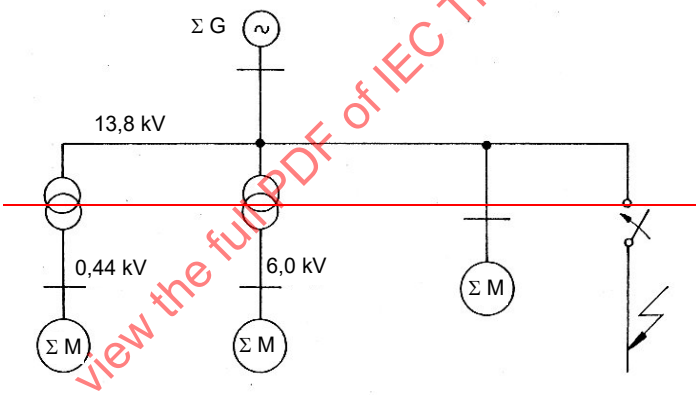

Figure B.13 – Network with contribution from generation and large motor load

If large high-voltage motors are present short-circuits with delayed current zeros will not only occur due to a non-simultaneous fault, but they are even possible in case of a simultaneous (bolted) fault (Figure B.13). If there is a fault the motors act as generators and feed back into the system a current with a high d.c. component. As they are slowing down they will gradually become out-of-phase with respect to the feeding system. The frequency of the current generated by the motors will drop below the generator frequency. As Figure B.14 shows, even if the short-circuit current from the generators has current zeros the superposition of the current generated by the motors results in a total short-circuit current with delayed current zeros.

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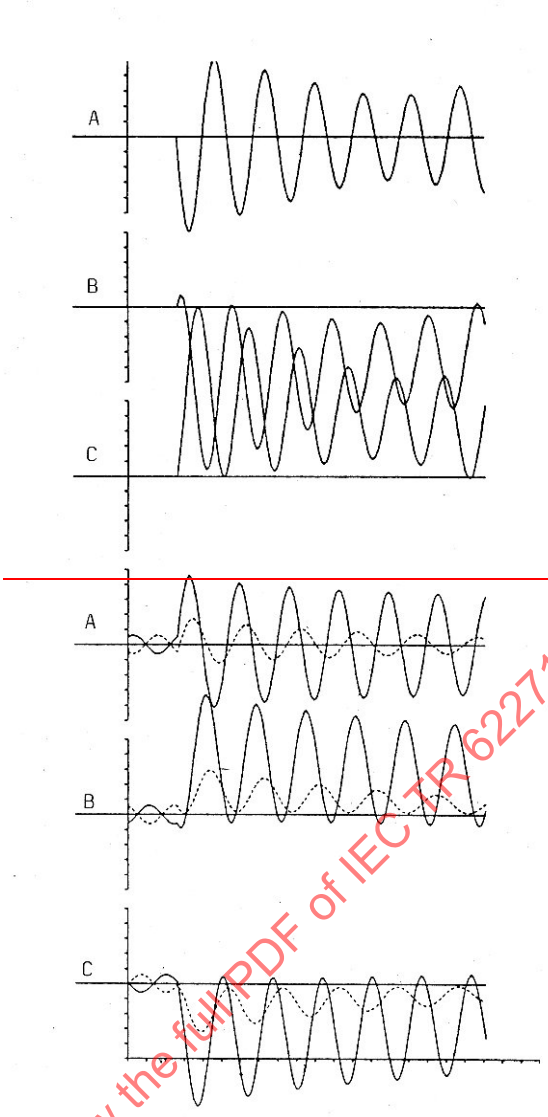

~~Key~~

~~Upper traces: Total fault current.~~

~~Lower traces:~~

~~– solid lines: generator fault current, d.c. time constant τ = 180 ms~~

~~– dotted lines: fault current generated by the motor~~

~~Figure B.14 – Computer simulation of a three-phase simultaneous fault with contribution from generation and large motor load~~

~~From Figure B.14 it can be determined that the probability of occurrence of a short-circuit current with delayed zeros is higher if the generator short-circuit current has a large d.c. component with a long d.c. time constant. This is the case if the fault location is close to the generators. If generation and motor load are located close to each other, the damping of the short-circuit current d.c. component is particularly low and the conditions assumed in Figure B.14 are met. Typical examples are offshore oil platforms where generation and load may be in the order of or even above 50 MVA and the connections are short and industrial plants which may be run in certain parts on their own power supply.~~

~~In industrial plants which are fed via transmission lines or cables these lines or cables act as damping elements for the d.c. component, and the resulting total fault current most probably has zeros in all three phases continuously from the fault inception.~~

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B.2.9 Three-phase interruption of currents with delayed zeros

Most distribution class voltage circuit-breakers have a common mechanism which is linked to the three poles via a common shaft. Therefore, all making and breaking operations are carried out three-phase. Accordingly, studies whether such a circuit-breaker is able to interrupt a fault current with delayed zeros must be carried out on a three-phase basis.

The sequence of a three-phase interruption may be shown taking a non-simultaneous fault in an unearthed system as an example. Consequently, the a.c. components and the d.c. components in the three phases add up to zero, respectively.

To cover the extremes it is considered that the short-circuit may occur at voltage zero as well as at voltage crest of one phase. The vector diagrams Figure B.15 and Figure B.16 show the a.c. and d.c. components of the currents in all phases at inception of the three-phase fault and after the interruption by the first-pole-to-clear. The a.c. components of the three-phase current are normalized to 1 p.u. and their decay is neglected in the vector diagrams. Likewise, no decay of the d.c. components is taken into account.

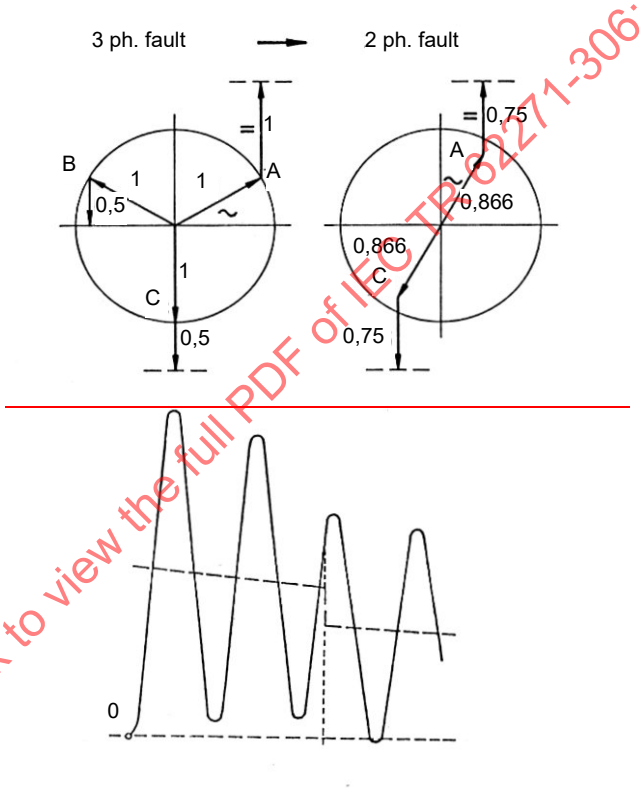

Figure B.15 – Short-circuit at voltage zero of phase A (maximum d.c. component in phase A) with transition from three-phase to two-phase fault

If a short-circuit occurs at voltage zero one phase has the maximum possible offset. This is considered to be phase A in Figure B.15, with a d.c. component of ±1 p.u. Consequently, the d.c. components in the two other phases are -0,5 p.u. In these phases there are always current zeros giving the corresponding circuit-breaker poles the possibility to clear. After interruption of the first phase (e.g. by pole B) there is a phase shift in the remaining two phases: their a.c. components become ±0,866 p.u. and their d.c. components ±0,75 p.u. Even the originally fully offset phase will have current zeros now and all circuit-breaker poles are able to clear.

Generally speaking, in case of a fault at voltage zero this phase shift will lead to a reduction of the d.c. component in the most offset last phase. In most cases there will be current zeros

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now also and the two last-to-clear poles are able to interrupt as well. Even if there are no current zeros immediately after the phase shift the current offset is reduced, leading to current zeros after one or two further cycles.

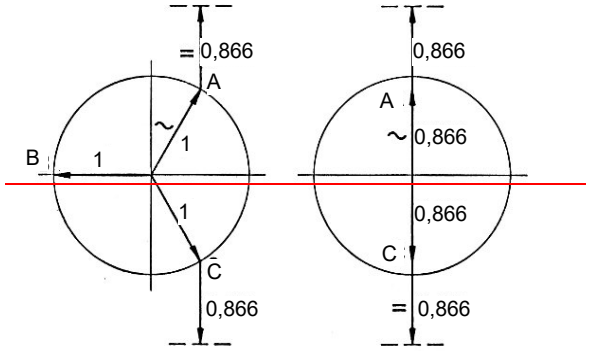

Figure B.16 – Short-circuit at voltage crest of phase B (phase B totally symmetrical) and transition from three-phase to two-phase fault

In case of a short-circuit at voltage crest the current in one phase will be totally symmetrical (phase B in Figure B.16). The other two phases then have a d.c. component of ±0,866 p.u. Accordingly, as long as this is a three-phase short-circuit all phases have current zeros. If the symmetrical current in phase B is interrupted first, the phase shift will change the a.c. components in the other two phases to ±0,866. The d.c. components in those phases remain unchanged. This means that the a.c. and d.c. components have equal amplitudes and the current will now only touch the zero line.

To determine whether a circuit-breaker is able to clear such a fault, it is therefore important to consider how the a.c. components and the d.c. components develop during the short-circuit. Both decay in a different manner. The a.c. components consist of a subtransient and a transient short-circuit current. While the subtransient short-circuit current decays with a time constant of 20 ms to 30 ms, the transient time constant may be in the order of several hundred milliseconds, even up to some seconds. The d.c. component has a time constant $\tau = L/R$ which is determined by the reactance and the resistance of the faulted circuit, including the generators, transformers and switchgear. On oil platforms it often has a value between 200 ms and 300 ms.

Depending on the load conditions of the generators, i.e. on their state of excitation before fault inception, the a.c. component may decay more rapidly than the d.c. component. Especially if the subtransient a.c. short-circuit current is of great significance the amplitude of the a.c. component may have become smaller than that of the d.c. component by the time the first phase is cleared. In that case there will be no current zeros in the one or two more offset last phases. The arc in these two circuit-breaker poles will now have to burn for another one or two cycles. As even the relatively small arc voltage of vacuum circuit-breakers contributes to the reduction of the d.c. time constant, the d.c. components will decrease further and current zeros will occur again giving the circuit-breaker to finally interrupt.

Therefore, of the two conditions of fault inception, the three-phase short-circuit at voltage crest might be considered more severe for three-phase interruption as there may be a possibility for the last poles-to-clear only with prolonged arcing. However, a short-circuit at voltage zero will stress a circuit-breaker with a higher d.c. component and thus with an overall higher current peak. These considerations show that each circuit configuration has to be regarded individually in order to determine the critical stress imposed upon the circuit-breaker. Above all it is necessary to evaluate, at the moment of contact separation, the amplitudes of the a.c. and the d.c. component and their time constants.

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B.2.10 Application of distribution voltage class circuit-breakers

As pointed out, already, the application of distribution class voltage circuit-breakers for the clearance of faults with delayed current zeros is based upon the assumption that these circuit-breakers will always be interrupted by three-pole operation. Accordingly, all analytical considerations and tests have to be carried out on a three-phase basis.

Although the arc voltage, as for vacuum circuit-breakers, may only be in the order of about 100 V experience shows that it has a non-negligible effect upon the decay of the d.c. component.

When tested according to IEC 62271-100 or IEEE C37.013 [61], the circuit-breaker has to clear a symmetrical short-circuit current or a short-circuit current with a d.c. component of some tens of percent at a moment when the power frequency recovery voltage is at its crest or near to it. This leads to a transient recovery voltage with a relatively high peak value. In case of a short-circuit current with a very high d.c. component the moment of current zero almost coincides with the moment of voltage zero of the power frequency recovery voltage. Thus, the transient recovery voltage stress immediately after current interruption becomes relatively low.

A circuit-breaker suited to clear faults with delayed current zeros must be able to make and withstand very high current amplitudes due to the d.c. components in the order of 130 %. Also, the contacts must be able to withstand thermally arc durations of two or even three cycles and still interrupt a fully offset short-circuit current. Consequently, it is advisable to use in such case a circuit-breaker with a higher short-circuit current rating than that which the particular application suggests.

According to test experience the contacts designed to absorb the energy connected with the breaking of such rated short-circuit current without being overheated are most likely capable to withstand the arc duration required to clear under the conditions of delayed current zeros.

B.2.11 Testing

To demonstrate the capability of distribution voltage class circuit-breakers to withstand and to clear faults with delayed current zeros three phase tests should be carried out in a similar circuit as described in B.2.6.1. The test circuit parameters (test voltage, frequency, TRV) shall correspond to those rated for a system of the particular application. The tests should cover both conditions as described in B.2.9:

a) with the maximum d.c. component in one phase, i.e. one phase fully offset, corresponding to a short-circuit occurring at voltage zero;

b) with practical no d.c. component in one phase, i.e. one phase fully symmetrical, corresponding to a short-circuit occurring at voltage crest.

To achieve the maximum offset current with a large d.c. time constant a special sequence has to be chosen in producing a three-phase non-simultaneous short-circuit (see B.2.6.1). Two phases are switched in when their phase-to-phase voltage passes through zero. The third phase is closed a quarter cycle later. By varying the delay of the making in the third phase the amount of asymmetry of the short-circuit current can be adjusted. The short-circuit generator should not be superexcited.

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B.1 General

This Technical Report does not cover generator circuit-breakers as they are not in the scope of IEC 62271-100. The circuit-breakers referred to in this annex are either located on the high-voltage side of the step-up transformer (e.g. as shown in Figure B.1) but close to generation, or controlling networks with a high density of generation and large motor loads (e.g. as shown in Figure B.13).

An example is the high-voltage circuit-breaker in the connection between a power plant and the high-voltage network (circuit-breaker CB1 in Figure B.1). Examples of the latter can be found on off-shore oil platforms, in the auxiliary networks of large power plants, or in certain industrial sites.

The intention of this annex is to show that it can be determined by calculation whether a circuit-breaker can interrupt currents with delayed zero crossings under given circumstances provided that the performance of that circuit-breaker has been tested in a circuit with currents of more than 100 % asymmetry.

B.2 Faults close to major generation

B.2.1 Overview

All circuit-breakers manufactured today are alternating current circuit-breakers, i.e. circuit-breakers that need current zeros to interrupt. However, there are occasions when the fault current does not have current zeros: how can today's gas and vacuum circuit-breakers manage such situations?

B.2.2 General

Under certain conditions, faults occurring close to a power station may lead to the generator currents not passing through zero. Since circuit-breakers can only clear at a current zero, this means that such currents could not be interrupted immediately and interruption would be delayed until current zeros occurred due to the DC component's decay. In actual fact, however, an arc is drawn between the opening circuit-breaker contacts with the effect that the DC components decay much more quickly. Considerable significance is therefore attached to the magnitude and variation of the arc voltage, the intensity of the gas flow and the design of the arc quenching arrangement. The arc drawn between the opening contacts may be regarded as a non-linear resistance which adds to the Ohmic resistances of the other circuit elements and which contributes to the reduction of the DC time constant of the fault current, whereas the AC component remains unaffected.

With regard to the degree of fault current asymmetry, the theoretical worst-case condition is a non-simultaneous unearthed fault. As an example, this fault can be a line-to-line short-circuit at voltage zero across two phases which after 90° becomes a three-phase fault at line-to-earth zero voltage in the third phase. This non-simultaneous fault inception produces the theoretically highest DC component of 136,6 %, i.e. it is 36,6 % higher than that of a simultaneous three-phase fault at line-to-earth voltage zero.

B.2.3 Fault location

The conditions for the occurrence of fully asymmetrical fault currents are closely linked to the resulting time constant of the DC component $\tau = L/R$, i.e. mainly to the ohmic resistance of the short-circuit path. Therefore, to be able to assess the interrupting capability of circuit-breakers in this particular case, only fault currents supplied by generators which – together with their transformers – account for the smallest X/R ratios, should be taken into consideration.

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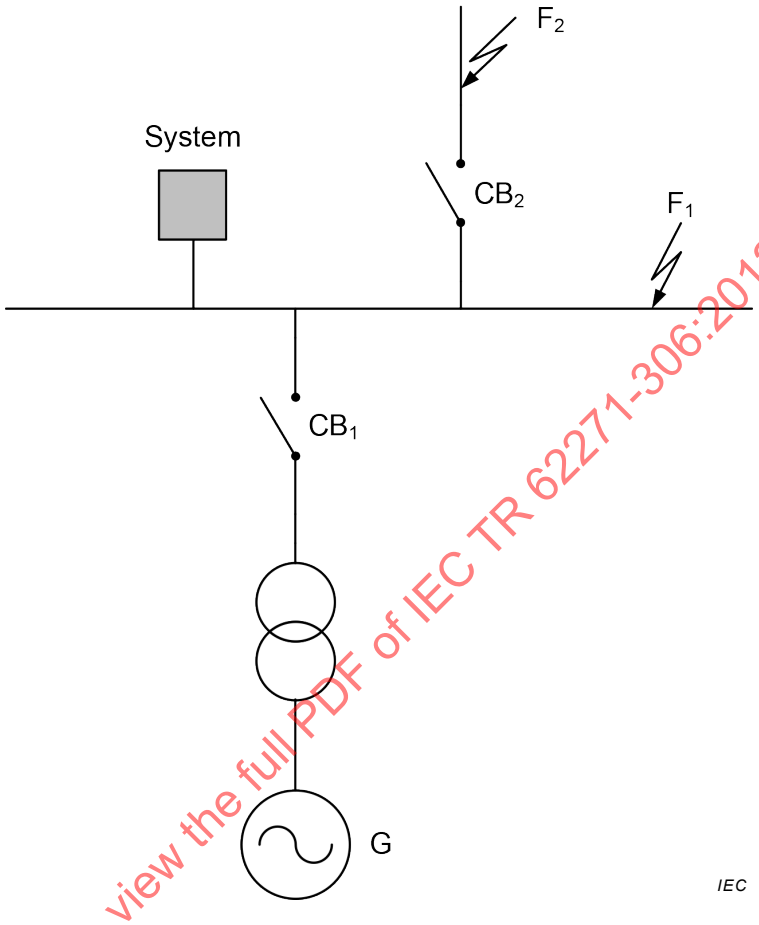
In the case of a fault that is being fed from a generator and also from the network via a transmission line, the total fault current is not likely to be fully asymmetric because of the relatively high ohmic resistance of the line or cable.

In the single-line diagram in Figure B.1 only faults at location F_1, which circuit-breaker CB_1 has to interrupt, should therefore be taken into account. Fault currents at location F_2 with its circuit-breaker CB_2 are subject to normal current zeros



Key

F_1, F_2: Fault locations

CB_1,CB_2: Circuit-breakers

G: Generator

Figure B.1 – Single-line diagram of a power plant substation

B.2.4 Effect of the generator operating conditions

B.2.4.1 Underexcited operation of the generator

With respect to current asymmetry the maximum stress on the circuit-breaker is determined by the generator loading as well as by the particular instant of fault inception. In underexcited operation, when the generator produces active power and consumes reactive power, not only does the initial value of the DC component becomes larger than that of the AC component, but the time constants and reactances of the generator transverse axis, which are more unfavourable than those of the longitudinal axis, also affect the variation of the AC component.

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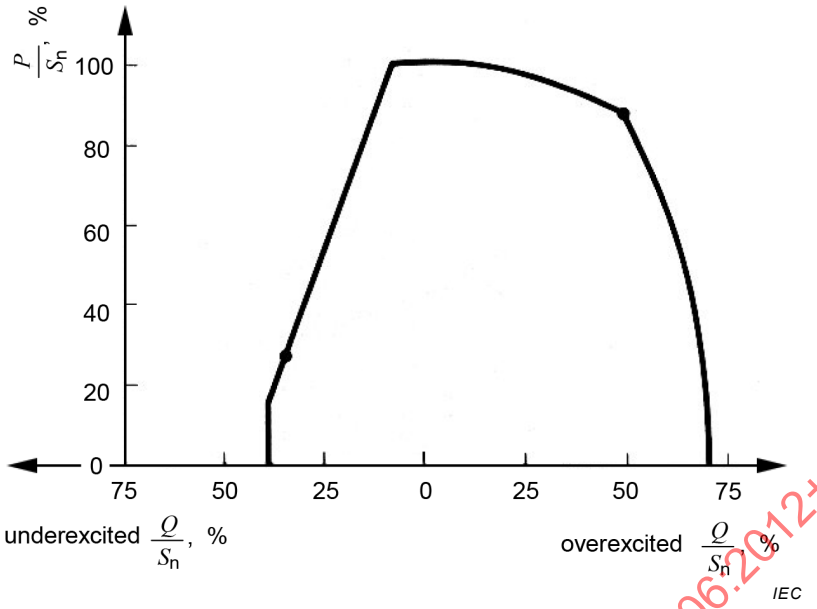
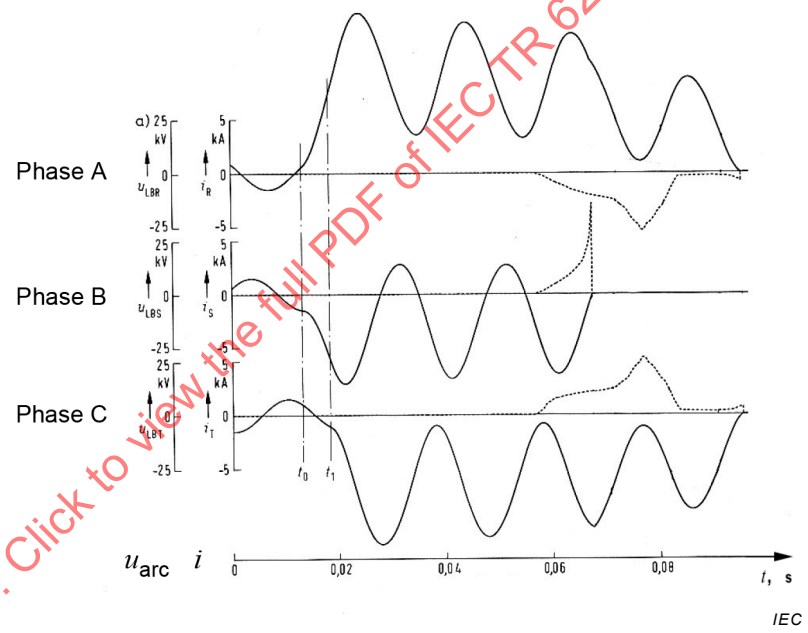


Figure B.2 – Performance chart (power characteristic) of a large generator



Key

t_0: two-phase fault at phase-to-phase voltage zero

t_1: transition to three-phase fault at third phase voltage zero

Figure B.3 – Circuit-breaker currents i and arc voltages u_{arc} in case of a three-phase fault following underexcited operation: non-simultaneous fault inception

For a generator taken as an example with an initial load of P = 30 % and Q = −35 % in accordance with the performance chart in Figure B.2 was found to be particularly critical.

Calculated currents and arc-voltages for non-simultaneous and simultaneous unearthed fault inception under these conditions are shown in Figure B.4 and Figure B.5. As there is no arc voltage involved during the first 55 ms, these currents (at 50 Hz) can be considered inherent for the initial 55 ms.

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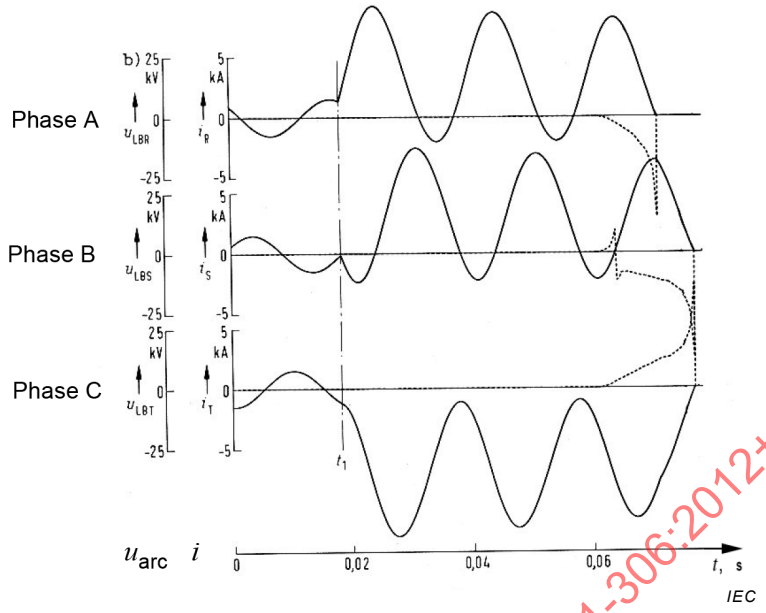

Figure B.4 – Circuit-breaker currents i and arc voltages u_{arc} in case of a three-phase fault following underexcited operation: Simultaneous fault inception at third phase voltage zero

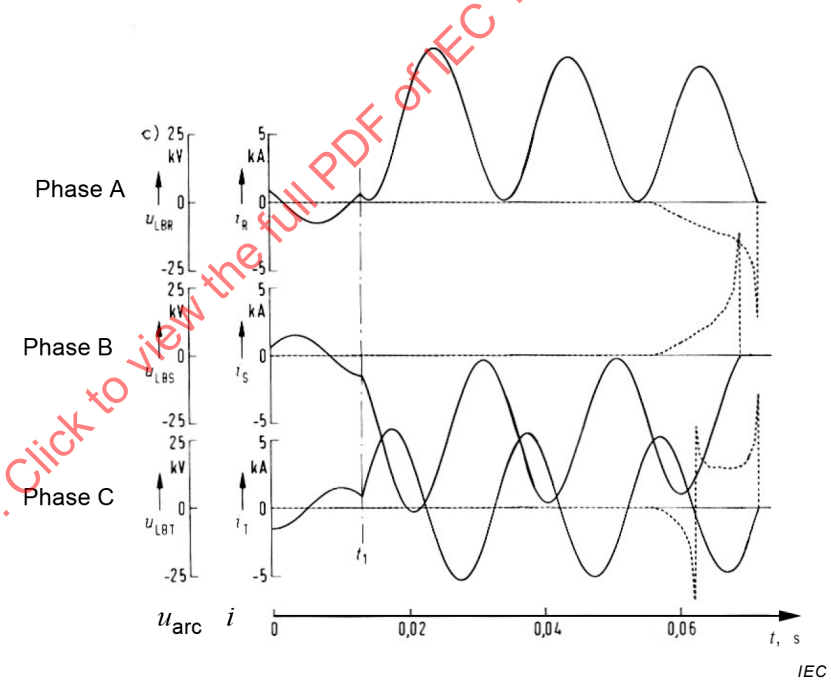

Figure B.5 – Circuit-breaker currents i and arc voltages u_{arc} in case of a three-phase fault following underexcited operation: Simultaneous fault inception at third phase voltage crest

In Figure B.3, the initially two-phase fault occurred across the upper two phases at time t_0. The third phase was subjected to the now three-phase fault at time t_1. It can be seen that a further DC component is added in the first phase to the DC component of the two-phase fault current resulting in an asymmetry of the current in this phase of more than 100 %.

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In the second phase, current zeros continue to occur, while the DC component in the third phase is, also, above 100 %, but not as high as in the first phase.

For a given SF_6 circuit-breaker, the arc voltage of which has been determined experimentally, it has been assumed that an effective arc voltage appears between the opening contacts 55 ms after fault inception. This takes into account the time until contact separation and some milliseconds for the development of the full gas flow. The current in the second phase is interrupted at the next current zero. Consequently, a phase shift takes place in the AC and in the DC components in the other phases: the DC component in the first phase decreases, while it increases in the third phase there, leading to an even higher current offset. However, due to the effect of the arc voltage, which acts as an additional resistance R_a and thus reduces the momentary value of the DC time constant to $\tau = L/(R + R_a)$, the currents are forced through zero in the first and third phase, as well, and are interrupted.

Figure B.4 and Figure B.5 show simultaneous unearthed faults which occur at time t_1. The DC components are less pronounced and the interruption takes a similar course as described for Figure B.3.

The arc voltage will also cause the fault currents to pass through zero in the event of a generator transformer fault (Figure B.6) but with the conditions otherwise the same as in Figure B.3.

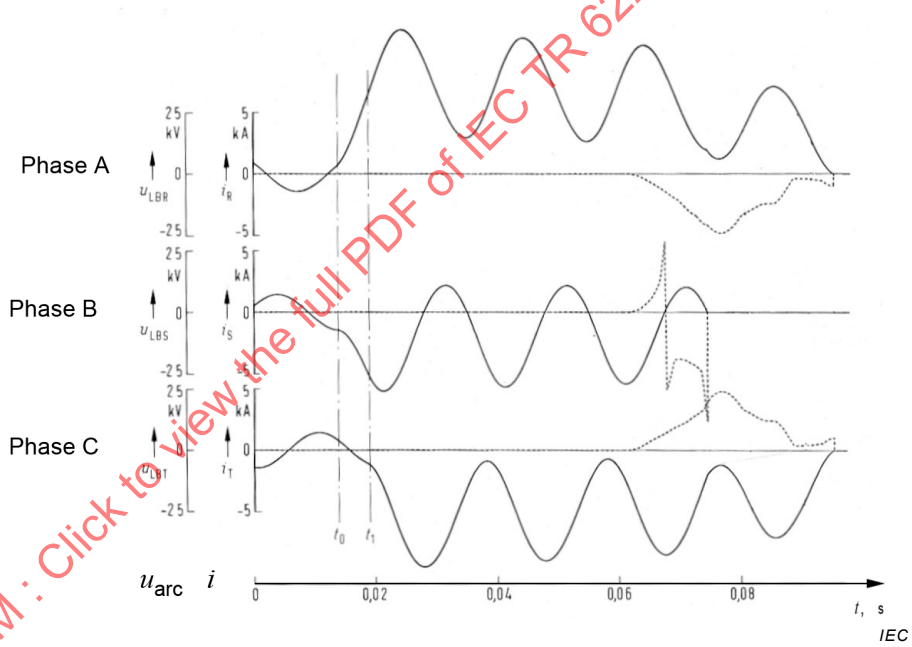

Figure B.6 – Circuit-breaker currents i and arc voltages u_{arc} under conditions of a non-simultaneous three-phase fault, underexcited operation and failure of a generator transformer

B.2.4.2 Overexcited operation of the generator

Fault clearance following overexcited loading of the generator, i.e. active-power and reactive-power output, subjects the circuit-breaker to lower stresses (Figure B.7). The maximum displacement of the currents from the zero line under fault conditions following full load operation is much smaller than that of the currents due to underexcited operation (Figure B.3).

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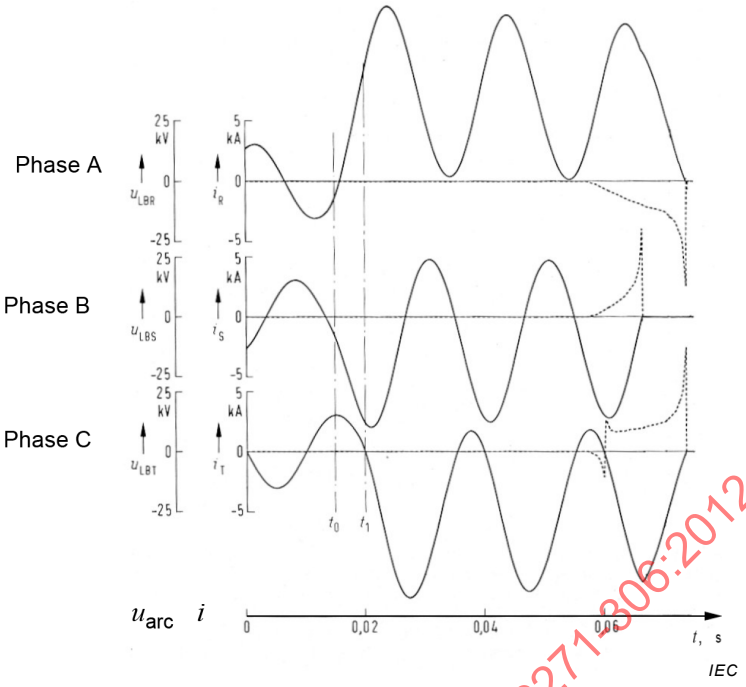

Figure B.7 – Circuit-breaker currents i and arc voltages u_{arc} under conditions of a non-simultaneous three-phase fault following full load operation

B.2.4.3 No-load operation of the generator

The calculated currents and arc voltages due to a non-simultaneous fault developing from no-load operation of the generator are shown in Figure B.8. As in the case of a fault following full load operation (Figure B.7), the displacement of the currents from the zero line is smaller than for underexcited operation.

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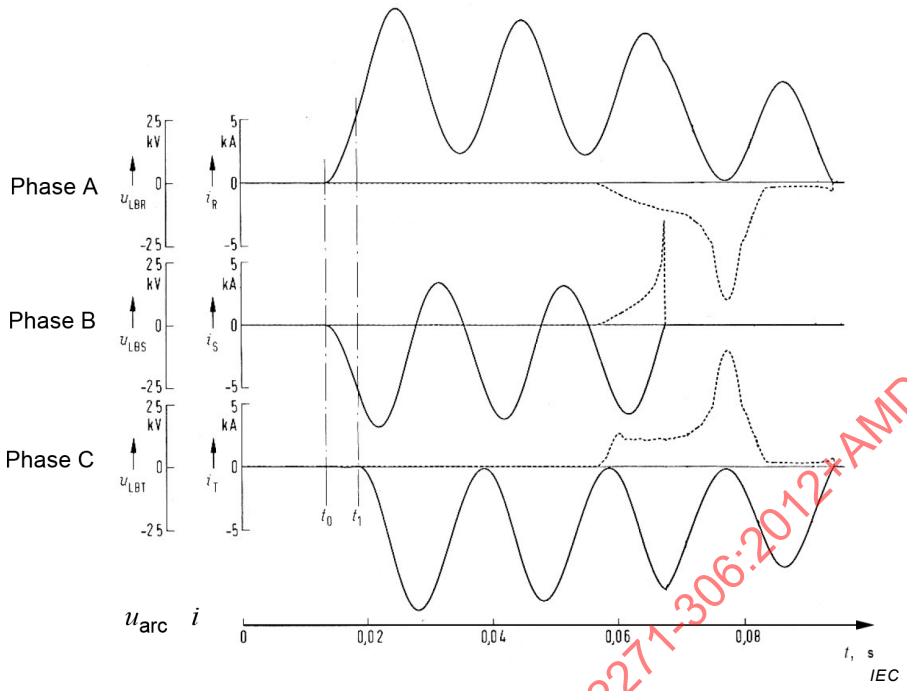

Figure B.8 – Circuit-breaker currents i and arc voltages u_{arc} under conditions of a non-simultaneous three-phase fault following no-load operation

B.2.4.4 Generator-source short-circuit

Delayed current zeros occur, if depending on the specific generator reactances and time constants, the AC component of the short-circuit current can decay faster than the DC component, which therefore exceeds 100 %.

Such a particular characteristic is basically observed at generators bigger than 50 MVA.

The worst case of delayed current zeros represents a bolted terminal fault, without involving of any free-in-air burning arc. Such a situation can occur when the circuit-breaker closes onto a closed earthing switch. Under this condition, only the arc voltage of the interrupter represents a resistance in the system, which damps the DC component and forces the current zeros earlier. Generally, the arc voltage of SF_6 interrupter can be up to 1 000 V, of vacuum interrupter only few tens of V. The arc resistance of vacuum interrupter is considerably lower.

B.2.4.5 Unsynchronized closing

It can be seen from Figure B.9 that not only fault conditions but also attempting to synchronize at an unsuitable differential angle may cause the current zeros to be delayed. Owing to the mean electrical moment which thereby occurs and the resulting speed variation the currents can be constricted to such an extent that they may no longer pass through zero in any of the phases. However, this does not occur until after a prolonged period because of the much higher mechanical time constants. Should the circuit-breaker operate in this constriction range, it still can interrupt the current due to the higher arc voltage as shown in Figure B.9.

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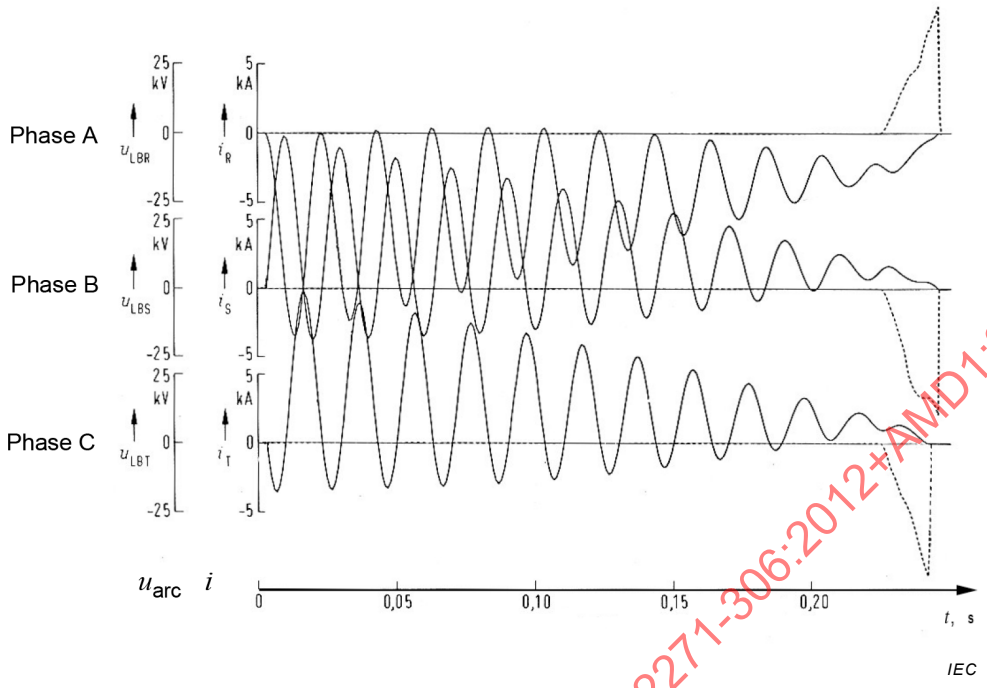

Figure B.9 – Circuit-breaker currents i and arc voltages u_{arc} under conditions of unsynchronized closing with 90° differential angle

During connection of the generator to the system or due to loss or lack of synchronism after a fault in the system, an out-of-phase current may appear across the circuit-breaker. The phase angle difference between rotating voltage phasors on each side of the circuit-breaker may reach full phase opposition at 180°. However, as this operation could be performed by the circuit-breaker on the high-voltage side of the step-up transformer, the out-of-phase switching duty is specified at 90° phase angle and a current corresponding to 50% of the rated short-circuit current (see Figure B.10).

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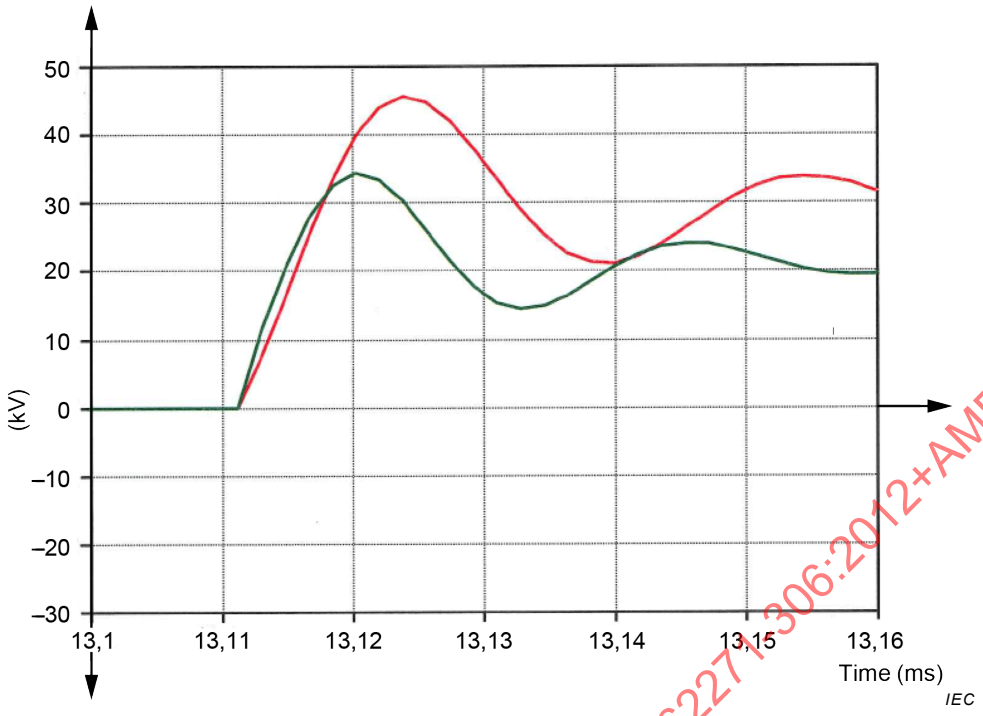

Figure B.10 – Comparison of TRV test curve for out-of-phase (red) and system-source short-circuit (green)

B.2.5 Proof of performance

B.2.5.1 Testing

Normally, testing of a high-voltage circuit-breaker under these conditions can only be carried out single-phase, i.e. on the circuit-breaker pole with the highest DC component. To produce DC components greater than 100 % for several cycles, the test circuit should have a high X/R ratio giving a DC time constant of possibly several hundred ms. The test voltage should be at least as high as the rated phase voltage, or in the case of unit testing, as high as the rated voltage across the most highly stressed interrupter for the first-pole-to-clear in an unearthed fault or the last phase-to-clear in an earthed system. The AC component of the test current has to cover the AC component of the short-circuit current of the generator considering the conditions stated in B.2.2 and B.2.3.

In practice, the test procedure in order to subject one pole to a short-circuit current with delayed current zeros is as follows (Figure B.11, Phase A).

In most cases the tests are made single-pole on one interrupter unit. The first two phases of the test circuit are switched in by a make-switch when their phase-to-phase voltage passes through zero. The third phase is switched in a quarter cycle later. By varying the delay of the making in the third phase, the amount of asymmetry of the short-circuit current can be adjusted. Figure B.11 shows the oscillogram of the current not affected by the arc, i.e. the inherent current of the test circuit. It can be seen that at the transition to the three-phase circuit a further DC component is added to the DC component of the two phase current with the effect that the current in phase A is displaced by more than 100 %. The short-circuit generators should not be superexcited to delay the current zero by several cycles due to the decaying AC component.

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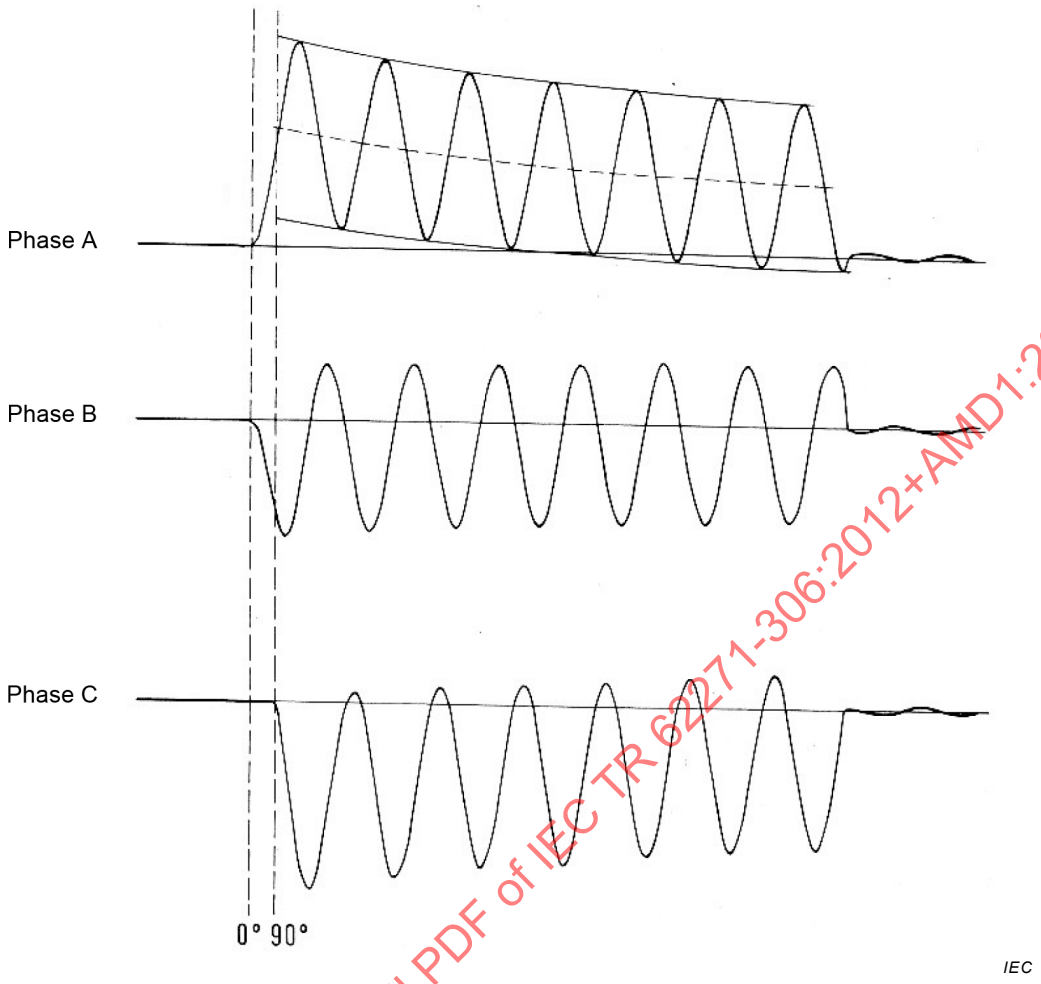

Example:

Test voltage: 70 kV

Test current: AC component: 2,63 kA r.m.s.

Current peak: 8,5 kA

1st current minimum: 850 A

2nd current minimum: 450 A

3rd current minimum: 260 A

Figure B.11 – Prospective (inherent) current

The contacts of the test breaker should be set to part about 1 ms after the initial inception of the current flow. Thus, the test circuit-breaker is subjected to the maximum asymmetrical current after contact separation. The arcing time is then varied systematically in order to determine the minimum and maximum times for each AC current and voltage step.

B.2.5.2 Calculation of the performance of a circuit-breaker

The arc characteristics measured during the tests are converted into a mathematical model in order to obtain details about the interrupting capability of the circuit-breaker in other situations or under the varied fault conditions, respectively. The model should be a true representation of the arc voltage variation from contact separation until arc extinction. The instantaneous values of the currents and corresponding arc voltages, which were taken from actual test oscillograms, produce the distribution of dots shown in Figure B.12 together with the mean tolerance band. The wide variation of the readings results from the instable and rather inconsistent arc behaviour.

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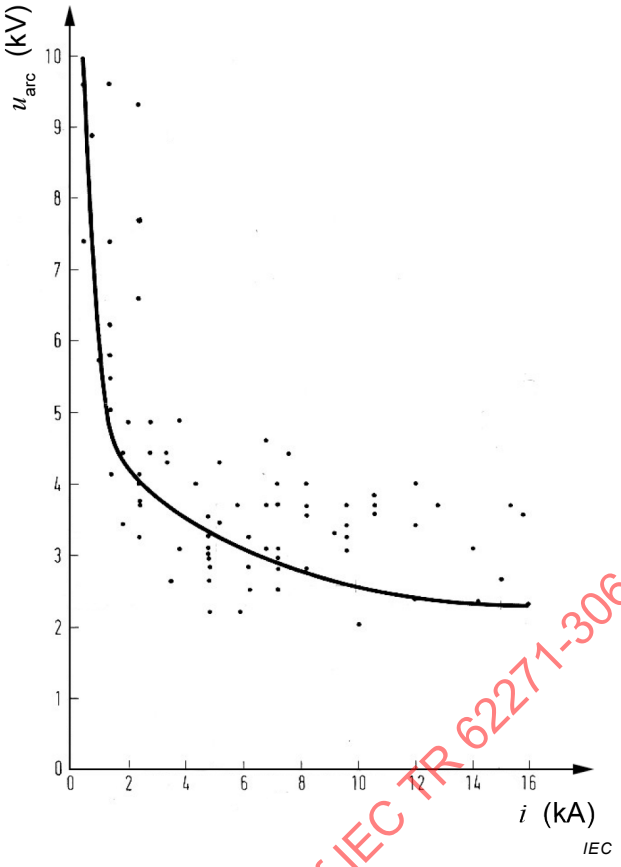

Figure B.12 – Arc voltage-current characteristic for a SF_6 puffer type interrupter

In addition to the voltage-current characteristic of the arc, the variation of the gas pressure in the arcing chamber, the extension of the arc by the gas flow and the contact distance, which rises with the arcing time should be taken into account. These circuit-breaker characteristics can be expressed mathematically by a standardized assessment function $e(t)$ with a maximum value of 1 (Figure B.13). Strictly speaking, this function has no physical significance.

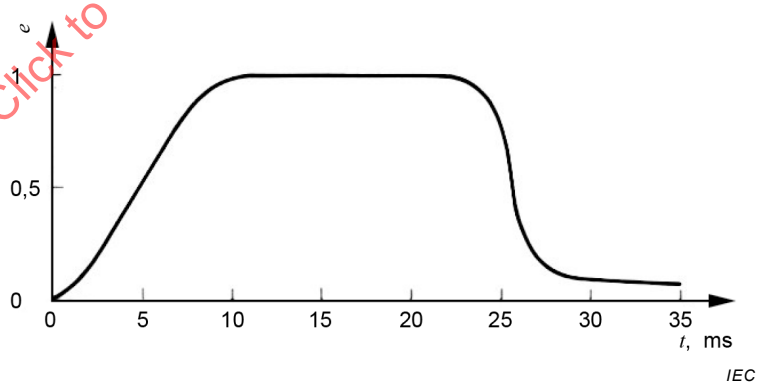

Figure B.13 – Assessment function $e(t)$

The total function of the arc voltage – as a function of time, the circuit-breaker characteristics and the instantaneous current value – is obtained by multiplying the individual functions shown in Figure B.12 and Figure B.13.

$$u_{arc}(t, i) = u_{arc}(i) \times e(t)$$

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Using this total arc voltage function u_{arc}, the arc drawn between the opening contacts may be regarded as a non-linear ohmic resistance, which mainly reduces the DC time constant of the fault current, while the AC component remains unaffected.

Other methods of calculation have also been developed to compare testing and simulation [125] and [140].

B.2.6 Distributed generation and large motors

In distribution voltage systems fault currents with delayed zero crossings may occur either in the proximity of a concentration of generation, or when switching-off large high-voltage motors, or in a combination of both. Even vacuum circuit-breakers with their relatively low arc voltage are well suited to clear under these conditions, provided they are designed to withstand the high-current peak values associated with such faults. Also, their contact configuration should be able to withstand prolonged arcing. In any case, it will be necessary to investigate the conditions of the particular application to determine the actual stress upon the circuit-breaker.

B.2.7 Conditions for fault currents with delayed zeros

In distribution voltage networks with an extremely large concentration of generation and motor load, the probability that short-circuit currents with a DC component well above 100 % will occur is even higher than in high-voltage systems. The DC time constant τ may be in the order of some hundreds of milliseconds. This means the current in at least one phase will have no current zeros for several cycles.

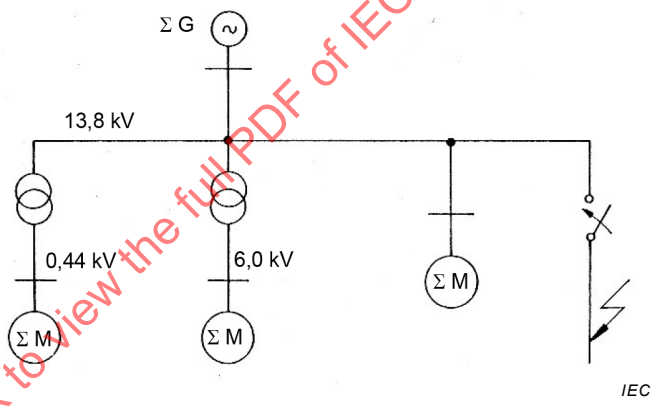

Figure B.14 – Network with contribution from generation and large motor load

If large high-voltage motors are present short-circuits with delayed current zeros will not only occur due to a non-simultaneous fault, but they are even possible in case of a simultaneous (bolted) fault (Figure B.14). If there is a fault the motors act as generators and feed back into the system a current with a high DC component. As they are slowing down, they will gradually become out-of-phase with respect to the feeding system. The frequency of the current generated by the motors will drop below the generator frequency. As Figure B.15 shows, even if the short-circuit current from the generators has current zeros, the superposition of the current generated by the motors results in a total short-circuit current with delayed current zeros.

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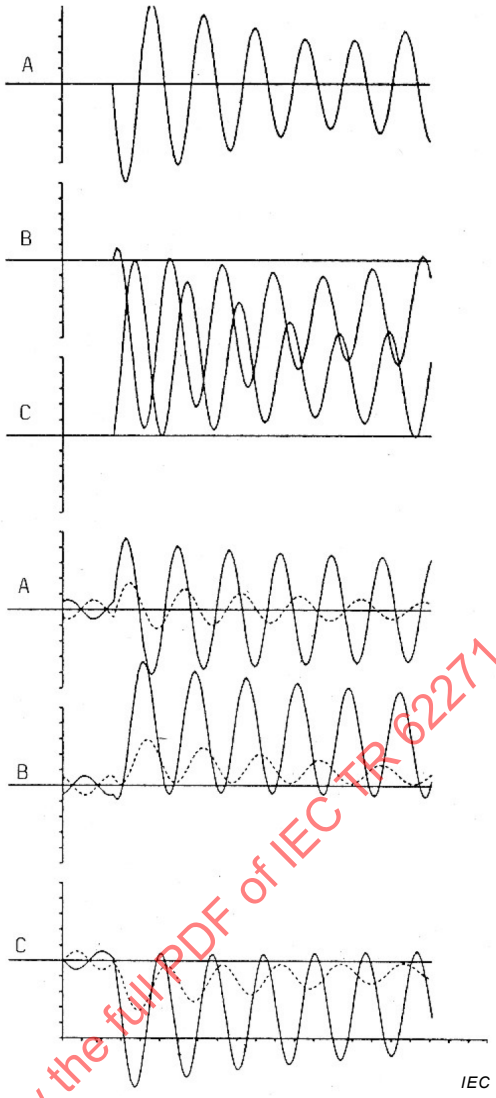

Key

Upper traces: Total fault current.

Lower traces:

– solid lines: generator fault current, DC time constant τ = 180 ms

– dotted lines: fault current generated by the motor

Figure B.15 – Computer simulation of a three-phase simultaneous fault with contribution from generation and large motor load

From Figure B.15 it can be determined that the probability of occurrence of a short-circuit current with delayed zeros is higher if the generator short-circuit current has a large DC component with a long DC time constant. This is the case if the fault location is close to the generators. If generation and motor load are located close to each other, the damping of the short-circuit current DC component is particularly low and the conditions assumed in Figure B.15 are met. Typical examples are offshore oil platforms where generation and load may be in the order of or even above 50 MVA and the connections are short, and industrial plants, which may be run in certain parts on their own power supply.

In industrial plants that are fed via transmission lines or cables, these lines or cables act as damping elements for the DC component, and the resulting total fault current most probably has zeros in all three phases continuously from the fault inception.

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B.2.8 Three-phase interruption of currents with delayed zeros

The evaluation whether a three-phase operated circuit-breaker is able to interrupt a fault current with delayed zeros should be done on a three-phase basis.

The sequence of a three-phase interruption may be shown taking a non-simultaneous fault in an unearthed system as an example. Consequently, the AC components and the DC components in the three phases add up to zero, respectively.

To cover the extremes, it is considered that the short-circuit may occur at voltage zero as well as at voltage crest of one phase. The vector diagrams Figure B.16 and Figure B.17 show the AC and DC components of the currents in all phases at inception of the three-phase fault and after the interruption by the first-pole-to-clear. The AC components of the three-phase current are normalized to 1 p.u. and their decay is neglected in the vector diagrams. Likewise, no decay of the DC components is taken into account.

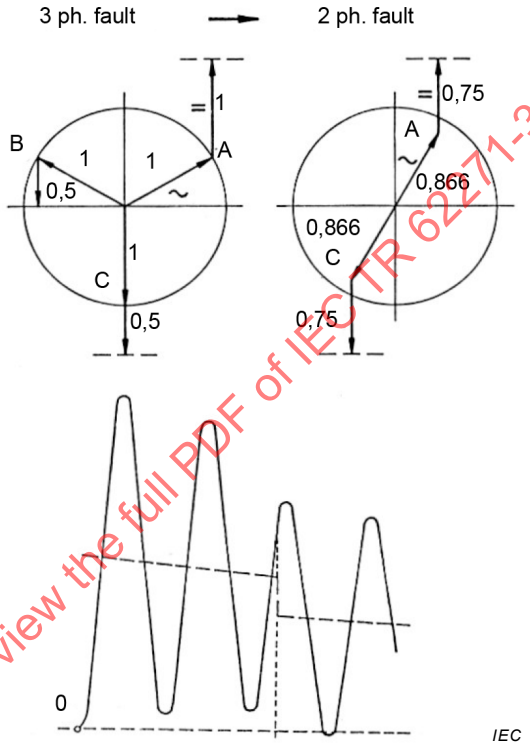

Figure B.16 – Short-circuit at voltage zero of phase A (maximum DC component in phase A) with transition from three-phase to two-phase fault

If a short-circuit occurs at voltage zero, one phase has the maximum possible offset. This is considered to be phase A in Figure B.16, with a DC component of ±1 p.u. Consequently, the DC components in the two other phases are -0,5 p.u. In these phases, there are always current zeros giving the corresponding circuit-breaker poles the possibility to clear. After interruption of the first phase (e.g. by pole B), there is a phase shift in the remaining two phases: their AC components become ±0,866 p.u. and their DC components ±0,75 p.u. Even the originally fully offset phase will have current zeros now and all circuit-breaker poles are able to clear.

Generally speaking, in the case of a fault at voltage zero, this phase shift will lead to a reduction of the DC component in the most offset last phase. In most cases, there will be current zeros now also and the two last-to-clear poles are able to interrupt as well. Even if there are no current zeros immediately after the phase shift, the current offset is reduced, leading to current zeros after one or two further cycles.

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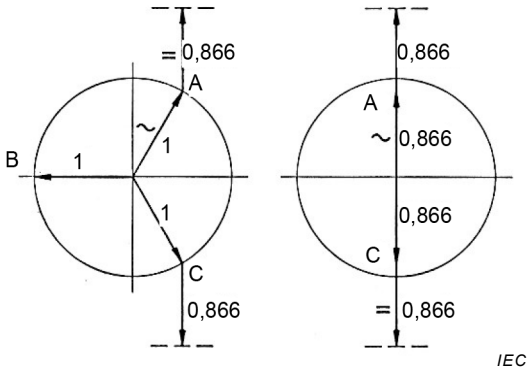

Figure B.17 – Short-circuit at voltage crest of phase B (phase B totally symmetrical) and transition from three-phase to two-phase fault

In the case of a short-circuit at voltage crest, the current in one phase will be totally symmetrical (phase B in Figure B.17). The other two phases then have a DC component of ±0,866 p.u. Accordingly, as long as this is a three-phase short-circuit, all phases have current zeros. If the symmetrical current in phase B is interrupted first, the phase shift will change the AC components in the other two phases to ±0,866. The DC components in those phases remain unchanged. This means that the AC and DC components have equal amplitudes and the current will now only touch the zero line.

To determine whether a circuit-breaker is able to clear such a fault, it is therefore important to consider how the AC components and the DC components develop during the short-circuit. Both decay in a different manner. The AC components consist of a subtransient and a transient short-circuit current. While the subtransient short-circuit current decays with a time constant of 20 ms to 30 ms, the transient time constant may be in the order of several hundred milliseconds, even up to some seconds. The DC component has a time constant $\tau = L/R$ which is determined by the reactance and the resistance of the faulted circuit, including the generators, transformers and switchgear. On oil platforms, it often has a value between 200 ms and 300 ms.

Depending on the load conditions of the generators, i.e. on their state of excitation before fault inception, the AC component may decay more rapidly than the DC component. Especially if the subtransient AC short-circuit current is of great significance the amplitude of the AC component may have become smaller than that of the DC component by the time the first phase is cleared. In that case, there will be no current zeros in the one or two more offset last phases. The arc in these two circuit-breaker poles will now have to burn for another one or two cycles. As even the relatively small arc voltage of vacuum circuit-breakers contributes to the reduction of the DC time constant, the DC components will decrease further and current zeros will occur again giving the circuit-breaker chance to finally interrupt.

Therefore, of the two conditions of fault inception, the three-phase short-circuit at voltage crest might be considered more severe for three-phase interruption as there may be a possibility for the last-poles-to-clear only with prolonged arcing. However, a short-circuit at voltage zero will stress a circuit-breaker with a higher DC component and thus with an overall higher current peak. These considerations show that each circuit configuration has to be regarded individually in order to determine the critical stress imposed upon the circuit-breaker. Above all, it is necessary to evaluate, at the moment of contact separation, the amplitudes of the AC and the DC component and their time constants.

B.2.9 Application of circuit-breakers for clearance of delayed current zeros

As pointed out already, the application of circuit-breakers other than generator circuit-breakers for the clearance of faults with delayed current zeros is based upon the assumption that these circuit-breakers will always be three-pole operated. Accordingly, all analytical considerations and tests have to be carried out on a three-phase basis.

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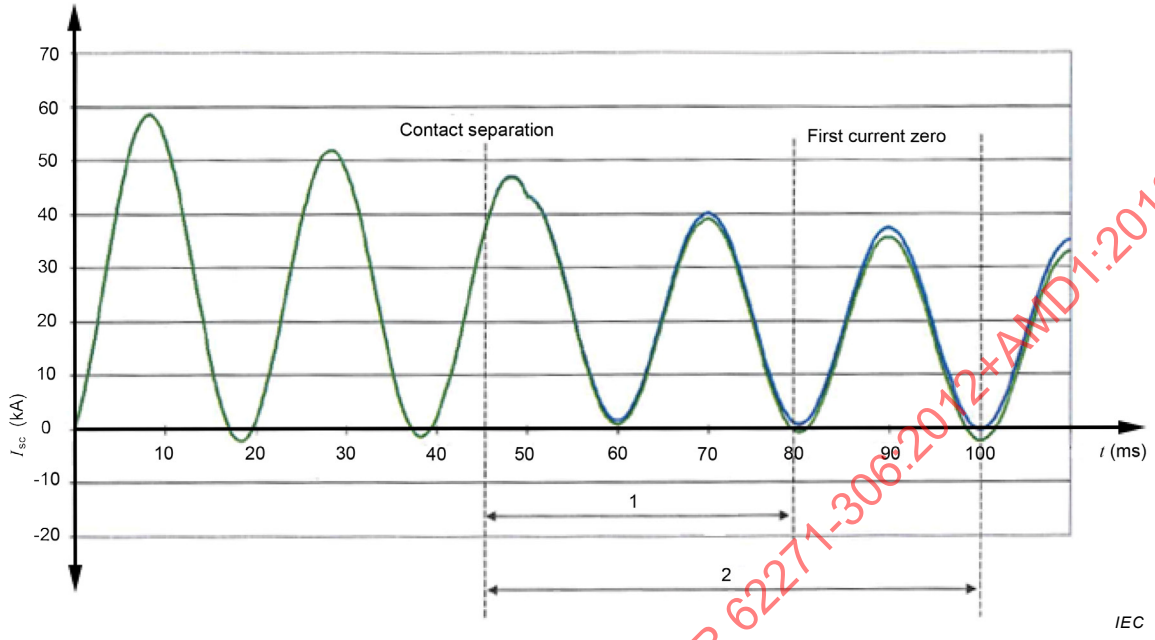
Although the arc voltage, as for vacuum circuit-breakers, may only be in the order of about 100 V, experience shows that it has a non-negligible effect upon the decay of the DC component.



1 t_{arc} = 36 ms and $\int (I_{sc} \times t)\mathrm{d}t = 849$ As

2 t_{arc} = 56 ms and $\int (I_{sc} \times t)\mathrm{d}t = 1\,252$ As

Figure B.18 – Comparison of current zero crossing with (green) and without (blue) influence of arc voltage

When tested according to IEC 62271-100, the circuit-breaker has to clear a symmetrical short-circuit current or a short-circuit current with a DC component of some tens of percent at a moment when the power frequency recovery voltage is at its crest or near to it. This leads to a transient recovery voltage with a relatively high peak value. In the case of a short-circuit current with a very high DC component, the moment of current zero almost coincides with the moment of voltage zero of the power frequency recovery voltage. Thus, the transient recovery voltage stress immediately after current interruption becomes relatively low.

A circuit-breaker suited to clear faults with delayed current zeros should be able to make and withstand very high current amplitudes due to the DC components in the order of 130 %. Also, the contacts should be able to withstand thermally arc durations of two or even three cycles and still interrupt a fully offset short-circuit current. Consequently, it is advisable to use in such case a circuit-breaker with a higher short-circuit current rating than that suggested by the particular application.

According to test experience, the contacts designed to absorb the energy connected with the breaking of such rated short-circuit currents without being overheated are most likely capable of withstanding the arc duration required to clear under the conditions of delayed current zeros.

B.2.10 Testing

To demonstrate the capability of circuit-breakers other than generator circuit-breakers to withstand and to clear faults with delayed current zeros, three-phase tests should be carried out in a similar circuit as described in B.2.6.1. The test circuit parameters (test voltage,

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frequency, TRV) should correspond to those rated for a system of the particular application. The tests should cover both conditions as described in B.2.9:

a) with the maximum DC component in one phase, i.e. one phase fully offset, corresponding to a short-circuit occurring at voltage zero;

b) with practical no DC component in one phase, i.e. one phase fully symmetrical, corresponding to a short-circuit occurring at voltage crest.

To achieve the maximum offset current with a large DC time constant, a special sequence has to be chosen in producing a three-phase non-simultaneous short-circuit (see B.2.6.1). Two phases are switched in when their phase-to-phase voltage passes through zero. The third phase is closed a quarter cycle later. By varying the delay of the making in the third phase, the amount of asymmetry of the short-circuit current can be adjusted. The short-circuit generator should not be superexcited.

B.3 Conditions for delayed current zeros on transmission networks

B.3.1 General

Over the last few years several failures of high-voltage SF_6 circuit-breakers have been reported around the world because of delayed current zeros on highly shunt compensated transmission lines.

System simulations performed by utilities confirm the phenomenon, which is present on a healthy phase in the following network conditions:

- shunt compensation of 50 % or more of a high-voltage transmission line;
- presence of a single-phase fault during three-phase line energisation;
- closing at or near voltage zero.

It has been shown that when these three conditions are met, the healthy phases can be exposed to a DC offset of several 100 A.

B.3.2 Example of field measurements

Figure B.19 illustrates a CO operating cycle where an air-blast circuit-breaker closes into a fault during energization of a 400 km highly shunt-compensated 735 kV transmission line.

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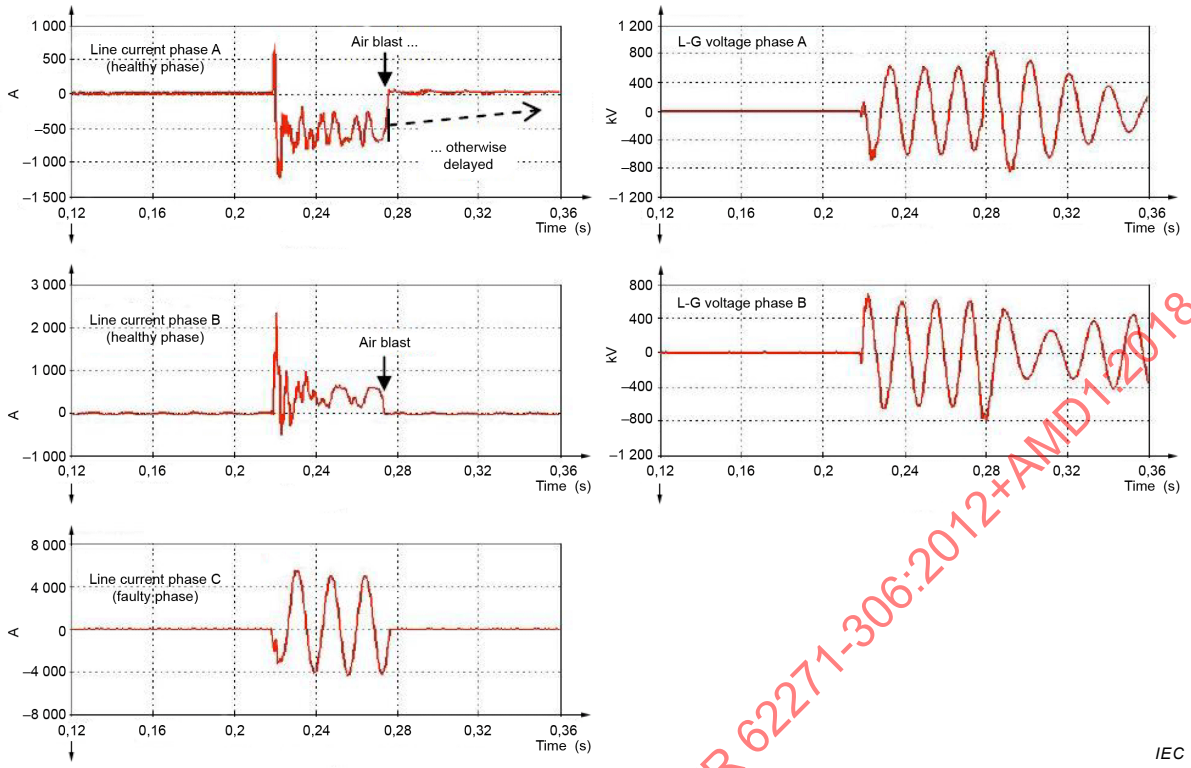

Figure B.19 – Recording of delayed current zero on A and B phase in the presence of a line-to-earth fault on C phase

B.3.3 Influence of arc voltage on the ability of the circuit-breaker to force a current zero

In the example given in Figure B.19, the air-blast circuit-breaker, owing to its high arc voltage, has the ability to force a current to zero and interrupt the current. Simulations have shown that a standard SF_6 circuit-breaker, because of its much lower arc voltage and blast time, would not have the capability to force a current zero.

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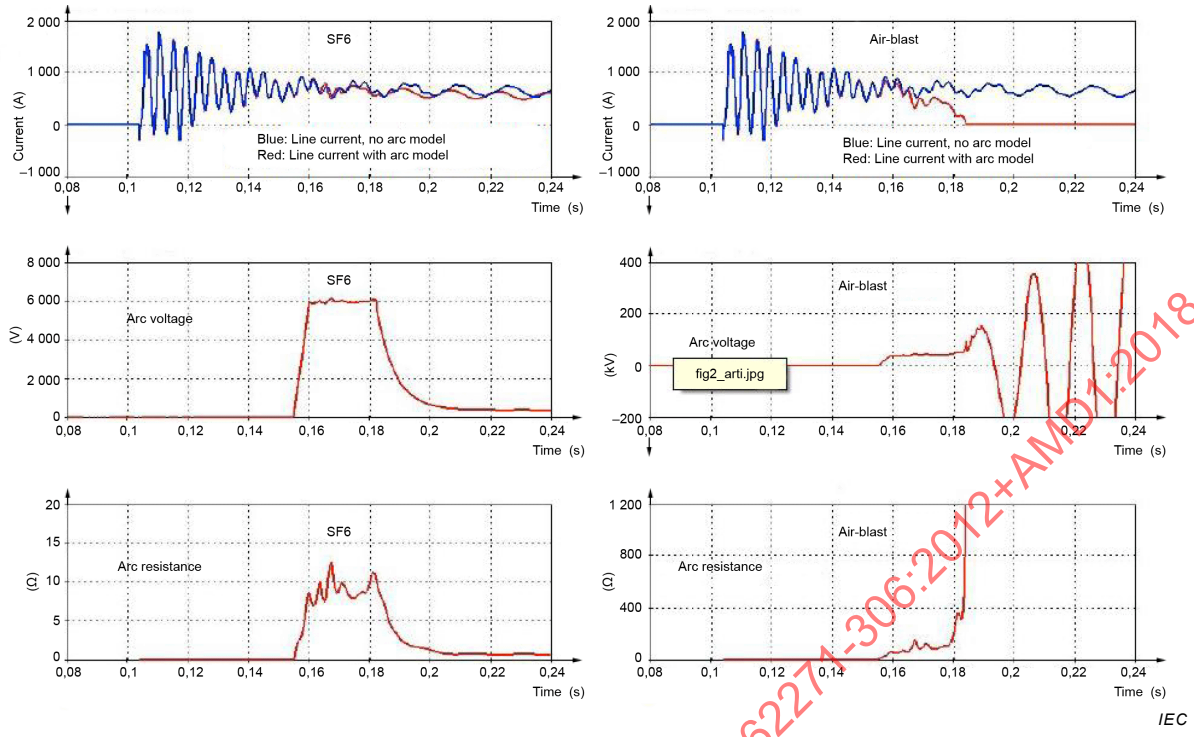

Figure B.20 – Influence of arc voltage of SF_6 vs. air-blast circuit-breaker

Figure B.20 illustrates the influence of arc voltage on the ability of the circuit-breaker to force a current zero, on the left for a 735 kV SF_6 circuit-breaker (4 series connected breaks per phase) and on the right for a 735 kV air-blast circuit-breaker (8 series connected breaks per phase). Typically the arcing voltage of an SF_6 interrupter is 5 times less than that for an air-blast circuit-breaker.

B.3.4 Mitigation techniques

B.3.4.1 Mitigations techniques to be considered when using SF_6 circuit-breakers

Simulations have shown that different mitigations techniques may be applied to force the current to zero such as insertion of a resistance between the reactor neutral and earth on the low voltage side of the shunt reactor winding. Figure B.21 illustrates the results of the simulation.

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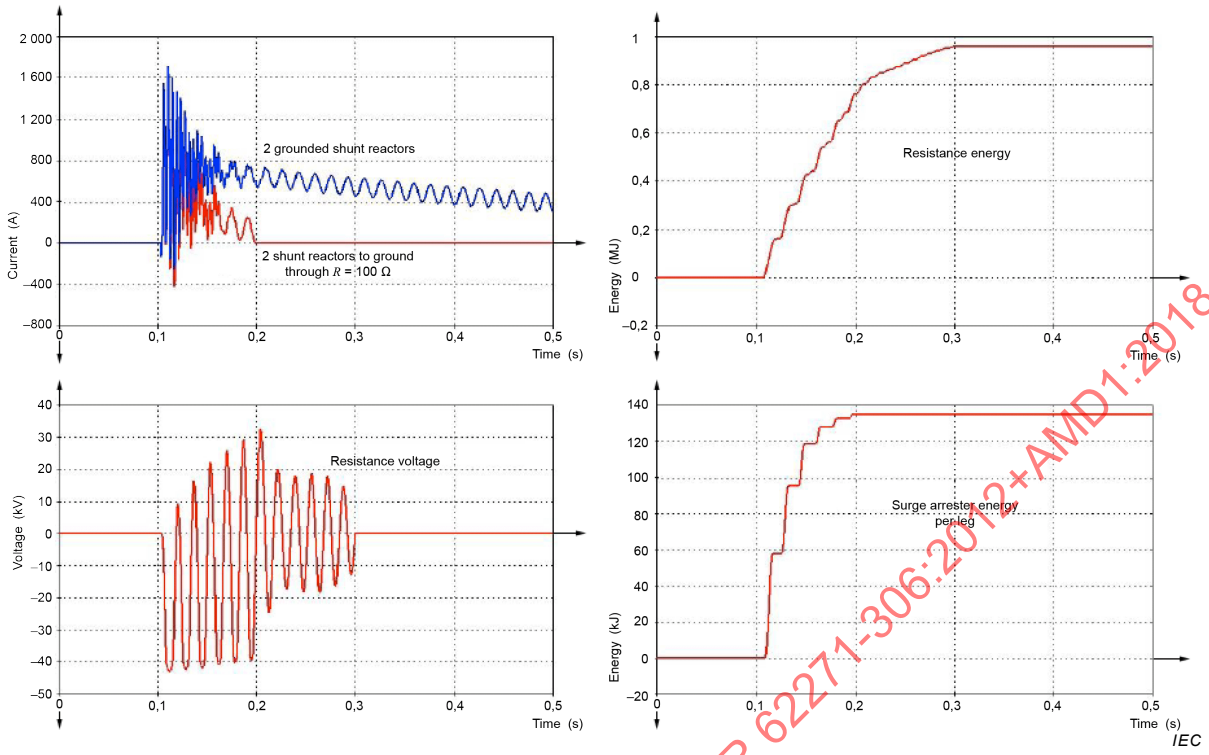

Figure B.21 – Earthing of the shunt reactor using a 100 Ω resistor for 200 ms insertion time

Another mitigation technique, which requires controlled closing at voltage peak, can eliminate the delayed current zero crossings, but remains risky because of increased switching transients.

Pre-insertion resistors can be used to mitigate the DC offset. The resistance value and the pre-insertion time used need to be evaluated on a case-by-case basis.

B.3.4.2 Possible modifications to SF_6 circuit-breaker design

In the past, circuit-breaker manufactures have developed SF_6 circuit-breakers that were capable of interrupting delayed current zero for series compensated applications or generator applications. Techniques, which include prolonged blast times or increased arc length during current interruption, can help meet this goal.

B.3.5 Testing of an SF_6 circuit-breaker capable of delayed current zero interruption

There are no requirements to demonstrate the capability of an SF_6 circuit-breaker to interrupt a current with delayed zero crossings. Testing has to be considered on a case-by-case basis.

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Annex C
(informative)

Parallel switching

Void

C.1 General

Parallel switching occurs when two or more circuit-breakers are tripped to interrupt a shared fault current. This is typically the case for such bus arrangements as double breaker, breaker-and-a-half, breaker-and-a-third and ring buses. Ideally, all of the circuit-breakers should interrupt at the same current zero and this would probably be the case if all circuit-breakers were of the same type and technology, and contact parting was simultaneous. In reality, the evolution of circuit-breakers has resulted in different circuit-breaker types and technologies being mixed quite randomly as stations are extended.

The purpose of this annex is to examine this switching case and to relate it to oil, air-blast, SF_6 and vacuum circuit-breakers operating in parallel in various combinations. Experience indicates that parallel switching is not so much an issue of concern but it is a frequently asked question and the purpose of this annex is to provide a better understanding of the switching duty. In this context it is important to note that circuit-breakers do not have a parallel switching rating but rather a certain inherent capability for the duty. Parallel switching is influenced primarily by circumstances relating to the progressive development of circuit-breakers and their actual application by and under the control of the users. It is therefore a user matter and this annex provides guidance as to how the user can assess parallel switching with the necessary technical support from the circuit-breaker manufacturers. Note that parallel switching should not be confused with evolving faults, the latter being a different phenomenon.

C.2 Circuit-breaker characteristics

Parallel switching is influenced by the types of circuit-breakers involved and their respective characteristics as follows:

- relative mechanical opening times;
- relative current levels;
- relative arc voltages;
- relative arcing windows;
- system and local impedances.

However, as will become apparent in C.3, the factors that need to be considered are the relative mechanical opening times, the relative arc voltages and to some degree the system and local impedances. Experience shows that the ranking of mechanical opening times from fastest to slowest most probably is as follows:

a) air-blast circuit-breakers;

b) SF_6 circuit-breakers;

c) oil circuit-breakers;

d) medium voltage circuit-breakers of all types.

The ranking of arc voltages from highest to lowest is as follows:

a) air-blast circuit-breakers;

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b) oil circuit-breakers;

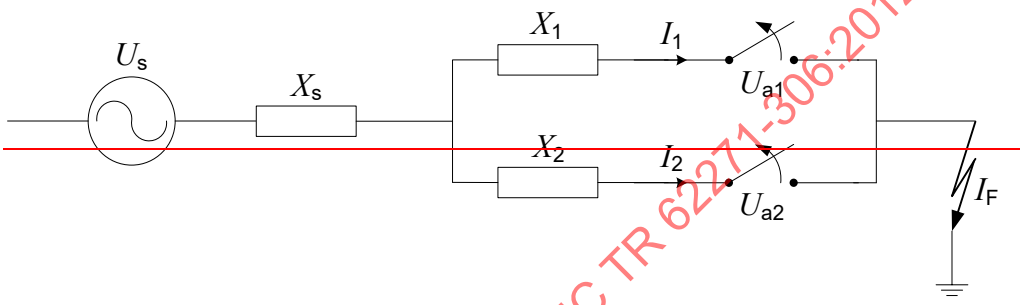
c) SF_6 circuit-breakers;

d) vacuum circuit-breakers.

As to the system and local impedances, the former will dominate and will give the same phase angle for the currents in the two circuit-breakers in parallel. The local impedances will determine the current division between the two circuit-breakers. If the circuit-breakers remain closed that current division will stand; however, once at least one of the circuit-breakers contacts part, it is the arc voltage that will dominate in determining the current division and the ultimate outcome.

C.3 Analysis and rules

The equivalent circuit for parallel switching analysis is shown in Figure C.1.



Key

U_s	Source voltage
X_s	Remote source impedance
X_1, X_2	Local impedances
I_F	Fault current
I_1, I_2	Current in circuit-breakers CB_1 and CB_2
U_{a1}, U_{a2}	Arc voltages of circuit-breakers CB_1 and CB_2

Figure C.1 – Equivalent circuit for parallel switching analysis

The system can be treated essentially as a constant current source. Ignoring resistance for simplicity and thinking in terms of absolute values, the following applies:

$$I_F = I_1 + I_2 \quad \text{(C.1)}$$

and

$$I_1 X_1 + U_{a1} = I_2 X_2 + U_{a2} \quad \text{(C.2)}$$

assuming that the contacts have parted on both circuit-breakers.

Combining Equations (C.1) and (C.2):

$$(I_F - I_2) X_1 - I_2 X_1 = U_{a2} - U_{a1}$$

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~~or~~

$$~~I_2(X_1 + X_2) = I_F X_1 + U_{a1} - U_{a2}~~$$

~~The condition for I_2 to go to zero, i.e. to commutate to CB_1 is:~~

$$~~I_F X_1 + U_{a1} - U_{a2} = 0~~$$

~~or~~

$$~~U_{a2} = I_F X_1 + U_{a1}~~ \quad ~~(C.3)~~$$

~~Likewise for I_1 to commutate to CB_2, the condition is:~~

$$~~U_{a1} = I_F X_2 + U_{a2}~~ \quad ~~(C.4)~~$$

~~The interpretation of Equations (C.3) and (C.4) is that the current will commutate from the first circuit-breaker to achieve an arc voltage equal to the open circuit voltage after commutation or, put more simply, the current will commutate from the circuit-breaker with the highest arc voltage to the circuit-breaker with the lower arc voltage. This is the basic rule of parallel switching.~~

~~The rule is illustrated in Figure C.2 which shows an actual case of a disconnector being used to parallel switch between two transmission lines. After contract parting, it can be seen that the arc voltage builds as the arc is elongated and the current gradually transfers to the parallel line. The current in the disconnector goes finally to zero when the arc voltage equals the open circuit voltage across the switch. Note that this switching event relies on a natural commutation and thus takes a number of cycles dependent on the series and parallel path impedances. In the case of circuit-breakers, the commutation is forced and rapid, and will take place within one half-cycle.~~

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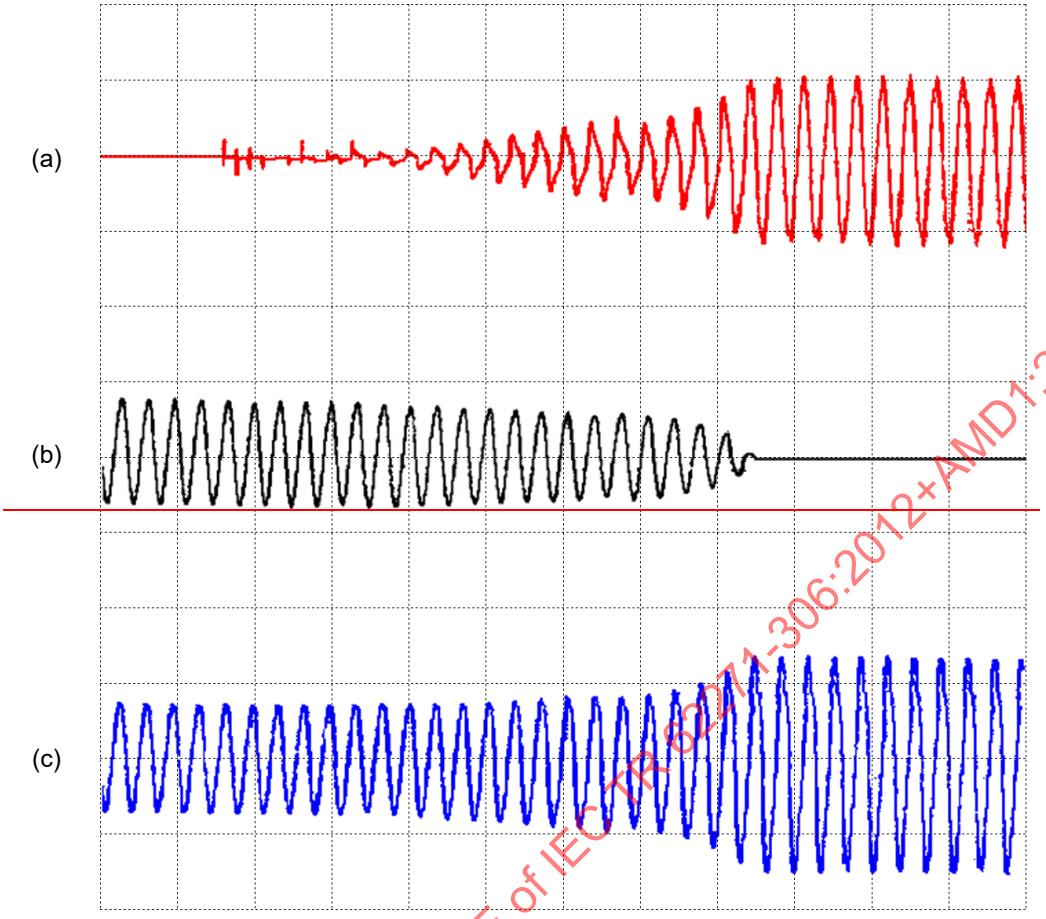

(a) Voltage across disconnector

(b) Current in disconnector

(c) Current in parallel transmission line

Figure C.2 – Parallel switching between transmission lines with disconnector

C.4 Parallel switching in practice

Clearly many parallel switching scenarios are possible in practice. A base case will be considered and then variations will be discussed in relation to this case.

The base case assumes simultaneous contact parting (in reality this may not always be the case particularly in fault events which cause several protection systems to operate) and about equal current in both circuit-breakers. Actual sharing of current in reality is most likely to be reasonably close, say in the 60 % / 40 % range at worst. Table C.1 shows the direction of current transfer for the base case (refer to Figure C.2) with regard only to the hierarchy of arc voltages and the rule discussed above.

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Table C.1 – Current transfer direction for parallel circuit-breakers with same contact parting instant and based on arc voltage

CB_1	Current transfer direction	CB_2
Oil	→ ←	Oil
Oil	←	Air Blast
Oil	→	SF_6
Oil	→	Vacuum
Air blast	→ ←	Air blast
Air blast	→	SF_6
Air blast	→	Vacuum
SF_6	→ ←	SF_6
SF_6	→	Vacuum
Vacuum	→ ←	Vacuum

For high-voltage circuit-breakers, the mechanical opening times can vary from 16 ms for air blast and some SF_6 circuit-breakers to about 25 ms for oil circuit-breakers. For medium voltage circuit-breakers, mechanical opening times can be quite long and in the range of 40 ms to 60 ms. Applying the rule, the following outcomes are probable:

- If the contact parting on the same phase of both circuit-breakers is within the same half-cycle, current will start to transfer from the circuit-breaker that opens first (with reference to Equations (C.3) and (C.4), the arc voltage needs only to achieve a voltage equal to the voltage across the parallel local impedance). If the transfer is not complete by the time the contacts part on the second circuit-breaker, then the transfer will be determined by the relative arc voltages.
- If the contact parting of the two circuit-breakers are in consecutive half-cycles, two outcomes are possible. If the contact parting of the first circuit-breaker to open is well prior to the current zero crossing but less than the minimum arcing time, then the current will transfer to the parallel circuit-breaker during the period of significant change of arc voltage at the latest. However, if the contact parting instant of the first circuit-breaker to open is close to the current zero crossing, it may not develop sufficient arc voltage to effect a transfer and the transfer may then be determined by the relative arc voltages once the contacts part on the parallel circuit-breaker.
- For medium voltage circuit-breakers, where the difference in contact parting times can span about one cycle at 50 Hz or more than one cycle at 60 Hz, the above outcomes also apply with the added possibility of two current zeros between the respective contact parting times. In the event of the latter possibility, the current will transfer from the first circuit-breaker to open at the second current zero at the latest.
- In the event of a large current imbalance but dependent on the relative contact parting instants and the circuit-breaker types, the circuit-breaker with the lower current will probably commutate its current to the other circuit-breaker.

Two references describing actual parallel switching tests between different circuit-breaker types are available and the above discussions can be tested against these tests [62, 63]. This is done in Table C.2.

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Table C.2 – Analysis of actual parallel switching tests

Test case	Predicted outcome	Actual outcome
CB_1: SF_6 puffer CB_2: SF_6 puffer I_1: 5 kA I_2: 35 kA Simultaneous contact parting just prior to current zero	Transfer from CB_1 to CB_2 due to negative characteristic of the arc voltage in CB_1	Transfer from CB_1 to CB_2
CB_1: SF_6 puffer CB_2: SF_6 puffer I_1: 5 kA I_2: 35 kA Contact parting in CB2 3 ms prior to that in CB_1 both well prior to current zero	Transfer from CB_1 to CB_2 around current zero crossing	Transfer from CB_1 to CB_2
CB_1: SF_6 puffer CB_2: SF_6 puffer I_1: 5 kA I_2: 35 kA Contact parting in CB_2 at current zero 7 ms prior to contact parting in CB_1	Transfer CB_2 to CB_1 on the basis of the staggered contact parting times	Transfer from CB_2 to CB_1
CB_1: SF_6 puffer CB_2: Minimum oil I_1: 4,6 kA I_2: 27,2 kA Simultaneous contact parting at current zero	Transfer from CB_1 to CB_2 based on low current and associated arc voltage in general or transfer from CB_2 to CB_1 if arc voltage builds up faster in CB_2	Transfer from CB_2 to CB_1
CB_1: SF_6 puffer CB_2: Minimum oil I_1: 4,6 kA I_2: 27,2 kA Simultaneous contact parting in both CB_1 and CB_2 in quarter cycle prior to current zero	Transfer from CB_1 to CB_2 based on low current and associated arc voltage given that the period of significant change of arc voltage is not involved	Transfer from CB_1 to CB_2

Based on the limited information in the reference, the outcomes appear reasonably predictable, although it may be argued that some cases fall into grey areas. However, it can be stated with certainty that, if the characteristics of the arc voltages of both circuit-breakers is known, then the outcome can be definitively predicted.

C.5 Conclusions

The perceived risk with parallel switching is that current transfer will occur after an arcing time greater than one loop and thus approach an evolving fault type situation. To avoid this, it is often suggested that one or other of the two circuit-breakers be staggered by a time equal to one loop of current. However, introducing a time delay into a protective trip operation is unlikely to find favour with any utility and, on a balance of probabilities basis, appears to be unnecessary. The reasons for this are discussed below bearing in mind that sometimes the unpredicted can indeed happen if only on a very low probability basis.

As noted earlier, experience indicates that parallel switching is not a real issue requiring resolution but rather one of understanding the duty. The analysis above supports the notion that the arc voltages alone may be the driver that ensures the transfer of current from one circuit-breaker to the other within a time period of one loop. There is, however, an inherent staggering of the opening times between the different circuit-breaker types and the question is how this influences the interaction between the two circuit-breakers. On the basis that the current will tend to transfer from the circuit-breaker which opens first, Table C.1 can be revised as shown below in Table C.3.

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Table C.3 – Current transfer directions for parallel circuit breakers with inherent opening times and arc voltages

	Current transfer direction based on:		
CB_1	Arc voltage	Opening time	CB_2
Oil	→ ←	– a	Oil
Oil	←	←	Air-blast
Oil	→	←	SF_6
Oil	→	→ b ←	Vacuum
Air-blast	→ ←	– a	Air-blast
Air-blast	→	→	SF_6
Air-blast	→	→	Vacuum
SF_6	→ ←	– a	SF_6
SF_6	→	→ b ←	Vacuum
Vacuum	→ ←	– a	Vacuum

a For like circuit-breakers with the same opening time, the current will transfer from the circuit-breaker with the highest arc voltage.

b Applies at medium voltage only and dependent on which circuit-breaker opens first.

At high-voltages, only in the case of an oil and an SF_6 circuit-breaker is there an apparent conflict between the hierarchy of the arc voltages and the opening time. Dependent on the difference between the contact parting times it follows that:

- if the contact parting time spread between the two circuit-breakers is at least a quarter-cycle, then the current in the SF_6 circuit-breaker will probably transfer totally to the oil circuit-breaker before it opens;
- if the contact parting time spread is less than a quarter-cycle, then either the above scenario will occur or the current will start to transfer to the oil circuit-breaker and then reverse direction due to the arc voltage in the oil circuit-breaker.

At medium voltages, the same reasoning applies for oil and SF_6 circuit-breakers as discussed above. Where an oil or SF_6 circuit-breaker is paralleled with a vacuum circuit-breaker, the following is likely to occur:

- if the vacuum circuit-breaker opens first, the current will transfer to the still closed oil or SF_6 circuit-breaker if a current zero crossing occurs before the latter circuit-breakers open; if no current zero crossing occurs, then the current in the latter circuit-breakers will transfer to the vacuum circuit-breaker on opening;
- if the vacuum circuit-breaker opens last, the total current will be transferred to it.

Finally, what is the influence of frequency? The answer to this is that 60 Hz is more favourable to successful parallel switching than 50 Hz. The reason for this is the more frequent occurrences of current zero crossings and their associated significant changes in arc voltage which are conducive to current transfer in one direction or the other.

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Annex D
(informative)

Application of current limiting reactors

D.1 General

Current limiting reactors applied to limit fault currents are usually installed at the substation distribution level [64]. Large capacity step-down substations are commonly used to supply distribution systems and the short-circuit levels on the low voltage buses and feeders can be very high. The reactors can be installed on the buses or the feeders, or even in the transformer neutrals. The preferred location for overhead distribution systems is on each feeder.

The advantages offered by the use of series reactors on feeders are:

- circuit-breakers, disconnectors and associated buswork can be rated for a lower short-circuit level;
- the short-circuit level imposed on downstream devices and customer installations is lower; also the possible risk for burndown of aerial conductors is virtually eliminated;
- the transformers are exposed only to the lower level faults which is significant given that the distribution feeder fault is the most common fault on power systems;
- joint use of poles for power distribution and communications purposes are facilitated;
- lighter construction of the distribution lines and the possibility to use expulsion fuses.

Important considerations when using series reactors include equipment cost, space requirements and the installation cost, Watt and var losses and regulation through the reactor. The reduction in the fault level is of the order of three or more: in one typical case in North America, where 5 mH reactors are applied in feeders, the fault level is limited to maximum 6 kA as opposed to in excess of 20 kA without the reactors. Overall reactor values in the range 2 mH to 5 mH are used.

Fewer bus reactors could be applied but such reactors are not attractive from a regulation perspective and watts loss. Transformer neutral reactors are also unattractive being effective only for single-line to earth faults.

Current limiting reactors are also used in shunt capacitor bank installations. The purpose of the reactors is to limit the inrush current through the bank circuit-breaker on energisation to 20 kA peak at 4 250 Hz. This applies to single bank energisation or back-to-back bank energisation. Reactor values in this application are in the range 0,5 mH to 5 mH.

Only dry-type reactors are used in these applications today. The reactor electrical characteristics are thus a low inductance value and low stray capacitance values in the order of a few hundred pF. The TRVs associated with the reactors on clearing feeder faults or faults between the reactor and the capacitor bank are fast rising with significant amplitudes. For the feeder case, circuit-breaker failures have been attributed to the reactor TRV [65].

D.2 Feeder case TRVs

Figure D.1 shows the measured TRV for a three-phase ungrounded fault on a 25 kV feeder with a current limiting reactor. This TRV shape is typical and shows a fast transient oscillation due to the reactor superimposed on the slower transient oscillation determined by the source impedance and the local capacitances [9].

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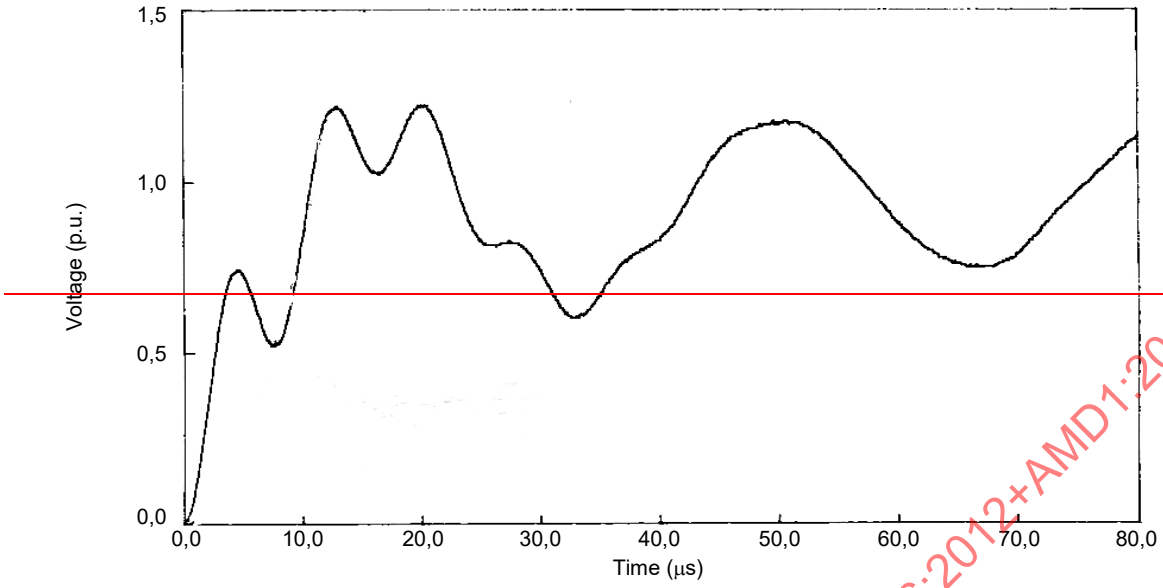
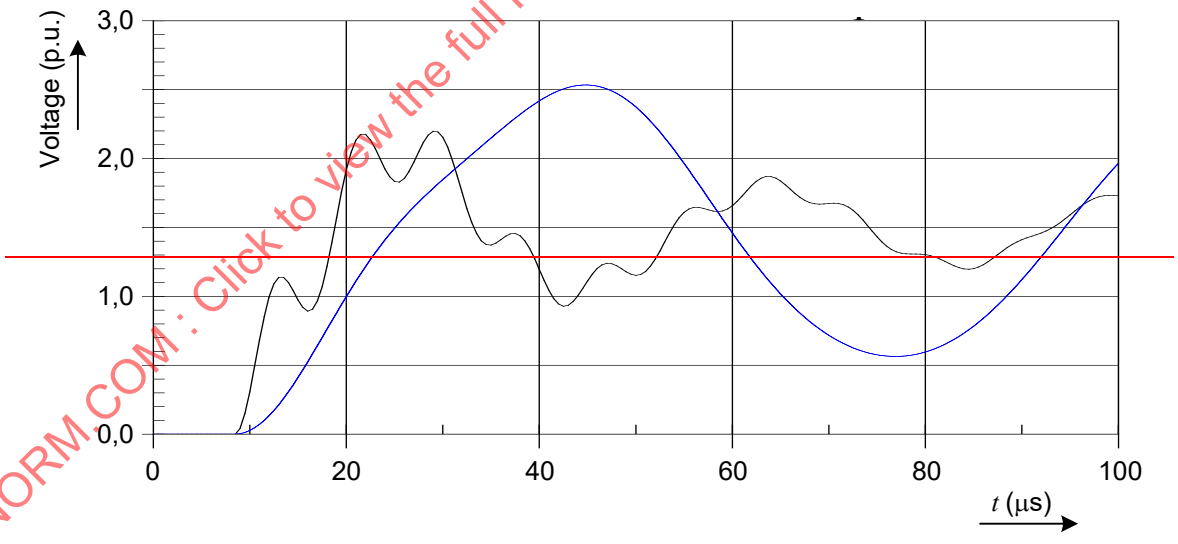


Figure D.1 – TRV for three-phase ungrounded fault on 25 kV feeder with current limiting reactor (1 p.u. = 30,6 kV peak)

The fast transient oscillation can be dealt with by adding a capacitor across the reactor. This approach has advantages over applying the capacitor to earth in that it can actually be installed inside the reactor assembly [65]. Figure D.2 shows an EMTP simulation for the case shown in Figure D.1 without and with 20 nF applied across the reactor. During normal service the capacitor is exposed to the minimal voltage drop across the reactor and only experiences high voltages on fault occurrence.



Solid line: TRV without capacitance

Dashed line: TRV with capacitance

Figure D.2 – EMTP simulation for case in Figure D.1 with and without parallel capacitance (1 p.u. = 20,4 kVpeak)

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D.3 Shunt capacitor case TRVs

This case can be illustrated by considering an EMTP study for a 66 kV, 50 MVAR ungrounded shunt capacitor bank with a 10 mH current limiting reactor. The TRV for a three-phase ungrounded fault between the reactor and the bank is shown in Figure D.3. The effect of the reactor is very evident as is further shown in Figure D.4.

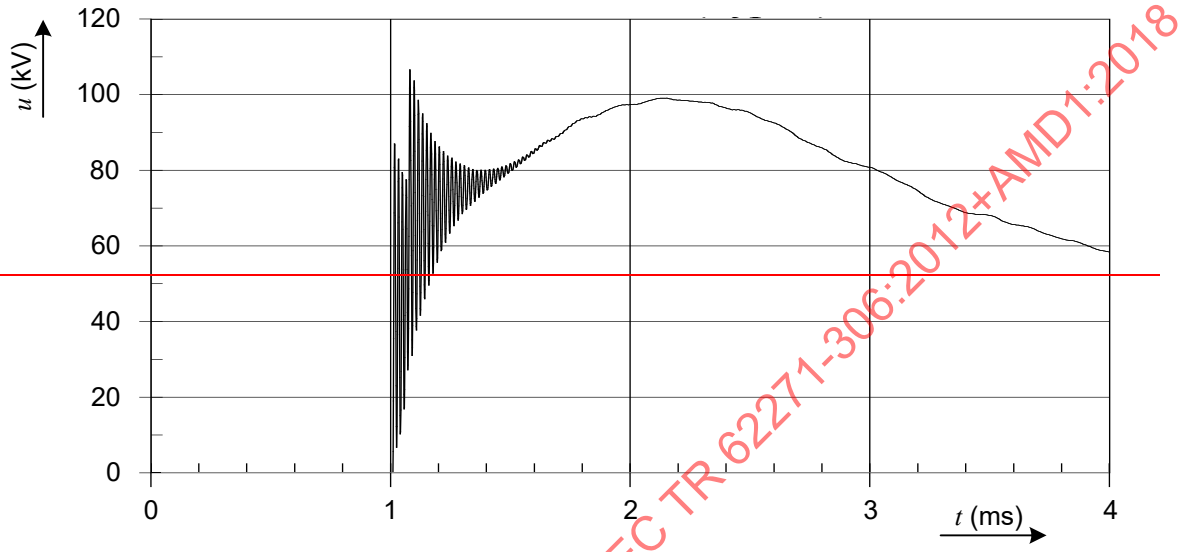

Figure D.3 – TRV for three-phase ungrounded fault on 66 kV shunt capacitor bank with 10 mH current limiting reactor

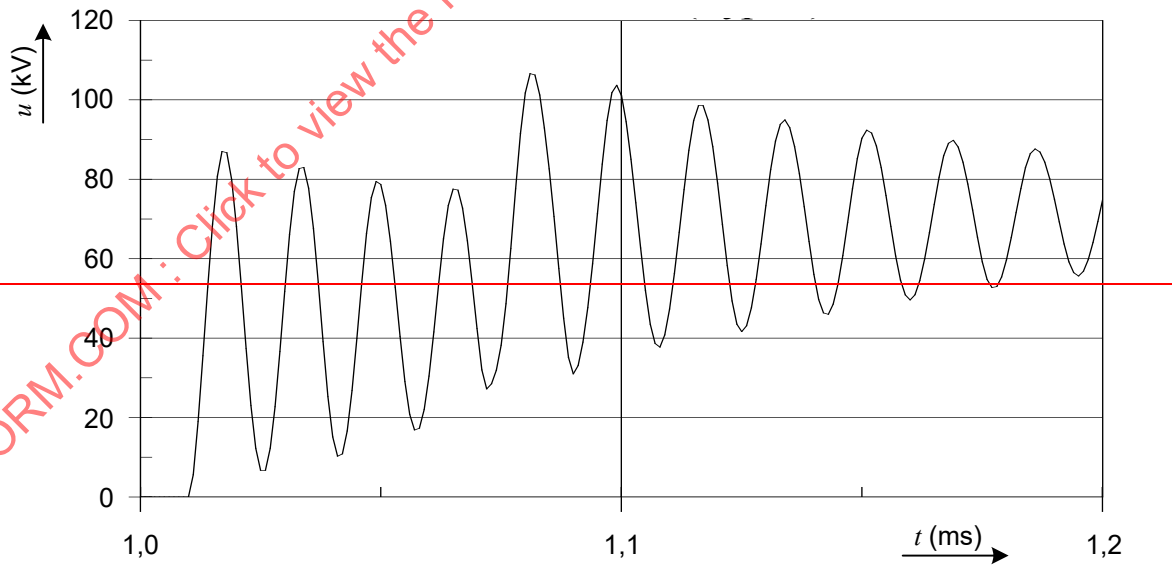

Figure D.4 – Initial part of TRV for three-phase ungrounded fault on 66 kV shunt capacitor bank with 10 mH current limiting reactor

The effect of adding a 20 nF capacitor across the reactor is shown in Figure D.5. The trace shows that the frequency of the reactor oscillation is reduced by about a factor of five.

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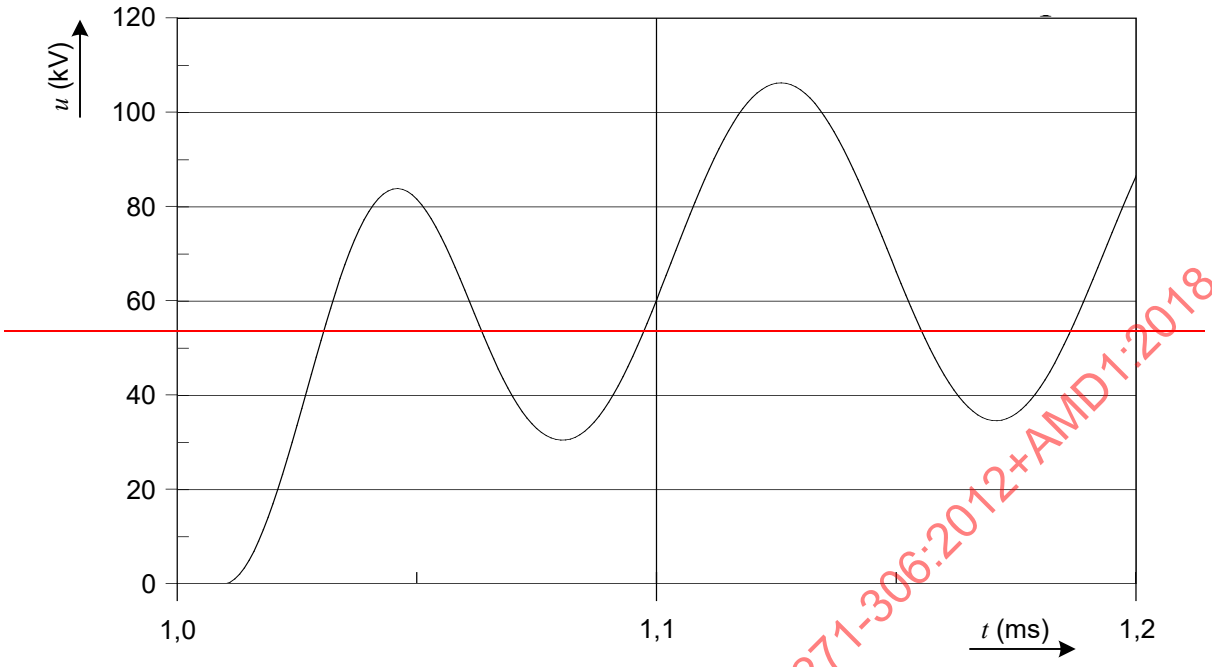

~~**Figure D.5 – Initial part of TRV for three-phase ungrounded fault on 66 kV shunt capacitor bank with 10 mH current limiting reactor with parallel 20 nF capacitor**~~

~~D.4 Conclusion~~

~~The use of current limiting reactors should always be associated with a TRV study. The TRVs produced by current-limiting reactors are often extremely severe (fast rate-of-rise, high frequency) and are generally significantly faster than those specified in IEC 62271-100. Mitigation capacitors installed across the current limiting reactor or phase-to-earth are generally required in order to decrease the resultant rate-of-rise of recovery voltage to a value for which the circuit-breaker has been designed and tested.~~

D.1 General

Series reactors were first applied at distribution voltage levels to limit fault currents on feeder circuits to values compatible with downstream devices [141]. The reactors are dry-type with low stray capacitances and the associated TRV is fast-rising, unless mitigation measures, such as the addition of capacitance across the reactors or line-to-ground, are taken [142].

A second early and continuing application of current limiting reactors is on shunt capacitor banks to limit inrush current to the standard values of 20 kA peak at 4 250 Hz and also the voltage dip. Typically, however, the reactors are installed between the bank circuit-breaker and the capacitor bank itself and, in the event of a fault between the reactor and the capacitor bank, the circuit-breaker is exposed to the above-noted TRV.

Current-limiting reactors are now commonly applied at transmission voltage levels to deal with rising fault levels in general, and also the effect of sudden addition of generation. Simply changing out a circuit-breaker for one with a higher short circuit current rating is very often not an option because other station equipment – buswork, disconnectors, CTs and so on – may also not be rated for the increased fault levels.

Current limiting reactors can be connected on either side of the circuit-breaker as shown in Figure D.1. From a TRV perspective, there will be oscillations associated with the source and

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reactor, which combined determine the TRV imposed on the circuit-breaker. A duality exists between the two arrangements such that the TRV is the same for both reactor locations. To calculate the TRV, consideration is given to the applicable first-pole-to-clear factor k_{pp} and the source and reactor oscillations. Since high-voltage systems are effectively earthed, X_0/X_1 = 3, this is the case that will be discussed, the circuit arrangement in Figure D.1 (b) in particular.

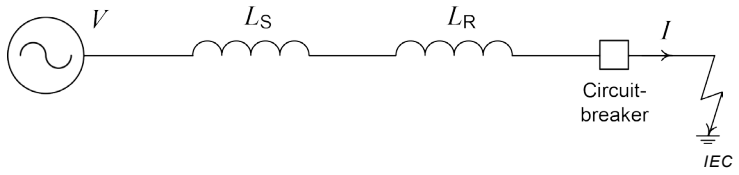


Figure D.1a – Reactor on the source side of the circuit-breaker

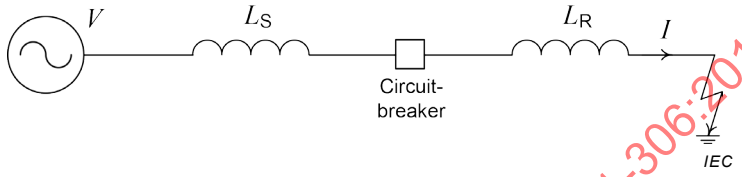


Figure D.1b – Reactor on load side of the circuit-breaker

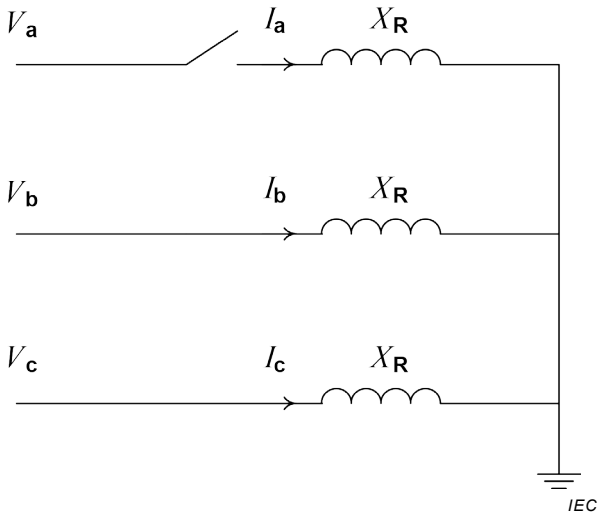
Key

V	Applicable source voltage
L_s	Source inductance
L_R	Current limiting reactor inductance
I	Fault current

Figure D.1 – Current limiting reactor location

D.2 Pole factor considerations

From Figure D.1(b), the three-phase circuit for first-pole-to-clear factor k_{pp} calculation is shown in Figure D.2.



Key

V_a, V_b, V_c	Phase voltages to earth

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I_a, I_b, I_c Phase currents

X_R Current limiting reactor impedance

Figure D.2 – Circuit for k_{pp} calculation

Using the symmetrical component method approach, k_{pp} is given by:

$$k_{pp} = \frac{3[X_0X_1 + X_R(X_R + X_1 + X_0)]}{(X_1 + X_R)(3X_R + X_1 + 2X_0)}$$

where X_1 and X_0 are the system positive and zero sequence impedances. X_R is the impedance of reactor X_R. Setting $X_0 = 3X_1$ for effectively earthed neutral systems, the equation can be re-written as:

$$k_{pp} = \frac{3\left[3 + \left(\frac{X_R}{X_1}\right)^2 + 4\left(\frac{X_R}{X_1}\right)\right]}{\left[7 + 3\left(\frac{X_R}{X_1}\right)^2 + 10\left(\frac{X_R}{X_1}\right)\right]} \quad \text{(D.1)}$$

and plotted in Figure D.3. $X_R = 0$, $k_{pp} = 1{,}2857$ p.u. as expected. In IEC 62271-100 k_{pp} is rounded to 1,3. The decay to $k_{pp} = 1$ is very gradual where the application can be treated on a single-phase basis.

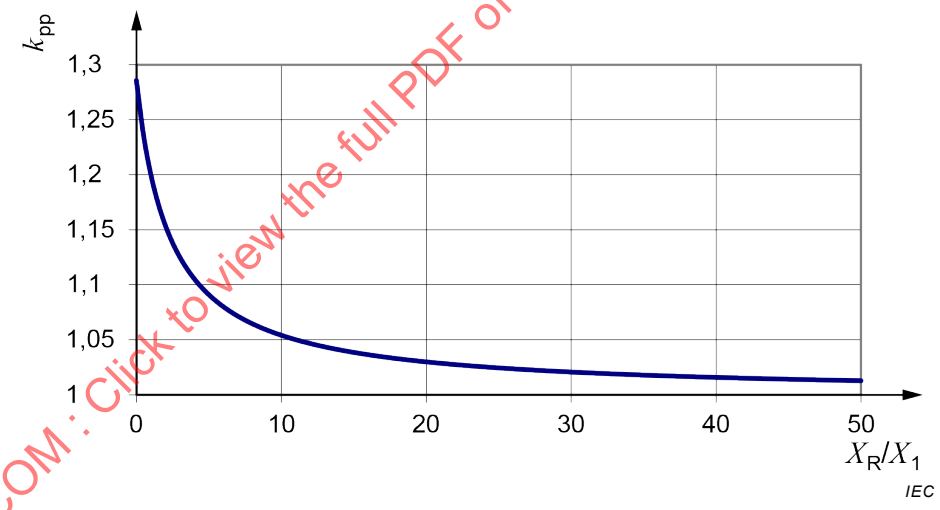

Figure D.3 – Variation of k_{pp} with ratio X_R/X_1

D.3 Oscillatory component calculation

The oscillatory circuits for TRV calculation for the arrangements of Figure D.1 are shown in Figure D.4 and Figure D.5.

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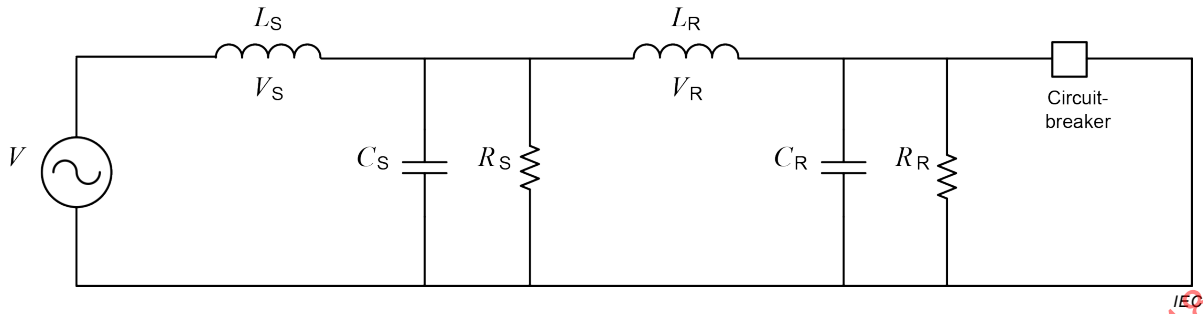
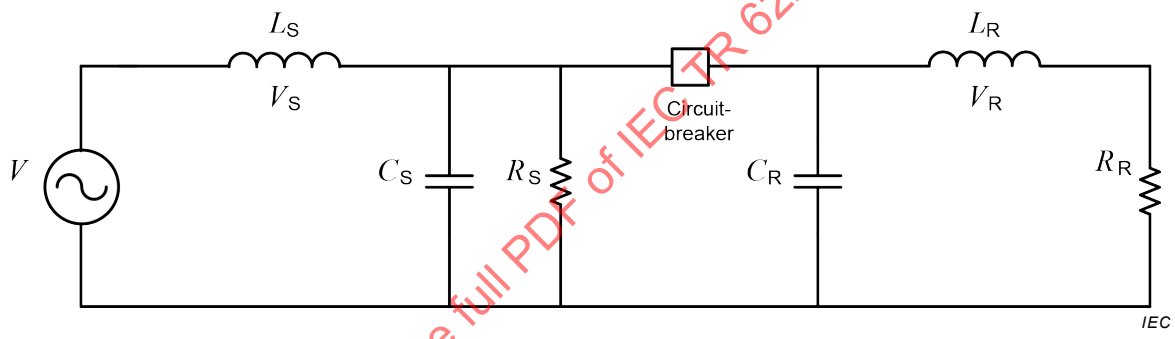


Key

L_s	Source circuit inductance	L_R	Reactor circuit inductance
C_s	Source circuit capacitance	C_R	Reactor circuit capacitance
R_s	Source circuit resistance	R_R	Reactor circuit resistance
V_s	Peak voltage across source inductance	V_R	Peak voltage across reactor inductance
V	Peak AC system voltage for first-pole-to-clear		

Figure D.4 – Oscillatory circuit for the circuit arrangement of Figure D.1(a)



Key

L_s	Source circuit inductance	L_R	Reactor circuit inductance
C_s	Source circuit capacitance	C_R	Reactor circuit capacitance
R_s	Source circuit resistance	R_R	Reactor circuit resistance
V_s	Peak voltage across source inductance	V_R	Peak voltage across reactor inductance
V	Peak AC system voltage for first-pole-to-clear		

Figure D.5 – Oscillatory circuit for the circuit arrangement of Figure D.1(b)

In both Figures D.4 and D.5 the values of V_s and V_R are given by:

$$V_s = \frac{L_s}{L_s + L_R} \times V \text{ and } V_R = \frac{L_R}{L_s + L_R} \times V .$$

Considering Figure D.4 and applying the principle of superposition, the circuit-breaker TRV u_{cb} is given by [134]:

$$u_{cb} = V_s\left[1 - f\left(d_1, t_{g1}\right)\right] + V_R\left[1 - f\left(d_2, t_{g2}\right)\right] = V - V_s\, f\left(d_1, t_{g1}\right) - V_R\, f\left(d_2, t_{g2}\right) \quad \text{(D.2)}$$

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where d_1 and d_2 are damping factors and t_{g1} and t_{g2} are generic times based on the oscillation frequencies and the function $f(d_x, t_{gx})$ is of the form.

$$f\left(d_x, t_{gx}\right) = e^{-d_x t_{gx}}\left(\cosh\sqrt{d_x^2 - 1}\; t_{gx} + \frac{d_x}{\sqrt{d_x^2 - 1}}\sinh\sqrt{d_x^2 - 1}\; t_{gx}\right)$$

or

$$f\left(d_x, t_{gx}\right) = e^{-d_x t_{gx}}\left(\cos\sqrt{1 - d_x^2}\; t_{gx} + \frac{d_x}{\sqrt{1 - d_x^2}}\sin\sqrt{1 - d_x^2}\; t_{gx}\right)$$

The function $f(d_1, t_{g1})$ is either hyperbolic or sinusoidal depending on whether the source TRV is overdamped or underdamped, respectively. The more conservative approach is to treat the source TRV as being underdamped. The function $f(d_2, t_{g2})$ is always underdamped because reactors are very low-loss devices.

The circuit-breaker TRV for the circuit arrangement of Figure D.5 is given by:

$$u_{cb} = V_s\left[1 - f\left(d_1, t_{g1}\right)\right] + V_R - V_R\left[1 - f\left(d_2, t_{g2}\right)\right] = V - V_s f\left(d_1, t_{g1}\right) - V_R\, f\left(d_2, t_{g2}\right)$$

and is the same equation as for the circuit arrangement of Figure D.4. A duality exists between the two circuit arrangements.

By way of example, take the actual case of a 10 Ω series reactor applied on a system operating at 225 kV to reduce the fault level from 31,5 kA to 9,2 kA. The scenario is shown in Figure D.6.

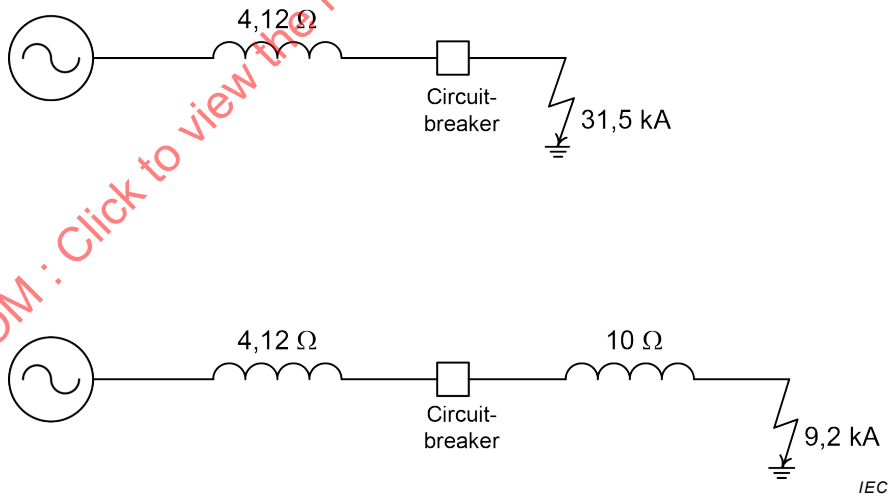

Figure D.6 – Series reactor application case

The actual source TRV will generally not be known and one approach is to use an equivalent standard TRV. In this case, since 9,2 kA is approximately 30 % of 31,5 kA, the source can first be represented as an equivalent T30 source with the following characteristics:

– First-pole-to-clear factor: k_{pp} = 1,138 p.u. (from Equation (D.1))
– Amplitude factor: k_{af} = 1,54 p.u.

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– t_3 = 80 µs
– V_s = 61 kV

and for the series reactor circuit

– First-pole-to-clear factor: k_{pp} = 1,138 p.u.
– Amplitude factor: k_{af} = 1,9 p.u.
– V_R = 148 kV

The circuit for the first-pole-to-clear is shown in Figure D.7.

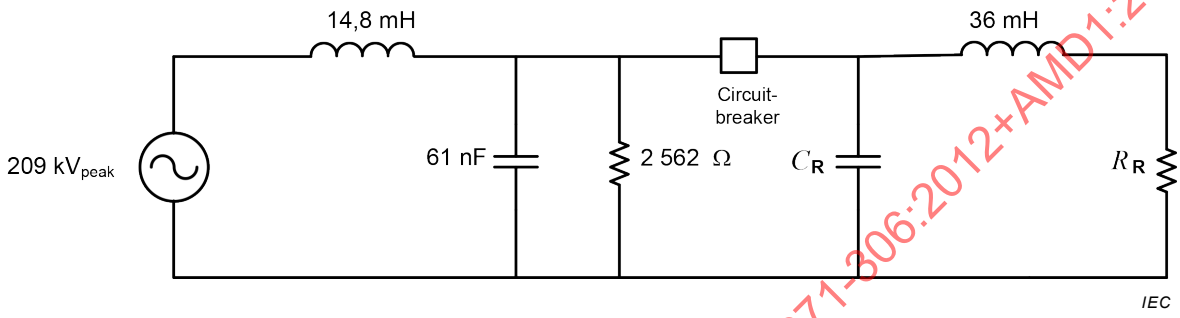

Figure D.7 – TRV calculation circuit

The circuit-breaker TRV u_{cb} is given by (from Equation (D.2)):

$$u_{cb} = 209\left[1 - 0{,}29e^{-0{,}192\,t_{g1}}\left(\cos 0{,}98\,t_{g1} + 0{,}198\sin 0{,}98\,t_{g1}\right) - 0{,}71e^{-0{,}033\,t_{g2}}\left(\cos t_{g2} + 0{,}033\sin t_{g2}\right)\right]$$

where 1 p.u. t_{g1} = 30 µs and t_{g2} varies dependent on the value chosen for the added capacitance C_R. The equation is plotted in Figure D.8 for values of C_R equal to 10 nF, 15 nF and 20 nF and in comparison to the envelope of the T30 TRV for a 245 kV circuit-breaker in accordance with IEC 62271-100.

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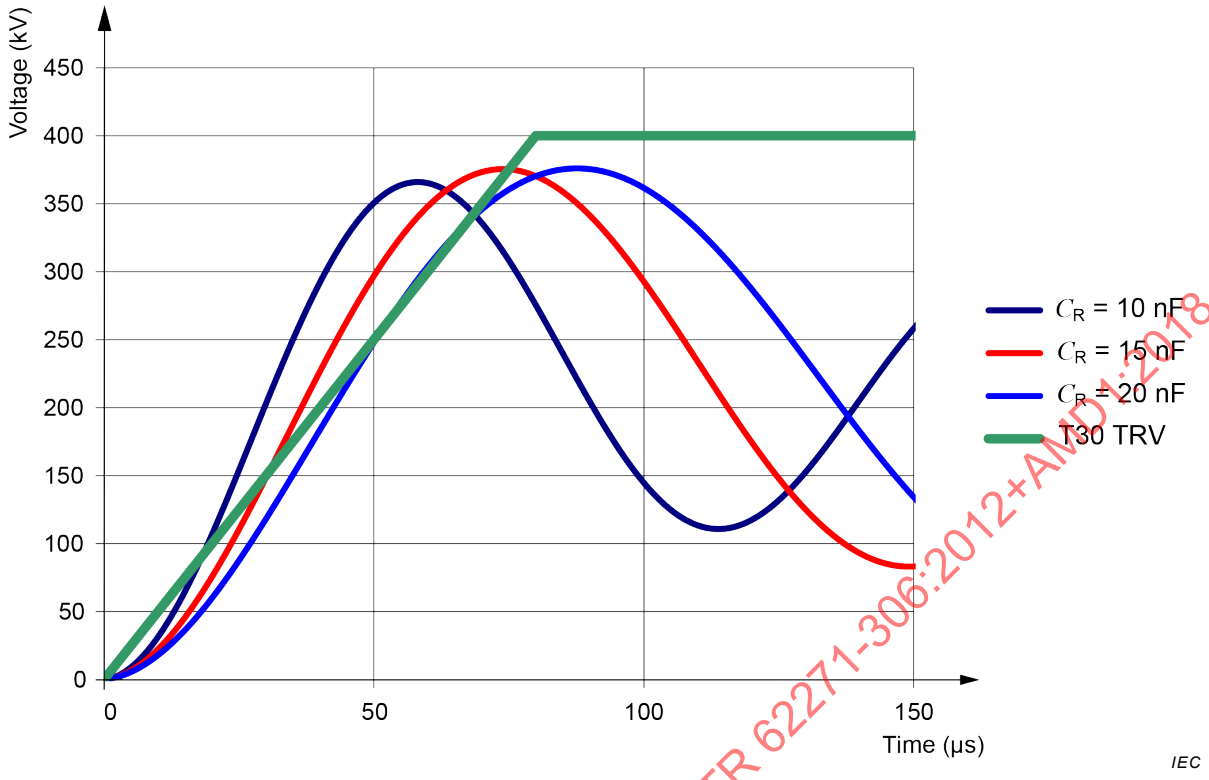

Figure D.8 – Circuit-breaker with T30 source and varying values of C_R

This represents an extreme case since the actual source TRV in principle is expected to be less onerous than the T30 TRV. The manner in which the source TRV degree of damping and frequency influence the circuit-breaker TRV is shown in Figure D.9 and Figure D.10 for the same C_R values as in Figure D.8. The effect of varying both the degree of damping and the frequency is shown in Figure D.11.

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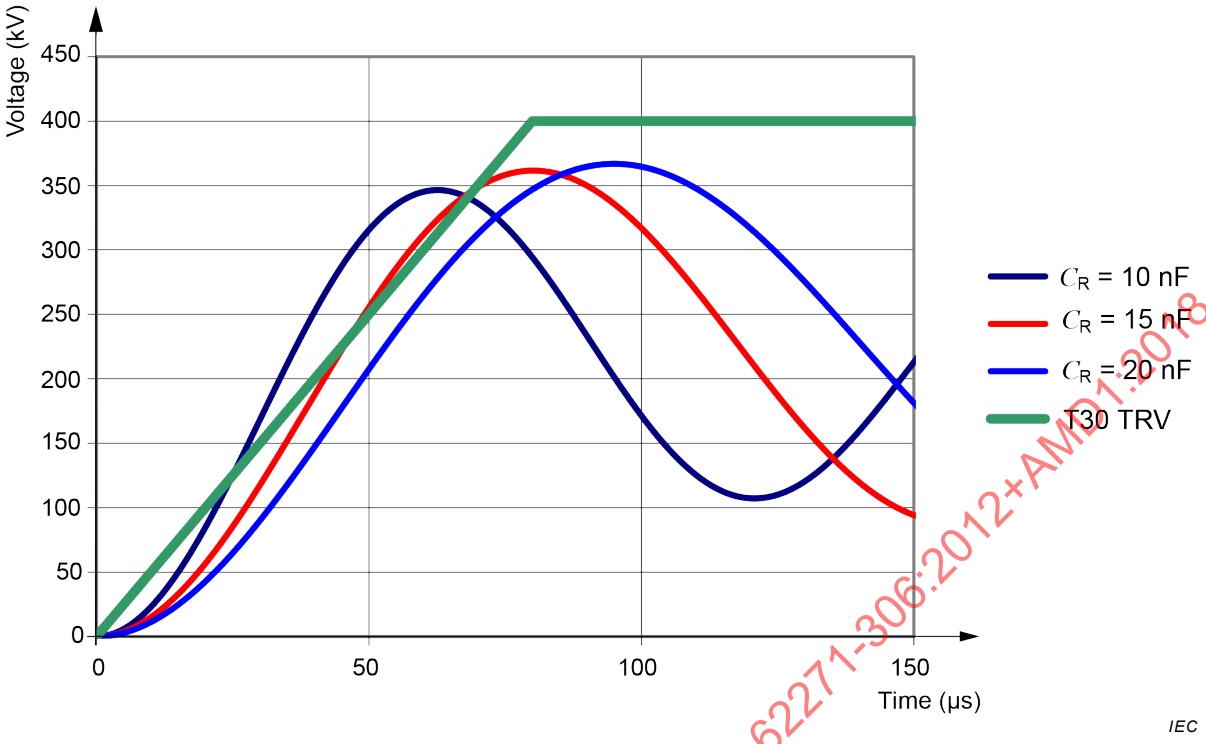

Figure D.9 – Circuit-breaker TRV with source TRV k_{af} = 1,4 p.u. (down from 1,54 p.u.) and t_3 unchanged at 80 µs

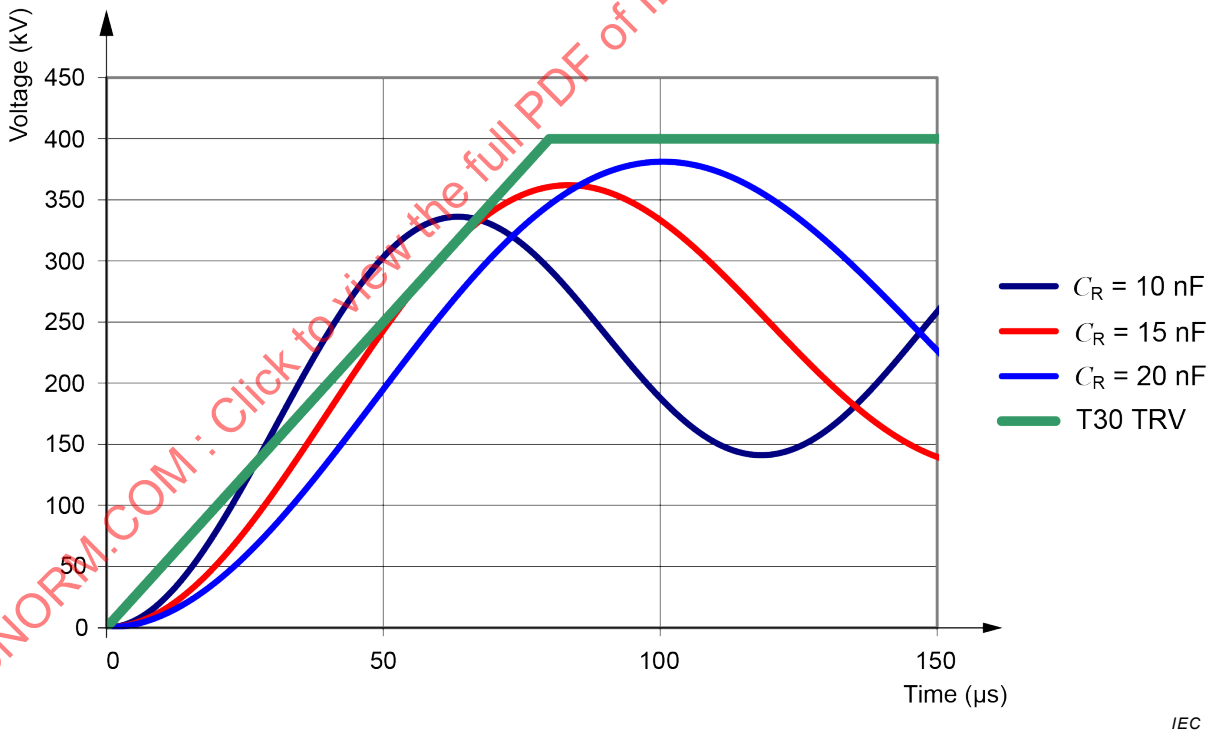

Figure D.10 – Circuit-breaker TRV with source TRV k_{af} unchanged at 1,54 p.u. and t_3 increased to 110 µs

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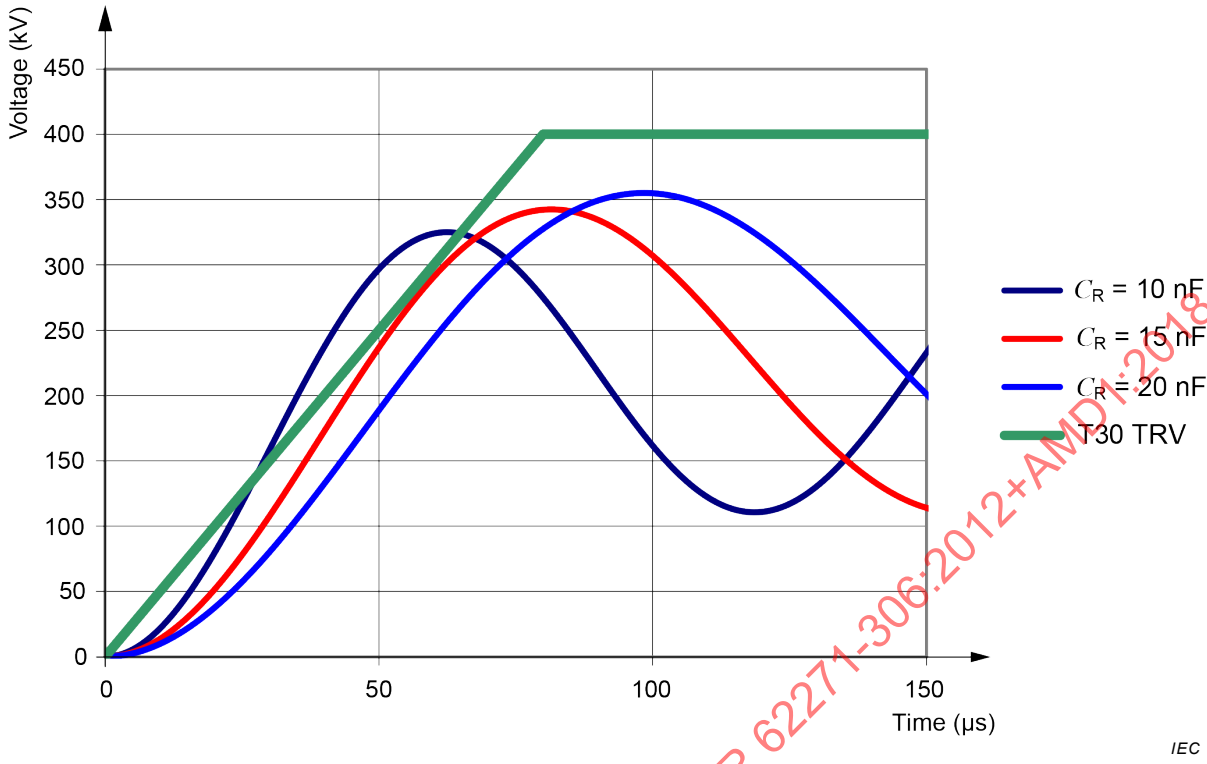

Figure D.11 – Circuit-breaker TRV with source TRV k_{af} = 1,4 p.u. and t_3 = 110 µs

Another possibility is to treat the application on a single phase basis, i.e. determine the C_R value assuming single-line-to-earth faults only. Regardless of the basic approach, the user should exercise judgment based on the knowledge of the system and associated transient study practices.

D.4 Series reactors on shunt capacitor banks

Series reactors are applied on shunt capacitor banks in order to limit inrush current magnitudes and frequencies to standardized limits. In the event of a fault between the reactor and the capacitor bank, the scenario is that shown in Figure D.1(b). Analysis is as discussed in D.3 with the note that the scenario can be avoided altogether if the reactors are located on the neutral side of the capacitor bank.

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Annex E
(informative)

~~Explanatory notes on the revision of TRVs for circuit-breakers of rated voltages higher than 1 kV and less than 100 kV~~

Guidance for short-circuit and switching test procedures for metal-enclosed and dead tank circuit-breakers

~~E.1 General~~

~~The text given in this annex originates from Annex L of IEC 62271-100:2008.~~

~~Following the decision taken at the SC17A meeting in Beijing (CN) in October, 2002, IEC SC 17A/WG35 has prepared a proposal for the revision of TRVs for circuit-breakers rated above 1 kV and less than 100 kV.~~

~~This proposal uses the input coming from former Working groups of CIGRE Study Committee A3 (Switching Equipment) that have studied the necessity to adapt the TRV requirements for circuit-breakers rated less than 100 kV. In 1983, a CIGRE SC A3 Task Force reported on Transient Recovery Voltages in Medium Voltage Networks. The results of the study have been published in Electra 88. Another CIGRE working group, WG 13.05, studied the TRVs generated by clearing transformer fed faults and transformer secondary faults. The results have been presented in Electra 102 (1985). In 1992, together with CIRED, CIGRE SC A3 created working group CC-03 to investigate again the definition of TRVs for medium voltage switchgear. The outcome of these investigations has been published in CIGRE Technical Brochure 134 (1998) and is in line with earlier studies.~~

~~E.2 Main modifications made~~

~~The main modifications introduced by this amendment can be summarized as follows:~~

~~a) In order to cover all types of networks (distribution, industrial and sub-transmission) in the range of rated voltages higher than 1 kV and less than 100 kV, and for standardization purposes, two types of systems are defined:~~

~~– cable systems~~

~~Cable-systems are defined in 3.1.132 of IEC 62271-100:2008.~~

~~– line systems~~

~~Line systems are defined in 3.1.133 of IEC 62271-100:2008.~~

~~b) A particular test duty T30 is specified for the special case of circuit-breakers intended to be connected to a transformer with a connection of small capacitance (cable length less than 20 m), in order to verify their capability to interrupt transformer-limited faults. This is covered in a new Annex M of IEC 62271-100:2008.~~

~~In the general case where the capacitance of the connection is high enough, the normal test duty T30 demonstrates the capability to interrupt transformer-limited faults.~~

~~c) Short-line fault is a mandatory duty for circuit-breakers with rated voltages 15 kV and above and directly connected to overhead lines. As specified already in this standard for circuit-breakers rated 48,3 kV and above, the rated short-circuit current must be higher than 12,5 kA (i.e. $I_{sc} \geq 16$ kA).~~

~~d) The special case of circuit-breakers installed immediately in series with a reactor is covered in a new subclause 8.103.7 of IEC 62271-100:2008.~~

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E.3 Terminal fault

E.3.1 TRV for circuit-breakers in line systems

Line systems are more common to the North American practice than to the European practice. Therefore the TRV ratings as listed in Table 2 of ANSI C37.06-2000 were the basis to define the new Table 25 of IEC 62271-100:2008. The values for t_3 are 0,88 times the T_2 values specified in ANSI.

NOTE The factor 0,88 is derived from a pure "1-cos" waveshape multiplied with ½ amplitude factor. The standard TRV wave-shape "1-cos" in ANSI C37.06-2000 for rated voltages less than 100 kV did not coincide with the precise mathematical equation for parallel or series damped circuits, for which another ratio t_3/T_2 is applicable.

Time t_3 for terminal fault and short-line fault is equal to $4{,}65 \times U_r^{0{,}7}$, with t_3 in microseconds and U_r in kV. The equation was derived from the values given in Table 2 of ANSI C37.06-2000 for rated voltages 15,5 kV, 25,8 kV, 48,3 kV and 72,5 kV. The same equation is used for other rated voltages.

The rate of rise of recovery voltage is derived from u_c and t_3.

Time t_3 for out-of-phase is taken as double the time t_3 for terminal fault.

E.3.2 Time delay

Time delay in Table 24 of IEC 62271-100:2008 for circuit-breakers in cable systems:

- The time delay t_d is as in the first edition of IEC 62271-100 published in 2001 for rated voltages less than 52 kV. The equation is generalized to all cable systems (rated voltage less than 100 kV).

Time delay in Table 25 of IEC 62271-100:2008 for circuit-breakers in line systems:

- The time delay t_d in Table 25 is $0{,}05 \times t_3$, as in the first edition of IEC 62271-100 published in 2001 for rated voltages 48,3 kV – 52 kV and 72,5 kV. The equation has been extended to the lower rated voltages as no change in the initial part of the TRV wave-shape is expected (the initial part is exponential, even with the short line lengths that can be met in distribution and sub-transmission systems). This requirement is not judged excessive as in the worst case (U_r = 15 kV) the time delay value of 2 µs is as specified for circuit-breakers with rated voltages higher than 72,5 kV.
- It recognizes the fact that at high short-circuit current the thermal phase of interruption, this time delay can be critical and that has to be taken into account. However, as shown in Tables 13 and 14 of the first edition of IEC 62271-100 published in 2001, such verification can be made when performing short-line fault tests. Therefore, as it is already the case for rated voltages higher than 38 kV, it is allowed to have a longer time delay during testing of T100, up to $0{,}15 \times t_3$, provided that short-line fault tests are performed. This possibility is indicated in Table 25 of IEC 62271-100:2008.

E.3.3 Amplitude factor for T100s and T100a

For circuit-breakers in cable systems, the value of 1,4 in the first edition of IEC 62271-100 published in 2001 is retained, due to the positive experience with past editions of this standard.

For circuit-breakers in line systems, the value of 1,54,defined in ANSI C37.06-2000 was taken.

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E.3.4 Amplitude factor for T60, T30 and T10

For circuit-breakers in cable systems, the value of 1,5 for T60 in the first edition of IEC 62271-100 published in 2001 is kept, due to the positive experience obtained. For T30 and T10, the amplitude factor has been raised from 1,5 to respectively 1,6 and 1,7, as the contribution to TRV comes mainly from the voltage variation across transformer(s) which has low damping, this combined with source voltage results to a TRV with a relatively high amplitude factor.

For circuit-breakers in line systems, the values were taken from ANSI C37.06-2000: 1,65 for T60, 1,74 for T30 and 1,8 for T10.

E.4 Short-line fault

In the first edition of IEC 62271-100, short-line fault requirements have been specified for circuit-breakers with a rated voltage of 52 kV and 72,5 kV, in the range of rated voltages considered in this edition, and directly connected to overhead-lines.

In this second edition, short-line fault requirements are specified for class S2 circuit-breakers with a rated voltage of 15 kV and above and directly connected (with busbar) to overhead-lines, irrespective of the type of network on the source side.

As the network and substation topology and layout for 48,3 kV is identical to those of 52 kV and 72,5 kV systems, the short-line test duty for 48,3 kV is specified in a way similar to 52 kV and 72,5 kV.

For the rated voltages 15 kV, 25,8 kV and 38 kV the characteristics and procedure are slightly different. As normally no equipment is connected to the line side of the circuit-breaker the line characteristics are adapted to virtually no delay capacitance: $t_{dL} < 0{,}1$ µs. As the line length to the fault location should correspond to realistic distances, the test duty L_{90} has been dropped and the tolerances on the line length for L_{75} have been adapted.

The short-line fault test specified is regarded as covering three-phase short-line faults as well as two-phase and single-phase faults for the following reasons:

- the representative surge impedance, seen from the terminals of the clearing pole, is such that for all cases the RRRV for all three poles to clear is covered by the specified characteristics listed in Table 8 of IEC 62271-100:2008;
- the single-phase short-line fault test, with an arcing window of (180°−dα), covers the requirement for the multi-phase fault cases for effectively-earthed and non-effectively earthed systems;
- the withstand of the peak value of TRV during three-phase fault interruption is demonstrated by terminal fault test duty T100.

E.5 Out-of-phase

Not enough system information is available to revise TRV parameters for breaking in out-of-phase condition. CIGRE SC A3 has been asked to investigate the system and service conditions leading to out-of-phase current clearing. Therefore, the TRV for out-of-phase breaking are basically unchanged.

The values of t_3 for out-of-phase are in all cases two times the value for terminal fault T100.

E.6 Series reactor fault

Due to the very small inherent capacitance of a number of current limiting reactors, the natural frequency of transients involving these reactors can be very high. A circuit-breaker

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~~installed immediately in series with such type of reactor will face a high frequency TRV when clearing a terminal fault (reactor at supply side of circuit-breaker) or clearing a fault behind the reactor (reactor at load side of circuit-breaker). The resulting TRV frequency generally exceeds by far the standardized TRV values.~~

~~In these cases it is necessary to take mitigation measures, such as the application of capacitors in parallel to the reactors or connected to earth. The available mitigation measures are very effective and cost efficient [66]. It is strongly recommended to use them, unless it can be demonstrated by tests that a circuit-breaker can successfully clear faults with the required high frequency TRV.~~

~~In the opinion of the members of WG 35 of IEC SC17A, the service experience with TRV mitigation measures is so good and the costs involved are relatively so low, that it makes no sense to specify special requirements for circuit-breakers for this type of application.~~

~~E.7 TRV for last clearing poles / tests circuit topology~~

~~In Table 2 of IEC 62271-100:2001, multipliers for transient recovery voltage values for second and third clearing poles are given for circuit-breakers with rated voltages higher than 72,5 kV. Under NOTE 1, it is stated that for voltages equal to or lower than 72,5 kV, the values are under consideration.~~

~~For circuit-breakers with rated voltages equal to or lower than 72,5 kV, as not enough information is available to define values other than those specified for higher rated voltages, IEC SC17A has decided during its meeting in Montreal (CA), October 2003, to extend the validity of Table 2 to all rated voltages higher than 1 kV. The values will be revised later on when the results of studies are published.~~

E.1 General

This annex contains additional guidance for test circuits and procedures for type testing relevant to short-circuit making and breaking and switching performance of metal-enclosed and dead tank circuit-breakers. Other methods are not excluded, provided that they supply the correct stresses to the circuit-breaker

E.2 General description of special features and possible interactions

E.2.1 General

Interactions, which might influence the test results and cannot be taken into account by unit testing or single-pole testing, will require full-pole or three-pole testing, respectively.

E.2.2 Influence of the surrounding parts of a substation

Integrated parts, for example busbar sections, feeding cables, bushings, voltage transformers, and surge arresters, may influence the prospective stresses of the test circuit.

The influence of these integrated parts of the system depends on the test sequence. On the one hand, the large capacitance of surrounding elements reduces the stress on the circuit-breaker in the case of SLF and terminal fault ITRV, while, on the other hand, switching of capacitor banks may be more severe when low-impedance connections are used.

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E.2.3 Interaction between poles, interrupting units and enclosures

E.2.3.1 General

Various types of interactions of a different physical nature can arise between the elements of the circuit-breaker considered. The most important are:

– mechanical;
– electrostatic;
– electro-magnetic;
– gas dynamical.

The intensity of these interactions will, in most cases, depend on the individual design of the object under test. If a special interaction is eliminated in a given design, it is no longer necessary to adjust the tests to cover this interaction. In that case, it is necessary to demonstrate that the interaction under consideration has negligible influence on the test results, which could be made by model calculation, or experimental demonstration, using special measuring techniques. The same demonstration could be applied for the judgement of the degree of interaction that has to be represented in tests. In addition, consideration should be given to the case of a switching device where the configuration is not symmetrical in respect to the terminals.

E.2.3.2 Mechanical interaction

Subclauses 6.102.3 and 6.102.4 of IEC 62271-100:2008 apply.

E.2.3.3 Electrostatic interaction

Subclause 6.102.4.2.2 of IEC 62271-100:2008 applies.

The voltage distribution between units of multi-break circuit-breakers, as well as the electric field in the contact gap, is influenced by the high capacitances and especially by the presence of the earthed enclosure and of other live parts. It may be different in various test sequences and for different earthing conditions.

The voltage distribution between units can be determined as a function of the capacitance across the units and to the enclosure. The maximum voltage gradients across the interrupting gaps on the contact surfaces depend also on the number of interrupters and, for the same circuit-breaker, on the position of the interrupting unit in the circuit-breaker, even when an ideal voltage distribution is assumed.

The electrical field in the contact interrupting gap is influenced by the following factors:

– short distances between live parts and the enclosure;
– presence of adjacent live parts.

Here, the determination of a representative stress depends on the individual design of the circuit-breaker and on the location of the most critical stress area.

E.2.3.4 Electromagnetic interaction

Both single- and three-pole circuit-breakers can experience electromagnetic interaction, which may cause additional forces on the arcs and on moving parts. In the case of three poles in one enclosure, the interaction between phases is pronounced.

Induced currents and return currents in the enclosure may cause additional effects, for instance a voltage drop between earthed parts affecting auxiliary or protective equipment.

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E.2.3.5 Gas dynamical interaction

Hot, ionised and/or contaminated exhaust gases may influence the dielectric strength between poles in a common enclosure and between the pole(s) and the enclosure. Similar effects may occur between the units of a pole with more than one interrupting unit.

E.2.4 Unit testing

Particular precautionary measures regarding interaction shall be taken (see 6.102.4.2.1 b) of IEC 62271-100:2008).

The required voltage stresses during the unit testing are:

– the full-pole transient recovery voltage and recovery voltage between the relevant live parts and the enclosures. The recovery voltage should preferably be AC;
– the portion of these voltages, depending on the number of tested units and on the voltage distribution, across the unit(s) submitted to tests.

All units shall break the short-circuit current, which guarantees the correct interaction between units and the correct influence on the insulation between live parts and the enclosure.

The most common method is to use a third bushing to apply the TRV. Special care needs to be taken in regard to modification of dielectric or exhaust behaviour when using a third bushing since any additional part will have some influence.

This bushing, connected between the unit(s) under test and the voltage circuit, allows the use of the other unit(s) as auxiliary circuit-breakers. This bushing should not produce any mechanical, electrostatic, or magnetic interaction with the unit(s) under test.

The synthetic circuit is shown in IEC 62271-101, both for current and for voltage injection. It consists of:

– a conventional synthetic test circuit that gives the required portion of the total TRV between the terminals of the unit(s) under test u_B;
– an additional test circuit (synthetic, DC, or AC source) that energizes the enclosure, insulated from earth, with a suitable voltage u_E.

In IEC 62271-101 an example relevant to a half-pole test, shows the required voltage u_B, u_E and the resulting voltage u_A between the terminal of the auxiliary unit(s) connected to the current circuit and the enclosure. The full-pole voltage stresses are applied between the earthed terminal of the units under test and the enclosure.

If it is not possible to apply the voltage stresses u_B and u_E at the same time, a multipart testing procedure can be used (see 6.102.4.3 of IEC 62271-100:2008). In the first part, only the performance of the unit(s) under test is checked (the enclosure of the circuit-breaker is earthed). In the second part, the insulation between the live parts of the pole and the enclosure is checked. This can be done, for example, with all units breaking the short-circuit current, but at a reduced voltage (dependent on the available current source) and applying voltage between the insulated enclosure and the earth. At the moment when the TRV peak is produced, the instantaneous value of the applied voltage to the enclosure shall be equal to the differences between the "reduced voltage" and the total TRV peak to be applied between the stressed terminal and the enclosure.

Test circuits without the use of a third bushing exist. The required voltage across the unit under test is produced for example by the shunting with large capacitors. Other methods exist. The validity of such circuits in regard to thermal switching capability need to be carefully examined

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Attention should be paid that during the basic short-circuit test duties, the arcing times are not considerably at variance with those obtained during the thermal verification test.

NOTE 1 In the past, some unit testing has been carried out in a test circuit in which not all units break the short-circuit current. Such a test circuit can only be used for cases with negligible interaction, due to gas circulation. This is, however, mostly not the case and is also very difficult to prove.

In this circuit, a portion of the circuit-breaker has been short-circuited. It is assumed that this does not produce any mechanical, electrostatic, or electromagnetic interaction, The interaction due to gas circulation deserves special attention.

Appropriate synthetic test circuits are shown in IEC 62271-101, both for current and voltage injection.

The value and polarity of the voltage u_E to be applied to the enclosure are such that the resulting voltage between the energized terminal of the circuit-breaker and the enclosure is equal to the required value of the full-pole test voltage.

NOTE 2 Insulation between live parts and enclosures during making and breaking short-circuit currents for most circuit-breakers can be proved by short-circuit test duties T100s and T100a. Short-circuit test duties T10, T30 and T60 can be performed by conventional unit test procedures.

NOTE 3 To uncouple the control circuit of the circuit-breaker from the energized enclosure, the fibre-optics transmission technique can be applied successfully; the power required to operate the closing and trip coils can be provided by a turbine generator group driven by compressed air.

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Annex F
(informative)

Current and test-duty combination for capacitive current switching tests

F.1 General

Capacitive current switching tests are described in 6.111 of IEC 62271-100:2008.

They consist of line charging (LC), cable charging (CC) and capacitor bank (BC) switching tests.

Each test consists of two test duties:

– test-duty 1 (TD1), with a percentage of rated capacitive current between 10 % and 40 %;
– test-duty 2 (TD2), with the full rated capacitive current (≥ 100 %).

The capacitive current switching cases are covered by the following test-duties:

– line-charging current, TD1 LC1
– line-charging current, TD2 LC2
– cable-charging current, TD1 CC1
– cable-charging current, TD2 CC2
– capacitor bank current, TD1 BC1
– capacitor bank current, TD2 BC2

As specified in 6.111.9 of IEC 62271-100:2008, test-duties can be combined to demonstrate the performance of the circuit-breaker to cover several applications or ratings.

Some examples are here given considering different ratings.

F.2 Combination rules

In 6.111.9 of IEC 62271-100:2008, rules are given for combining different test-duties.

- voltage: the maximum voltage of the different test-duties has to be used;
- current: the combination rule changes with test-duty 1 and 2.
  – TD1:
  The rule to test with a current between 10 % and 40 % of the relevant rated capacitive current of the specific test-duty applies. Each current value fulfilling this rule can be used for a test combination and TD1 can cover two or more cases, otherwise TD1 shall be repeated with the appropriate current value;
  – TD2:
  The test current must be equal to or higher than the maximum rated value of the test-duties that are going to be combined. One TD2, performed with this current, covers the lower current ratings even if their rated current is much lower.
- operation: a CO operation covers an O operation;
- number of operations: the highest number has to be considered for the same test-duty.

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F.3 Examples

F.3.1 General

To exemplify the combination rules, the following three different cases are considered:

– Case 1: 145 kV, tested single-pole according to class C2 (see F.3.2);
– Case 2: 36 kV, tested three-pole according to class C2 (see F.3.3);
– Case 3: 245 kV, tested single-pole according to class C1 (see F.3.4).

There is more than one possibility to combine the test-duties applying the rules given by IEC 62271-100.

F.3.2 Case 1: 145 kV, tested single-pole according to class C2

F.3.2.1 General

From Table 9 of IEC 62271-100:2008 the following rated currents have been selected.

Rated voltage U_r 145 kV (r.m.s.)
Rated line-charging breaking current I_l 50 A(r.m.s.)
Rated cable charging breaking current I_c 160 A(r.m.s.)
Rated single capacitor bank breaking current I_{sb} 400 A(r.m.s.)

The capacitive voltage factors are: 1,4 for LC, 1,2 for CC and 1,0 for BC.

The required test duties are summarized in Table F.1.

Table F.1 – Summary of required test-duties for covering the capacitive current switching without any test-duty combination

Test-duty	k_c	I_n A	I_{min} A	I_{max} A	Total number of operations	Number of operations	Number of CO operations	Distributed operations	Number of electrical degrees	Number of operations with minimum arcing time	Number of operations with maximum arcing time	Pressure
LC1	1,4	50	5	20	48	48	0	24	15	12	0	Min.
LC2	1,4	50	50		48	24	24	24	30	12	0	Rated
CC1	1,2	160	16	64	48	48		24	15	12	0	Min.
CC2	1,2	160	160		48	24	24	24	30	12	0	Rated
BC1	1,0	400	40	160	48	48		36	15	12	0	Min.
BC2	1,0	400	400		120	0	120	36	15	84	0	Rated

The total number of shots without any test-duty combination is 360.

Applying the combination rules, the complete capacitive current switching test program can be covered with one TD2 and two TD1 (TD1a, TD1b) or one TD1 and two TD2 (TD2a and TD2b).

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F.3.2.2 Test-duty 2 combination

F.3.2.2.1 General

Depending on the combination it can be decided to perform TD2 with the most severe capacitive voltage factor and the maximum rated current and the highest number of shots, or perform two TD2 as follows (see Figure F.1):

– one covering only BC2;
– one covering LC2, CC1 and BC1 at the same time (see TD1/TD2 combination).

In this case the quenching medium pressure has to be set at minimum as required for TD1.

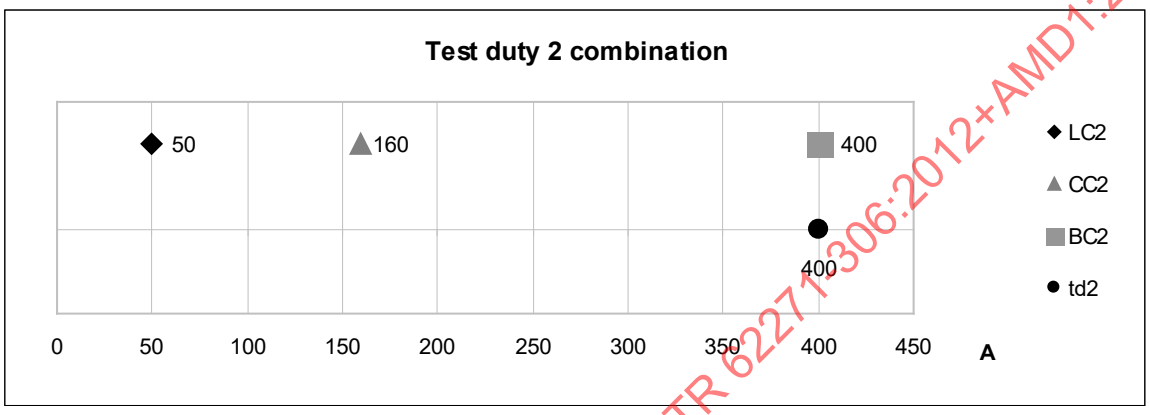

Figure F.1 – Test-duty 2 combination for Case 1

Table F.2 – Case where TD2 covers LC2, CC2 and BC2

	LC2	CC2	BC2	combination value
Capacitive voltage factor	1,4	1,2	1,0	1,4
Rated current A	50	160	400	400
Number of operations	48	48	120	120
Operation type	CO	CO	CO	CO

If the TD2 combination only needs to cover CC2 and BC2 it can be performed at lower voltage (i.e. by using a capacitive voltage factor of 1,2 instead of 1,4). In this case a second test-duty has to be performed covering LC2. This will be shown in the TD1/TD2 combination.

Table F.3 – Combination values for the case where TD2 covers only CC2 and BC2

	LC2	CC2	BC2	Combination value
Capacitive voltage factor		1,2	1,0	1,2
Rated current A		160	400	400
Number of operations		48	120	120
Operation type		CO	CO	CO

LC2 will be covered by an additional TD2.

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F.3.2.2.2 TD1 combination

For TD1 the current range is 10 % – 40 % of the rated capacitive current, which means that two test-duties are needed, since it is not possible to obtain a current value fulfilling this requirement for current of 50 A, 160 A and 400 A.

There are 2 possibilities for the combination:

a) Combining CC1 and BC1 selecting a current between 10 % of BC1 and 40 % of CC1 and adding then a TD1 test-duty with current between 10 % and 40 % of LC1.

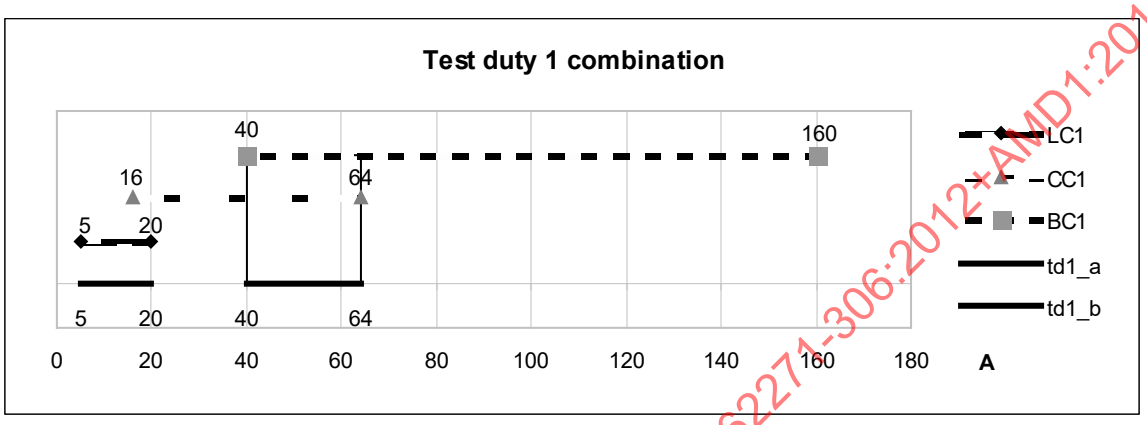

Figure F.2 – TD1 combination for case a)

Table F.4 – Combination values for case a): the combined TD1 covers CC1 and BC1

	LC1	CC1	BC1	combination value
Capacitive voltage factor	1,4	1,2	1,0	1,2
Rated current A	5-20	16-64	40-160	40-64
Number of operations	48	48	48	48
Operation type	O	O	O	O

An additional TD1 is needed to cover LC1.

b) Combining LC1 and CC1 selecting a current between 10 % of CC1 and 40 % of LC1 and adding then a TD1 test duty with a current between 10 % and 40 % of BC1.

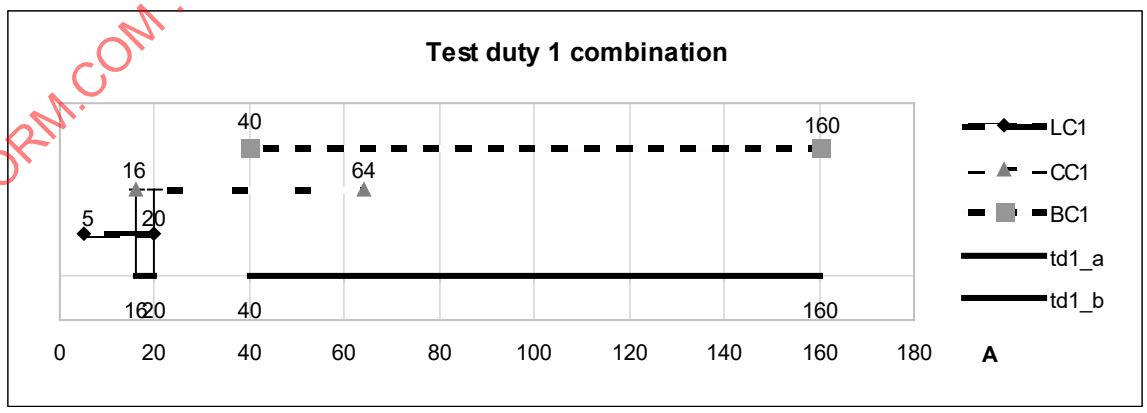

Figure F.3 – TD1 combination for case b)

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Table F.5 – Combination values for case b): the combined TD1 covers LC1 and CC1

	LC1	CC1	BC1	Combination value
Capacitive voltage factor	1,4	1,2	1,0	1,4
Rated current A	5-20	16-64	40-160	16-20
Number of operations	48	48	48	48
Operation type	O	O	O	O

An additional TD1 is needed to cover BC1.

F.3.2.3 TD1/TD2 combination

TD2 is carried out covering LC2 as well as CC1 and BC1.

For that reason the current value has to be selected between 50 A and 64 A, and the capacitive voltage factor should be that of LC1 (i.e. 1,4).

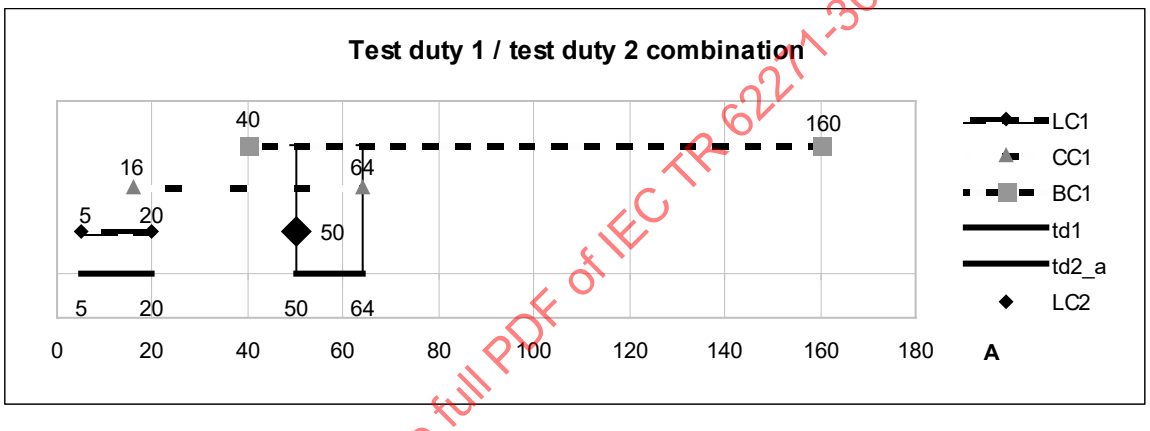

Figure F.4 – TD1/TD2 combination for Case 1

Table F.6 – Combination values for a TD2 covering LC2, CC1 and BC1

	LC2	CC1	BC1	Combination value
Capacitive voltage factor	1,4	1,2	1,0	1,4
Rated current A	>50	16-64	40-160	50-64
Number of operations	48	48	48	48
Operation type	CO	O	O	CO

F.3.2.4 Combination summary

The complete test program LC, CC and CC that would consist of 360 operations can be fulfilled with one of the two following combinations having 216 operations.

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Table F.7 – Summary of the possible test-duty combination for a 145 kV circuit-breaker, tested single-pole according to class C2

Test-duty	k_c	I_n A	I_{min} A	I_{max} A	Total number of operations	Number of O operations	Number of CO operations	Distributed operations	Number of electrical degrees	Number of operations with minimum arcing time	Number of operations with maximum arcing time	Pressure
Full test program for 145 kV circuit-breaker (LC, CC and BC), class C2, tested single-pole												
LC1	1,4	50	5	20	48	48	0	24	15	12	0	Min.
LC2	1,4	50	50		48	24	24	24	30	12	0	Rated
CC1	1,2	160	16	64	48	48		24	15	12	0	Min.
CC2	1,2	160	160		48	24	24	24	30	12	0	Rated
BC1	1,0	400	40	160	48	48		36	15	12	0	Min.
BC2	1,0	400	400		120	0	120	36	15	84	0	Rated
Combination 1: LC1; CC1 and BC1; LC2, CC2 and BC2												
TD1a	1,4		5	20	48	48	0	24	15	12		Min.
TD1b	1,2		40	64	48	48	0	24	15	12		Min.
TD2	1,4		400		120	0	120	36	15	84		Rated
Combination 2: LC1 and CC1; BC1; LC2, CC2 and BC2												
TD1a	1,4		16	20	48	48	0	24	15	12		Min.
TD1b	1,0		40	160	48	48	0	24	15	12		Min.
TD2	1,4		400		120	0	120	36	15	84		Rated
Combination 3: LC1; CC1, BC1 and LC2; CC2 and BC2												
TD1	1,4		16	20	48	48	0	24	15	12		Min.
TD2a	1,4		50	64	48	0	48	24	15	12		Min.
TD2b	1,2		400		120	0	120	36	15	84		Rated

F.3.3 Case 2: 36 kV, tested three-pole according to class C2

F.3.3.1 General

From Table 9 of IEC 62271-100:2008 the following rated currents have been selected:

Rated voltage U_r 36 kV (r.m.s.)
Rated line-charging breaking current I_l 10 A(r.m.s.)
Rated cable charging breaking current I_c 50 A(r.m.s.)
Rated single capacitor bank breaking current I_{sb} 400 A(r.m.s.)

Since in this case three-pole tests are considered, the earthing connections described in 6.111.4 and 6.111.5 shall be followed.

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Table F.8 – Neutral connection prescriptions for three-phase capacitive tests

	Neutral of supply circuit	Neutral of the capacitor
BC	Earthed	U_r < 52 kV isolated U_r ≥ 52 kV as in reality
LC and CC	According to the system k_{pp} = 1,5: Isolated k_{pp} = 1,3: Effectively earthed	U_r < 52 kV $C_1 = 3 \times C_0$ U_r ≥ 52 kV $C_1 = 2 \times C_0$

The required test-duties are summarized in Table F.9.

Table F.9 – Summary of required test-duties for covering the capacitive current switching without any test duty combination

Test-duty	k_c	I_n A	I_{min} A	I_{max} A	Total number of operations	Number of operations	Number of CO operations	Distributed operations	Number of electrical degrees	Number of operations with minimum arcing time	Number of operations with maximum arcing time	Pressure
LC1	1,4	10	1	4	24	24	0	12	15	12	0	Min.
LC2	1,4	10	10		24		24	12	15	12	0	Rated
CC1	1,2	50	5	20	24	24	0	12	15	12	0	Min.
CC2	1,2	50	50		24		24	12	15	12	0	Rated
BC1	1,0	400	40	160	24	24	0	12	15	12	0	Min.
BC2	1,0	400	400		80		80	16	15	64	0	Rated

The total number of operations without any test-duty combination is 200.

Applying the combination rules the complete capacitive current switching test program can be covered in this case with either one test-duty 2 (TD2) and three test-duties 1 (TD1, TD1b, TD1c), or with two test-duties 1 covering LC1 and CC1 and 2 test-duties 2 covering CC2 and BC1 and BC2.

F.3.3.2 Test-duty 2 combination

Depending on the combination, it can be decided to perform TD2 only with the most severe connection of the neutral point of the supply circuit, the maximum rated current and the highest number of shots, or perform two test-duties 2 as follows:

– one test-duty covering only BC2;
– another test-duty CC2 and BC1 at the same time (see TD1/TD2 combination).

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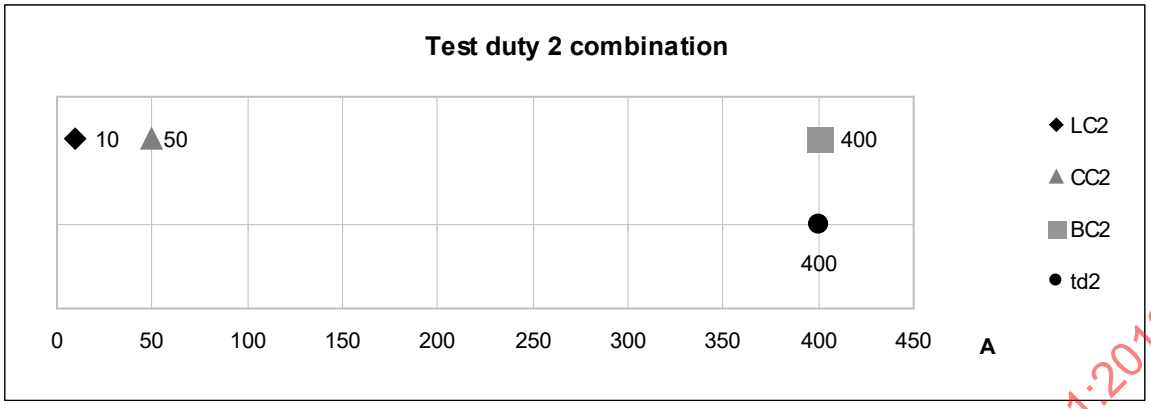

Figure F.5 – TD2 combination for Case 2

a) Case with only one TD2.

Table F.10 – Combination values for a TD2 covering LC2, CC2 and BC2

	LC2	CC2	BC2	Combination value
Neutral of supply circuit	unearthed	unearthed	earthed	unearthed
Rated current (A)	10	50	400	400
Number of operations	24	24	80	80
Operation type	CO	CO	CO	CO

b) If 2 test-duties are performed it is possible to use one covering LC2, CC2 and BC1 (see F.3.3.4) and the other covering only BC2. The test-duty covering BC2 can be performed with earthed neutral point of the supply circuit.

Table F.11 – Values for the additional TD2 for covering only BC2

	BC2	Combination value
Neutral of supply circuit	earthed	earthed
Rated current (A)	400	400
Number of operations	80	80
Operation type	CO	CO

F.3.3.3 Test-duty 1 combination

With the given ratings there is no possibility to combine TD1 test-duties since there is no overlapping of the 10 % – 40 % current ranges.

A TD1 has to be performed 3 times for each current value in the range of 10 % – 40 % of the relevant current rating.

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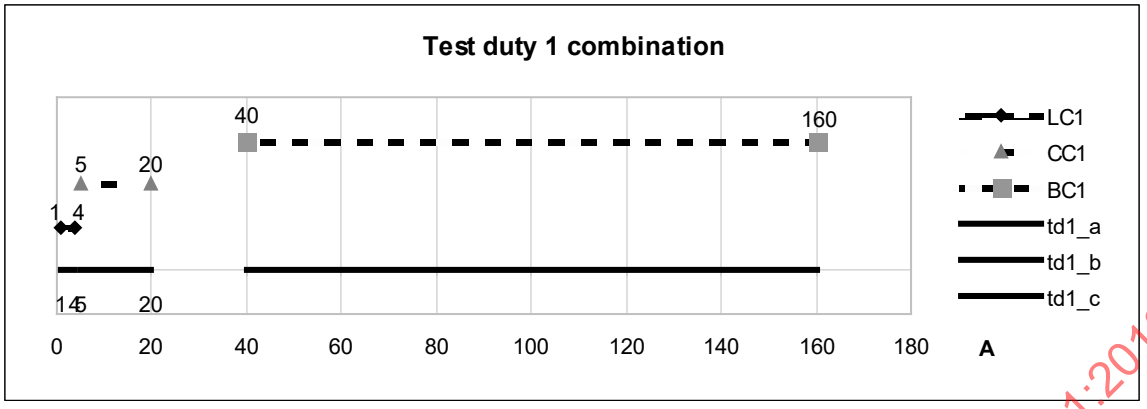

No combination possible since there is no overlapping of the three current ranges.

Figure F.6 – TD1 combination

Table F.12 – Values for the three a TD1 that shall be performed since no combination is possible

Test-duty	I_{min} A	I_{max} A	Total number of operations	Number of O operations	Number of CO operations	Distributed operations	Number of electrical degrees	Number of operations with minimum arcing time	Number of operations with maximum arcing time	Pressure
TD1a	1	4	24	24	0	12	15	12	0	Min.
TD1b	5	20	24	24	0	12	15	12	0	Min.
TD1c	40	160	24	24	0	12	15	12	0	Min.

F.3.3.4 TD1/TD2 combination

In this case a TD2 is use to cover TD1. This means that the neutral point connection shall be the same as for TD1 and pressure has to be set to the minimum.

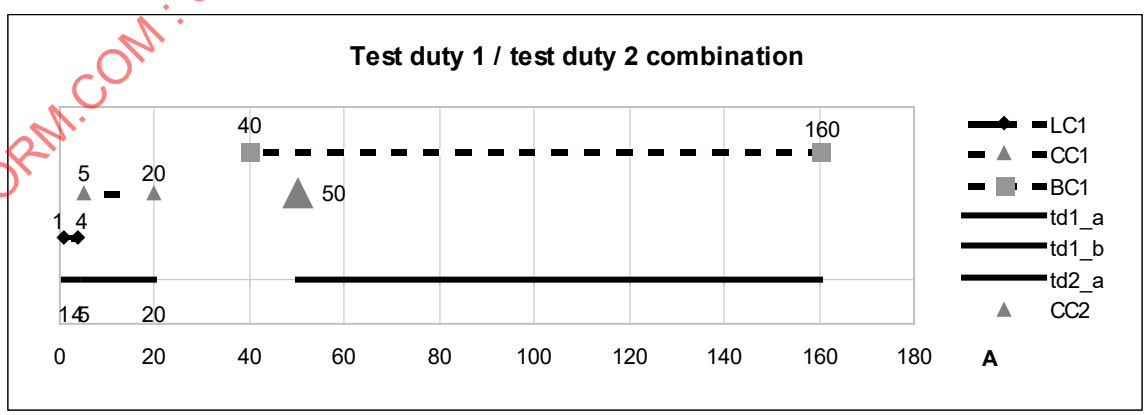

Figure F.7 – TD1/TD2 combination for Case 2

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Table F.13 – Combination values for a TD2 covering LC2, CC2 and BC1

	LC2	CC2	BC1	combination value
Neutral of supply circuit	unearthed	unearthed	earthed	unearthed
Rated current A	>10	>50	40-160	50-160
Number of operations	24	24	24	24
Operation type	CO	CO	O	CO

F.3.3.5 Combination summary

The complete test program LC, CC and BC that would consist of 200 operations can be fulfilled with the following two combinations consisting of 152 operations.

Table F.14 – Summary of the possible test-duty combination for a 36 kV circuit-breaker tested under three-phase conditions according to class C2

Test-duty	Neutral	I_n A	I_{min} A	I_{max} A	Total number of operations	Number of O operations	Number of CO operations	Distributed operations	Number of electrical degrees	Number of operations with minimum arcing time	Number of operations with maximum arcing time	Pressure
Full test program for 36 kV circuit-breaker (LC, CC and BC), class C2, tested three-pole												
LC1	unearthed	10	1	4	24	24		12	15	12	0	Min.
LC2	unearthed	10	10		24		24	12	15	12	0	Rated
CC1	unearthed	50	5	20	24	24		12	15	12	0	Min.
CC2	unearthed	50	50		24		24	12	15	12	0	Rated
BC1	earthed	400	40	160	24	24		12	15	12	0	Min.
BC2	earthed	400	400		80		24	12	15	64	0	Rated
Combination 1: LC1; CC1; BC1; LC2, CC2 and BC2												
TD1a	unearthed		1	4	24	24	0	12	15	12	0	Min.
TD1b	unearthed		5	20	24	24	0	12	15	12	0	Min.
TD1c	unearthed		40	160	24	24		12	15	12	0	Min.
TD2	earthed		400		80	0	80	16	15	64	0	Rated
Combination 2: LC1; CC1; LC2, CC2 and BC1; BC2												
TD1a	unearthed		1	4	24	24		12	15	12	0	Min.
TD1b	unearthed		5	20	24	24		12	15	12	0	Min.
TD2a	unearthed		50	160	24		24	12	15	12	0	Min.
TD2b	earthed		400		80		80	16	15	64	0	Rated

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F.3.4 Case 3: 245 kV, tested single-pole according to class C1

F.3.4.1 General

From Table 9 of IEC 62271-100:2008 the following rated currents have been selected.

Rated voltage U_r 245 kV (r.m.s.)
Rated line-charging breaking current I_l 125 A(r.m.s.)
Rated cable charging breaking current I_c 250 A(r.m.s.)
Rated single capacitor bank breaking current I_{sb} 400 A(r.m.s.)

The capacitive voltage factors are also different being: 1,4 for LC, 1,2 for CC and 1,0 for BC.

The required test-duties are summarized in Table F.15.

Table F.15 – Summary of required test-duties for covering the capacitive current switching without any test-duty combination

Test-duty	k_c	I_n A	I_{min} A	I_{max} A	Total number of operations	Number of operations	Number of CO operations	Distributed operations	Number of electrical degrees	Number of operations with minimum arcing time	Number of operations with maximum arcing time	Pressure
LC1	1,4	125	12,5	50	24	24		12	30	6	6	Rated
LC2	1,4	125	125		24		24	12	30	6	6	Rated
CC1	1,2	250	25	100	24	24		12	30	6	6	Rated
CC2	1,2	250	250		24		24	12	30	6	6	Rated
BC1	1,0	400	40	160	24	24		12	30	6	6	Rated
BC2	1,0	400	400		24		24	12	30	6	6	Rated

The number of operations is now smaller since the circuit-breaker is tested according to class C1.

The total number of shots without any test-duty combination is 144.

Applying the combination rules, the complete capacitive current switching test program can be covered with one TD2 and one TD1.

This is possible since the current rating of line-charging, cable-charging and capacitor bank are closer to each other in comparison to the previous example, which enables a common overlapping for all of three test-duties 1: LC1, CC1 and BC1.

F.3.4.2 Test-duty 2 combination

All three test-duties 2 can be covered with one test TD2 that shall be performed with the highest voltage factor, the maximum rated current and the highest number of shots.

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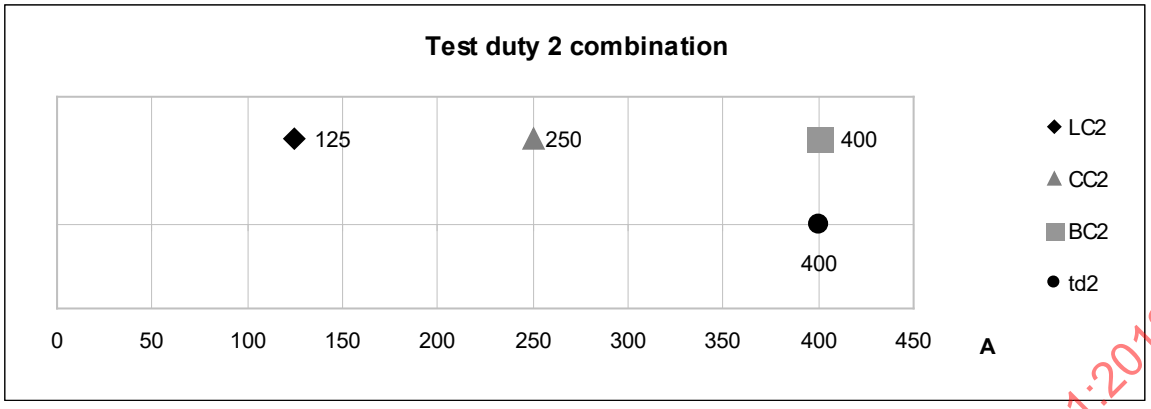

Figure F.8 – TD2 combination for Case 3

Table F.16 – Combination values for a TD2 covering LC2, CC2 and BC2

	LC2	CC2	BC2	Combination value
Voltage factor	1,4	1,2	1,0	1,4
Rated current A	125	250	400	400
Number of operations	24	24	24	24
Operation type	CO	CO	CO	CO

F.3.4.3 TD1 combination

For TD1 in this case it is possible to find a range of tested current that can fulfil at the same time the 10 % – 40 % rule of every capacitive current defined for line-charging, cable-charging and capacitor bank.

As shown in Figure F.9, selecting a current in the range between 40 A and 50 A it is possible to stay inside every 10 % – 40 % range.

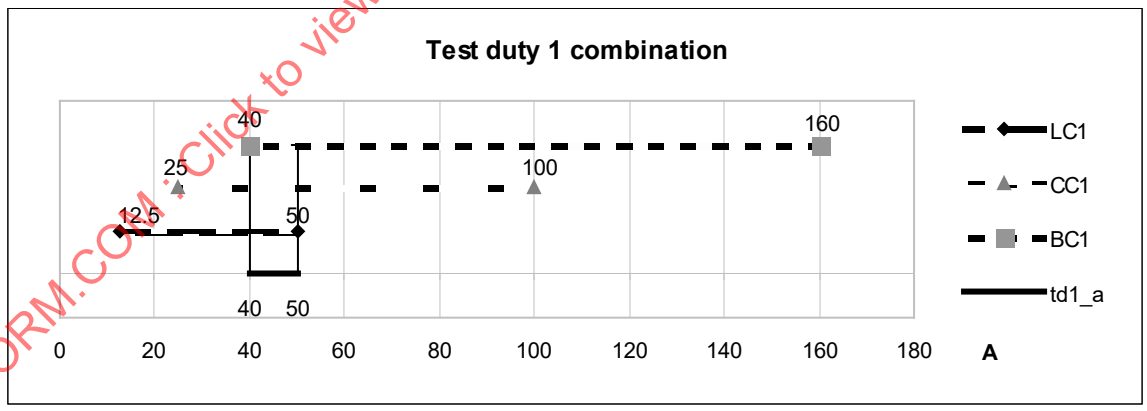

Figure F.9 – TD1 combination for Case 3

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Table F.17 – Combination values for a TD1 covering LC1, CC1 and BC1

	LC1	CC1	BC1	Combination value
Voltage factor	**1,4**	1,2	1,0	1,4
Rated current A	12.5-50	25-100	40-160	40-50
Number of operations	24	24	24	24
Operation type	O	O	O	O

F.3.4.4 Combination summary

The complete test program LC, CC and BC that would consist of 144 operations can be fulfilled with the following combination consisting of 48 operations.

Table F.18 – Summary of the possible test-duty combination for a 245 kV circuit-breaker, tested single-phase according to class C1

Test-duty	k_c	I_n A	I_{min} A	I_{max} A	Total number of operations	Number of O operations	Number of CO operations	Distributed operations	Number of electrical degrees	Number of operations with minimum arcing time	Number of operations with maximum arcing time	Pressure
Full test program for 245 kV circuit-breaker (LC, CC and BC), class C1, tested single-pole												
LC1	1,4	125	12,5	50	24	24		12	30	6	6	Rated
LC2	1,4	125	125		24		24	12	30	6	6	Rated
CC1	1,2	250	25	100	24	24		12	30	6	6	Rated
CC2	1,2	250	250		24		24	12	30	6	6	Rated
BC1	1,0	400	40	160	24	24		12	30	6	6	Rated
BC2	1,0	400	400		24		24	12	30	6	6	Rated
Combination 1: LC1; CC1 and BC1; LC2, CC2 and BC2												
TD1	1,4		40	50	24	24		12	30	6	6	Rated
TD2	1,4		400		24		24	12	30	6	6	Rated

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Annex G
(informative)

Grading capacitors

G.1 Grading capacitors

G.1.1 General

Grading capacitors are accessories to high-voltage circuit-breakers and are mainly used to control the voltage distribution across the individual breaking units of a multi-unit circuit-breaker. They are mounted in parallel with the breaking units.

The presence of additional capacitance across the circuit-breaker contacts modifies the line side TRV in the case of short-line faults. For this reason, capacitors can also be found on single-unit circuit-breakers. In the latter case, they are mounted in parallel with the breaking unit or to earth. Their function is solely to influence the line side TRV, they do not participate in voltage distribution. This type of application is not dealt with in this annex.

Grading capacitors consist of a number of capacitor packages inside an insulated housing. Design and test requirements are given in IEC 62146-1 [9].

G.1.2 Capacitor characteristics

G.1.2.1 Equivalent circuit

A possible a.c. equivalent circuit of a capacitor can be approached by the circuit given in Figure G.1.

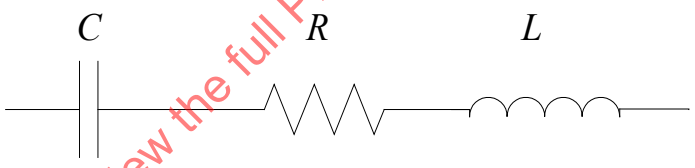

Figure G.1 – Equivalent circuit of a grading capacitor

In Figure G.1 C represents the capacitance of the grading capacitor and R the losses and L the internal inductance.

G.1.2.2 Tanδ, power factor and quality factor

For the determination of tanδ, power factor and quality factor, the inductance in Figure G.1 can be neglected. The equivalent circuit is given in Figure G.2.

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9 To be published.

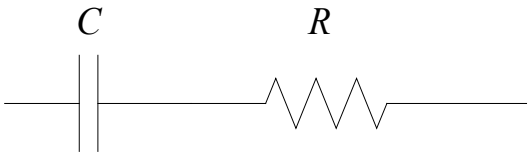

Figure G.2 – Equivalent circuit for determination of tanδ, power factor and quality factor

Figure G.3 shows the vector diagram of the capacitor impedances.

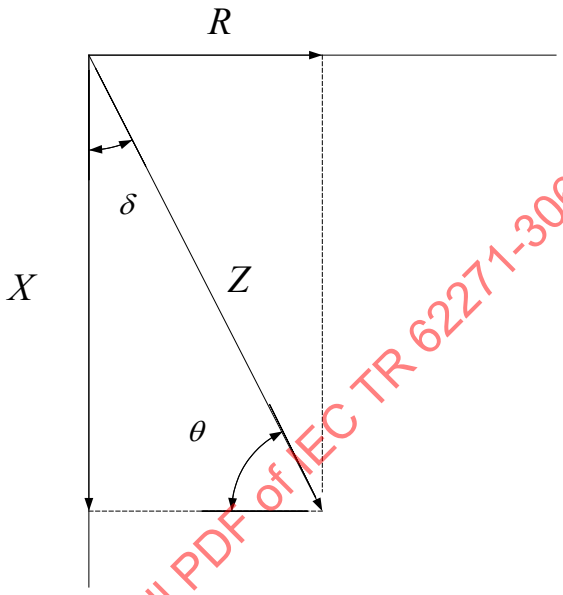

Figure G.3 – Vector diagram of capacitor impedances

The following capacitor characteristics can be derived:

$$X = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

$$Z = \sqrt{R^2 + X^2} = \sqrt{R^2 + \frac{1}{\omega^2 C^2}}$$

The dielectric loss angle is δ (see Figure G.3). The dissipation factor $\tan\delta = \frac{R}{X} = \omega RC$ is also known as Dissipation Factor (DF).

Power factor (PF) = $\cos\theta = \sin\delta = R/Z$.

For relatively low values of R, Z is approximately equal to X, in other words: δ, $\sin\delta$ and $\tan\delta$ are equivalent. As a result, the power factor and dissipation factor are nearly equal.

The quality factor $Q = X/R = 1/\tan\delta$.

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G.1.2.3 Grading capacitor resonance frequency

The grading capacitor has its own internal resonance frequency at the point where the impedances cancel each other. To determine the internal resonance frequency, the circuit shown in Figure G.1 is used and the resistance is neglected.

The internal resonance f_i frequency is: $f_i = \frac{1}{2\pi\sqrt{LC}}$

G.1.3 Application considerations

G.1.3.1 Shocks and vibration

Grading capacitors mounted on circuit-breakers are exposed to shocks and vibrations as a result of the operation of the circuit-breaker. The manufacturer should ensure that the grading capacitors have been properly type tested.

G.1.3.2 Ferroresonance

When a circuit-breaker with grading or parallel capacitors is installed in a substation, the capacitors may form a resonance circuit together with any ferromagnetic inductance (i.e. magnetic instrument transformers and power transformers) present in the substation. This can give rise to ferroresonance in case the circuit-breaker is in the open position.

The risk of ferroresonance increases with increasing grading capacitance values.

G.1.3.3 Shunt reactors

Shunt reactor switching may expose the grading capacitors to the effect of a re-ignition of the interrupter. The steep transient of the second parallel oscillation stresses the capacitors and may puncture the dielectric of the individual capacitor packages inside the grading capacitor.

G.1.3.4 Exposure to d.c. voltages

In applications where capacitive currents are switched (capacitor banks, no-load overhead lines and no-load cables), the load side of the circuit-breaker remains at a d.c. voltage whereas the source side is exposed to a power frequency voltage. In such applications the grading capacitor may be exposed to a d.c. voltage.

The grading capacitor has to withstand the discharge of the trapped charge in the grading capacitor during closing of the circuit-breaker or restrike during opening.

G.1.3.5 Consideration of using grading capacitor in low temperature climates

Grading capacitors using an oil/film or oil/paper or oil/paper and film dielectric system fitted on circuit-breakers intended for low temperature applications, generally when $T_L \leq$ -40 °C, should be properly designed and tested to withstand the dielectric stresses produced by system overvoltages and nominal system voltage. This is an issue for circuit-breakers intended to be used in open position for relatively long periods of time (for example for shunt capacitor bank or for shunt reactor circuit-breakers).

At low temperatures, the viscosity of the dielectric liquid used increases and may no longer be able to extinguish the partial discharges that may occur when a system overvoltage is applied to an open circuit-breaker. In case that the partial discharges cannot be extinguished when the applied voltage returns to nominal system voltage, this may lead to premature element(s) failure(s) within the grading capacitor.

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A special voltage withstand test at low ambient air temperature as defined in IEC 62146-1[10] is required to demonstrate the performance of a grading capacitor for use in low temperature climate conditions.

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[10] To be published.

Annex H
(informative)

Circuit-breakers with opening resistors

H.1 General

This annex is applicable to circuit-breakers in which a resistor is inserted in series with the circuit to be interrupted. This resistor is connected in parallel to the main interrupter at least for breaking operations. During interruption the main interrupter transfers the current to the resistor and then the resistor interrupters connected in series to the resistor break the remaining current.

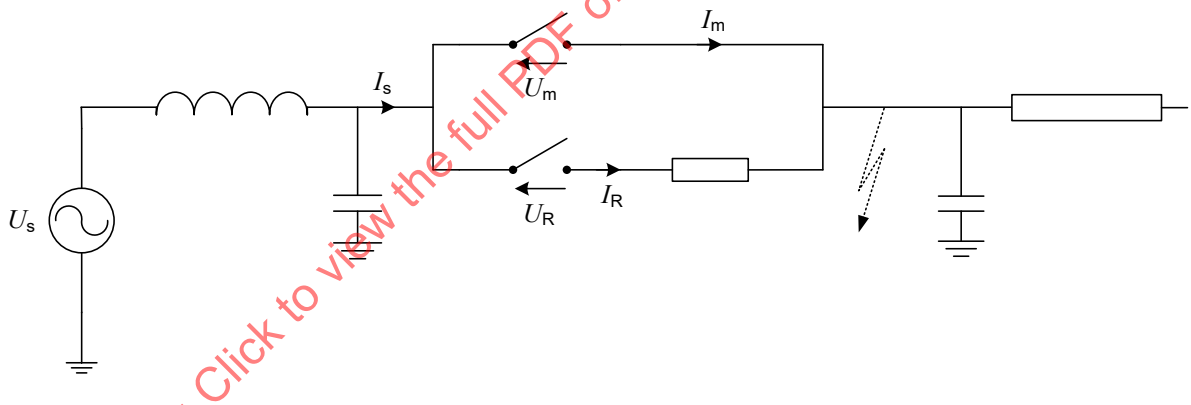
CIGRE WG A3.22 has reviewed the phenomena of breaking operation with opening resistors. The results of this review are published in [67] and [68] and other technical papers. The purpose of this annex is to provide guidance in the use of Annex R of IEC 62271-100:2008, Amendment 1, by indicating basic consideration and show practical examples.

Opening resistors are used for various situations, such as:

a) limitation of switching overvoltages. In case of application at rated voltages of 800 kV and above the main reason for using opening resistors;

b) increasing short-line fault interruption capability. Mainly used for air blast circuit-breakers.

A typical system configuration is shown in Figure H.1.



Key

I_m	Current through the main interrupter	U_m	Voltage across the main interrupter
I_R	Current through the resistor	U_R	Voltage across the resistor interrupter
I_s	Source side current	U_s	Source side voltage

Figure H.1 – Typical system configuration for breaking with opening resistors

H.2 Background of necessity of overvoltage limitation

Application of closing and opening resistors can reduce overvoltages not only phase-to-earth but also between phases at the remote terminal. It may not be possible to limit overvoltages by surge arresters. There are no effective measures to limit overvoltages associated with earth faults, except those near substations that can be reduced by surge arresters [67].

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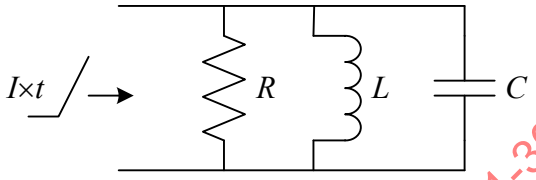
H.3 Basic theory on the effect of opening resistors

H.3.1 General

There are several methods to estimate the effect of the insertion of an opening resistor into a circuit for short-circuit current breaking. Analysis by electromagnetic transient programs is widely used. Detailed calculation is possible but it depends on the analytical model. Another method is using simple LCR circuit. This method is useful to understand the basic characteristics of the effect of the resistors. This method is described in H.3.2. Another method is using Laplace transformation applying TRV envelopes. This is explained in H.3.3.

H.3.2 RLC method

Figure H.2 shows the circuit diagram used for the RLC method.



Key

R	Resistor
L	Inductance
C	Capacitance
$I \times t$	Current ramp injected into the circuit

Figure H.2 – Circuit diagram used for the RLC method, ramp current injection

To calculate the TRV, the following equations apply:

Initial conditions: $u(0) = 0$ and $\frac{\mathrm{d}u(0)}{\mathrm{d}t} = 0$

$$\frac{\mathrm{d}^2u}{\mathrm{d}t^2} + \frac{1}{RC}\frac{\mathrm{d}u}{\mathrm{d}t} + \frac{1}{LC}u = \frac{I}{C} \tag{H.1}$$

and

$$d_\mathrm{p} = \frac{R_\mathrm{cd}}{R}, \text{ with } R_\mathrm{cd} = 0{,}5\sqrt{\frac{L}{C}} = 0{,}5Z \tag{H.2}$$

$d_\mathrm{p} > 1 \rightarrow R < R_\mathrm{cd}$: overdamped case

$$u(t) = \left[1 - e^{-d_\mathrm{p} t_\mathrm{g}}\left(\cosh\sqrt{d_\mathrm{p}^2 - 1} \times t_\mathrm{g} + \frac{d_\mathrm{p}}{\sqrt{d_\mathrm{p}^2 - 1}}\sinh\sqrt{d_\mathrm{p}^2 - 1} \times t_\mathrm{g}\right)\right] \tag{H.3}$$

$d_\mathrm{p} = 1 \rightarrow R = R_\mathrm{cd}$: critically damped case

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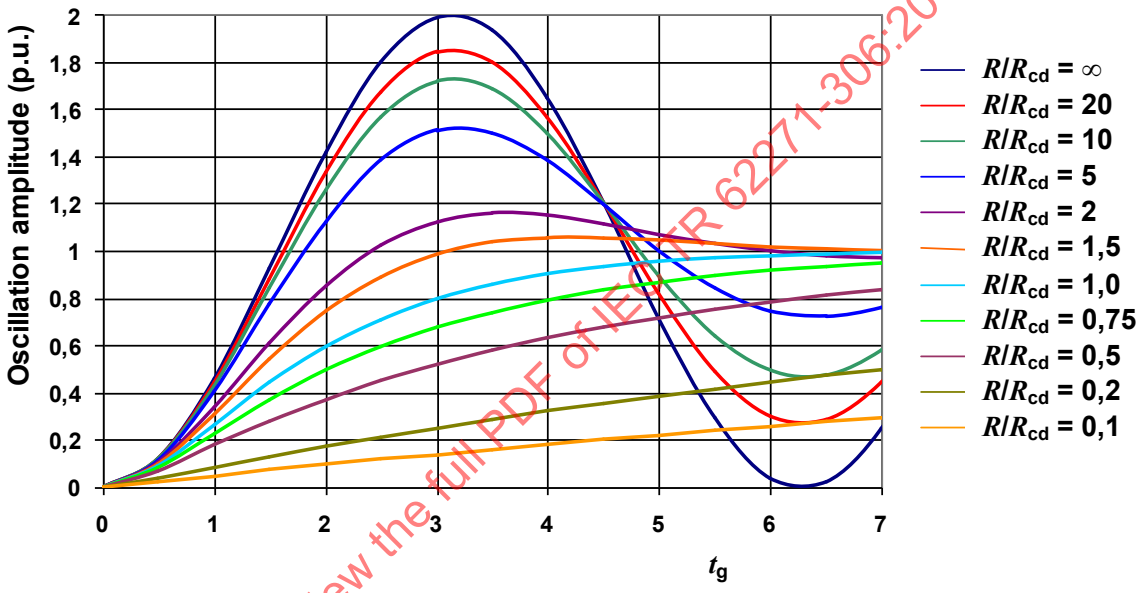
$$u(t) = 1 - e^{-t_g}\left(1 + t_g\right) \tag{H.4}$$

$d_p < 1 \rightarrow R > R_{cd}$: underdamped case

$$u(t) = \left[1 - e^{-d_p t_g}\left(\cos\sqrt{1-d_p^2} \times t_g + \frac{d_p}{\sqrt{1-d_p^2}}\sin\sqrt{1-d_p^2} \times t_g\right)\right] \tag{H.5}$$

NOTE t_g is the generic time given by $t_g = t/\sqrt{LC}$, where t is the real time.

Figure H.3 shows the relationship between the TRV peak and the critical damping.



Key

R	Equivalent resistance: Opening resistor in parallel with the circuit resistance
R_{cd}	Critical damping resistance
t_g	Generic time given by $t_g = t/\sqrt{LC}$ where t is the real time

Figure H.3 – Relationship between TRV peak and critical damping

H.3.3 Laplace transform

As shown in Figure H.4, any kind of waveshape, approximated by superimposed ramp elements looking at each time step (a uniform time step is suggested for the following calculations) can be represented by a polynomial in the Laplace domain as follows.

$$F(s) = \left(\frac{1}{s^2}\right)\left(F_0 + F_1 e^{-Ts} + F_2 e^{-2Ts} + F_3 e^{-3Ts} + F_4 e^{-4Ts} + \ldots\ldots\ldots\right) \tag{H.6}$$

where

s is the Laplace operator;

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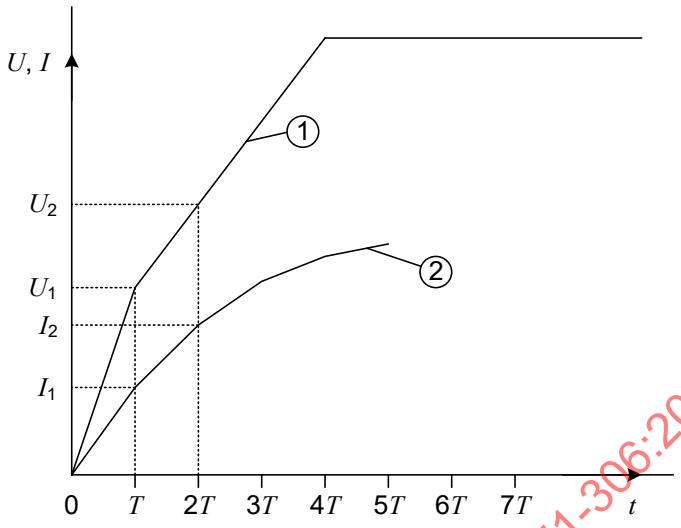
$F(s)$ is the circuit response in the Laplace domain;

F_i is a constant;

T is a time step in the Laplace domain.



Key

1	TRV
2	Injected current
T	Time step
U	Voltage
I	Injected current

Figure H.4 – Approximation by superimposed ramp elements

The TRV can be described by the following equation:

TRV = [Injected current]×[Circuit function]

In the Laplace domain the following equations apply:

$$TRV(s) = \left(\frac{1}{s^2}\right)\left(U_0 + U_1 e^{-Ts} + U_2 e^{-2Ts} + U_3 e^{-3Ts} + U_4 e^{-4Ts} + \ldots\ldots\right) \quad \text{(H.7)}$$

$$I(s) = \left(\frac{1}{s^2}\right)\left(I_0 + I_1 e^{-Ts} + I_2 e^{-2Ts} + I_3 e^{-3Ts} + I_4 e^{-4Ts} + \ldots\ldots\right) \quad \text{(H.8)}$$

where

s is the Laplace operator;

U_i, I_i are the voltage and current coefficients in the Laplace domain, respectively.

Applying the concept shown before also in Laplace domain, the circuit function $Z(s)$ is obtained from Equation (H.7) divided by Equation (H.8),

$$Z(s) = \frac{TRV(s)}{I(s)} = \left(Z_0 + Z_1 e^{-Ts} + Z_2 e^{-2Ts} + Z_3 e^{-3Ts} + Z_4 e^{-4Ts} + \ldots\ldots\right) \quad \text{(H.9)}$$

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Any modifying condition, to be applied, can be introduced to Equation (H.7) and/or (H.8) resulting in the same type of equations.

For the inverse transformation process to the TRV in the time domain, the following equations apply:

$$TRV(t) = L^{-1}[I(s) \times Z(s)] \tag{H.10}$$

where $[I(s) \times Z(s)]$ is expressed as:

$$I(s) \times Z(s) = \left(\frac{1}{s^2}\right)\left(F_0 + F_1 e^{-Ts} + F_2 e^{-2Ts} + F_3 e^{-3Ts} + F_4 e^{-4Ts} + ...\right) \tag{H.11}$$

Then the inverse transformation process can be simplified, where F_i corresponds to the change of slope of TRV at the relevant time step points.

When using an opening resistor Equation (H.9) for $Z(s)$ should be shunted by a resistor R (connected in parallel), this gives:

$$ZR(s) = \frac{R \times Z(s)}{R + Z(s)} = \left(ZR_0 + ZR_1 e^{-Ts} + ZR_2 e^{-2Ts} + ZR_3 e^{-3Ts} + ZR_4 e^{-4Ts} + ...\right) \tag{H.12}$$

The TRV modified by the resistor can be calculated using the product of Equation (H.8) and (H.12) and also applying the inverse transformation.

H.3.4 Examples

H.3.4.1 Example using the RLC method

Initial condition:

– Rated voltage U_r 1 100 kV
– Rated short-circuit breaking current I_{sc} 50 kA
– Rated frequency f_r 50 Hz

Typical waveshapes are given in Figure H.5. It should be noted that for T100 and T60 the reflection is not shown.

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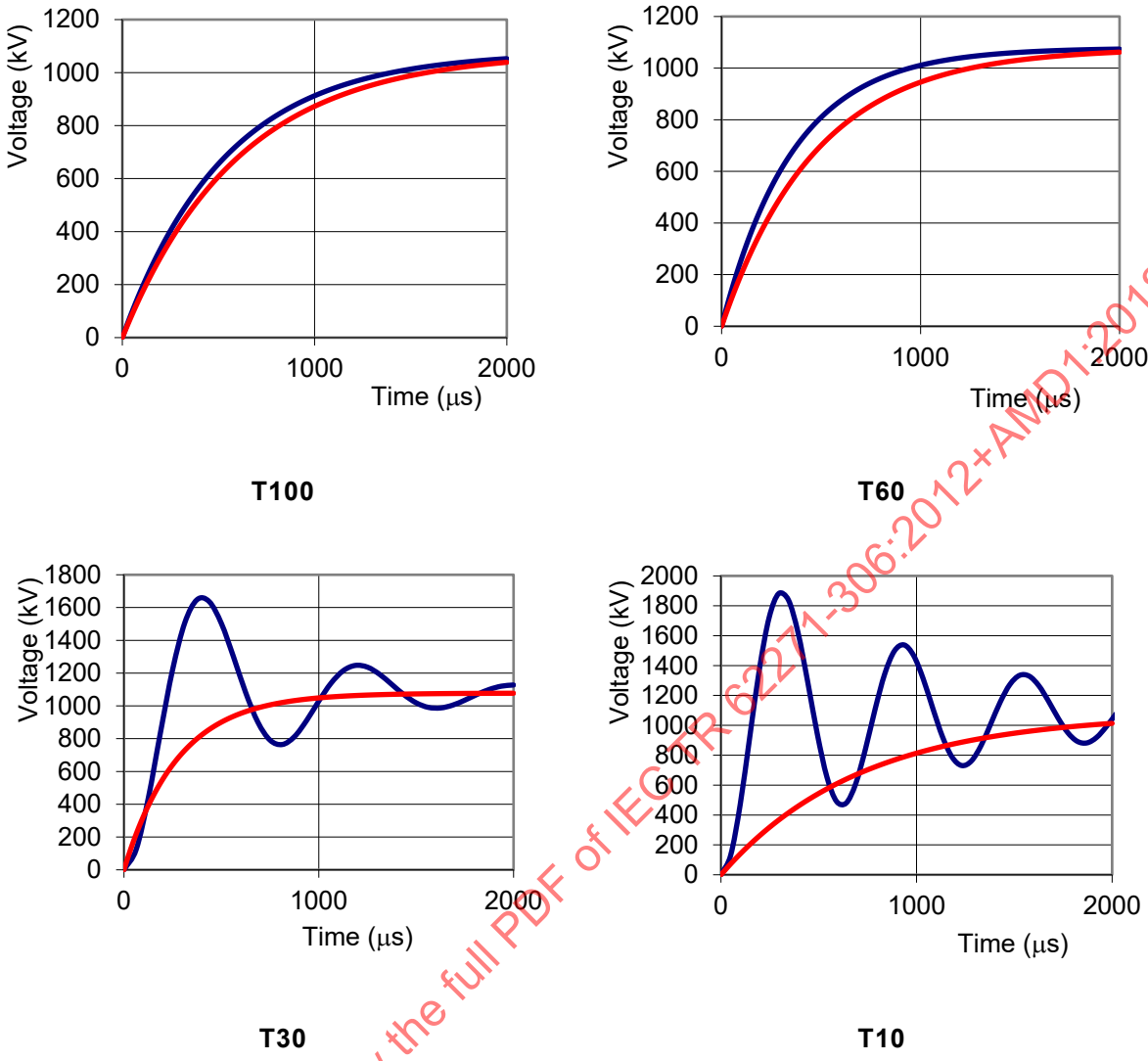

Blue trace: without opening resistor

Red trace: with 700 Ω opening resistor

Figure H.5 – Results of calculations done with RLC method

The curves in Figure H.5 show the effect of the opening resistor on the TRV waveshapes. The effects on TRV peak and rate of rise are more pronounced for the lower (T30 and T10) currents and are almost negligible for the higher (T100 and T60) currents.

H.3.4.2 Example using Laplace transform

H.3.4.2.1 Basic TRV condition (in accordance with IEC 62271-100)

– Rated voltage U_r 1 100 kV
– Rated short-circuit breaking current I_{sc} 50 kA
– Rated frequency f_r 50 Hz
– TRV T100s

The TRV has the following parameters:

– u_1 808 kV;
– t_1 404 µs;

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– u_c 1 617 kV;

– t_2 1 212 μs.

The values for the Laplace transform are chosen as follows.

a) i is the number of time steps, where the step time T is normalized to unity to simplify the calculation process hereafter. This method is recommended. In this case 404 μs is unity.

The step time width can relate to the approximation error corresponding to differences between curves and segment straight lines.

b) υ_i is the TRV value (in kV) at each step point (kV) derived from the requirements in IEC 62271-100;

c) i_i is the relevant injection current value (in kA) at each step point derived from I_{sc} = 50 kA, f_r = 50 Hz wave shape;

d) U_i is the voltage coefficient in the Laplace domain, corresponding to the change of slope of the TRV waveshape at each step point. See Equation (H.7) and the following.

$$U_i = \upsilon_{(i+1)} - 2\upsilon_i + \upsilon_{(i-1)} \tag{H.13}$$

e) I_i is the current coefficient in the Laplace domain, corresponding to change of slope of injected current at each time step point. See Equation (H.8) and the following.

$$I_i = i_{(i+1)} - 2i_i + i_{(i-1)} \tag{H.14}$$

f) Z_i is the impedance coefficient obtained from U_i and I_i. See Equation (H.9) and the following.

$$\sum_{i=0}^{i} Z_i = \frac{\sum_{i=0}^{i} U_i e^{-is}}{\sum_{i=0}^{i} I_i e^{-is}} \tag{H.15}$$

g) F_i is the TRV coefficient corresponding to the change of slope of the TRV in each point. Values are obtained from the product of I_i and Z_i.

$$F_i = \sum_{j=0}^{i} Z_j \times I_{(i-j)} \tag{H.16}$$

h) υ_i is the TRV value which should be identical to (H.7). υ_i is calculated by the inverse Laplace transform as:

$$\upsilon_i = \sum_{k=0}^{(i-1)} (i-k) \times F_k \tag{H.17}$$

H.3.4.2.2 With opening resistor

In the example an opening resistor having a value of 700 Ω is connected across the circuit-breaker terminals, i.e. shunting the circuit.

a) ZR_i is the resistor paralleled impedance coefficient obtained from the following equation:

$$\sum_i ZR_i e^{-is} = \frac{700 \times \sum_i Z_i e^{-is}}{700 + \sum_i Z_i e^{-is}} \tag{H.18}$$

b) FR_i is the resistor paralleled TRV coefficient similar to (H.12)

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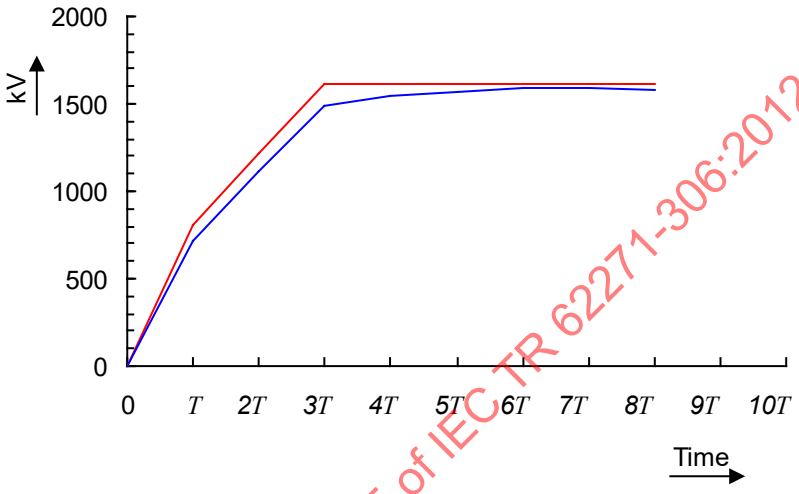
$$FR_i = \sum_{j=0}^{i} ZR_j \times I_{(i-j)} \quad \text{(H.19)}$$

c) uR_i is the TRV value modified by opening resistor from the following

$$uR_i = \sum_{k=0}^{(i-1)} (i-k) \times FR_k \quad \text{(H.20)}$$

Calculated results are shown in Figure H.6.



Key

Red line	TRV envelope for T100s, based on the conditions given in H.3.4.2.1
Blue line	TRV envelope for T100s with 700 Ω opening resistor
T	Time step, T = 404 µs

Figure H.6 – Example of a calculation of the TRV across the main interrupter for T100 using 700 Ω opening resistors

Using the same method as used for the calculation of the TRV for T100, the TRV for T10 can be calculated. The results are given in Figure H.7.

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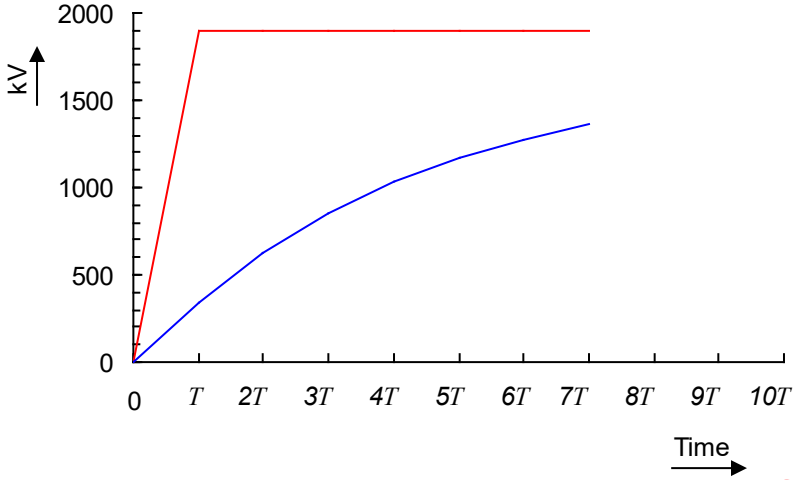
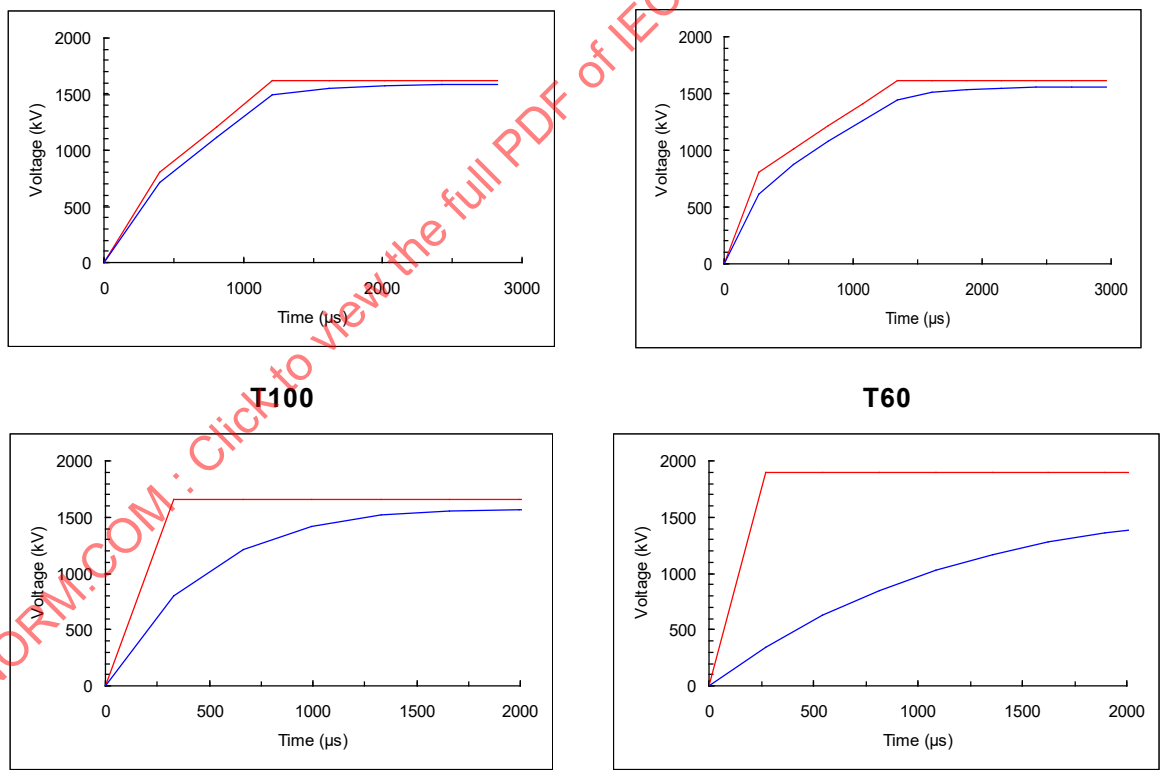


Key

Red line	TRV envelope for T10, based on conditions given in IEC 62271-100
Blue line	TRV envelope for T10 with 700 Ω opening resistor
T	Time step, T = 271 µs

Figure H.7 – Example of a calculation of the TRV across the main interrupter for T10 using 700 Ω opening resistors

Typical waveshapes in the time domain are given in Figure H.8.



Key

Red line	TRV envelope
Blue line	TRV envelope 700 Ω opening resistor

Figure H.8 – Typical TRV waveshapes in the time domain using the Laplace transform

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H.3.4.2.3 TRV for resistor interrupter

Using the same approach as that for the TRV on the main interrupter as described in 3.4.2.1, the TRV across the resistor interrupter can be calculated using the concept of the current injection method as follows.

$$\mathrm{TRV_{RI}} = \frac{\mathrm{TRV} \times I_{\mathrm{R\,peak}}}{I_{\mathrm{sc\,peak}}} + (R \times I_{\mathrm{R}}) \qquad \text{(H.21)}$$

where

$\mathrm{TRV_{RI}}$ is the TRV of the resistor interrupter;

TRV is the TRV in accordance with IEC 62271-100;

$I_{\mathrm{R\,peak}}$ is the resistor current peak;

$I_{\mathrm{sc\,peak}}$ is the breaking current peak;

R is the value of the opening resistor in Ω;

I_{R} is the resistor current (sinusoidal wave).

H.4 Review of TRV for circuit-breakers with opening resistors for various interrupting duties

H.4.1 General

RLC and Laplace analysis on TRVs for circuit-breakers with opening resistors has been conducted in various studies. Some examples are described in [68].

H.4.2 Terminal faults

H.4.2.1 TRV across the main interrupters

For the lower terminal fault test duties (T10 and T30), the peak voltage u_{c} and RRRV are reduced by the opening resistor resulting in a less severe TRV. It should be noted that the opening resistors have a similar effect on the TRV associated with transformer limited faults.

For terminal fault test duties T60 and T100, the peak voltage u_{c} and RRRV are also reduced by opening resistors, but the effect is limited.

H.4.2.2 TRV across the resistor interrupters

The application of opening resistors results in a reduction of the current to be interrupted to a few kA. The peak voltage u_{c} and RRRV will be reduced compared to the case without the opening resistors. For T30, T60 and T100, u_{c} is in the order of 1 200 kV and the RRRV is approximately 0,5 kV/μs for an 1 100 kV circuit-breaker.

An example obtained from an 1 100 kV application in Japan is shown in Figure H.9.

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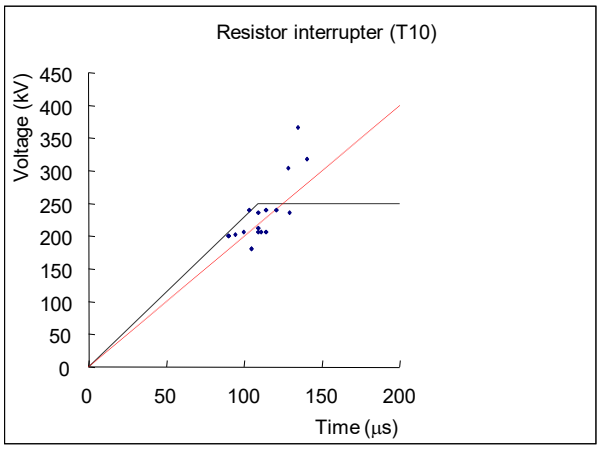

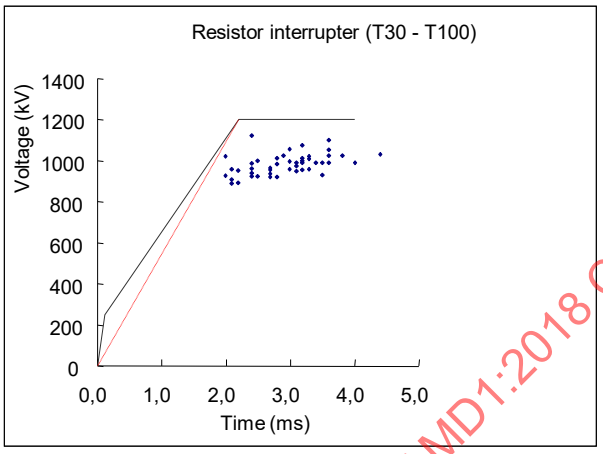

Black line: Envelope 2,3 kV/µs – 250 kV
Red line: 2 kV/µs
Blue dots: Simulation results

Black line: Envelope 2,3 kV/µs – 250 kV
1 200 kV – 2,2 ms
Red line: Envelope 1200 kV – 2,2 ms
Blue dots: Simulation results

Figure H.9 – TRV plots for resistor interrupter for a circuit-breaker with opening resistor in the case of terminal faults

H.4.3 Short-line fault (SLF)

H.4.3.1 TRV across the main interrupters

Application of opening resistors results in a reduction of the RRRV for SLF.

H.4.3.2 TRV across the resistor interrupters

Similar to the case of terminal fault, the interrupting current is low (approximately 1 kA) and the RRRV will be reduced. An example for 1 kA, 50 Hz and an opening resistor of 700 Ω is

$$\text{RRRV} = \frac{\mathrm{d}i}{\mathrm{d}t}(Z+R) = 2\pi f_{\mathrm{r}}\sqrt{2}\times 1\times(330+700)\times 10^{-6} = 0{,}46 \text{ kV/µs}.$$

H.4.4 Out-of-phase switching

H.4.4.1 TRV across the main interrupters

After the main interrupters interrupt the current, the voltage across them is the voltage shared by the opening resistors and that voltage is lower than without opening resistors, because the total voltage is shared by the opening resistors and the system impedance including lines and transformers. Two networks are distinguished:

– Network 1: a system consisting of a transformer on one side of the circuit-breaker and a transmission line on the other side. A typical TRV waveshape is shown in Figure H.10;
– Network 2: a system consisting of transmission lines on both sides of the circuit-breaker without transformers in the vicinity. A typical TRV waveshape is shown in Figure H.11.

H.4.4.2 TRV across the resistor interrupters

After the resistor interrupters interrupt the current, the TRV between the resistor interrupters is the difference between the TRVs of both sides of the circuit-breaker.

The TRVs of main and resistor interrupters after out-of-phase interruption with/without opening resistors are shown in Figures H.10 through H.13 and are summarised in Table H.1.

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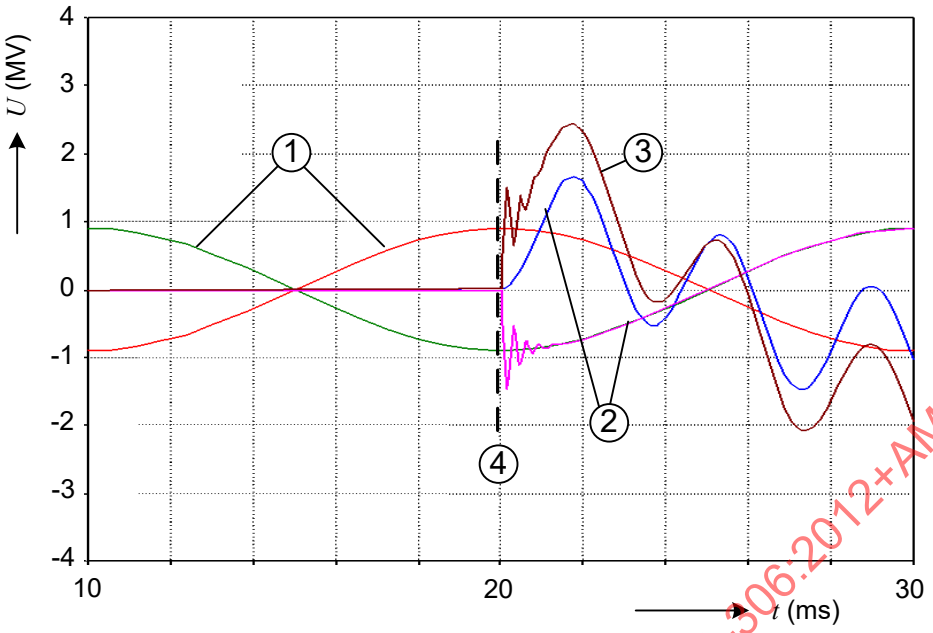

Key

1 (red and green lines)	Source voltage
2 (pink and blue lines)	Voltage at the circuit-breaker terminals
3 (brown line)	Voltage across the circuit-breaker
4 (dotted line)	Current interruption

Figure H.10 – Typical waveforms for out-of-phase interruption – Network 1 without opening resistor

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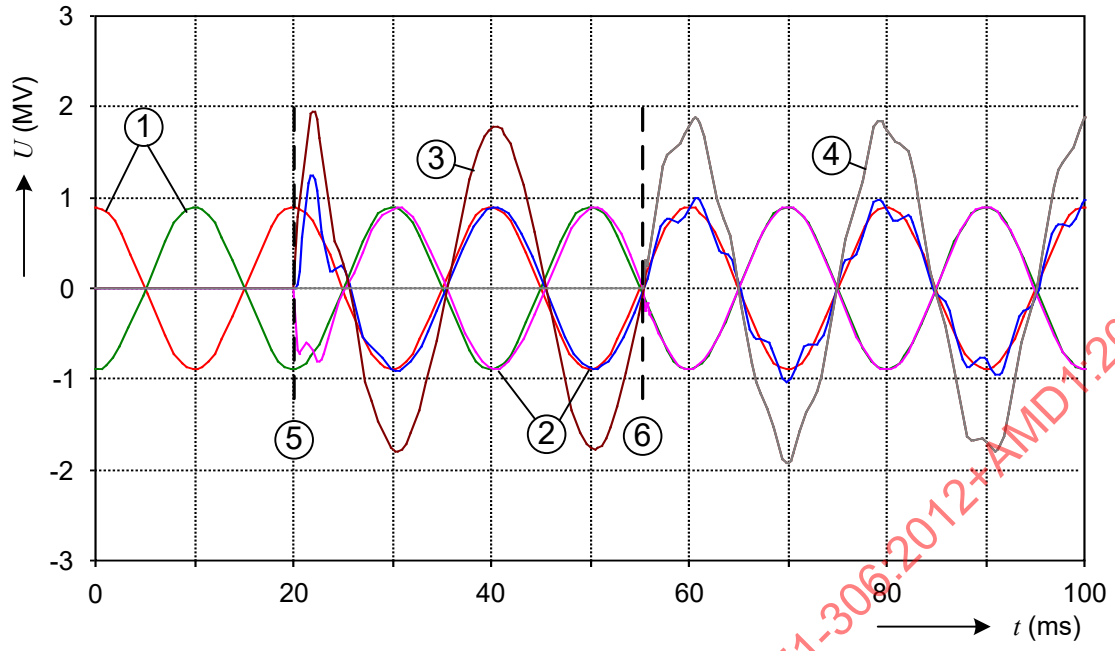

Key

1 (red and green lines)	Source voltage	4 (grey line)	Voltage between resistor interrupters
2 (pink and blue lines)	Voltage at CB terminal	5	Current interruption of the main interrupters
3 (brown line)	Voltage between main interrupters	6	Current interruption of the resistor interrupters

Figure H.11 – Typical waveforms for out-of-phase interruption – Network 1 with opening resistor (700 Ω)

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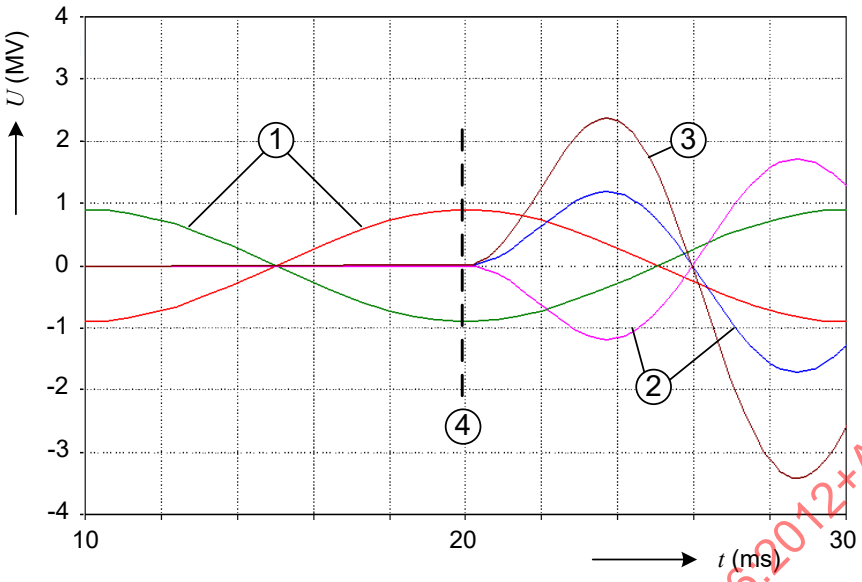

Key

1 (red and green lines)	Source voltage
2 (pink and blue lines)	Voltage at the circuit-breaker terminals
3 (brown line)	Voltage across the circuit-breaker
4	Current interruption

Figure H.12 – Typical waveforms for out-of-phase interruption – Network 2 without opening resistor

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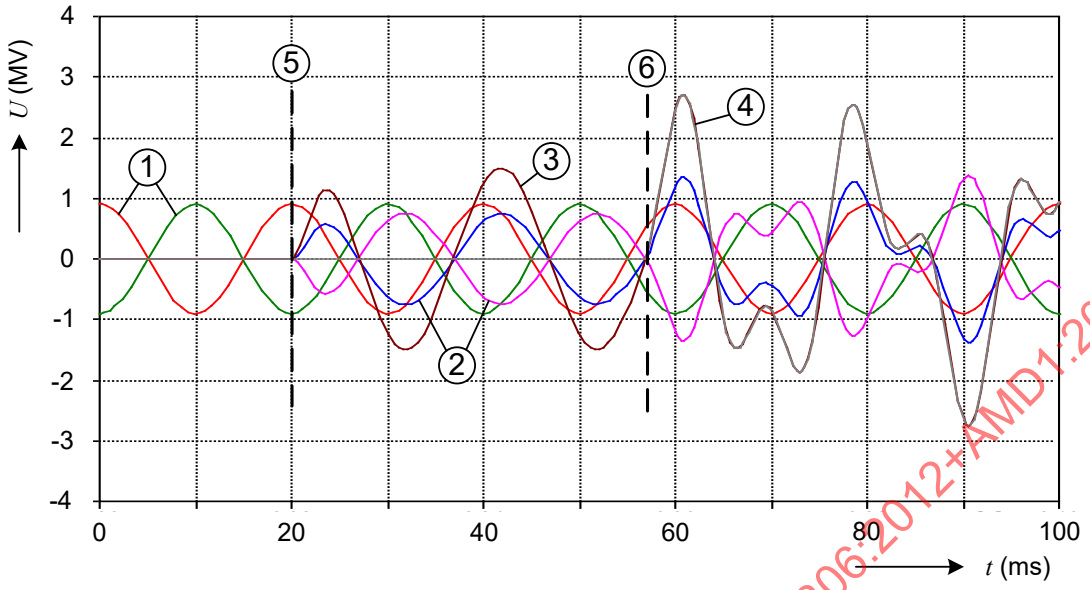

Key

1 (red and green lines)	Source voltage	4 (grey line)	Voltage between resistor interrupters
2 (pink and blue lines)	Voltage at CB terminal	5	Current interruption of the main interrupters
3 (brown line)	Voltage between main interrupters	6	Current interruption of the resistor interrupters

Figure H.13 – Typical waveforms for out-of-phase interruption – Network 2 with opening resistor (700 Ω)

Table H.1 – Summary of TRV between main and resistor interrupters after out-of-phase interruption with/without opening resistor

	Without opening resistor	With opening resistor of 700 Ω	
	Main interrupter	Main interrupter	Resistor interrupter
	p.u.	p.u.	p.u.
Network 1	2,6	2,1	2,0
Network 2	2,7	1,2	3,0

H.4.5 Example of TRVs for short-circuit test-duties for circuit-breakers with opening resistors

Calculations performed on the Japanese 1 100 kV system are summarised in Table H.2 and Table H.3.

The recovery voltage peak of the resistor interrupter u_{cR} is increased up to u_c which is the peak value of the TRV without opening resistor. Although in reality the t_2 time may be longer, its value has been set to 1 458 µs for OP2 of main interrupter and T100, T60, T30 and T10 for resistor interrupter and 2 326 µs for OP2 of resistor interrupter as the longest.

Note that u_c of the main interrupter tends to be higher when t_2 becomes longer.

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Table H.2 – TRV on main interrupter with opening resistor for T100,T60,T30, T10, OP and SLF U_r = 1 100 kV, I_{sc} = 50 kA, R = 700 Ω

Test duty	t_1 (μs)	u_1 (kV)	RRRV (kV/μs)	t_2 or t_3 (μs)	u_c (kV)	Recovery voltage peak (kV)
T100s	404	716	1,77	1 212	1 492	1 078
T100a(major)	404	545	1,35	1 212	991	1 078
T100a(minor)	404	528	1,31	1 282	1 264	1 078
T60	269	611	2,27	1 212	1 427	1 077
T30	-	-	2,41	332	800	1 075
T10	-	-	1,27	271	344	1 053
OP2	-	-	1,11	1 458	1 625	1 777
SLF	337	696	2,07	1 011	1 303	829

Table H.3 – TRV on resistor interrupter for T100s, T60, T30, T10, OP2 and SLF with opening resistor of 700 Ω

Test duty	t_1 (μs)	u_{1R} (kV)	RRRV (kV/μs)	t_2 (μs)	u_{cR} (kV)	Recovery voltage peak (kV)
T100s	404	128	0,32	1 458	426	904
T60	269	100	0,37	1 458	446	907
T30	-	-	0,34	1 458	497	907
T10	-	-	0,5	1 458	729	940
OP2	-	-	0,85	2 326	1 981	1 796
SLF	337	110	0,33	1 011	307	695

NOTE 1 Terminal faults with currents lower than T10 can lead to TRV peak values and RRRV higher than those of T10. They could be covered by OP2 but with a higher RRRV than given in the table.

NOTE 2 u_{1R} and u_{cR} are the corresponding voltage values of u_1 and u_c of the TRV across the contacts of resistor interrupter, respectively.

The resulting TRV waveshapes may be overdamped or underdamped, depending on the test duty and the values of the opening resistor. Typical examples are shown in Figure H.3.

H.4.6 Capacitive current switching

H.4.6.1 General

Figure H.14 shows an example of analysis of capacitive current switching by a circuit-breaker with opening resistors.

a) the recovery voltage before interruption of resistor interrupter is reduced to approximately 1/3 of the case without opening resistors;

b) after interruption of resistor interrupter, the recovery voltage does not differ significantly from the case without opening resistors. Compared to the case without resistors, the amplitude decreases slightly but the initial slope is higher. The recovery voltage stresses both main and resistor interrupters.

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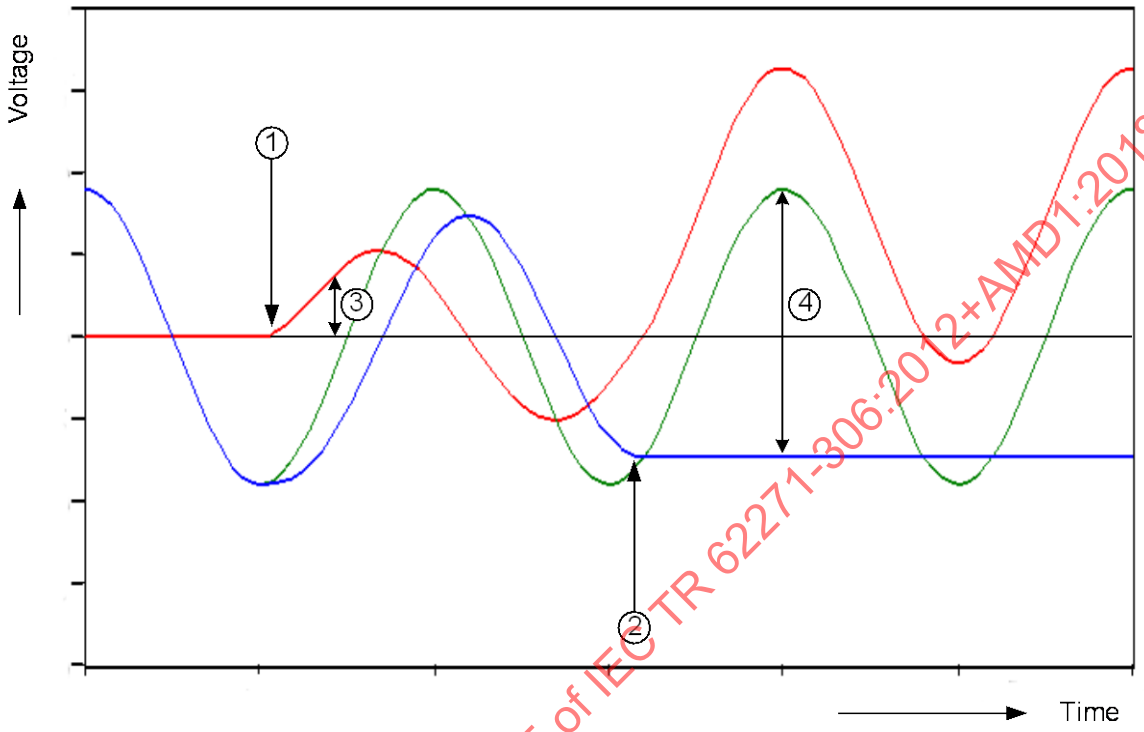
It should be noted that, even after the interruption of the resistor interrupter, the severity of the capacitive current switching duty does not change since the peak of the recovery voltage and the initial slope are comparable to the case without opening resistors. This case is illustrated in Figure H.14.



Key

	Voltage across the terminals of the main interrupter
	Source side voltage
	Load side voltage
1	Interruption of main interrupter
2	Interruption of resistor interrupter
3	Voltage across the terminals of the main interrupter
4	Voltage across the terminals of the resistor interrupter

Figure H.14 – Typical recovery voltage waveshape of capacitive current switching on a circuit-breaker equipped with opening resistors

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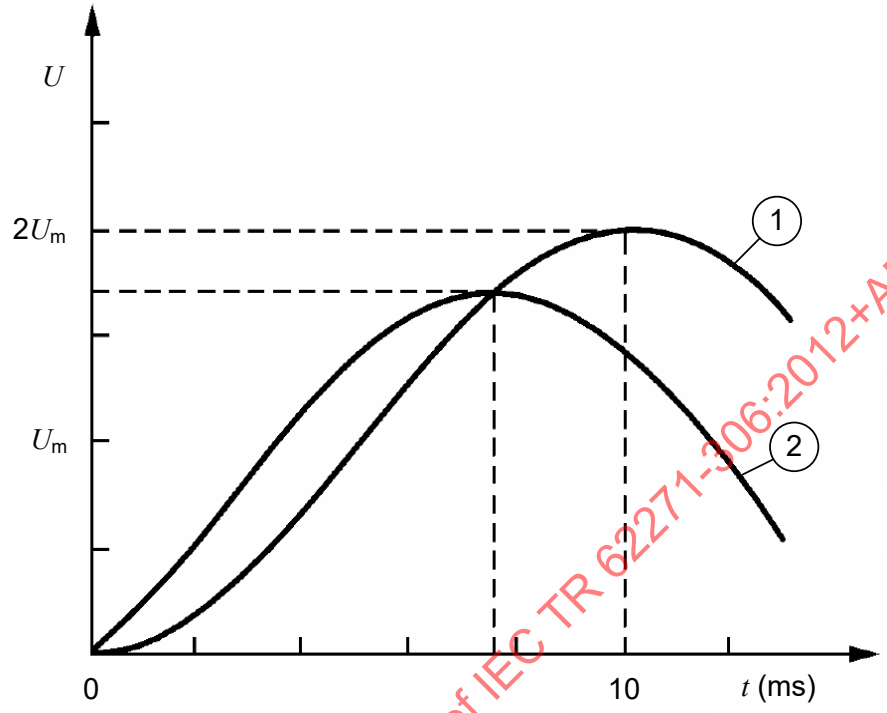
H.4.6.2 Recovery voltage across the main interrupter

The recovery voltage across the main interrupter is the voltage across the opening resistor generated by the current though the resistor. Assuming that the current to be interrupted is 1 000 A at a system voltage of 1 100 kV, then the resulting impedance has a similar value as that of the opening resistors. The recovery voltage will have a peak of approximately half of the value that would be obtained without the opening resistors.

H.4.6.3 Recovery voltage across the resistor interrupter

The phase angle between the current through the opening resistor and voltage is shifted from 90° to a value of θ (=$\tan^{-1}(\omega CR)$), where C is line side capacitance and R is opening resistance value). The recovery voltage across the resistor interrupter is the difference between the line side residual voltage at the current zero of resistor interrupter and the source side voltage. As the line length increases, the residual voltage reduces as a larger

capacitance leads to a recovery voltage that has a sinusoidal waveform as indicated in Figure H.15. A short line having a small capacitance will have larger residual voltage and the recovery voltage has a 1- cos waveform, see Figure H.15.



Key

1 Basic condition and for short lines, $U(t) = U_m(1-\cos\omega t)=k_c \times U_r/\sqrt{3}(1-\cos\omega t)$

2 Long line (210 km), $U(t) = U_m(\cos\theta-\cos(\omega t-\theta))$

Figure H.15 – Recovery voltage waveforms across the resistor interrupter during capacitive current switching by a circuit-breaker with opening resistors

H.5 Performance to be verified

H.5.1 General

During a breaking operation with opening resistors the following items need to be verified:

– the timing of the main contacts in relation to the resistor contacts;
– the effect of the exhaust gas on the insulation to earth;
– the thermal capacity of resistor.

These items are illustrated in Figure H.16.

The type tests to be performed on the circuit-breaker with opening resistor are referred to Annex R of IEC 62271-100:2008, Amendment 1. Additionally, the thermal capacity of the resistor needs to be verified. For the resistor interrupter T10, OP2 and capacitive current switching performance will be sufficient because there is no significant difference in breaking current and the TRVs for T100, T60, and T30 are covered by T10 and OP2 as shown in Table H.2.

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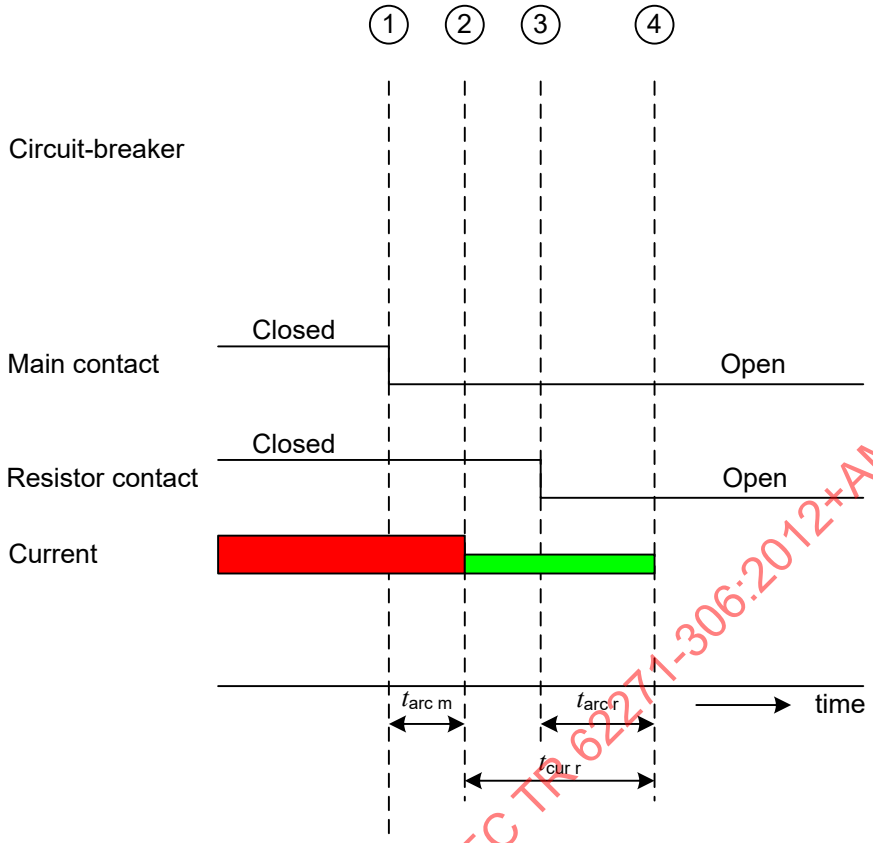

Key

1	Contact separation in the main interrupter
2	Current interruption of the main interrupter
3	Contact separation in the resistor interrupter
4	Current interruption of the resistor interrupter
	Current flow in the main interrupter
	Current flow in the resistor interrupter
$t_{arc\ m}$	Arcing time of the main interrupter
$t_{arc\ r}$	Arcing time of the resistor interrupter
$t_{cur\ r}$	Time duration of current through resistor

Figure H.16 – Timing sequence of a circuit-breaker with opening resistor

Most tests will be performed as unit test and/or multi-part test. To verify the insulation withstand between live parts and earth during breaking tests and taking account of electromagnetic effect, full pole test for T100s and T100a are preferable for the main interrupter. For resistor interrupter T10 is a representative test for terminal faults. SLF tests are not necessary for the resistor interrupter because of the low current and low du/dt. Tests may be performed as unit test, but the out-of-phase test should preferably be performed as a full pole test.

Due to limitation of testing facilities it is anticipated that synthetic test methods will be used. In case of synthetic tests the following items should be observed:

– appropriate timing of mechanical and electrical operation including pre-arcing time and arcing time for breaking shall be verified;

– the number of operations for the tests will be limited by the thermal capacity of resistors and by their cooling time constant;

– capacitive current switching tests will be performed without the opening resistors.

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When synthetic tests are performed, they are split into several parts:

– test of main interrupter;
– test of resistor interrupter;
– test of the resistor(s);
– a possible combination of a test on the main and resistor interrupters and (a part of) resistors.

H.5.2 Test on the main interrupter

H.5.2.1 Terminal fault, out-of-phase switching and short-line-faults

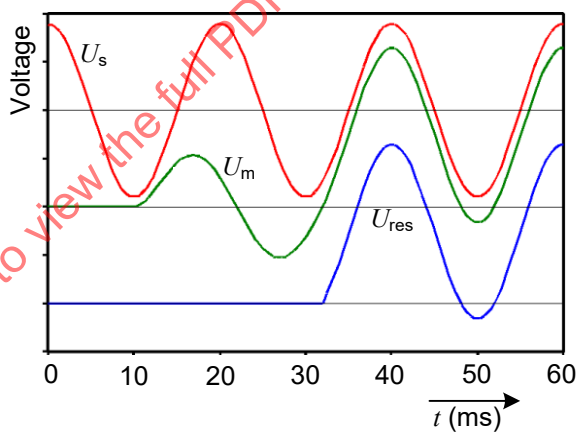
These tests are verified by synthetic tests because of the limitation of the testing facilities. Details are given in IEC 62271-101.

H.5.2.2 Capacitive current switching tests

The line-charging current switching tests are separated in two parts:

a) LC2 with the first part of the recovery voltage (a sine wave) to verify that no restrikes or re-ignitions occur. In case of a re-ignition, the test may be repeated using a direct test circuit that provides the correct recovery voltage;
b) LC1 with the second part of the recovery voltage (a 1 – cos wave).

An alternative way to perform the tests using a single test is to cover the recovery voltage in a single test using the same number of tests as described in 6.111.9 of 62271-100:2008. Figure H.17 shows the current and voltage for main and resistor interrupters for capacitive current switching test with opening resistor.



Key

U_m	Voltage across main interrupter
U_{res}	Voltage across resistor interrupter
U_s	Source voltage

Figure H.17 – Voltage waveshapes for line-charging current breaking operations

H.5.3 Terminal fault,OP and SLF tests on resistor interrupter

The breaking current value is in the order of 1 kA or less when selecting an opening resistor with a resistance value between 500 Ω and 2 000 Ω. The short-circuit current is assumed to be between 40 kA and 63 kA. Then the current for the resistor interrupter is less than 1 kA and is considered to be covered by T10. In case of OP2, the current will be in the order of 2 kA.

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Similar to the case of the main interrupter, the TRV parameters should be calculated for each system condition.

Typical TRV values are shown in Table H.2 which shows a case with 1 100 kV, 50 Hz, I_{sc} = 50 kA and R = 700 Ω. The tests are performed using a synthetic test method. Details are given in IEC 62271-101.

H.5.4 Test on the resistor

The duty of the opening resistor is decided considering most onerous condition from practical point of view. Most of the faults will be terminal faults in the order of T30 to T60, and the frequency of occurrence will be in the order of several times per day at most considering transmission systems at voltages of 800 kV and above. Such transmission systems are characterized by tall towers and substantial distances between the lines. In such systems faults between phases or earth faults occur less frequent compared to the lower voltage class. Assuming that five successive full terminal faults occur, the energy consumed by the opening resistor is equal to one out-of-phase make and break plus one terminal fault breaking. Out-of-phase conditions will occur rarely, but the voltage applied across the resistor is the maximum. Based on these considerations, it was decided to use one out-of-phase make and break plus one terminal fault break.

The stresses to be applied are one T100s opening duty, (O operation only) followed by one out-of-phase make-break duty (CO-operation).

Generally, the mechanical insertion time for the opening resistor is 30 ms.

H.5.5 Combination of tests

Depending on the design, tests on the main interrupter, resistor interrupter and/or resistors may be combined. An example is given here:

– main interrupter and resistor interrupter;
– main interrupter and resistor;
– resistor interrupter and resistor;
– main interrupter, resistor interrupter and resistor.

The thermal and electrical interaction between above-mentioned combinations should be verified.

The necessity and practical method of the test are quite dependent on the circuit-breaker design and the users, the manufacturers and the testing station are requested to be well discussed.

A full pole test is preferable for verification of the dielectric withstand between live parts and enclosure in case of a dead tank or GIS circuit-breaker.

H.6 Time sequence of main and resistor interrupters

Confirmation of the mechanical insertion time is done by no-load operation and combination of breaking tests. It should be ensured that the mechanical insertion time of the opening resistor is longer than maximum arcing time of the main interrupter.

Confirmation of the insertion time the closing resistor is in the circuit is done by no-load operation and performing a making test during test duty T100s.

NOTE Closing and opening resistors are combined in some designs.

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H.7 Current carrying performance

The opening resistor shall be capable of carrying the fault current for specified period without any abnormality such as remarkable spark emission, flashover to the adjacent parts, cracks, etc.

H.8 Dielectric performance during breaking tests

Dielectric performance is to be verified between live parts and earth.

During breaking tests flashover should not occur between the main contacts, between the main and resistor contacts and between resistors and main or resistor contacts parts.

The test conditions are based on 6.2.11 of IEC 62271-100:2008.

H.9 Characteristics of opening resistors

H.9.1 General

Subclauses H.9.2 and H.9.3 specify the opening resistors.

H.9.2 Resistor value

The values of opening resistors are determined by taking the overvoltages generated by breaking operations and insulation design of the transmission system into account. In case opening resistors have a function of closing resistors in common, overvoltages and making capability for closing will also be taken into account.

H.9.3 Electrical insertion time for resistors

The time during which the resistor is inserted in the circuit is determined by taking the overvoltages generated by breaking operations and insulation design of the transmission system into account. The electrical insertion time for the opening resistor should be longer than the maximum arcing time of the main contacts.

Typical calculated values of opening resistors are shown in Table H.4.

The assumptions for the calculations are as follows:

– ohmic value of opening resistor: 700 Ω;
– mechanical insertion time: 30 ms;
– duty of opening resistor: 1 O (T100s) + 1 O (OP2);
– rated voltage: 1 100 kV;
– rated frequency: 50 Hz;
– rated breaking current: 50 kA.

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Table H.4 – Example of calculated values on main and resistor interrupter

Duties		Basic specifications		
Main interrupter	Short-circuit	T10	Breaking current	8 kA
			u_c	1 385 kV
			t_3	461 µs
			RRRV	3 kV/µs
		T100s	Breaking current	50 kA
			u_1	990 kV
			RRRV	2 kV/µs
			u_c	1 385 kV
			t_2	1 485 µs
	SLF	L90	Breaking current	45 kA
			RRRV	8 kV/µs
			Z	450 Ω
			k_{af} (line side)	1,4
	Out-of-phase	OP2	Breaking current	12,5 kA
			u_1	1 200 kV
			RRRV	2 kV/µs
			u_c	2 160 kV
			t_2	1 800 µs
	Capacitive current	Sine wave	Current	1 000 A
			u_c	900 kV
		1-cos wave	Current	1 000 A
			u_c	2 515 kV
Resistor interrupter	Short-circuit	Common for T100s, T100a, T60, T30, T10	Breaking current	1 000 A
			u_1	550 kV
			RRRV	3 kV/µs
			u_c	1 200 kV
			t_2	550 µs
	Out-of-phase switching	OP2	Breaking current	2 000 A
			u_1	1 750 kV
			RRRV	2 kV/µs
			u_c	2 160 kV
			t_2	1 800 µs
	Capacitive current	1-cos wave	Breaking current	1 000 A
			u_c	2 515 kV
		Quasi sine wave	Breaking current	600 A
			u_c	2 000 kV
			RRRV	0,34 kV/µs
Opening resistor	Insertion time			30 ms
	Thermal duty			86~96 MJ

NOTE The calculation of the thermal duty of the resistor does not take account of a possible combination of opening and closing resistor.

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Annex I
(informative)

Circuit-breaker history

Circuit-breakers are one of the great inventions of the 20th century enabling the power systems of today and their contribution to modern society. The various circuit-breaker types were developed over overlapping periods with each taking a number of years before reaching commercial application.

The earliest circuit-breakers were of the bulk oil type with the first, those of Kelman in the early 1900s, consisting of a crude arrangement of switches in separate wooden barrels connected in series and gang operated. Bulk oil circuit-breakers evolved over the next 30 years, the principal developers in the United States being Slepian of Westinghouse and Prince and Skeats of General Electric. In Europe, bulk oil circuit-breakers reigned until the early 1950s and then were totally supplanted by minimum oil circuit-breakers. Bulk oil circuit-breakers are in use up to 360 kV with eight breaks in series, while the minimum oil type are used up to 420 kV with up to ten breaks in series. Some utilities actually continued acquiring these types of circuit-breaker into the 1990s.

The development of air-blast circuit-breakers took place in Europe, first by Whitney and Wedmore of the British Electrical Research Association in 1926 with further development in Germany and Switzerland in the 1930s and 1940s. These circuit-breakers came into prominent use in the 1960s and in fact became the enablers of EHV systems at 500 kV and above. Air blast circuit-breakers were manufactured into the early 1980s when they were supplanted by the lower cost and less complex SF_6 puffer type circuit-breakers. Air magnetic circuit-breakers are a variation of air-blast circuit-breakers in use at medium voltages up to 52 kV.

Already in the 1930s SF_6 gas was recognized for its unique dielectric properties (patent by F.S. Cooper of General Electric on its use in capacitors and gas insulated cables). The use of SF_6 gas for current interruption was patented by H.J. Lingal, T.E. Browne and A.P. Storm of Westinghouse in 1951 but the first SF_6 circuit-breakers did not appear on the market until around 1960. These circuit-breakers were of the dual pressure type based on the axial blast principles used in air-blast circuit-breakers and had a relatively short manufacturing life span to about 1980. Puffer type SF_6 circuit-breakers (often referred to as single pressure SF_6 and actually based on a principle invented by Prince and used in the so-called impulse type bulk oil circuit-breaker where the oil flow was produced by a piston driven by the operating mechanism) were developed in the 1970s and rapidly supplanted the dual pressure type. Further evolution of SF_6 circuit-breakers has led to rotating arc technology up to 72,5 kV and self-blast technology both of which have the advantage of requiring lesser transmission of energy from the operating mechanism to the interrupters and thus lower mechanical stresses.

The first vacuum switch patent was granted around 1890 and the first HV vacuum switch was demonstrated in the 1920's, however, the first commercial HV vacuum switches were not sold until the 1950's. Vacuum is now used widely in high-voltage load break switches at medium voltages up to 38 kV and up to 230 kV as a switching only attachment to air break disconnect switches. Vacuum was first made available in HV vacuum circuit-breakers (VCBs) in the 1960's and by 1990, vacuum became the predominant interrupter technology in medium voltage circuit-breakers through 38 kV. Vacuum circuit-breakers are now in service at 84 kV in some countries with developments in progress for ratings up to 145 kV. VCBs are also now available as generator circuit-breakers for smaller generator applications through normal currents of 7 000 A and interrupting currents through 75 kA.

The manufacturing timelines for six major circuit-breaker types are shown in Figure I.1.

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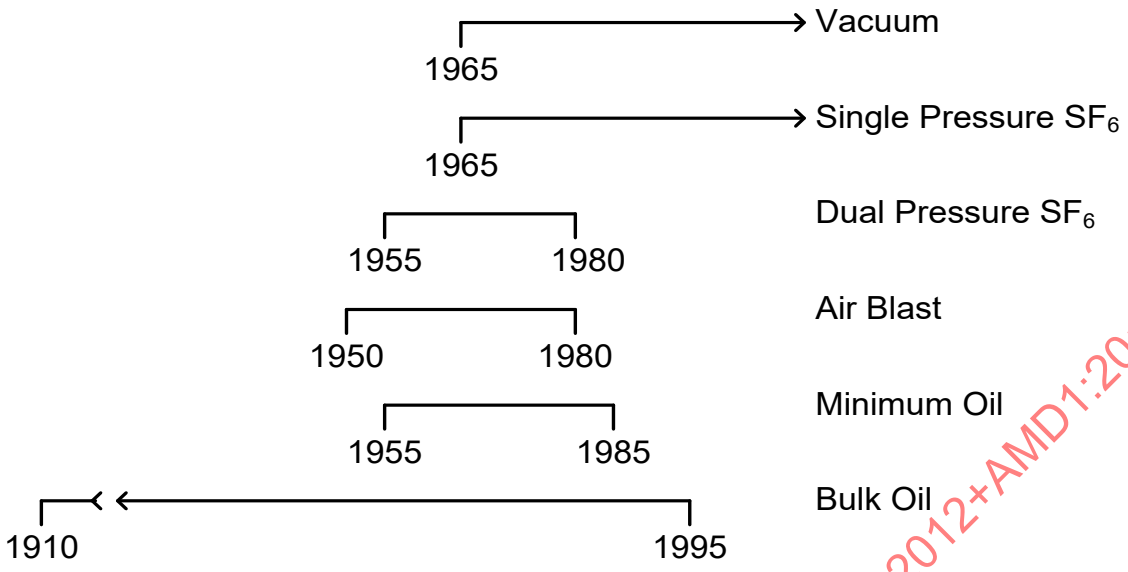

Solid lines indicate approximate or ongoing manufacturing periods.

Figure I.1 – Manufacturing timelines of different circuit-breaker types

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Bibliography

General references

[1] I. Miller and J.E. Freund, *Probability and Statistics for Engineers*, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1965

[2] CIGRE Technical Brochure 304, *Guide for the application of IEC 62271-100 and IEC 62271-1 – Part 1 – General subjects,* October 2008

[3] G.E. Hayes and H.G. Romig, *Modern Quality Control*, Revised Edition, Glencoe Publishing Company, 1982

[4] D.J. Cowden, *Statistical Methods in Quality Control*, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1957

[5] J.M. Juran and F.M. Gryna, *F.M. Juran's Quality Control Handboo*", 4th Edition, McGraw-Hill, Inc., 1988

[6] CIGRE WG 3.10, *Transient Recovery Voltage in High-voltage Networks – terminal faults*, CIGRE Session 1968, Report 13-10, August 1968

[7] Electra 88, *Transient recovery voltages in medium voltage networks. Report of the TF: TRV parameters for medium voltage circuit-breakers,* 1983

[8] Electra 102, *A review of transformer TRV conditions*, May 1983, pp. 91-122

[9] CIGRE Technical Brochure 134, *Transient recovery voltages in medium voltage networks*, December 1998

[10] IEEE C37.04b-2008, *Amendment to IEEE Standard for Rating Structure for AC High-Voltage Circuit-Breakers Rated on a Symmetrical Current Basis to change the description of Transient Recovery Voltage for harmonization with IEC 62271-100*, April 2009

[11] ANSI/IEEE C37.06-2009, *AC High-Voltage Circuit-breakers Rated on a Symmetrical Current Basis – Preferred Ratings and Related Required Capabilities*, November 2009

[12] G. Catenacci and CIGRE WG13-01, Contribution on the study of the initial part of the Transient recovery Voltage, Electra 46 (1976), p. 39

[13] C.Dubanton, *Initial Transient Recovery Voltage, Current Interruption in High-Voltage Networks*, Plenum Publishing Corporation, 1978, pp 185 – 203

[14] R. Graf, *ITRV modification by interaction between SF_6-breaker and the test circuit.* CIGRE session paper 13-01 (1976)

[15] W.Hermann, K.Ragaller, *Interaction between arc and network in the ITRV regime, Current Interruption in High-Voltage Networks*, Plenum Publishing Corporation, 1978, pp 205 – 229

[16] Ch. Dubanton, G. Gervais, Van Nielen. *Surge impedance of overhead lines with bundle conductors during short-line faults*, Electra 17, April 1971

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

[17] Dr H.Meyer, Chairman of CIGRE Study Committee 3. *Communication dated 19th August 1963 to the Central Office of the IEC, regarding short-line fault problems*; 17A (CIGRE)1, September 1963

[18] CIGRE WG 13-01, *Practical application of arc physics in circuit-breakers. Survey of calculation methods and application guide*, Electra 118, May 1988

[19] A.Braun, K.H. Hinterthür, H.Lipken, B.Stein, O.Völcker, *Characteristic values of the transient recovery voltage for different types of short-circuits in an extensive 420kV system*, ETZ-a vol 97 (1976) pp 489 to 493

[20] R.G.Colclaser, L.E.Berkebile and D.E.Buettner, *The effect of capacitors on the short line fault component of TRV, IEEE Transactions on Power Apparatus and Systems*, Vol. PAS 90, N°02 March-April 1971, pp. 660-669

[21] A. F.Gabrielle, P. P. Marchenko, and G. S. Vasell, *Electrical Constants and Relative Capabilities of Bundled Conductor Transmission Lines*, *IEEE Transactions on Power Apparatus and Systems,* vol. 83, Jan 1964, pp 78-92

[22] CIGRE Technical Brochure 47, *Line-Charging Current Switching of HV Lines – Stresses and Testing Part 1 and 2*, October 1996

[23] IEEE C62.22-1997, *IEEE Guide for the Application of Metal-Oxide Surge Arresters for AC Systems*

[24] CIGRE Technical Brochure 134:2000, *Transient recovery voltages in medium voltage networks*

[25] van der Sluis, L., and Janssen, A.L.J., *Clearing faults near shunt capacitor banks, IEEE transactions on power delivery*, Vol. 5, No. 3, July 1990, pp. 1346-1354

[26] IEEE 1036-1992, *IEEE Guide for Application of Shunt Capacitors*

[27] R. Eriksson and V.S. Rashkes, *Three-phase interruption of single and two-phase faults: Breaking stresses in the healthy phase*, Electra 67, 1980, pp. 77-92

[28] CIGRE Technical Brochure 83, *Final Report of the Second International Enquiry on High-voltage Circuit-breaker Failures and Defects in Service*, June 1994

[29] CIGRE Technical Brochure 167, *User Guide for the Application of Monitoring and Diagnostic Techniques for Switching Equipment for Rated Voltages of 72.5kV and Above*, August 2000

[30] CIGRE Technical Brochure 165*, Life Management of Circuit-breakers*, August 2000

[31] D. Dufournet, *Arc Modelling Applied to Small Inductive Currents Interruption*, CIGRE Paper No. 13-01, 1988

[32] J.A. Bachiller, E. Cavero, F. Salamanca and J. Rodriguez, *The Operation of Shunt Reactors in the Spanish 400 kV Network – Study of the Suitability of Different Circuit-breakers and Possible Solutions to Observed Problems*. CIGRE Paper No. 23-106, 1994

[33] IEEE C57.21-2006, *IEEE Standard Requirements, Terminology, and Test Code for Shunt Reactors Rated Over 500 kVA*

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

[34] A.K. McCabe, G. Seyrling, J.D. Mandeville and J.M. Willieme, *Design and Testing of a Three-Break 800 kV SF_6 Circuit-breaker with ZnO Varistors for Shunt Reactor Switching*, Proceedings IEEE PES T&D Conference 1991

[35] D.F. Peelo and J.H. Sawada, *Experience with Controlled Transmission Line Autoreclosing and Controlled Shunt Reactor Switching on B.C. Hydro System*, CIGRE Paper No. 13-101, 1998

[36] D. Braun, W. Hellmann and A. Plessl, *Application Criteria for SF_6 and Vacuum Circuit-breakers*, ABB Review 4/99

[37] IEEE Standard C37.015, *IEEE Application Guide for Shunt Reactor Switching*, 1993

[38] Electra 75, *Interruption of small inductive currents*, Chapter 3, Part A., March 1981

[39] J.F. Perkins, *Evaluation of Switching Surge Overvoltages on Medium Voltage Power Systems, IEEE Transactions of Power Apparatus and Systems*, Vol. PAS-101(6), June 1982

[40] A. Greenwood and M. Glinkowski, *Voltage Escalation in Vacuum Switching Operations, IEEE Transactions on Power Delivery*, Vol. 3, No. 4, October 1988

[41] M. Murano, T. Fujii, H. Nishikawa, S. Nishiwaki and M. Okawa, *Voltage Escalation in Interrupting Inductive Current by Vacuum Switches, IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-93, 1974

[42] J.P. Eichenberg, H. Hennenfent and L. Liljestrand, *Multiple Restrikes Phenomenon when Using Vacuum Circuit-breakers to Start Refiner Motors*, Pulp & Paper Canada 98:7,1977

[43] A. Luxa and A. Priess, *Switching of Motors During Start-up*, Siemens Power Engineering and Automation VII, 1985

[44] S.H. Telander, M.R. Wilhelm and K.B. Stump, *Surge Limiters for Vacuum Circuit-breakers, IEEE Transactions on Industry Applications*, Vol. 24, No. 4, 1988

[45] Y. Murai, T. Nitta, T. Takami and T. Itoh, *Protection of Motor from Switching Surge by Vacuum Switch, IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-93, 1974

[46] R.E. Pretorius, *Guide for the Application of Switching Surge Suppressors to Medium Voltage Motors*, Report for Electric Power Coordinating Committee, South Africa

[47] R.E. Pretorius, *The Suppression of Internal Overvoltage Surges in Industrial High-voltage Systems*, The Certified Engineer, July 1981, South Africa

[48] A.M. Chaly, A.T. Chalaya, V.N. Poluyanov and I.N. Poluyanova, *The Peculiarities of Interruption of the Medium Voltage Motors by VCB with CuCr Contacts*, IEEE 18th International Symposium on Discharges and Electrical Insulation in Vacuum, Eindhoven 1998

[49] G.C. Damstra, *Virtual chopping phenomena switching three-phase inductive currents*, CIGRE SC 13 colloquium, Helsinki, Finland, 1981

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

[50] W.M.C. van den Heuvel, J.E. Daalder, M.J.M. Boone and L.A.H. Wilmes, *Interruption of Dry-Type Transformer in No-Load by a Vacuum Breaker*, Eindhoven University of Technology Report 83-E-141, August 1983

[51] F. Rizk, *Arc Instability and Time Constant in Air-Blast Circuit-breakers*, CIGRE Paper No. 107, 1964

[52] F. Rizk, *Arc Response to a Small Unit-Step Current Pulse*, Elteknik, Volume 7, Part 2, February 1964

[53] A.U. Dowell, G.E. Gardner, R.J. Urwin, F.P. Matraver and W. Watson, *A Review of Switchgear Testing Requirements Including the Interruption of Low Inductive Currents,* CIGRE Paper No. 13-02, 1976

[54] M. Murano, S. Yanabu, H. Ohashi, H. Ishizuka and T. Okazaki, *Current Chopping Phenomenon of Medium Voltage Circuit-breakers*, IEEE Transactions Vol. PAS-96, No. 1, January/February 1977

[55] S. Berneryd, C.E. Solver, L. Ahlgren and R. Eriksson, *Switching of Shunt Reactors Comparison Between Field and Laboratory Tests*, CIGRE Paper No. 13-04, 1976

[56] J.C. Henry, G. Perrissin and C. Rollier, *The Behaviour of SF_6 Puffer Circuit-breakers Under Exceptionally Severe Conditions*, CIGRE Paper No. 13-08, 1978

[57] R. Eriksson, S. Berneryd and A. Eriksson, *Laboratory and Field Tests with a 420 kV SF_6 Puffer Breaker for a Gas Insulated Substation*, IEEE Conference on High-voltage Switchgear Publication 182, 1979

[58] Electra 173, *Specified Time Constants for Testing Asymmetric Current Capability of Switchgear,* August 1997, pp 19-31

[59] D. Dufournet, J.M. Willième, G. Montillet, *Design and Implementation of an SF_6 Interrupting Chamber Applied to low range Generator Circuit-breaker suitable for Interruption of Current having a Non-zero Passage*, IEEE Transactions on Power Delivery, vol. 17, N°4, October 2002

[60] CIGRE 2002 Paper 13-01, *Generator Circuit-breaker, SF_6 Breaking Chamber Interruption of Current with non-zero passage – Influence of cable connection on TRV of system-fed faults*, D. Dufournet – J.M. Willième

[61] IEEE Standard C37.013-1997, *Standard for High-Voltage Generator Circuit-Breakers Rated on a Symmetrical Current Basis*

[62] S.S. Berneryd, *Improvement Possible in Testing Standards for High-Voltage Circuit-breaker. Harmonization of ANSI and IEC Testing, (See Discussion.) IEEE Transactions on Power Delivery*, Vol. 3, No. 4, October 1988

[63] S.S. Berneryd, *Parallel switching with SF_6 puffer circuit-breakers*, IWD 13-00 (WG11)06

[64] K.K. Nishikawara, *Application of Current Limiting Reactors in Substations*, Canadian Electrical Association Spring Meeting, March 1980, Montreal, Canada

[65] D.F. Peelo, G.S. Polovick, J.H. Sawada, P. Diamanti, R. Presta, A. Sarshar and R. Beauchemin, *Mitigation of Circuit-breaker Transient Recovery Voltages Associated with Current Limiting Reactors*, IEEE Transactions on Power Delivery, Vol. 11, No. 2, April 1996

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

[66] *IEEE Transactions on Power Delivery*, Vol. 11, No. 2, April 1996, pp 865-870

[67] CIGRE Technical Brochure 362, *Technical requirements for substation equipment exceeding 800 kV*, 2008

[68] CIGRE Technical Brochure 456, *Background of technical specifications for substation equipment exceeding 800 kV AC*, 2011

[69] ANSI C37.06.1-2000, *Guide for High-Voltage Circuit Breakers Rated on Symmetrical Current Basis Designated "Definite Purpose for Fast Transient Recovery Voltage Rise Times"*

[70] IEEE Std C37.09-1999, *IEEE Standard Test Procedure for AC High-Voltage Circuit Breakers Rated on a Symmetrical Current Basis*

[71] ISO 3, *Preferred numbers – Series of preferred numbers*

IEC standards

[72] IEC 60050-601, *International Electrotechnical Vocabulary – Chapter 601: Generation, transmission and distribution of electricity – General*

[73] IEC 60050-604, *International Electrotechnical Vocabulary – Chapter 604: Generation, transmission and distribution of electricity – Operation*

[74] IEC 60059, *IEC standard current ratings*

[75] IEC 60077 (all parts), *Railway applications – Electric equipment for rolling stock*

[76] IEC 60143-2, *Series capacitors for power systems – Part 2: Protective equipment for series capacitor banks*

[77] IEC 60694, *Common specifications for high-voltage switchgear and controlgear standards*

[78] IEC 60721-2-3, *Classification of environmental conditions – Part 2: Environmental conditions appearing in nature – Air pressure*

[79] IEC 60943, *Guidance concerning the permissible temperature rise for parts of electrical equipment, in particular for terminals*

[80] IEC 61633, *High-voltage alternating current circuit-breakers – Guide for short-circuit and switching test procedures for metal-enclosed and dead tank circuit-breakers*[11]

[81] IEC 62271-100:2001, *High-voltage switchgear and controlgear – Part 100: High-voltage alternating-current circuit-breakers*[12]
Amendment 1:2002
Amendment 2:2006

[82] IEC 62271-108, *High-voltage switchgear and controlgear – Part 108: High-voltage alternating current disconnecting circuit-breakers for rated voltages of 72,5 kV and above*

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

[11] This publication was withdrawn.

[12] This publication was withdrawn.

[83] IEC 62271-109, *High-voltage switchgear and controlgear – Part 109: Alternating-current series capacitor by-pass switches*

[84] IEC 62271-302, *High-voltage switchgear and controlgear – Part 302: Alternating current circuit-breakers with intentionally non-simultaneous pole operation*

[85] IEC 62271-308, *High-voltage switchgear and controlgear – Part 308: Guide for asymmetrical short-circuit breaking test duty T100a*[13]

References to Clause 2

[86] Allan Greenwood, *Electrical Transients in Power Systems*, John Wiley & Sons, Inc., New York: ISBN 0-471-62058-0

[87] Ruben D. Garzon, *High-voltage Circuit-breakers, Design and Application*, Marcel Dekker Inc., New York- ISBN 0-8247-9821-x

[88] Editor: C.H. Flurscheim: *Power circuit-breaker theory and design*, Peter Peregrinus Ltd., Stevenage: ISBN 0-906048-70-2

[89] Roberto Colombo: *Disjuntores em sistemas de potencia (port.)*, Nobel, Sao Paulo: ISBN 85-213-0381-5

[90] Editor: Manfred Lindmayer: *Schaltgeräte, Grundlagen, Aufbau, Wirkungsweise*, Springer Verlag, Berlin: ISBN 3-540-16706-4. New York: ISBN 0-387-16706-4.

[91] Lou van der Sluis: *Transients in Power Systems*, John Wiley & Sons, Ltd, ISBN 0-471-48639-6.

[92] IEEE C37.010, 1999: *Application Guide for AC High-Voltage Circuit-breakers Rated on a Symmetrical Current Basis*

References to Clause 6

[93] B.Calvino et al., *Quelques aspects des containtes supportées par les disjoncteurs HT à la coupure d'un court-circuit*, CIGRE session paper 13-08 (1974)

[94] C. Guilloux, Y. Therme, P.G. Scarpa: *Measurement of post arc current in H.V. circuit-breakers. Application to short circuit tests with ITRV*. IEEE Transactions on Power Delivery, vol.8 (1993), No.3, pp. 1148-1154

References to Clause 7

[95] ANSI/IEEE C37.011-2005, *Application Guide for Transient Recovery Voltage for AC High-Voltage Circuit-breakers*, February 2006

[96] D. Dufournet, *Harmonization of IEC and IEEE Standards for High-Voltage Circuit-Breakers and Guidance for Non-standard Duties*, CIGRE International Technical Colloquium, September 12&13, 2007

[97] C.L.Wagner, D.Dufournet, G.Montillet, *Revision of the Application Guide for Transient Recovery Voltage for AC High-Voltage Circuit-breakers of IEEE C37.011: A Working*

[13] This publication was withdrawn.

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

Group Paper of the High-voltage Circuit-breaker Subcommittee, IEEE Transactions on Power Delivery, January 2007, pp 161-166.

[98] Smith K., Dufournet D. *Harmonization of IEC and IEEE TRV waveforms, Tutorial on Power Circuit-breakers*, presented at IEEE PES General Meeting in Pittsburgh, 2008.

[99] ANSI/IEEE Standards C37.04, *IEEE Standard Rating Structure for AC High-Voltage Circuit-Breakers*, Clause 5.11.4.2; and ANSI/IEEE C37.09, *IEEE Standard Test Procedure for AC High-Voltage Circuit-Breakers*, Clause 4.6.5.4

[100] A. Greenwood, *Electrical Transients in Power Systems* (book), 2nd Edition, John Wiley & Sons Inc. 1991, Chapter 9.7.3

[101] C. H. Flurscheim (Ed.). *Power circuit-breaker theory and design* (book), Peter Peregrinus Ltd., 2nd Edition 1982, Chapter 3.3.2

[102] E. Bolton, D. Birthwhistle, P. Bownes, M.G. Dwek, G.W. Routledge. *Overhead-line parameters for circuit-breaker application*, Proc. of the IEE, power, vol. 120, No. 5, 1973, pp 561 to 573

[103] R.G. Colclaser, Jr., J.E. Beehler, T.F. Garrity. *A field study of the short-line fault component of transient recovery voltage, IEEE Trans. Power Apparatus and Systems*, Vol. PAS-94, No. 6, 1975, pp. 1943 to 1953

[104] U. Habedank, R. Kugler, *Theoretical and experimental studies of the critical line length for the interruption of short-line faults, IEEE Trans. Power Apparatus and Systems*, Vol. PAS 100, July 1981, pp 3345-3357

[105] B.Thorén, *Short-line faults*. Elteknik 9 (1966) N°2 (February)

References to Clause 9

[106] McCauley (T.M.), Pelfrey (D.L.), Roettger (W.C.), Wood (C.E.). *The impact of Shunt Capacitor Installations on Power Circuit-breaker Applications. IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-99, N°6 (1980-11)

[107] O'Leary (R.P.), Harner (R.H.), *Evaluation of Methods for Controlling the Overvoltages Produced by Energization of a Shunt Capacitor Bank*, CIGRE Session 1988, Report 13-05 (1988).

[108] Heidman (D.E.), Johnson (I.B.), Titus (C.H.), Wilson (D.D.), *Switching of Extra-High-Voltage Circuits, Surge reduction with circuit-breaker resistors. IEEE Transactions on Power Apparatus and Systems*, Vol.83 (1964-12)

[109] Konkel (H.E.), Legate (A.C.), Ramberg (H.C.), *Limiting switching surge overvoltages with conventional power circuit-breakers. IEEE Transactions on Power Apparatus and Systems*, Vol.96 (1977-03)

[110] CIGRE WG 13-02, *Switching overvoltages in EHV and UHV systems with special r eference to closing and reclosing transmission lines*, Electra N°30 (1973-10)

[111] *Electrical Transmission and Distribution Book.* East Pittsburgh, Pa.: Westinghouse Electric Corporation, 1950

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

[112] IEEE Committee Report Bibliography on Switching of Capacitive Circuits Exclusive of Series Capacitors, *IEEE Transactions on Power Apparatus and Systems,* vol PAS 89, Jun/Jul 1970, pp 1203-1207

[113] Johnson, I.B.; Schultz, A.J.; Schultz, N.R.; and Shores, R.B., *AIEE Transaction*, pt III, 1955 pp 727-736

[114] H.M. Pflanz and G.N. Lester, *Control of Overvoltages on Energizing Capacitor Banks. IEEE Transactions on Power Apparatus and Systems*, vol. PAS-92, pp. 907 – 915, No. 3, May/June 1973

References to Clause 13

[115] E. Haginomori et al., *TRVs and Fault Clearing Stresses in Extra-high-voltage Radial Networks*, Electrical Engineering in Japan Vol. No. 4 1994

[116] A. Braun et al., *Characteristic Values of the Transient Recovery Voltage for Different Types of Short-circuits in an Extensive 420 kV System*. etz-a Volume 97 (1976) pp 489 to 493

[117] P. Baltensperger et al., *Transient Recovery Voltage in High-voltage Networks – Terminal Fault*, CIGRÉ session paper 13-10, 1968

[118] R. G. Colclaser Jr., J. E. Beehler, and T. F. Garrity, *A Field Study of Bus Fault Transient Recovery Voltages*. IEEE Trans. PAS 95 (1976), 1769-1776

[119] R. Harner and J. Rodriguez, *Transient Recovery Voltages Associated with Power-system, Three-phase Transformer Secondary Faults*, IEEE Transactions, Vol. PAS-91, September/October 1972

[120] P. G. Parrott. ,*A Review of Transformer TRV Conditions*, ELECTRA No. 102 pages 87-118.

[121] CIGRÉ Technical Brochure 362, *Technical Requirements for Substation Equipment Exceeding 800 kV*, December 2008

References to Clause 16

[122] IEEE Standard C37.015, *IEEE Application Guide for Shunt Reactor Switching*, 1993

NOTE IEEE C37.015 includes an extensive list of references which are not repeated here.

References to Annex I

[123] *The Vacuum Interrupter, Theory, Design and Application by Paul G. Slade*, © 2008 by Taylor & Francis Group CRC Press – Taylor & Francis Group, 6000 Broken Sound Parkway NW, Suite 300, Boca Raton, FL 33487-2742, ISBN 13: 978-0-8493-9091-3 (Hardcover)

[124] *Vacuum Switchgear by Allan Greenwood*, IEE Power Series 18, © 1994, IEE, London, UK, ISBN 0 85296 855 8

[125] CIGRE 2002 Paper 13-01, *Generator Circuit-breaker, SF6 Breaking Chamber Interruption of Current with non-zero passage – Influence of cable connection on TRV of system-fed faults*, D. Dufournet – J.M. Willième

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

[126] IEEE C37.011 – 2011, *IEEE Guide for the Application of Transient Recovery Voltage for AC High-Voltage Circuit Breakers*

[127] A. F.Gabrielle, P. P. Marchenko, and G. S. Vasell, *Electrical Constants and Relative Capabilities of Bundled Conductor Transmission Lines, IEEE Transactions on Power Apparatus and Systems*, vol. 83, Jan 1964, pp 78-92

[128] CIGRE Technical Brochure 134:2000, *Transient recovery voltages in medium voltage networks*

[129] van der Sluis, L., and Janssen, A.L.J., *Clearing faults near shunt capacitor banks, IEEE transactions on power delivery*, Vol. 5, No. 3, July 1990, pp. 1346-1354

[130] IEEE 1036-1992, *IEEE Guide for Application of Shunt Capacitors*

[131] R. Eriksson and V.S. Rashkes, *Three-phase interruption of single and two-phase faults: Breaking stresses in the healthy phase*, Electra 67, 1980, pp. 77-92

[132] IEC 60068-1, *Environmental testing – Part 1: General and guidance*

[133] IEC TS 60816, *Guide on methods of measurement of short duration transients on low-voltage power and signal lines*

[134] D.F. Peelo, *Current Interruption Transient Calculation*, John Wiley & Sons Ltd., April 2014

[135] IEEE C57.142 – 2010: *IEEE Guide to Describe the Occurrence and Mitigation of Switching Transients Induced by Transformers, Switching Device, and System Interaction*

[136] W.M.C. van den Heuvel, J.E. Daalder, M.J.M. Boone and L.A.H. Wilmes, *Interruption of Dry-Type Transformer in No-Load by a Vacuum Breaker*, Eindhoven University of Technology Report 83-E-141, August 1983

[137] J.F. Perkins, *Evaluation of Switching Surge Overvoltages on Medium Voltage Power Systems, IEEE Transactions of Power Apparatus and Systems*, Vol. PAS-101(6), June 1982

[139] G.C. Damstra, *Virtual chopping phenomena switching three-phase inductive currents*, CIGRE SC 13 colloquium, Helsinki, Finland, 1981

[139] Electra 173, *Specified Time Constants for Testing Asymmetric Current Capability of Switchgear*, August 1997, pp 19-31

[140] D. Dufournet, J.M. Willième, G. Montillet, *Design and Implementation of an SF6 Interrupting Chamber Applied to low range Generator Circuit-breaker suitable for Interruption of Current having a Non-zero Passage*, IEEE Transactions on Power Delivery, vol. 17, N°4, October 2002

[141] K.K. Nishikawara, *Application of Current Limiting Reactors in Substations*, Canadian Electrical Association Spring Meeting, March 1980, Montreal, Canada

[142] D.F. Peelo, G.S. Polovick, J.H. Sawada, P. Diamanti, R. Presta, A. Sarshar and R. Beauchemin, *Mitigation of Circuit-breaker Transient Recovery Voltages Associated with Current Limiting Reactors*, IEEE Transactions on Power Delivery, Vol. 11, No. 2, April 1996

IECNORM.COM : Click to view the full PDF of IEC TR 62271-306:2012+AMD1:2018 CSV

[143] T. Fuhrmann, S. Schlegel, S. Großmann and M. Hoidis: Investigations on stationary electrical joints with a bare and a silver or nickel coated contact partner regarding the permissible temperature limit according to ANSI IEEE and IEC, DOI:10.1109/HOLM.2014.7031050

[144] CIGRE Technical Brochure 430: SF_6 tightness guide – 2010, ISBN: 978-2-85873-118-3

[145] IEC 62271-37-013:2015: High-voltage switchgear and controlgear – Part 37-013: Alternating-current generator circuit-breakers

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

Part 306: Guide to IEC 62271-100, IEC 62271-1 and other IEC standards related to alternating current circuit-breakers

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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This Consolidated version is not an official IEC Standard and has been prepared for user convenience. Only the current versions of the standard and its amendment(s) are to be considered the official documents.

This Consolidated version of IEC TR 62271-306 bears the edition number 1.1. It consists of the first edition (2012-12) [documents 17A/1003A/DTR and 17A/1021/RVC] and its amendment 1 (2018-08) [documents 17A/1161/DTR and 17A/1169/RVDTR]. The technical content is identical to the base edition and its amendment.

This Final version does not show where the technical content is modified by amendment 1. A separate Redline version with all changes highlighted is available in this publication.

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The main task of IEC technical committees is to prepare International Standards. However, a technical committee may propose the publication of a technical report when it has collected data of a different kind from that which is normally published as an International Standard, for example "state of the art".

IEC 62271-306, which is a technical report, has been prepared by subcommittee 17A: High-voltage switchgear and controlgear, of IEC technical committee 17: Switchgear and controlgear.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62271 series, published under the general title *High-voltage switchgear and controlgear*, can be found on the IEC website.

The document follows the structure of IEC 62271-1 and IEC 62271-100. The topics addressed appear in the order they appear in IEC 62271-1 and IEC 62271-100.

The committee has decided that the contents of the base publication and its amendment will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION to the Amendment

At the SC 17A meeting held in Delft (NL) in 2013, the decision was made form a new maintenance team (MT 57) with the task to amend/revise IEC 62271-306. The objective was to update the publication to amendment 2 of IEC 62271-100. Together with MT 34 (IEC 62271-1), MT 36 (IEC 62271-100) and MT 28 (IEC 62271-101) the decision was made to move some of the informative annexes to IEC 62271-306.

This amendment includes the following significant technical changes.

– Annex G of IEC 62271-1:2007 has been included;
– Annexes E, G, H, J, L and Q of IEC 62271-1:2007 have been included;
– I.2 of IEC 62271-100:2008 + A1:2012 has been included;
– Informative parts of Annex O of IEC 62271-100:2008 have been included;
– Former Clause 14 has been added to Clause 13;
– Clause 14 now has heading "Synthetic making and breaking tests". This clause contains annexes A, B, C, D and G of IEC 62271-101;
– Clause 9 has been restructured;
– 16.4 (No-load transformer switching) has been rewritten;
– Annex B has been expanded to include information about fully compensated transmission lines and cables;
– Annex D has been rewritten.

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HIGH-VOLTAGE SWITCHGEAR AND CONTROLGEAR –

Part 306: Guide to IEC 62271-100, IEC 62271-1 and other IEC standards related to alternating current circuit-breakers

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1 General

1.1 Scope

This part of IEC 62271 is applicable to a.c. circuit-breakers designed for indoor or outdoor installation and for operation at frequencies of 50 Hz and 60 Hz on systems having voltages above 1 000 V.

NOTE While this technical report mainly addresses circuit-breakers, some clauses (e.g. Clause 5) apply to switchgear and controlgear.

This technical report addresses utility, consultant and industrial engineers who specify and apply high-voltage circuit-breakers, circuit-breaker development engineers, engineers in testing stations, and engineers who participate in standardization. It is intended to provide background information concerning the facts and figures in the standards and provide a basis for specification for high-voltage circuit-breakers. Thus, its scope will cover the explanation, interpretation and application of IEC 62271-100 and IEC 62271-1 as well as related standards and technical reports with respect to high-voltage circuit-breakers.

Rules for circuit-breakers with intentional non-simultaneity between the poles are covered by IEC 62271-302.

This technical report does not cover circuit-breakers intended for use on motive power units of electrical traction equipment; these are covered by the IEC 60077 series.

Generator circuit-breakers installed between generator and step-up transformer are not within the scope of this technical report.

This technical report does not cover self-tripping circuit-breakers with mechanical tripping devices or devices which cannot be made inoperative.

Disconnecting circuit-breakers are covered by IEC 62271-108.

By-pass switches in parallel with line series capacitors and their protective equipment are not within the scope of this technical report. These are covered by IEC 62271-109 and IEC 60143-2.

In addition, special applications (among others parallel switching, delayed current zero crossings) are treated in annexes to this document.

1.2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60060-1:2010, *High-voltage test techniques – Part 1: General definitions and test requirements*

IEC 60071-1:2006, *Insulation co-ordination – Part 1: Definitions, principles and rules*

IEC 60071-2:1996, *Insulation co-ordination – Part 2: Application guide*

IEC 60376, *Specification of technical grade sulfur hexafluoride (SF_6) for use in electrical equipment*

IEC 60480, *Guidelines for the checking and treatment of sulfur hexafluoride (SF_6) taken from electrical equipment and specification for its re-use*

IEC 62146-1, *Grading capacitors for high-voltage alternating current circuit-breakers*[1]

IEC 62271-1:2007, *High-voltage switchgear and controlgear – Part 1: Common specifications*

IEC 62271-4, *High-voltage switchgear and controlgear – Part 4: Handling procedures for sulphur Hexafluoride (SF_6)* [2]

IEC 62271-100:2008, *High-voltage switchgear and controlgear – Part 100: Alternating-current circuit-breakers*
Amendment 1:2012
Amendment 2:2017

IEC 62271-101:2012, *High-voltage switchgear and controlgear – Part 101: Synthetic testing*

IEC 62271-102:2001, *High-voltage switchgear and controlgear – Part 102: Alternating current dosconnectors and earthing switches*

IEC 62271-110:2012, *High-voltage switchgear and controlgear – Part 110: Inductive load switching*

IEC 62271-310, *High-voltage switchgear and controlgear – Part 310: Electrical endurance testing for circuit-breakers above a rated voltage of 52 kV*

2 Evolution of IEC standards for high-voltage circuit-breaker

Questions arise frequently concerning the basis and interpretation of standards IEC 62271-100 and IEC 62271-1. In most cases, these questions were due to a lack of background knowledge of the values and requirements laid down in these standards.

A selected number of reference textbooks is listed in the Bibliography. It must be remembered that the technology of high-voltage circuit-breakers is continuously progressing and will continue to do so in the future. Therefore, it is advisable to use such textbooks primarily as a source of information on network behaviour, such as switching conditions, transients, etc., and not for switchgear design.

As the installation of standard equipment in general is more economical than special designs, the application guide will help the utility and industrial engineers in the selection of the appropriate ratings to conform to their needs and specifications. It will enable them to judge which rating is necessary when specifying their circuit-breakers. This should take into account that in future high-voltage networks which will be worked harder and closer to their limits and that high-voltage circuit-breakers of present day technology are designed and procured for a lifetime of several decades. It is recognised that certain conditions may necessitate

[1] To be published.

[2] To be published.

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requirements which are outside the circuit-breaker standards. In such cases, the technical report will help to specify the various ratings or possible additional testing to verify the suitability of the circuit-breaker for a specific application or condition.

Standards should be written fit for purpose, i.e. they should reflect general system requirements to ensure that the installed equipment works properly. Although it is recognised that not 100 % of all conditions occurring in service can be covered, long term experience with high-voltage switchgear standards shows that system conditions are generally covered adequately. Nevertheless, the feedback from service and new developments in equipment and networks must be taken into account in their revision, making standardization an ongoing process. This technical report will be a forum to provide the necessary information concerning the background of changes in the standards.

Technical specification aspects are not generally considered in standards. However, this application guide will address such aspects where appropriate.

As high-voltage transmission and distribution systems and high-voltage circuit-breakers developed it was found necessary to provide standards for circuit-breakers, first on national basis. For example, already in 1923 the first edition of the British Standard B.S.S. No. 116 for circuit-breakers was issued.

In the late 1920s it was recognized that an international agreement should be obtained for a specification for high-voltage circuit-breakers, particularly with respect to their behaviour under short-circuit condition. This lead to the establishment of the "IEC Advisory Committee No. 17" which met for the first time in Stockholm in 1930 and drafted some preliminary recommendations on the international standardization of circuit-breakers.

After a series of specially convened meetings the first IEC Specification No. 56 for Alternating-Current Circuit-Breakers, Chapter I, Rules for Short-Circuit Conditions, was issued in the summer of 1937, with international approval and recognition as a basis upon which to establish national specifications. The first edition of IEC 56 was bilingual and consisted of 55 pages.

Also at that time, already, the need was seen to have Certificates of Ratings issued by approved Testing Authorities to confirm the compliance with Standard Specifications.

The second world war interrupted the further work on the IEC circuit-breaker standards. In 1954 the second edition was published which used and continued the concept of the first edition. It was intended that the IEC Specification No. 56 should ultimately incorporate five chapters which were to be discussed in the following order:

Chapter I	Rules for short-circuit conditions.
	First edition of Publication 56 to be revised and enlarged in a second edition.
Chapter II	Rules for normal-load conditions.
	Part 1 – Rules for temperature-rise.
	Part 2 – Rules for operating conditions.
Chapter III	Rules for strength of Insulation.
Chapter IV	Rules for the selection of circuit-breakers for service.
Chapter V	Rules for the maintenance of circuit-breakers in service.

Actually, the second edition, as the first one, did not progress beyond Chapter I. It was bilingual and had a total of 77 pages. According to its scope it covered a.c. circuit-breakers of 1 000 V and above.

Some major features were:

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– the breaking capacity was expressed in MVA by 2 values, one for a symmetrical and the other for an asymmetrical breaking current;

– the TRV, defined as "restriking voltage", was of single frequency. The amplitude factor or crest value and the TRV frequency or rate-of-rise were not specified but to be evaluated in the tests;

– the first-pole-to-clear factor in general was 1,5. However, in a note allowance was made to use 1,3 for circuit-breakers for earthed systems;

– 50 Hz and 60 Hz were no problem, as for making and breaking tests the tolerance of the frequency was ±25 %;

– the short-circuit current breaking tests consisted of test-duties 1 to 5 with 10 %, 30 %, 60 % and 100 % of the rated symmetrical and the rated asymmetrical breaking current.

Edition 3 was issued in 1971 with a new structure. It applied to high-voltage a.c. circuit-breakers rated above 1 000 V and had six parts which were published as separate booklets:

Publication 56-1:	Part 1: General and definitions.
Publication 56-2:	Part 2: Rating.
Publication 56-3:	Part 3: Design and construction.
Publication 56-4:	Part 4: Type tests and routine tests.
Publication 56-5:	Part 5: Rules for the selection of circuit-breakers for service.
Publication 56-6:	Part 6: Information to be given with enquiries, tenders and orders and rules for transport, erection and maintenance.

IEC 56 consisted of 294 pages when it was issued, but over the years a large number of amendments was added. Out-of-phase was covered by its own publication, IEC 267.

The third edition was the first comprehensive IEC Standard on high-voltage circuit-breakers meeting the originally intended goals. It included, also, the general requirements which are now compiled in IEC 62271-1.

Compared to the second edition a large number of changes were introduced:

– for the first time mechanical tests, tests on insulation properties, tests on auxiliary and control circuits, temperature rise tests, etc., were specified;

– the R 10 series is used for rated normal and breaking currents;

– the TRV (first time to use this term) representation by two or four parameters and the definitions as used up to today are installed;

– for rated voltages up to 100 kV the first-pole to clear factor is 1,5, for 123 kV and above it is alternatively 1,3 or 1,5;

– the supply side rate-of-rise of TRV for 123 kV and above for terminal fault is 1,0 kV/μs for TD 4; 2,0 kV/μs for TD 3 and 5,0 kV/μs for TD 2;

– the short-line fault is introduced. The specified surge impedance is 480 Ω for lines with 1 conductor/phase (52 – 245 kV < 40 kA), 375 Ω for 2 conductors/phase and 330 Ω for 3 or 4 conductors per phase. The line side peak factor is 1,7, 1,6, or 1,5, respectively. The source side rate-of-rise is 0,67 kV/μs;

– test for capacitive current switching (line and cable charging, single capacitors) are prescribed;

– not only type tests, but also routine test procedures are defined.

Edition 4 of IEC 56, published 1987, followed the scheme of the 3rd edition. However, to avoid a duplication of requirements in the various standards for high-voltage switching equipment, IEC 56 was reduced to those requirements that were specific for high-voltage a.c. circuit-breakers. The "common clauses for high-voltage switchgear and controlgear" was published as a separate standard in 1980 with reference number IEC 694.

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Edition 4 of IEC 60056 consisted of one book of 329 pages. To conform with actual service conditions some major changes were incorporated:

– as all systems rated 245 kV and higher are effectively earthed only a first-pole-to-clear factor 1,3 is specified for these voltage levels. For 100 kV to 170 kV alternatives 1,3 and 1,5 are specified;
– based on a large number of network investigations the supply side rate-of-rise of TRV is increased to 2,0 kV/μs for 100 %, 3,0 kV/μs for 60 % and 5,0 kV/μs for 30 % rated breaking current;
– to take into account the clashing of the conductors of a line phase due to the forces of the short-circuit current, which makes it similar to a single conductor, a uniform surge impedance of 450 Ω is specified for all short-line fault tests. The line side peak value is 1,6, the supply side rate-of-rise 2,0 kV/μs;
– the initial Transient Recovery Voltage (ITRV) is introduced for rated voltages of and above 100 kV;
– out-of-phase specifications are included;
– to prove that capacitive current breaking is performed without restrikes the number of tests per duty is increased;
– also, the number of operations during mechanical type tests is increased from 1 000 to 2 000.

And still, IEC 60056 continued to grow. The 4th edition was revised, resulting in the first edition of IEC 62271-100 published in 2001. The first edition of IEC 62271-100 had 575 pages. The structure of the document was retained but its content was revised taking into account service experience and requirements by the utilities:

– classifications of circuit-breaker are introduced with respect to mechanical and (for medium voltage) electrical endurance and restrike behaviour when switching capacitive loads;
– more severe test conditions are prescribed for circuit-breakers to prove a very low probability of restrikes in capacitive current switching;
– for type tests the number of test specimen is limited;
– some test procedures are prescribed in more detail;
– critical current tests and single-phase and double-earth fault tests are treated in particular;
– tolerances are given on practically all test quantities during type tests;
– special cases time constants, longer than 45 ms, are specified for the different levels of rated voltages.

The first edition of IEC 62271-100 was revised and the second edition was published in 2008. The following major changes were made:

– the introduction of harmonised (IEC and IEEE) TRV waveshapes for rated voltages of 100 kV and above (amendment 1 to the first edition);
– the introduction of cable and line systems with their associated TRVs for rated voltages below 100 kV (amendment 2 to the first edition);
– the inclusion of IEC 61633 (Guide for short-circuit and switching tests procedures for metal enclosed and dead tank circuit-breakers) and IEC 62271-308 (Guide for asymmetrical short-circuit breaking test duty T100a).

IEC 60694 covered common matters for equipment falling under the responsibility of subcommittees IEC SC 17A and SC 17C, such as circuit-breakers, disconnectors and earthing switches, switches and their combinations with other equipment, gas-insulated substations, etc. Mainly, these specifications concerned normal and special service conditions, ratings and tests on dielectric withstand, normal and short-circuit current carrying auxiliary and control circuits, and common rules for design and construction. The first edition had 78 pages.

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The experience with this standard on common specifications was very positive. Therefore, when the decision was made to revise IEC 694 this was largely to take into account items which had not been covered by standards, so far. Very little had to be changed or updated in the existing clauses of the first edition. This second edition with title "Common specifications for high-voltage switchgear and controlgear" published in 1996 with reference IEC 60694, has, among others, additional chapters which deal with safety aspects of electrical, mechanical, thermal and operational nature. This had, in particular, consequences for the rules for design and construction as well as tests which now, also, covered topics such as interlocking, position indication, degree of protection by enclosures and tightness. A new and important item that was introduced was electromagnetic compatibility (EMC). Naturally, service and test experiences which had been gathered on the basis of the first edition reflected in the revision. For example, the number of test specimen became limited, the conditions for identification of the test object became more pronounced, and the criteria to pass the test were written in a more exact manner.

The second edition of IEC 60694 was revised and published in 2007 as the first edition of IEC 62271-1.

Manufacturers, users and test laboratories recognize that the reliability of high-voltage switchgear is of crucial importance for the safety and availability of the supply of electric energy. The overall high level of reliability and performance which is common today has its roots in the very good quality of the standards for high-voltage switchgear and controlgear. They are continuously updated to reflect the actual status of the respective technologies.

3 Classification of circuit-breakers

3.1 General

IEC 62271-100 defines the following classes of circuit-breakers:

– Class E1 and E2 of electrical endurance are defined in 3.4.112 and 3.4.113 of IEC 62271-100:2008;
– Class C1 and C2 for capacitive current switching are defined in 3.4.114 and 3.4.115 of IEC 62271-100:2008;
– Class M1 and M2 of mechanical endurance are defined in 3.4.116 and 3.4.117 of IEC 62271-100:2008;
– Class S1 and S2 for specific system application are defined in 3.4.119 and 3.4.120 of IEC 62271-100:2008.

The different classes and their specific applications are discussed in detail in this subclause.

3.2 Electrical endurance class E1 and E2

Two classes are defined for circuit-breakers rated ≤ 52 kV:

– Class E1: basic electrical endurance;
– Class E2: electrical endurance covering the expected operating life of the circuit-breaker.

A circuit-breaker class E1 has a basic electrical endurance, whereas a circuit-breaker of class E2 is designed such as not to require maintenance of the interrupting parts of the main circuit during its expected operating life.

There is no mandatory requirement for electrical endurance for circuit-breakers rated > 52 kV in IEC 62271-100.

Class E2 is defined in IEC 62271-310 for circuit-breakers > 52 kV in the same way as for circuit-breakers ≤ 52 kV. This application is restricted to circuit-breakers used for overhead lines. IEC 62271-310 proposes a unified test procedure for this class E2.

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Class E2 is intended for a low maintenance circuit-breakers used for applications where frequent fault currents are switched.

3.3 Capacitive current switching class C1 and C2

Two classes are defined:

– Class C1: low probability of restrike;

– Class C2: very low probability of restrike.

IEC 60056 contained a definition of the term "restrike-free circuit-breaker". This definition was removed when the capacitive current switching requirements and test procedures were revised. The revised requirements and test procedures were first published in the first edition of IEC 62271-100 (published in 2001). The reason why the term "restrike-free circuit-breaker" was deleted from the standard was because it did not correspond to a physical reality.

The first edition of IEC 62271-100 introduced the term "restrike probability" during the type tests, corresponding to a certain probability of restrike in service, which depends on several parameters (see 9.4.6). For this reason, the term cannot be quantified in service.

The main differences in restrike performance between class C1 and C2 type tests are the number of tests shots and the allowable number of restrikes. Class C2 tests are performed on a pre-conditioned circuit-breaker. Pre-conditioning is done performing 3 breaking operations at 60 % of the rated short-circuit current. The pre-conditioning was derived based on CIGRE statistics and is considered to create interrupter wear that is broadly representative of long term service conditions.

The choice for the user between class C1 and C2 depends on:

– the service conditions;

– the operating frequency;

– the consequences of a restrike to the circuit-breaker or to the system.

Class C1 is acceptable for medium-voltage circuit-breakers and circuit-breakers applied for infrequent switching of transmission lines and cables.

Class C2 is recommended for capacitor bank circuit-breakers and those used on frequently switched transmission lines and cables.

The above given conditions are essential when choosing the circuit-breaker for a capacitive switching application, the needed performance class and the voltage factor should be known and demonstrated by the relevant type test. It is important to note that the performance class may vary for different capacitive current switching applications. For example, a circuit-breaker used to switch an overhead line may be tested for class C1 whereas the same circuit-breaker is tested in accordance with class C2 for capacitor bank switching.

3.4 Mechanical endurance class M1 and M2

Two classes are defined:

– Class M1, normal mechanical endurance, a circuit-breaker mechanically type tested for 2 000 operations;

– Class M2, extended mechanical endurance, a circuit-breaker mechanically type tested for 10 000 operations).

As a general rule, the number of operations of high-voltage circuit-breakers switching transmission lines is relatively small, and class M1 is sufficient.

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For particular applications, such as frequent switching of reactors, capacitor banks, industrial applications, specification of class M2 is recommended.

It should be noted that it is always possible, in the case of a very special use (pumping station, etc.), to request a larger number of operations than that recommended for class M2.

3.5 Class S1 and S2

3.5.1 General

Two classes are defined:

– Class S1, circuit-breakers intended for use in cable systems;

– Class S2, circuit-breakers intended for use in line systems or in a cable system with direct connection (without cable) to overhead lines.

3.5.2 Cable system

A cable system is a system in which the TRV during breaking of terminal fault at 100 % of short-circuit breaking current does not exceed the two-parameter envelope derived from Table 1 of IEC 62271-100:2008.

NOTE 1 This definition is restricted to systems of rated voltages higher than 1 kV and less than 100 kV.

NOTE 2 Circuit-breakers of indoor substations with cable connection are generally in cable-systems.

NOTE 3 A circuit-breaker in an outdoor substation is considered to be in a cable-system if the total length of cable (or equivalent length when capacitors are also present) connected on the supply side of the circuit-breaker is at least 100 m. However if in an actual case with an equivalent length of cable shorter than 100 m a calculation can show that the actual TRV is covered by the envelope defined from Table 1 of IEC 62271-100:2008, then this system is considered as a cable system.

NOTE 4 The capacitance of cable-systems on the supply side of circuit-breakers is provided by cables and/or capacitors and/or insulated bus.

3.5.3 Line system

A line system is a system in which the TRV during breaking of terminal fault at 100 % of short-circuit breaking current is covered by the two-parameter envelope derived from Table 2 of IEC 62271-100:2008 and exceeds the two-parameter envelope derived from Table 1 of IEC 62271-100:2008.

NOTE 1 This definition is restricted to systems of rated voltages equal to or higher than 15 kV and less than 100 kV.

NOTE 2 In line-systems, no cable is connected on the supply side of the circuit-breaker, with the possible exception of a total length of cable less than 100 m between the circuit-breaker and the supply transformer(s).

NOTE 3 Systems with overhead lines directly connected to a busbar (without intervening cable connections) are typical examples of line-systems.

3.6 Conclusion

A circuit-breaker is defined by its complete rating, i.e. the basic short-circuit rating and, for example, with or without out-of-phase switching, with or without overhead line capacitive current switching as well as by the endurance classification such as E1, M2, etc.

It is the technical and economic responsibility of the user to select the type of circuit-breaker and its endurance classes according to:

– the technical needs, derived from the point of application and the proposed usage on the user's system;

– the management of the user's circuit-breaker population;

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– the user's maintenance policy, which is increasingly linked to the system availability and life cycle costs;

– the cost of the circuit-breakers, with preference for the purchase of standard circuit-breakers.

4 Insulation levels and dielectric tests

4.1 General

Insulation co-ordination is defined as follows (see 3.1 of IEC 60071-1:2006).

insulation co-ordination
selection of the dielectric strength of equipment in relation to the operating voltages and overvoltages which can appear on the system for which the equipment is intended and taking into account the service environment and the characteristics of the available preventing and protective devices

[SOURCE: IEC 60050-604:1987, 604-03-08, modified]

Dealing with insulation co-ordination, it should be kept in mind the difference between "voltage surges" stressing the insulation in service, and "voltage impulses" used in conventional tests.

TC 28 has classified the different types of overvoltages that can appear in the system and related those to a standardized test voltage. This relationship is given in Table 1 of IEC 60071-1:2006 and is repeated here for convenience (see Table 1).

The current insulating levels for switchgear and controlgear were prepared in 1971 by a joint working group with experts from CIGRE Study Committee A3 and from IEC Subcommittee 17A, when longitudinal and phase-to-phase insulations were not dealt with by the edition of IEC 60071-1 valid at that date. It was considered that the longitudinal insulation might have two very different purposes:

– the working function, that is the separation of two parts of a network;

– the isolating function, to ensure that no voltage is applied on a part of the network where people might be working.

For the isolating function, it was considered that the dielectric withstand of the interrupting gap of a load switch or of a circuit-breaker was not reliable enough, due to its pollution by arc by-products. The isolating function should be provided by a device meeting the requirements of IEC 62271-102 for its expected life.

When an insulation coordination study is made in accordance with the process described in IEC 60071-1, all the electric stresses likely to occur at a given site and with a given probability are taken into account. This is done with respect to the insulation phase-to-earth, phase-to-phase and longitudinal stresses. These are classified according to their front duration whatever their origins. The influence of any voltage protective devices is also considered, see Table 1 of IEC 60071-1:2006. Note that what is called "temporary" overvoltage includes the stresses generated at various frequencies, such as harmonics. The numerous correction factors are applied to each of them to take care of:

– performance criterion: the basis on which the insulation is selected so as to reduce to an economically and operationally acceptable level the probability that the resulting voltage stresses imposed on the equipment will not cause damage to equipment insulation or affect continuity of service;

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– statistical distribution: it is normally accepted to disregard those overvoltages which have a probability of occurrence less than 2 %;

– inaccuracy of input;

– effect of the equipment test assembly;

– dispersion in production;

– ageing in service: if not otherwise specified, an ageing factor of 15 % is considered for internal insulation and 5 % for external insulation;

– altitude correction.

To reduce the duration and the costs of the tests, only two types of test voltage shapes are in practical use. These are the power frequency and the standard lightning impulse voltages, for equipment up to and including 245 kV (Range I), and the standard switching and standard lightning impulse voltages, for equipment above 245 kV (Range II). For voltage range I the inherent switching surge strength (in p.u.) is higher than the magnitude of the surges at that voltage. In other words, the amount of insulation that is required to satisfy the lightning impulse and power frequency tests automatically exceed the requirements for the maximum switching surges that can occur on the system. Conversion factors are given in IEC 60071-2 so that "slow-front overvoltages" in range I or short-duration overvoltages of range II be covered by the selected test voltage shapes.

In using this approach, it follows that:

– no overvoltages larger than those used to assess the insulation levels are thought likely to occur on the incoming terminal of a switching device;

– a different probability uncertainty and performance criterion can be applied depending on whether they apply to the working function or to the isolating function. By convention, it was decided that the insulation of the "isolating distance" be the closest value to the IEC 60071-1 value but with a 15 % excess over the phase-to-earth insulation;[3]

– although no power frequency tests are required by IEC 60071-1 for range II it can be agreed that product standards may add them when necessary, which is the case with switchgear and controlgear, due to their elaborated design, and because it is a convenient voltage shape for routine tests (IEC 60071-1 deals only with type tests and does not consider the safety aspects).

There are some differences between the insulation levels stated in IEC 60071-1 and those in IEC 62271-1:

– not all of the insulation levels of IEC 60071-1 are taken into IEC 62271-1. This is because the first standard is designed for every type of equipment and some of its values are not used in the latter for switchgear;

– the switching impulse withstand voltage of longitudinal insulating is lower in IEC 62271-1. It should be noted that there are only two cases where longitudinal insulation stress occurs:

  - when a line crosses another line or a busbar;
  - and the case of switchgear and controlgear.

  In the first case, it is easy and economical to use longer clearances; it is more difficult to increase the longitudinal insulation of switchgear and controlgear, and not really necessary, as explained in 4.6. In fact, the insulation levels specified in IEC 62271-1 have been used successfully for more than twenty years (for rated voltages of 800 kV or less), and IEC TC 28, responsible of IEC 60071, agreed that switchgear standards keep their values (see minutes of meeting RM 3606/TC 28).

The splitting into two voltage ranges is done mainly in consideration of neutral earthing systems: in range II, it is considered usual that the neutrals are solidly earthed. Therefore, the

3 Nevertheless, the only safe condition to work on a network is to earth it on each side of the work site.

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voltage stresses are lower. This explains why the same lightning withstand voltage is required for 245 kV and for 300 kV.

Background information on insulation levels and associated testing is provided in 4.6.

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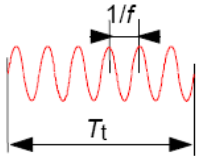
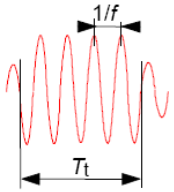
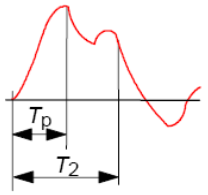
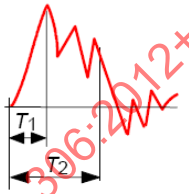
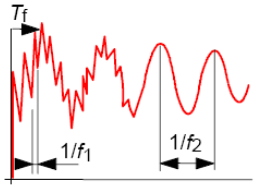
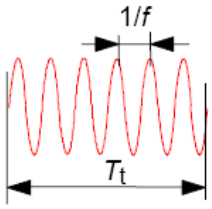
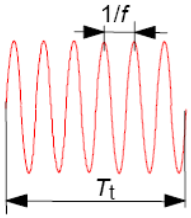
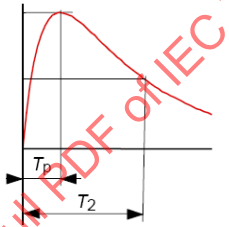
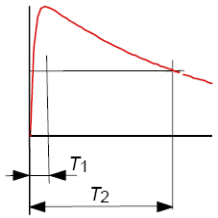
Table 1 – Classes and shapes of stressing voltages and overvoltages (from IEC 60071-1:2006, Table 1)

Class	Low frequency		Transient		
	Continuous	Temporary	Slow-front	Fast-front	Very-fast front
Voltage or overvoltage shapes					
Range of voltage or overvoltage shapes	f = 50 Hz or 60 Hz $T_t \geq$ 3 600 s	10 Hz < f < 500 Hz 0,02 s ≤ T_t ≤ 3 600 s	20 µs < T_p ≤ 5 000 µs T_2 ≤ 20 ms	0,1 µs < T_1 ≤ 20 µs T_2 ≤ 300 µs	T_f ≤ 100 ns 0,3 MHz < f_1 < 100 MHz 30 kHz < f_2 < 300 kHz
Standard voltage shapes	 f = 50 Hz or 60 Hz T_t [a]	 48 Hz ≤ f ≤ 62 Hz T_t = 60 s	 T_p = 250 µs T_2 = 2 500 µs	 T_1 = 1,2 µs T_2 = 50 µs	[a]
Standard withstand voltage test	[a]	Short-duration power frequency test	Switching impulse test	Lightning impulse test	[a]

[a] To be specified by the relevant apparatus committees.

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4.2 Longitudinal voltage stresses

Normally a circuit-breaker does not have a disconnecting function, this is the duty of the disconnector.

NOTE Circuit-breakers having a disconnecting function are covered by IEC 62271-108.

For its working function, it has firstly to withstand the recovery voltage after having extinguished the arc. In the open position it may be stressed by the power frequency voltage on one terminal with the other stressed by any of the following voltages:

– the D.C voltage resulting from the trapped charge of the overhead line in the case of no-load line or capacitor bank switching;

– power frequency voltage in out-of-phase condition, in the case when busbars or generators are switched;

– a slow-front surge in the case of a switching operation at the remote end;

– a possible fast front surge in the case of a lightning stroke.

The open circuit-breaker is normally isolated by a disconnector and may be stressed only for a short period. That is normally not the case for shunt reactor, capacitor bank, filter and bus tie (busbar) circuit-breakers. For bus tie circuit-breakers the two bus voltages rarely have a large phase shift. Exposed situations where complete out-of-phase voltages will be present for minutes do exist, e.g. in the case of circuit-breakers used for synchronisation purposes, sometimes with a higher component on the generator side.

4.3 High-voltage tests

The standard dealing with high-voltage insulation tests is IEC 60060-1, but the various types and values of dielectric tests are specified in IEC 60071-1, because their statistical meaning is to be taken into account in the process of designing insulation co-ordination. It must be kept in mind that each test voltage shape is a conventional shape to evaluate the behaviour of the insulation when stressed by various voltage stresses, short duration, slow-front or fast front (see Table 1 of IEC 60071-1:2006).

Disruptive discharge voltages are subject to random variations and usually a number of observations must be made in order to obtain a statistically significant value of the withstand voltage. Ideally, the best would be to use a test procedure providing some statistical results. To do that, it is necessary to have an idea of the limit and therefore to have at least one disruptive discharge. But if the test object includes a non-self-restoring part in its insulation system, to reach the limit would mean some destructive effect. In many cases, the insulation is composed of self-restoring parts and of non-self-restoring mixed together. Therefore, several procedures are proposed, supposedly having the same severity, which means that the probability that a "good" specimen is rejected (risk of the manufacturer) is the same as a "bad specimen" being accepted (risk of the user):

– for complete self-restoring insulation (air at atmospheric pressure associated with glass or porcelain), the "up and down" procedure provides the U_{50} value, the critical disruptive level, and an estimate of the standard deviation. It is called "procedure D" in IEC 60060-1:2010;

– for clearly defined non self-restoring insulation, "procedure A" of the same standard assess an assumed withstand voltage (three shots without disruptive discharge);

– for insulation systems composed of mixed self-restoring and non-self-restoring insulation, a compromise was found with procedures B or C, where no disruptive discharges are allowed on the non-self-restoring part of the insulation. Subclause 5.3.4 of IEC 60071-2:1996 shows how procedure B and C give the same probability to pass a test at 90 % of the maximum withstand value. This is with a much better selectivity with procedure B. The question most likely to be raised in the laboratory occurs when the last (or last two) applications of the test voltage leads to disruptive discharges, and whether they are on self-restoring insulation or not. For this reason IEC 62271-1 requires 5 non-

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disruptive discharges to conclude the test. This is aimed at giving confidence that the non-self-restoring insulation is likely to be sound.

Another problem may exist when applying atmospheric correction factors for external insulation in the case that the insulation system of the switchgear and controlgear consists of internal and external insulation in parallel. Subclause 4.3.6 of IEC 60060-1:2010 gives some guidance on how to perform the tests.

The following additional concerns may exist:

– the test voltage across longitudinal insulation or phase-to-phase is higher than the test voltage phase-to-earth. Procedures for those cases are given in 6.2.5.2 of IEC 62271-1:2007;
– three-phase switchgear and controlgear in the same enclosure: test voltages are usually applied between phase and earth, across longitudinal insulation of each pole and phase to phase separately.

4.4 Impulse voltage withstand test procedures

4.4.1 General

The purpose of this subclause is to explain the basis for the several impulse voltage withstand test methods used to verify the insulation integrity of high-voltage switching devices.

In 6.2.5 of IEC 62271-1:2007 the application of the test voltage and test conditions are given. This subclause prescribes several test series, such as testing across the open switching device, to earth, and between phases, as well as tests with power frequency and impulses with positive and negative voltage polarity. Each of these test series has to be considered individually as each of them has to show that the individual insulation under test meets the particular requirements. According to the philosophy of insulation coordination these requirements are based on a flashover probability of 10 %. This should be met by each individual insulation, as well as by the whole switching device. Consequently, adding up all tests performed on the switching device is not justified and does not give any information on the withstand probability of the whole device.

4.4.2 Application to high-voltage switching devices

For impulse tests, the following two procedures are given in 6.2.4 of IEC 62271-1:2007:

– Procedure B of IEC 60060-1:2010: 15 consecutive impulses at the rated lightning or switching impulses at the rated withstand voltage for each test condition and each polarity. The test object is considered to have passed the test if the number of disruptive discharges (flashovers) on the self-restoring part of the insulation does not exceed two for each series of 15 impulses and if no disruptive discharge occurs on non-self-restoring insulation. This method is referred to as the 15/2 method;
– As an alternative, procedure C of IEC 60060-1:2010 may be applied. In this case the test consists of three consecutive impulses for each test condition and each polarity. The test has been passed if no disruptive discharge occurs. If one disruptive discharge (flashover) occurs on the self-restoring part of the insulation, then 9 additional impulses may be applied. If no disruptive discharge occurs during these additional impulses the test object is considered to have passed the test. This test procedure is referred to as the 3/9 method. The 3/9 method is accepted only when all three phases are tested.

The theory on which the test procedures are based is described in 4.4.5.

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4.4.3 Additional criteria to pass the tests

4.4.3.1 Procedure B

Based on the 15/2 method, IEC 62271-100 states additional criteria to pass the tests. If disruptive discharges occur during the application of 15 test impulses it shall be demonstrated that they did not occur on non-self-restoring insulation (SF_6 gas is considered self-restoring). Evidence that damage has not occurred to non-self-restoring insulation can be confirmed by five consecutive impulse withstands following the last disruptive discharge. If permissible disruptive discharges occur within the last five test impulses sufficient additional verification impulses may be applied in order to achieve five consecutive withstands. A disruptive discharge is permissible during the additional verification impulses if only one such discharge occurred during the first 15 test impulses. This procedure leads to a maximum possible number of 25 impulses per series.

4.4.3.2 Procedure C

The original test method required in ANSI/IEEE C37.09 was the so-called 3/3 method. Three test impulses are applied with the following possibilities:

– all three impulses are withstands, then the test is successful and complete;
– if one disruptive discharge occurs, then three further impulses are applied and all must be withstands for the test to be successful;
– if two disruptive discharges occur, the test is a failure.

This method was later modified to the 3/9 method which simply means a disruptive discharge in the application of the first three impulses shall be followed by 9 withstands. The tolerance on the peak voltage is $^{+3}_{0}$ % in accordance with ANSI/IEEE C37.09, whereas it is ±3 % in accordance with IEC 62271-1.

4.4.4 Review and perspective

The statistical sampling plans on which the various test methods discussed above are based are described in 4.4.5.

Subclause 6.2.4 of IEC 62271-1:2007 states that the 15/2 method is the preferred test procedure and further that procedure C of IEC 60060-1:2010 “may be used when all three poles are tested”. Neither of these statements is of the “mandatory” or “advisory” nature that one expects to find in an IEC standard and presents both the manufacturer and user with a choice to be made. The attributes of both test series are shown in Table 2 and will be discussed from two perspectives, namely, insulation coordination and quality assurance.

Table 2 – 15/2 and 3/9 test series attributes

Test series	Probability of passing the test (%)	Risk (%)	
		Manufacturer (α)	User (β)
15/2	76	4,9	29,2
3/9	82	4,6	53,6
NOTE The values in column 2 are based on a flashover probability of 10 %.			

The principles and practices of insulation coordination are described in IEC 60071-1 and IEC 60071-2. In the context of insulation coordination, withstand voltage is defined as the voltage at which there is a 10 % probability of flashover. Figure 1 is derived from the operating characteristics of the two test series shown in Figure 4. The 15/2 test series has a

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76 % probability of passing the test which compares favourably to the 82 % probability for the 3/9 test series. The former test series is thus the more onerous.

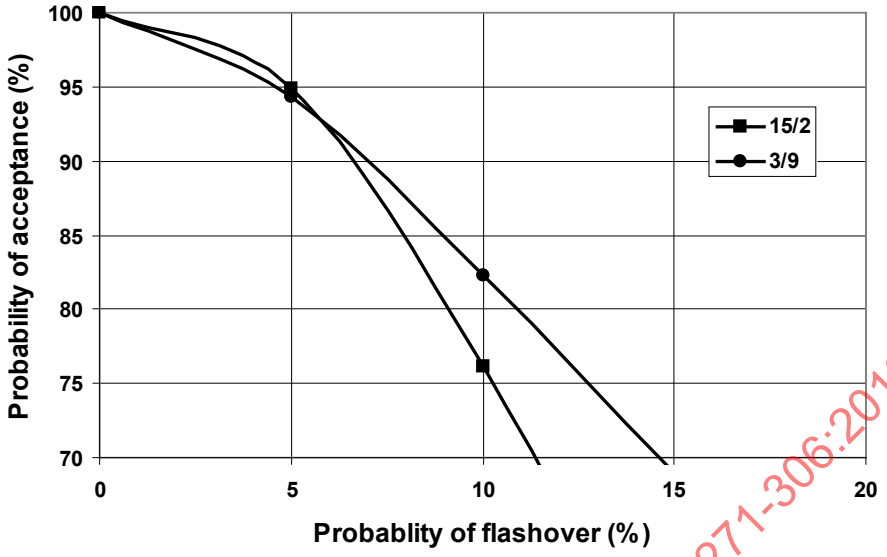

Figure 1 – Probability of acceptance (passing the test) for the 15/2 and 3/9 test series

Taking the quality assurance perspective, it is reasonably argued that a 10 % probability of flashover is too high and that 5 % is a more reasonable and applicable number. Figure 2 shows that the probability of acceptance at 5 % probability of flashover are 94,86 % and 94,7 % for the 15/2 and 3/9 test series, respectively. The corresponding probabilities of rejection are 5,14 % and 5,73 %, respectively, and the argument continues that, on this basis, the two test series are statistically equivalent. However, it is not legitimate to compare two statistical sampling plans at one point only; in fact, equivalent plans would have both similar manufacturer risks at 95 % probability of acceptance (Figure 2) and user risks at 10 % probability of acceptance as shown in Figure 3. With reference to Table 2, the manufacturer risks are near equal but there is a significant difference in the user risks with the 3/9 test series giving the higher risk.

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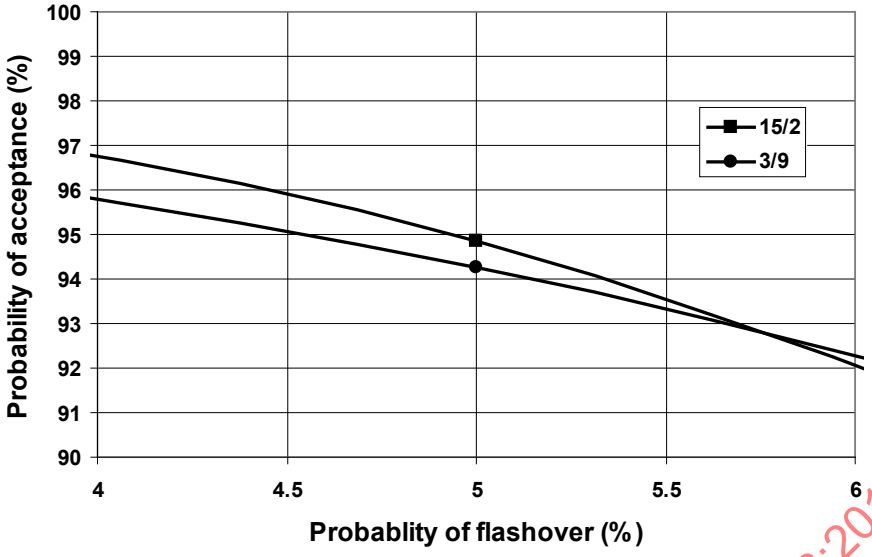

Figure 2 – Probability of acceptance at 5 % probability of flashover for 15/2 and 3/9 test series

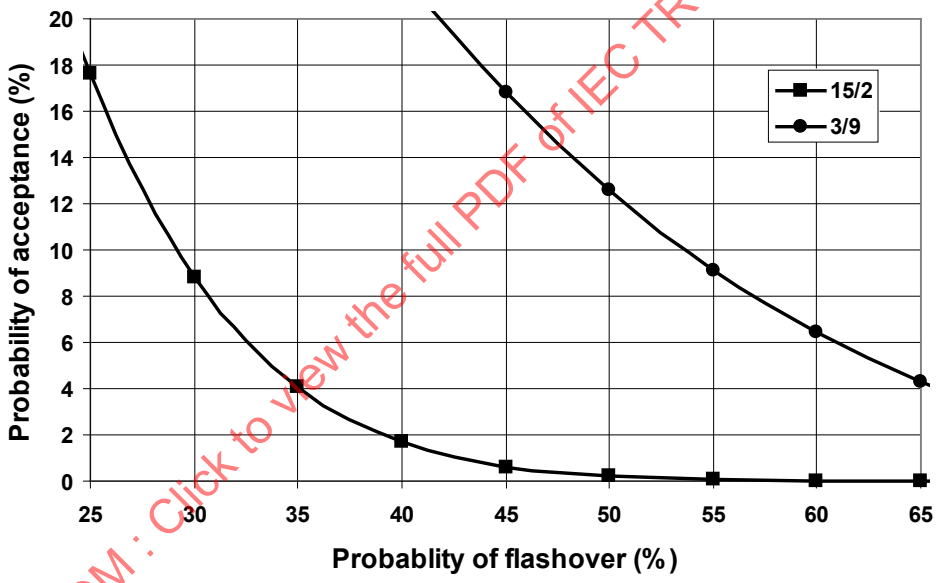

Figure 3 – User risk at 10 % probability of flashover for 15/2 and 3/9 test series

In reality, the 3/9 test series is used and accepted only in the United States and the 15/2 test series is favoured elsewhere.

The purpose of type testing is to demonstrate that the test object meets the requirements. If it does not pass the test, the reason has to be shown, and exactly what has to be improved or changed in order to justify the repetition of the test. For the new test, a new test object should be submitted which should be an improved device. One should not use the same test object or a second one of the same kind in the expectation of success in a second or third attempt.

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4.4.5 Theory

4.4.5.1 General

Originally invented to test insulators, and described in IEC 60060-1, the statistical considerations from which the impulse voltage withstand test procedures were derived actually apply to batches (or lots), i.e. to testing of a relatively large number of samples. Therefore, they are suited in a limited way, only, to prove the quality of individual items, such as switchgear.

Nevertheless, as the procedures have been generally accepted for impulse voltage withstand testing of high-voltage switchgear it may be justified to present their mathematical background.

4.4.5.2 Additive probabilities

According to one axiom of probability the probability function for mutually exclusive events is additive [1] [4]. For example the probability of event A or event B is the sum of their individual respective probabilities providing the two events are mutually exclusive.

4.4.5.3 Special law of multiplication

According to the special law of multiplication the probability that a number of independent events will all occur is the product of their individual respective probabilities [1]. For example the probability of event A and event B is the product of their individual respective probabilities providing the two events are independent.

4.4.5.4 Binomial distribution

The relative merit of the individual plans is analysed by means of the binominal probability distribution and two other relations from probability theory. However, the probability theory has a limited applicability when the number of samples is small or, in the extreme case, when this number is down to one. Yet, this analysis may be useful to understand the background of the test procedures defined in IEC 60060-1 and 6.2.4 of IEC 62271-1:2007 and IEC 62271-100.

Impulse tests are statistically a set of repeated trials. Letting "n" represent the number of trials and "r" the number of test failures, the tests can be analysed using the binominal probability distribution on the basis that the following assumptions apply [1]:

a) There are only two possible outcomes for each trial, "success" or "failure". (Textbooks usually assign the outcome associated with "r" as a success, without inferring that success is necessarily a desirable outcome. In our particular case we are designating the outcome associated with "r" a failure because in the context of dielectric testing a disruptive discharge is a failure.);

b) The probability of failure is constant from trial to trial and is denoted as "p"; the probability of success is thus $(1 - p)$;

c) There are "n" trials, where "n" is a given constant;

d) The "n" trials are independent.

The probability of r failures in n trials for a probability of failure p is given by:

$$b(r, n, p) = \binom{n}{r} p^r (1-p)^{n-r}$$

4 Numbers between square brackets refer to the references in the bibliography.

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where $\binom{n}{r} = \frac{n!}{r!(n-r)!}$

It follows from the axiom described above that the cumulative probability of r or fewer failures in n trials is:

$$B(r, n, p) = \sum_{r=0}^{r} \binom{n}{r} p^r (1-p)^{n-r}$$

$B(r,n,p)$ is the probability of acceptance of the test based on a single sampling plan where a maximum of "r" failures are allowed.

In the case of sampling schemes consisting of more than one sampling plan, the cumulative probability distributions for the respective plans are combined in accordance with the axiom and law described above to yield the probability of acceptance for various values of "p" using that scheme.

P_a will be denoted as the probability of acceptance using a particular sampling scheme.

To illustrate the application of the theory, the 3/9 method is considered. The acceptable outcomes are 3/0 or (3/1 and 9/0):

$$P_a = \binom{3}{0} p^0 (1-p)^{3-0} + \left[\binom{3}{1} p^1 (1-p)^{3-1} \times \binom{9}{0} p^0 (1-p)^{9-0} \right]$$

$$= \frac{3!}{0!(3-0)!}(1-p)^3 + \left[\frac{3!}{1!(3-1)!} p(1-p)^2 \times \frac{9!}{0!(9-0)!}(1-p)^9 \right] = (1-p)^3 + 3p(1-p)^{11}$$

The plot of P_a as a function of "p" is usually called an operating characteristic curve.

An equation and associated operating characteristic curve can be similarly developed for the 15/2 test series [2].

The operating characteristic curves for the 15/2 and 3/9 test series are plotted in Figure 4.

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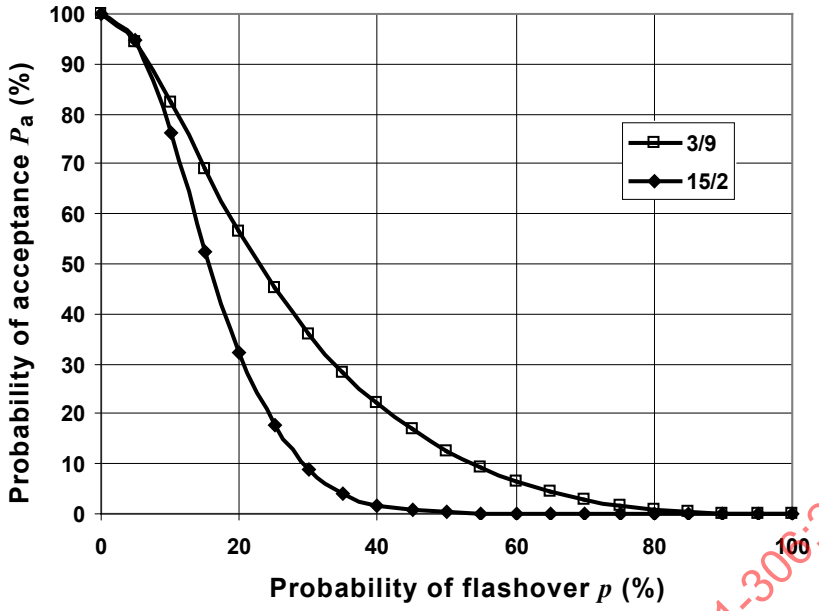

Figure 4 – Operating characteristic curves for 15/2 and 3/9 test series

4.4.5.5 Comparison of the different test methods

4.4.5.5.1 General

The various test methods are actually statistical sampling plans developed to distinguish between "good" and "bad" products out of a larger number of samples, the 15/2 method being a single sampling plan and the 3/9 method being a double sampling plan. The notion of sampling implies risk: the manufacturer's risk is that a "good" product will be rejected (fails the test) and the risk of the user is that a "bad" product will be accepted (passes the test). In reality both risks are mitigated by design safety margins and the ultimate question is which plan gives the best product quality.

To make a comparison between the different methods, two quantities need to be defined (again, it must be remembered that these considerations apply to a large number of samples and not to testing of an individual test object).

4.4.5.5.2 Manufacturer's risk (α risk)

The manufacturer's risk is the probability that a "good" lot will be rejected by the sampling plan. This risk is usually set at 5 % (corresponds to 95 % acceptance) and is stated in conjunction with a numerical definition of "good" quality such as an Acceptable Quality Level (AQL). Ideally the AQL is the value of "p" corresponding to a value of P_a equal to 95 %. The AQL is thus the maximum percent defective that, for the purpose of sampling inspection (testing in this case), can be considered satisfactory as a process average.

4.4.5.5.3 User's risk (β risk)

The user's risk is the probability that a "bad" lot will be accepted by the sampling plan and is stated in conjunction with a numerical definition of "bad" quality such as a Lot Tolerance Percent Defective (LTPD). In quality assurance procedures, when checking and selecting the acceptable samples out of a lot, a user's risk of 10 % is common and LTPD is the lot quality (i.e. value of "p") for which there is a 10 % probability of acceptance, i.e. 10 % of such lots will be accepted.

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The α and β risks for the operating characteristic curves of Figure 4 are shown in Figure 5 and Figure 6 and summarized in 4.4.6.

Another measure for comparison of sampling plans is to consider how well the plans discriminate between "good" and "bad" lots. An ideal plan would discriminate absolutely between the "good" and "bad" lots as is shown in Figure 7 for an AQL of 10 %; all lots to the left of the vertical acceptance line will be accepted and those to the right will be rejected. The closer the actual sampling plan comes to the ideal plan, the better its discrimination.

Readers interested in a more detailed description of statistical sampling are referred to the referenced textbooks on quality control [3, 4, 5].

4.4.6 Summary of 15/2 and 3/9 test methods

The theoretical analysis is summarized in Table 3 and in Figure 5, Figure 6 and Figure 7.

Table 3 – Summary of theoretical analysis

Method	Description	Number of acceptable outcomes	AQL (%)	LTPD (%)	Comments
15/2	As for 15/2M except that one (1) disruptive discharge permissible in the verification impulses if only one such discharge occurred in the basic 15 impulses	38	5	29,2	Addresses the disadvantages of the 15/2 and 15/2M while retaining the principle of maximum two (2) disruptive discharges permissible
3/9	Basic 3 impulses, one (1) disruptive discharge permissible in which event nine (9) further impulses applied with no disruptive discharges permissible	3	4,6	53,5	Used only in the United States

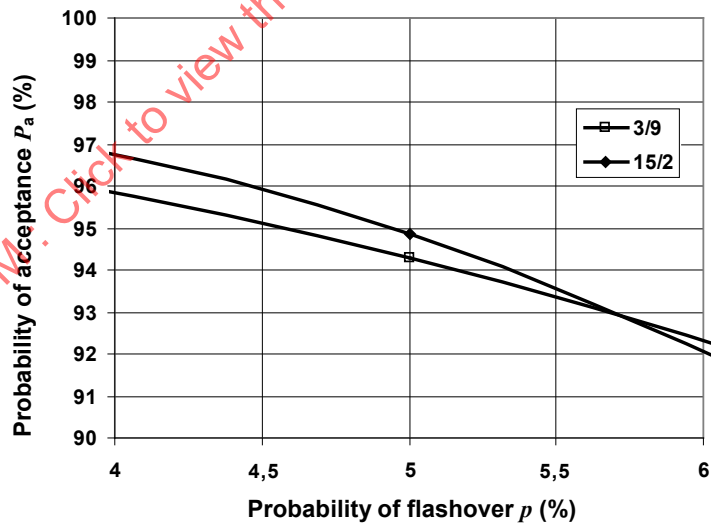

Figure 5 – α risks for 15/2 and 3/9 test methods

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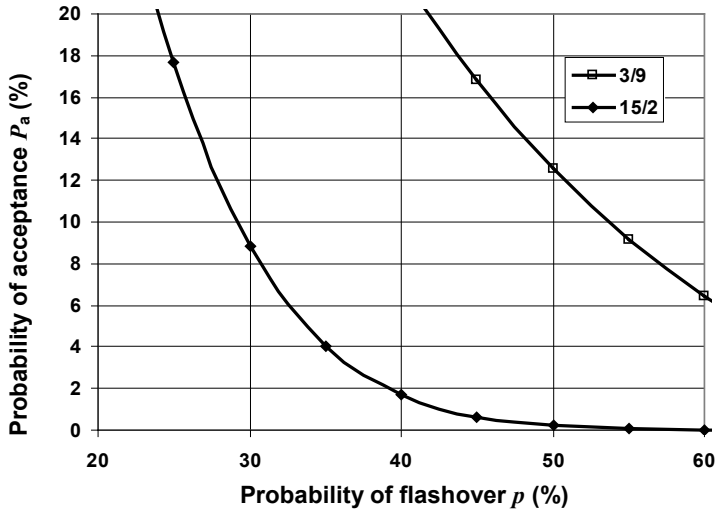

Figure 6 – β risks for 15/2 and 3/9 test methods

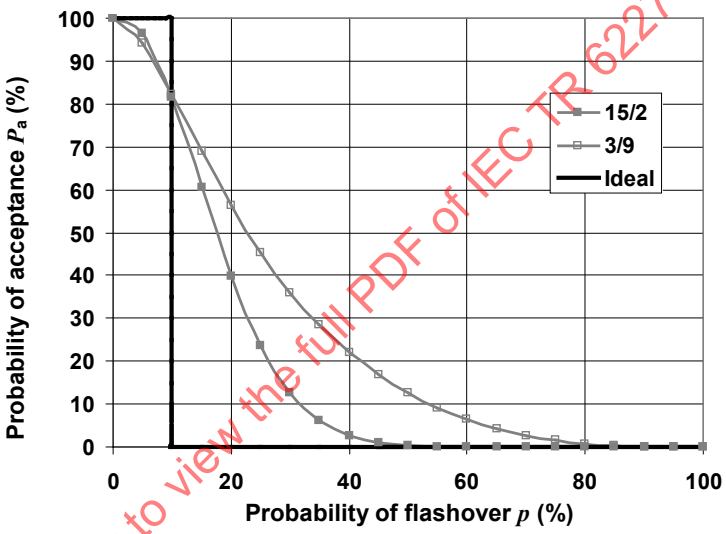

Figure 7 – Ideal sampling plan for AQL of 10 %

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4.4.7 Routine tests

It should be noted that routine tests are detailed in the relevant standards. The power frequency test is used because it is most suitable for factory conditions.

4.5 Correction factors

4.5.1 Altitude correction factor

4.5.1.1 General

In the determination of the required withstand voltages, a number of factors have to be taken into account: the atmospheric correction factor k_{at} and a safety factor k_s. These factors are multipliers to be applied to the insulation level (see 4.5.1.2).

An effect of altitude is the reduction of the atmospheric pressure. A reduced atmospheric pressure reduces the disruptive voltage of a given gap in air. Subclause 4.2.2 of IEC 60071-2:1996 provides equations for derating insulation levels according to the voltage

shape and to the electrode configurations based on measurements made in HV laboratories. The difficulty occurs when it comes to switching surges. So, in IEC 62271-1, it was proposed and accepted to simplify the altitude correction factor as shown in Figure 1 of this standard. In addition, these equations are general for any altitude above sea level. But in the process of assessing insulation level in IEC 60071-1, a correction is already included to cover use up to 1 000 m. As a consequence, the insulation levels stated in IEC 62271-1 are valid up to 1 000 m and, for higher altitudes, the equation for the correction factor is modified accordingly.

The altitude correction is applicable to external insulation only and is incorporated into the atmospheric correction factor, since the air density is a function of the altitude. The dielectric strength is dependent on the air density. The altitude dependence on the atmospheric pressure is given in IEC 60721-2-3 in tabular form. IEC TC 28 (Insulation coordination) has transferred the information given in IEC 60721-2-3 into Equation (1) that deviates by no more than 1 % from the information given in IEC 60721-2-3:

$$\frac{b_0}{b} = e^{H/8150} \tag{1}$$

where

b_0 is the standard barometric pressure, 101,3 kPa (or 1 013 mbar);

b is the pressure at altitude H above sea level (Pa);

H is the altitude above sea level (m).

The air density correction factor is given as (IEC 60060-1):

$$k_d = \delta^m \tag{2}$$

with $\delta = \frac{b}{b_0} \times \frac{273 + t_0}{273 + t}$

where,

k_d is the air density correction factor;

δ is the air density;

t_0 is the standard reference temperature, 20 °C;

t is the actual ambient temperature;

m is an exponent dependent on the minimum discharge path and other attributes. Values of m can be derived from Figure 4 of IEC 60060-1:2010. These values are based on measurements performed at altitudes up to 2 000 m.

The fixed (and conservative) values for m are given for convenience, more detailed values are given in IEC 60071-2. The values are reproduced here from IEC 62271-1 (see Table 4):

Table 4 – Values for *m* for the different voltage waveshapes

m	Power frequency	Switching impulse	Lightning impulse
Phase-to-earth	1	0,75	1
Phase-to-phase	1	1	1
Longitudinal	1	0,9	1

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Combining Equations (1) and (2) and assuming standard reference temperature applies, the following equation is obtained for the altitude correction factor:

$$k_{alt} = e^{m\left(\frac{H}{8\,150}\right)} \quad (3)$$

Subclause 2.2.1 of IEC 62271-1:2007 specifies the following altitude correction factor:

a) altitudes up to and including 1 000 m: $k_{alt} = 1$

b) altitudes higher than 1 000 m: $k_{alt} = e^{m\left(\frac{H-1\,000}{8\,150}\right)}$ (4)

where

k_{alt} is the altitude correction factor;

H is the altitude in m above sea level;

m is an exponent.

The specification of the altitude correction factor as given in IEC 62271-1 has been based on the following considerations.

The safety factors used are k_s = 1,05 for external insulation and k_s = 1,15 for internal insulation.

Considering the overall correction k_{total} = ($k_{alt} \times k_s$) as a function of the altitude at constant humidity and temperature, assuming m = 1, the following can be determined:

External insulation: at 0 m k_{total} = 1,05 and at 1 000 m k_{total} = 1,19

Internal insulation: k_{total} = 1,15 (independent of altitude)

For a circuit-breaker having internal and external insulation in parallel (which is frequently the case), the overall correction factors are nearly equal at 1 000 m. This means that the safety factor of 1,15 covers the requirements for both internal and external insulation up to an altitude of 1 000 m.

As the safety factor is included in the required withstand voltages, these voltages are valid up to and including 1 000 m.

4.5.1.2 Examples of application of the altitude correction factor

Example 1: A 245 kV circuit-breaker is going to be installed in a substation at an altitude of 1 800 m above sea level. The user specification for the insulation level is 1 050 kV at site level. Which circuit-breaker will fulfil these requirements?

The required insulation level at standard atmospheric conditions (sea level) will be obtained applying the altitude correction factor (Equation (4)) and the following considerations:

– For lightning impulse and power frequency m = 1, hence k_{alt} = 1,103. This means that the circuit-breaker needs to be tested at sea level with a voltage of 1 050 × k_{alt} = 1 158 kV.

– The nearest standardized impulse voltage is 1 175 kV, which belongs to a system voltage of 362 kV.

– The requirement for the power frequency withstand at sea level is 507 kV (dry and wet). Regarding the test to earth this is not fully covered by the requirements for a 362 kV circuit-breaker. However, a 362 kV circuit-breaker has been tested with switching impulse (dry and wet), which gives higher stresses on the external insulation compared to the

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power frequency test, hence one can safely assume that a 362 kV circuit-breaker fulfils the requirements of a 245 kV circuit-breaker used at 1 800 m above sea level.

Conclusion: The 245 kV circuit-breaker fulfilling the requirements for an altitude of 1 800 m will be a circuit-breaker having an insulation level belonging to a system voltage of 362 kV. Application of surge arresters with the intent to lower the insulation level of the substation may result in a more advantageous choice of equipment.

Example 2: A 245 kV circuit-breaker is tested in a testing station that is located at an altitude of 800 m above sea level. What are the correct test values?

Test values and conditions for testing of switchgear and controlgear is referring to standard atmospheric conditions. As the testing station is located at 800 m above sea level, the test values for external insulation need to be corrected to the standard atmospheric conditions. Applying Equation (3) using H = 800 and m = 1 gives k_{alt} = 1,103.

The test values for external insulation in the testing station may be reduced to 1 050/k_{alt} = 952 kV_{peak} for the lightning impulse withstand test and 417 kV r.m.s. for the power frequency test, providing the circuit-breaker has external insulation only. When the circuit-breaker has both internal and external insulation, k_{alt} = 1.

Example 3: The circuit-breaker of Example 2 is tested in the same testing station at an altitude of 800 m for application at an altitude of 1 800 m. What is the correct test voltage?

The testing values at sea level have been derived in Example 1 and are 1 158 kV for the lightning impulse withstand test and 507 kV r.m.s. for the power frequency withstand test.

Application of Equation (3) (calculated in Example 2) to these values give the following result:

– lightning impulse withstand test: 1 050 kV_{peak};
– power frequency withstand test: 460 kV.

Again, this is only valid for the external insulation of the circuit-breaker.

4.5.2 Humidity correction factor

IEC 62271-1 deviates from IEC 60060-1 with respect to the humidity correction factor h to be applied during dry tests of switchgear and controlgear having a rated voltage above 1 kV and up to and including 52 kV.

In fact, the correction factors as defined in IEC 60060-1 do not fully apply to switchgear and controlgear having a rated voltage above 1 kV and up to and including 52 kV in which dielectric stress implies short distances and highly stressed insulating surfaces, and where the location and length of the disruptive discharge are practically impossible to define. The disruptive discharge depends on temperature and humidity as shown in Figure 8:

- in area 3 and 4, the external insulation behaves as an air gap;
- in area 2, due to high absolute moisture content, it is observed that disruptive discharges generally occur along the insulating surface and cannot be considered as if in air. In case of high moisture content with condensation, the weakest point may become the surface instead of the air gap;
- the cases corresponding to area 1 practically do not exist except for the zone near the standard conditions.

In order to avoid varying interpretations and have a practical approach for laboratories, a simplified method to determine w values is preferred to the calculation as given in IEC 60060-1. It was based on the experience of IEC 60694:1981 in which the factor w value equal to 1 had been used for long time by laboratories with satisfactory results especially in

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area 3 of Figure 8 ($h \leq 11$ g/m^3), and on recent results in area 2 ($h > 11$ g/m^3) showing that taking $w = 0$ gives good correlation with experimental data.

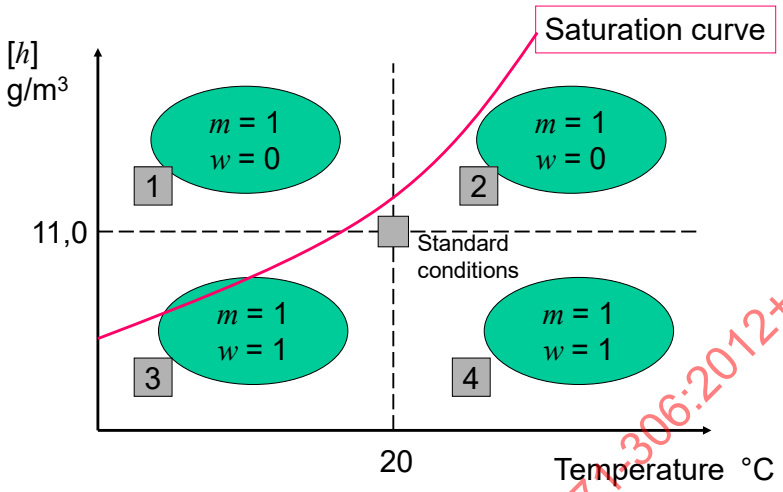

Figure 8 – Disruptive discharge mode of external insulation of switchgear and controlgear having a rated voltage above 1 kV up to and including 52 kV

4.6 Background information about insulation levels and tests

4.6.1 Specification

4.6.1.1 General

The rated insulation levels are mainly based on the requirements of IEC 60071-1. The application guide IEC 60071-2 explains the relationship between the nominal system voltage and the standardized insulation levels. However, these standards are intended to be applied to all types of equipment: insulators, cables, power transformers, etc. Therefore, some related considerations need to be addressed in applying them to high-voltage switchgear and controlgear.

4.6.1.2 Phase-to-earth

The insulation levels have been selected taking into account the values most commonly used for switchgear and controlgear.

In addition to IEC 60071-1, a rated short-duration power-frequency withstand voltage is required for rated voltages higher than 245 kV, in order to verify internal insulation voltage withstand capability with respect to temporary overvoltages.

4.6.1.3 Phase-to-phase

No changes are made to the specifications of IEC 60071-1 for the insulation between poles.

4.6.1.4 Longitudinal insulation

Since no other IEC product standards specify requirements for longitudinal insulation, SC 17A has developed its own set of rated withstand values.

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4.6.1.5 Isolating distance

In addition to the requirements of insulation coordination, the standard specifies insulation of the “isolating distance”. This is to cover special conditions which are to be met by disconnectors to provide an additional safety factor (1,15) (see 5.102 of IEC 62271-102:2001).

The intent of the isolating distance is not to provide fundamental-coordination but to require that any disruptive discharge occurs phase-to-earth on the switching device rather than between its open contacts. Exceptions may occur, for example when high creepage distances to earth are required. However, it is generally recognized that when work has to be carried out on a high-voltage conductor, safety is assured only when the conductor is directly connected to earth. Local safety rules should apply.

4.6.1.6 Combined voltage tests

A combined voltage test is one in which two separate sources, generating voltages against earth, are connected to two terminals of the test object (see Clause 9 of IEC 60060-1:2010 and Tables 2a and 2b of IEC 62271-1:2007).

Such tests are required for switchgear and controlgear of 300 kV and above to demonstrate longitudinal voltage withstand capability. They may also be useful for testing where the test voltage between two live parts is specified to be higher than the phase-to-earth value.

The components of the combined voltage tests have been specified based on the following considerations:

a) Short-duration power-frequency withstand voltage

The specified power-frequency withstand voltage values correspond to the most severe situation of full load rejection after disconnection of a generator at full load. The overvoltage on the generator side of the switching device may reach up to 1,5 times the system voltage and may last up to 3 s with a possible phase shift. At the same time, the network side of the switching device is energized at the normal operating voltage. The sum of the two voltages in out-of-phase condition is 2,5 times the system voltage, extended here to 2,5 the rated voltage.

b) Switching impulse withstand voltage

The switching impulse voltage value specified phase to earth in Column 4 of Table 2 of IEC 62271-1:2007 is designed to cover the highest slow-front overvoltage likely to occur at the switching device terminal. This occurs at the remote end of a line after fast reclosing from the other end on a trapped charge. This highest overvoltage is of the same polarity as the power-frequency voltage of the network at this instant and therefore is not to be used when the maximum stress across a switching device is the consideration. The maximum longitudinal stress takes place when an overvoltage occurs on the polarity opposite to the power-frequency voltage of the system. The maximum value for this case occurs on closing from the remote end and is lower than the value occurring on reclosing. Therefore, the values of switching impulse specified in Column 6 of Table 2 of IEC 62271-1:2007 are lower than those of Column 4 of Table 2 of IEC 62271-1:2007.

c) Lightning impulse

In the process of designing insulation coordination, IEC 60071-1 takes into account the probability of occurrence of a particular event in order to determine the performance criteria. The likelihood that the maximum fast-front overvoltage occurs on the terminal of a switching device at the instant when its opposite terminal is energized with the maximum system voltage at opposite polarity is small. Therefore, the specified lightning impulse to be considered in this particular case need not be as high as for the general case. The reduction of about 5 % of the power frequency voltage that appear in IEC 60694 has been changed in IEC 62271-1 to a tolerance on the total test voltage of $^{+3}_{-0}$ %.

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4.6.2 Testing

4.6.2.1 Test of the longitudinal insulation with the alternative method

To be strictly in compliance with the preferred method, the voltage between the energized terminal and the base frame U_f should be equal to the rated withstand voltage phase to earth. But it is difficult to control this voltage during the test of the longitudinal insulation. The value of U_f has been fixed considering the following facts:

– the test voltage between any terminal and the base frame cannot exceed the rated phase to earth withstand voltage without risk;

– the electric field stress across open contacts is mainly dependent on the voltage across them, and to a lesser extent on the voltage to earth;

– the determination of the rated withstand voltage of the isolating distance is not that accurate;

– a safety factor is included in the process of insulation coordination (see IEC 60071-1) to account for such testing difficulties.

4.6.2.2 Test between phases for rated voltages above 245 kV

4.6.2.2.1 Voltage sharing between the two switching impulse components of the phase-to-phase test

The actual ratio of the two components may have any value in the network. In order to simplify the tests, IEC 60071-1 decided to specify balanced components (same amplitude with opposite polarities). Since this leads to a less severe condition, the total test voltage was increased to cover any realistic case (see Annex A of IEC 60071-2:1996). Therefore, if the same total test voltage is applied by an unbalanced sharing of the components, the test is more difficult than required.

In reality few laboratories have two impulse generators and the peak of a power-frequency voltage may replace one component. However, this leads to power-frequency voltages higher than specified phase-to-earth and for a rather long duration. Therefore, some compromise is necessary depending on the actual phase-to-earth withstand voltage of the switching device and on the facilities of the laboratory.

4.6.2.2.2 Wet tests

No wet switching impulse tests are normally necessary between phases for the following reasons:

– enclosed insulation does not need wet tests;

– insulation between phases exposed to precipitation is atmospheric air only and is not sensitive to this influence for switchgear and controlgear of rated voltage above 245 kV.

4.6.3 Combined voltage tests of longitudinal insulation

4.6.3.1 Tolerance on the power-frequency voltage component

According to IEC 60060-1, the tolerance of the power-frequency component voltage for a test with a duration longer than 1 min should be maintained within ±3 % of the specified level. This allows for some variations from the main voltage without permanent adjustment. During a combined voltage test, however, the laboratory has also to monitor many other parameters from the impulse voltage source. Therefore a higher tolerance is acceptable for the power frequency component with the understanding that the test voltage to be considered is the actual total voltage across the open contacts or the isolating distance. The tolerance on the total voltage is $^{+3}_{-0}$ %.

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4.6.3.2 Atmospheric correction factor

For atmospheric corrections the parameter g (4.3.4.3 of IEC 60060-1:2010) shall be calculated considering combined or composite test voltage value. The parameter $k1$ and k_2 (4.3.4.1 and 4.3.4.2 of IEC 60060-1:2010) shall be calculated for the higher of the two test voltages and be applied to both.

4.7 Lightning impulse withstand considerations of vacuum interrupters

4.7.1 General

The lightning impulse withstand voltage performance of vacuum interrupters has some characteristics that must be considered when testing. The breakdown voltage between the open contacts of a switching device in general depends on two things.

– the gaseous material between the contacts, and

– the contact surfaces.

In cases with high pressure gases at or above the normal atmospheric pressure, the gas exerts a major influence on breakdown in comparison to the contacts. In cases with vacuum gaps the contact surfaces exert the major influence.

Electrical breakdown between the contacts in a gas gap is called avalanche breakdown. The electrons that are accelerated by the electric field between the contacts collide with neutral atoms or molecules and knock off an increasing number of new electrons until a complete breakdown of the gap occurs. A *key* parameter influencing these collisions is the mean free path. The mean free path is the distance between collisions of electrons with neutral atoms or molecules as the electrons are accelerated by the electric field between the contacts. In a gas gap, the mean free path is a very small fraction of a millimetre and hence an even smaller fraction of the contact gap. Hence breakdown between the open contacts of a gas interrupter depends largely on the type of gas and the gas pressure.

In a vacuum gap, the gas pressure is 8 to 10 orders of magnitude less than the normal atmospheric pressure. In contrast, the mean free path in a vacuum gap is 10 or more times greater than the distance between the contacts. Hence breakdown between the open contacts of a vacuum interrupter is determined largely by the condition of the contact surfaces.

4.7.2 Conditioning during vacuum interrupter manufacturing

The procedure used to increase the breakdown voltage of a vacuum gap is called "*conditioning*" or "*seasoning*". Conditioning is of great practical importance to improve the withstand voltage capability and achieve the required lightning impulse withstand voltage performance of vacuum interrupters. At the end of the manufacturing process all vacuum interrupter will go through a conditioning process. The common procedure used by all leading vacuum interrupter manufacturers to condition vacuum interrupters is voltage conditioning where the contacts are blocked in the open position and an a.c.-voltage is applied across the open contact gap. The conditioning voltage level is chosen such that the vacuum interrupter can subsequently be able to pass its rated lightning impulse withstand voltage and can therefore be safely applied at the required voltage rating in circuit-breakers that comply with standards like, e.g., IEC, IEEE.

If the lightning impulse withstand voltage test is done immediately after the seasoning operation when the contacts are still in the blocked open position, the impulse voltage withstand performance is at its best. However, after the contacts are allowed to touch, some microscopic roughness occurs that reduces to a small degree the lightning impulse withstand voltage performance of the interrupter. In addition, mechanical cycling of a switching device once the interrupter is installed can also result in some small reduction of the lightning impulse withstand voltage performance of the interrupter.

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4.7.3 De-conditioning in service

Most common causes for de-conditioning in service are:

- high inrush currents during contact closure, for example during the making of an capacitive current with a high peak inrush current;
- interruption of high short-circuit currents (≥ 10 kA);
- passage of high currents (≥ 10 kA) through closed contacts.

The interruption of many high short-circuit currents often reduces the lightning impulse withstand voltage capability. So over time, the impulse withstand voltage capability of the vacuum interrupter may be reduced below the rated value.

4.7.4 Re-conditioning in service

In contrast, various phenomena can improve the lightning impulse voltage withstand performance, such as one or more breakdowns during impulse voltage testing or arcing between the contacts when breaking current. The interruption of load currents or lower fault currents (< 5 kA) can often re-condition the contacts from the effects of inrush currents or high currents passed through the vacuum interrupter contacts.

4.7.5 Performing lightning impulse withstand voltage tests

NOTE 3 of 6.2.4 of IEC 62271-1:2007 may be applied for the preliminary impulse voltage tests. This note does not specify how many preliminary tests nor how many breakdowns are acceptable.

After the completion of the preliminary impulse voltage tests, the official certification tests at the rated withstand voltage are performed in accordance with 6.2.4 of IEC 62271-100:2008.

5 Rated normal current and temperature rise

5.1 General

This section of the guide also applies to other switchgear and controlgear components of similar basic construction to circuit-breakers and hence it is written making reference to switchgear and controlgear rather than circuit-breakers alone.

5.2 Load current carrying requirements

5.2.1 Rated normal current

The switchgear and controlgear is designed for applications where the load current does not exceed the rated normal current under specific conditions. These conditions are:

– the altitude above sea level for the application is 1 000 m or less;
– the ambient temperature does not exceed 40 °C and the average value, measured over a period of 24 h, does not exceed 35 °C.

NOTE 1 No correction factor is applied for altitudes up to 2 000 m. For altitudes higher than 2 000 m refer to 5.2.2.4.

When choosing the switchgear and controlgear for an application the following parameters should be taken into account:

– the expected maximum load current. The rated normal current of the switchgear should be selected from the R10 series, specified in IEC 60059.

NOTE 2 The R10 series is based on the work of a French army engineer (Col. Charles Renard), who proposed in the 1870s a set of preferred numbers for use with the metric system. His system was adopted in 1952 as

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international standard ISO 3. Renard's system of preferred numbers divides the interval from 1 to 10 into 5, 10, 20, or 40 steps. The factor between two consecutive numbers in a Renard series is constant (before rounding), namely the 5th, 10th, 20th, or 40th root of 10 (1,58; 1,26; 1,12 and 1,06, respectively), which leads to a geometric sequence. This way, the maximum relative error is minimized if an arbitrary number is replaced by the nearest Renard number multiplied by the appropriate power of 10.

The R10 series is based on the following equation: $R(i) = 10^{\frac{i}{10}}$, where i is the i^{th} element of the series.

– the expected maximum ambient temperature around the switchgear. For ambient temperatures up to 40 °C no special requirements are given.

5.2.2 Load current carrying capability under various conditions of ambient temperature and load

5.2.2.1 General

The rated normal current is based on the maximum permissible total temperature limitations of various parts of the switchgear and controlgear when it is carrying its rated normal current at an ambient temperature of 40 °C. The total temperature of these parts under service conditions depends both on the actual load current and the actual ambient temperature. It is therefore possible to operate at a current higher than the rated normal current when the ambient temperature is less than 40 °C, provided that the allowable temperature limit is not exceeded. Similarly, when the ambient temperature is higher than 40 °C, the current must be reduced to less than the rated normal current to keep the total temperature within the allowable limits.

The methods of calculating the allowable current under various conditions of ambient temperature and load are given in 5.2.2.2 through 5.2.2.4. For some high ambient temperature conditions, it may not be practical to reduce the current sufficiently to keep the total temperatures within their allowable limits. Forced air cooling will help in many cases. Temperature limits of associated equipment such as cables and current transformers must be considered as this heat transfer is not taken into account during type testing. However no advice can be given for these cases or the similar effects of solar radiation which also must be considered.

5.2.2.2 Continuous load current capability based on actual ambient temperature

If the ambient temperature is above 40 °C, parts of the switchgear and controlgear may exceed the specific limits given in Table 3 of IEC 62271-1:2007, when carrying its rated normal current. In this case a higher rated normal current range for the switchgear and controlgear has to be selected. For load currents which are lower than the rated normal current of the circuit-breaker, a permissible maximum ambient temperature for that load current can be calculated with the help of Equation (5):

$$\theta_a = \theta_{max} - \left(\frac{I_a}{I_r}\right)^{1,8} \times (\theta_r) \quad (5)$$

where

I_a is the allowable continuous load current, in A, at actual ambient temperature θ_a (I_a is not to exceed two times I_r);

I_r is the rated normal current, in A;

θ_{max} is the allowable hottest spot total temperature (θ_{max} = θ_r + 40), in °C;

θ_r is the allowable hottest spot temperature rise at rated normal current, in K;

θ_a is the allowable or actual ambient temperature, in °C.

NOTE The exponent would normally be 2, since the heat development in the switchgear and controlgear is proportional to the square of the current. Due to radiation and convection, the exponent may vary. Experience has

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shown that the exponent, depending on switchgear and controlgear design and components within the switchgear and controlgear, generally is in the range of 1,6 to 2,0. A value of 1,8 represents a compromise that covers most cases and is used in this application guide.

If Equation (5) is solved for the current I_a the allowable continuous load current at an actual ambient temperature θ_a can be calculated as given in Equation (6).

$$I_a = I_r \left(\frac{\theta_{max} - \theta_a}{\theta_r} \right)^{1/1,8} \quad (6)$$

The design features of switchgear and controlgear dictate the appropriate values of θ_{max} and θ_r to be used in the calculation. The major components of a circuit-breaker have several different temperature limitations which are specified in Table 3 of IEC 62271-1:2007. The values for θ_{max} and θ_r should be determined as follows:

a) if the actual ambient temperature is less than 40 °C, the component with the highest specified values of allowable temperature limitations should be used for θ_{max} and θ_r;

b) if the actual ambient temperature is greater than 40 °C, the component with the lowest specified values of allowable temperature limitations should be used for θ_{max} and θ_r.

The use of these values in the calculation will result in an allowable continuous current which will not cause the temperature of any part of the switchgear to exceed the permissible limits.

Example: A circuit-breaker that has been tested for 3 150 A rated normal current at an ambient temperature of 40 °C will carry a maximum load current of 2 500 A. What is the highest permissible ambient temperature?

As the estimated load current is less than rated current a higher ambient temperature is permissible. For the calculation θ_{max} and θ_r should be chosen as described under b).

In this case the lowest specified value in Table 3 of IEC 62271-1:2007 is θ_{max} = 90 °C and θ_r = 50 K for the bare bolted connection in air. With Equation (5) the maximum permissible ambient temperature in this example is

$$\theta_a = \theta_{max} - \left(\frac{I_a}{I_r} \right)^{1,8} \times (\theta_{max} - 40) = 57\ °C$$

5.2.2.3 Short-time load current capability

When switchgear and controlgear has been operating at a current level below its allowable continuous load current I_a, it is possible to increase the load current for a short time to a value greater than the allowable current without exceeding the permissible temperature limitations. There are different factors which influence the length of time period t_s of the overcurrent I_s. These are:

– the magnitude of the current I_s itself;
– the magnitude of the initial current I_i carried prior to the application of I_s;
– the thermal time characteristic (thermal time constant) of the switchgear and controlgear;
– the ambient temperature prior to and during application of overcurrent I_s.

The allowable duration of current I_s can be calculated directly by use of the Equation (7) and Equation (8):

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$$t_s = \tau \left[-\ln \left\{ 1 - \frac{\theta_{max} - Y - \theta_a}{Y \left\langle (I_s / I_i)^{1,8} - 1 \right\rangle} \right\} \right] \quad (7)$$

$$Y = (\theta_{max} - 40) \times \left(\frac{I_i}{I_r} \right)^{1,8} \quad (8)$$

where

θ_{max} is the allowable hottest spot total temperature (see Table 3, IEC 62271-1:2007), in °C;

θ_a is the actual ambient temperature in °C;

I_i is the initial current carried prior to application of I_s, in A (maximum current carried by the circuit-breaker during the 4 hour period immediately preceding the application of current I_s);

I_s is the short-time load current, in A;

I_r is the rated normal current, in A;

τ is the thermal time constant of circuit-breaker, derived from temperature rise test in h;

t_s is the permissible time for carrying current I_s at ambient θ_a after initial current I_i, time is given in the same unit as τ, h;

Y is the a coefficient used for convenience, in K.

The time duration of the current I_s determined in this way will not cause the total temperature limits of the switchgear and controlgear to be exceeded, provided that the following requirements are fulfilled:

a) the switchgear, and in particular the main contacts, shall have been well maintained and in essentially new condition;

b) the value used for current I_i is the maximum current carried by the switchgear during the 4 hour period immediately preceding the application of current I_s. To achieve the current value it is necessary to have a record of the current flow over the last 4 hours;

c) at the end of the period, the current I_s is reduced to a value which is not greater than the current I_a;

d) the value of current I_s is limited to a maximum value of two times rated normal current I_r. Otherwise actual overheating may occur as the heat from hot spots cannot be distributed fast enough to colder regions.

NOTE If the temperature rise due to the short-time load current I_s does not exceed θ_{max}, I_s is in an acceptable steady state. Thus the allowable time t_s is indefinite. Use of Equation (5) gives the information regarding the need, or otherwise, to apply Equation (7) and Equation (8).

Example: An SF_6 gas-insulated metal-enclosed switchgear with rated normal current carrying capability of I_r = 3 150 A (having a temperature rise of 65 K at 3 150 A) will carry a short-time load current I_s of 3 600 A. Before application of the short-time load current the initial current I_i was 2 500 A, the ambient temperature θ_a is 30 °C.

The highest total temperature θ_{max} = 115 °C is taken for bolted silver-coated connections in SF_6.The thermal time constant, derived from the type test, is 1,5 h. Generally, the time constant can be considered independent of the load and the temperature of the equipment.

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With Equation (7) and Equation (8) the allowable time t_s is calculated to

$$t_s = 1{,}5\left[-\ln\left\{1-\frac{115-Y-30}{Y\left\langle\left(\frac{3600}{2500}\right)^{1{,}8}-1\right\rangle}\right\}\right] = 2{,}22\,\text{h}$$

from Equation (8):

$$Y = (115-40)(2500/3150)^{1{,}8} = 49{,}5\,\text{K}$$

After 2 h and 13 min the current has to be reduced to the maximum allowable current I_a which can be calculated with the help of Equation (6).

5.2.2.4 Influence of the altitude of switchgear and controlgear location

If the switchgear and controlgear relies on natural circulation of the ambient air and is located at an altitude between 2 000 m and 4 000 m, correction is unnecessary. The reason for this is that the increase of temperature rise at higher altitude due to the reduced cooling effect of the air is compensated for by the reduced maximum ambient temperature at that altitude (see Table 5). Consequently the final temperature is relatively unchanged at a given current.

Table 5 – Maximum ambient temperature versus altitude (IEC 60943)

Altitude m	Maximum ambient air temperature °C
0 – 2 000	40
2 000 – 3 000	30
3 000 – 4 000	25

5.3 Temperature rise testing

5.3.1 Influence of power frequency on temperature rise and temperature rise tests

A test performed at a specific frequency is considered to be valid for the same current rating at a lower rated frequency.

In the case of open type switchgear and controlgear without ferrous parts adjacent to the current path a test performed at 50 Hz is also valid for 60 Hz provided that the temperature rise values recorded during the 50 Hz test do not exceed 95 % of maximum permissible values.

Caution is needed when tests performed at 50 Hz on switchgear and controlgear with ferrous parts are to be used to prove the performance of the switchgear and controlgear when rated for 60 Hz. The reason is that the ferrous parts adjacent to the current-carrying parts will have a frequency dependant heating effect due to the magnetic and eddy current losses. This will influence the temperature rise of the switchgear and controlgear.

5.3.2 Test procedure

The test procedure, the test arrangement and the tolerances for current, frequency and ambient temperature are given and described in 6.5 of IEC 62271-1:2007. The temperature

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rise is defined as the difference between the temperature of the part under consideration and the ambient temperature.

The duration of the test is determined by the time constant of the test object and the requirement to reach a stable value for the temperature rise. This condition is assumed to be satisfied when the increase of temperature rise does not exceed 1 K/h. This case will normally be met after a test duration of five times the thermal time constant of the test object. Care should be taken that this requirement is checked at the temperature rise values for each measurement point in relation to the ambient temperature (see Table 6). The change of the ambient temperature during the last quarter of the test period shall not exceed 1 K/h.

Table 6 – Some examples of the application of acceptance criteria for steady state conditions

Value	Example 1	Example 2	Example 3	Example 4
Change of absolute temperature during the last 1 h on the measurement point in K	1,8	0,5	1,1	0,8
Change of ambient temperature during the last 1 h in K	0,1	1,2	0,1	-0,6
Change of temperature rise of the measurement point during last 1 h in K	1,7	-0,7	1,0	1,4
Result	Steady state not reached. Change of temperature rise exceeds 1 K/h.	Steady state not reached Change of ambient temperature exceeds 1 K/h.	Steady state reached. All criteria fulfilled.	Steady state not reached. Change of temperature rise exceeds 1 K/h.

In Figure 9 the values are shown which have to be taken into account to check the steady state condition. At steady state the following conditions need to be fulfilled

– the increase of temperature rise ($\Delta\theta_c$) does not exceed 1 K in 1 h;

– the change in ambient temperature ($\Delta\theta_a$) during the last quarter of the test duration does not exceed 1 K in 1 h.

The values $\Delta\theta_c$ and $\Delta\theta_a$ are shown in Figure 10 which is an expansion of the relevant section of Figure 9. As mentioned above this condition will normally be reached after a test time of five times the time constant of the test object (see Figure 9).

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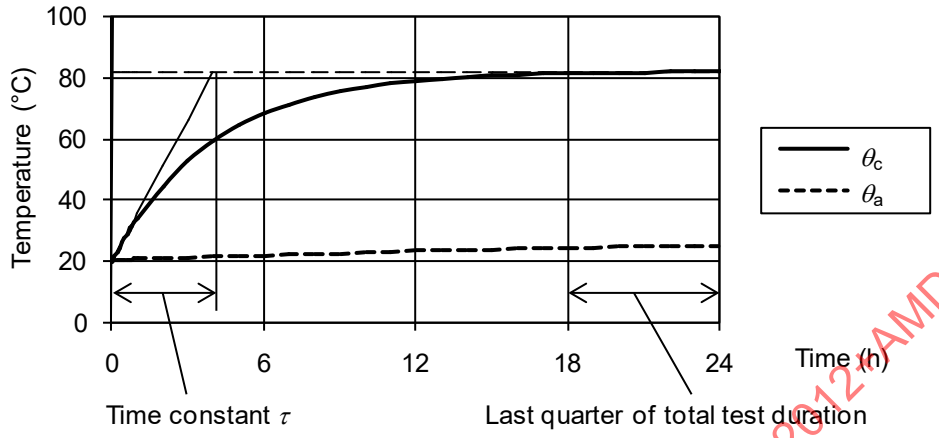

Figure 9 – Temperature curve and definitions

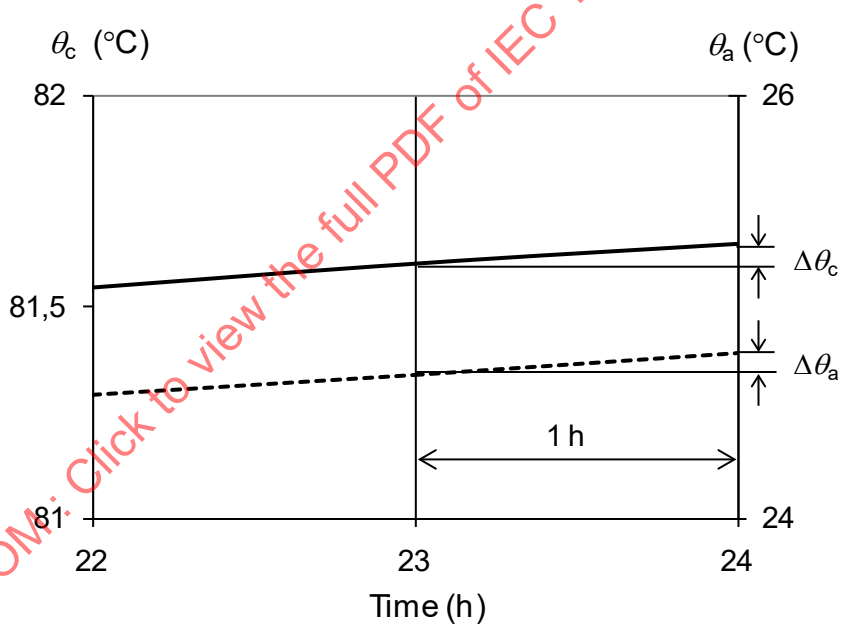

Figure 10 – Evaluation of the steady state condition for the last quarter of the test duration shown in Figure 9

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5.3.3 Temperature rise test on vacuum circuit-breakers

The temperature rise tests on vacuum circuit-breakers are performed in the same manner as for other types of circuit-breakers and switchgear and controlgear. However, it is not possible to connect a thermometer or thermocouple to the main contacts of the interrupter unit. As stated in IEC 62271-1 the temperature at the terminals or connection parts of the vacuum bottle is taken as the qualifying measurement. The temperature rise of these parts shall not exceed the limits given in Table 3 of IEC 62271-1:2007.

5.3.4 Resistance measurement

The procedure for measurement of the resistance of circuits is described in 6.4 of IEC 62271-1:2007.

The recommended minimum value of the injected current is 50 A d.c. to ensure that any surface contamination (sulfides or oxides) is broken down and that there is a sufficient voltage drop such that it can be measured accurately.

5.4 Additional information

5.4.1 Table with ratios I_a/I_r

In Table 7 the following variables are used:

– I_a is the allowable continuous load current, in A, at actual ambient temperature θ_a;
– I_r is the rated normal current, in A;
– θ_{max} is the allowable hottest spot total temperature ($\theta_{max} = \theta_r + 40$), in °C;
– θ_r is the allowable hottest spot temperature rise at rated normal current, in K.

Table 7 – Ratios of I_a/I_r for various ambient temperatures based on Table 3 of IEC 62271-1:2007

Maximum ambient temperature °C	Limiting temperature of different switchgear components °C									
	θ_{max}	70	80	90	100	105	115	120	130	155
	θ_r	30	40	50	60	65	75	80	90	115
		Ratios of I_a/I_r								
60	a	0,54	0,68	0,75	0,79	0,81	0,84	0,85	0,86	0,89
50	a	0,79	0,85	0,88	0,90	0,91	0,92	0,92	0,93	0,95
40		1,00	1,00	1,00	1,00	1,00	1,00	1,00	1,00	1,00
30	b	1,17	1,13	1,10	1,08	1,08	1,07	1,06	1,06	1,04
20	b	1,32	1,25	1,20	1,17	1,16	1,14	1,13	1,11	1,09
10	b	1,47	1,36	1,29	1,25	1,23	1,20	1,19	1,17	1,13
0	b	1,60	1,46	1,38	1,32	1,30	1,26	1,25	1,22	1,18
-10	b	1,72	1,56	1,46	1,40	1,37	1,32	1,30	1,27	1,22
-20	b	1,84	1,66	1,54	1,46	1,43	1,38	1,36	1,32	1,26
-30	b	1,95	1,75	1,62	1,53	1,50	1,44	1,41	1,37	1,30

a for limiting current at this ambient temperatures, use lowest θ_{max} and θ_r.

b for limiting current at this ambient temperatures, use highest θ_{max} and θ_r.

5.4.2 Derivation of temperature rise equations

The temperature rise equations used for calculation of allowable time of a overload current are derived in the following manner:

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Let

θ_s is the total temperature, in °C, that would be reached if the overload current I_s were applied continuously at ambient θ_a;

θ_i is the total temperature, in °C, due to continuous current I_i at ambient θ_a;

θ_t is the total temperature, in °C, at some time t after current is raised from I_i to I_s.

I_i is the initial current carried prior to application of I_s, in A (maximum current carried by the circuit-breaker during the 4 hour period immediately preceding the application of current I_s);

I_s is the overload current, in A;

I_r is the rated normal current, in A;

Then

$$\theta_t = (\theta_s - \theta_i) \times \left(1 - e^{-t/\tau}\right) + \theta_i \tag{9}$$

Let $\theta_t = \theta_{max}$; solve for t.

Then

$$t_s = -\tau \ln\left[1 - \frac{\theta_{max} - \theta_i}{\theta_s - \theta_i}\right] \tag{10}$$

where

$$\theta_i = (\theta_{max} - 40\ °C) \times \left(\frac{I_i}{I_r}\right)^{1,8} + \theta_a \tag{11}$$

and

$$\theta_s = (\theta_{max} - 40\ °C) \times \left(\frac{I_s}{I_r}\right)^{1,8} + \theta_a \tag{12}$$

For the special case where the initial current is zero, the equations in this form are useful. By substitution and further manipulation, the equations given in 5.2.2.3 in terms of Y are obtained; these are convenient to use in the more usual case where the initial current is not zero.

6 Transient recovery voltage

6.1 Harmonization of IEC and IEEE transient recovery voltages

6.1.1 General

The Transient Recovery Voltage (TRV) is defined by a waveform of voltage versus time and is the voltage impressed by the circuit across the opening contact gap in the circuit-breaker. The TRV peak is generally higher than the power frequency recovery voltage peak. However, as the TRV is damped out, the voltage across the opening contact gap in the circuit-breaker becomes the power frequency recovery voltage within a couple of milliseconds and that recovery voltage is then the system voltage of the circuit being interrupted. TRV waveform requirements were first specified in IEC and IEEE circuit-breaker standards in 1971. At that

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time, the two standards organizations each chose different waveforms to describe the same basic electrical transient. The TRV waveforms have been harmonized through a common work done by IEC SC 17A and the IEEE Switchgear Committee between 1997 and 2009. Since the approval of the relevant IEEE standards concluded in November 2009, TRV envelopes and parameters are (with few exceptions) harmonized for rated voltages higher than 1 kV and up to and including 800 kV. On the IEC side, the revisions were implemented first in amendments 1 and 2 to the first edition of IEC 62271-100 and additional changes were introduced in edition 2.0.

The first changes made to IEC 62271-100 and the relevant C37 series of IEEE standards on high-voltage circuit-breakers focused on TRVs for rated voltages of 100 kV and above. These TRV changes were adopted by IEC in May 2002.

The second set of changes was focused on voltages above 1 kV and less than 100 kV, where the waveforms used by IEC and IEEE were basically the same in that they both described a 1-cosine waveform. The main differences were that the IEC values for the TRV peak were lower and the Rate of Rise of Recovery Voltage (RRRV) was slower, which is a characteristic of cable connected systems. The IEEE values for the TRV peak were higher and the RRRV was faster, which is a characteristic of line connected systems. The harmonization process resulted in a compromise such that each standard adopted the other's set of values and that the less severe set of values was intended for application in cable connected systems and the more severe set of values for application in line connected systems. In summary, manufacturers and users will have two sets of TRV requirements to choose from that are distinguished by the application as in primarily cable connected distribution circuits or overhead line connected distribution circuits. The TRV changes to IEC for voltages above 1 kV and less than 100 kV were adopted in October 2006. These same TRV changes were later adopted by IEEE.

6.1.2 A summary of the TRV changes

6.1.2.1 The TRV harmonization plan

Working Group 23 of IEC SC 17A was formed in 1995 to prepare and execute a plan to harmonize power test procedures used in short-circuit testing of high-voltage circuit-breakers. The working group initially addressed differences in the table of tests to be performed. Upon completion of changes to the test procedures, the differences in TRV were then the *key* remaining differences that required harmonization. The following summarizes the harmonization approach developed.

6.1.2.2 Affected standards

The affected documents at the time the harmonization project began were the following.

– IEC 60056 (all parts), *High-voltage alternating current circuit-breakers*;[5]

– IEEE C37.04:1979, *IEEE standard rating structure for ac high-voltage circuit-breakers rated on a symmetrical current basis*;

– ANSI C37.06:1979, *AC high-voltage circuit-breakers rated on a symmetrical current basis – Preferred ratings and related required capabilities*;

– IEEE C37.09:1979, *IEEE standard test procedure for ac high-voltage circuit-breakers rated on a symmetrical current basis*;

– IEEE C37.011:1979, *IEEE application guide for transient recovery voltage for ac high-voltage circuit-breakers rated on a symmetrical current basis*.

These documents cover the rating, testing and application of high-voltage circuit-breakers. They were revised during the harmonization process.

[5] This series of standards was withdrawn.

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6.1.2.3 Similarities between the standards

The **Key** similarities between IEC and IEEE TRVs at the beginning of the harmonization activity were as follows:

a) RRRV at 100 % of rated I_{sc} (short-circuit current);
   - both standards used 2 kV/μs as the RRRV;
   - both standards used a time delay of 2 μs.

b) Peak TRV;
   - both standards used a first-pole-to-clear factor (k_{pp}) of 1,3 for effectively grounded systems at 245 kV and above;
   - both standards had maximum peaks of the TRV wave that are nearly the same and which are reached at about the same time.

c) Short-Line fault (SLF)
   - both standards used the same surge impedance of 450 Ω and the same time delays of either 0,2 μs at rated voltages less than 245 kV or 0,5 μs at rated voltages of 245 kV and above;
   - both standards used a peak factor of 1,6;

d) Initial TRV (ITRV)
   - both standards had the same requirements.

6.1.2.4 Differences between the standards

The *key* remaining differences between IEC and IEEE TRVs at the time the harmonization project began were the following.

a) IEEE used an exponential/1-cosine wave (Ex-Cos) description which defines all points as a curved function of time. The Ex-Cos wave shape can be explained with an analytical approach to TRV calculation. The initial exponential part of the TRV is the response of a parallel $L - Z$ circuit consisting of the inductance L of the local sources in parallel with the surge impedance Z of the lines connected to the bus. The later 1-cosine part of the TRV is an approximation to the TRV wave later in time when the exponential TRV that travelled as a wave out on the transmission system returns as a positive reflection from the first open circuit discontinuity. This analytical approach allows the TRV to be calculated for a given application condition and provides a similarly derived rated envelope for comparison.

b) IEC used a 4-parameter straight line description which allowed a TRV wave to be described in terms of simple straight lines. The 4-parameter TRV did not correspond to the response of a circuit that can be analysed. However, the 4-parameter TRV did allow the results of a measured or a calculated TRV wave to be described as simple straight lines for comparison to a similar set of straight lines as the rated envelope.

c) The Ex-Cos and the 4-parameter TRVs were comparable initially and at their peaks, but they diverged in the middle as shown in Figure 11, which shows both TRV envelopes for 100 % of rated short-circuit current at 145 kV.

d) Other differences existed between the TRVs at fractional ratings. For example, at 30 % of the rated short-circuit current; IEC used a 4-parameter envelope while IEEE used a 1-cosine (2-parameter) TRV. In addition, the peak voltages and times to peak were close, but not the same at both 30 % and 10 % of the rated short-circuit current for TRV peaks at rated voltage less than 245 kV.

e) Finally, in 1999 IEEE set the first-pole-to-clear factor to be 1,3 for voltages under 245 kV while IEC had values listed for both 1,3 and 1,5.

Overall, the differences in TRV requirements between the two standards were judged to be small.

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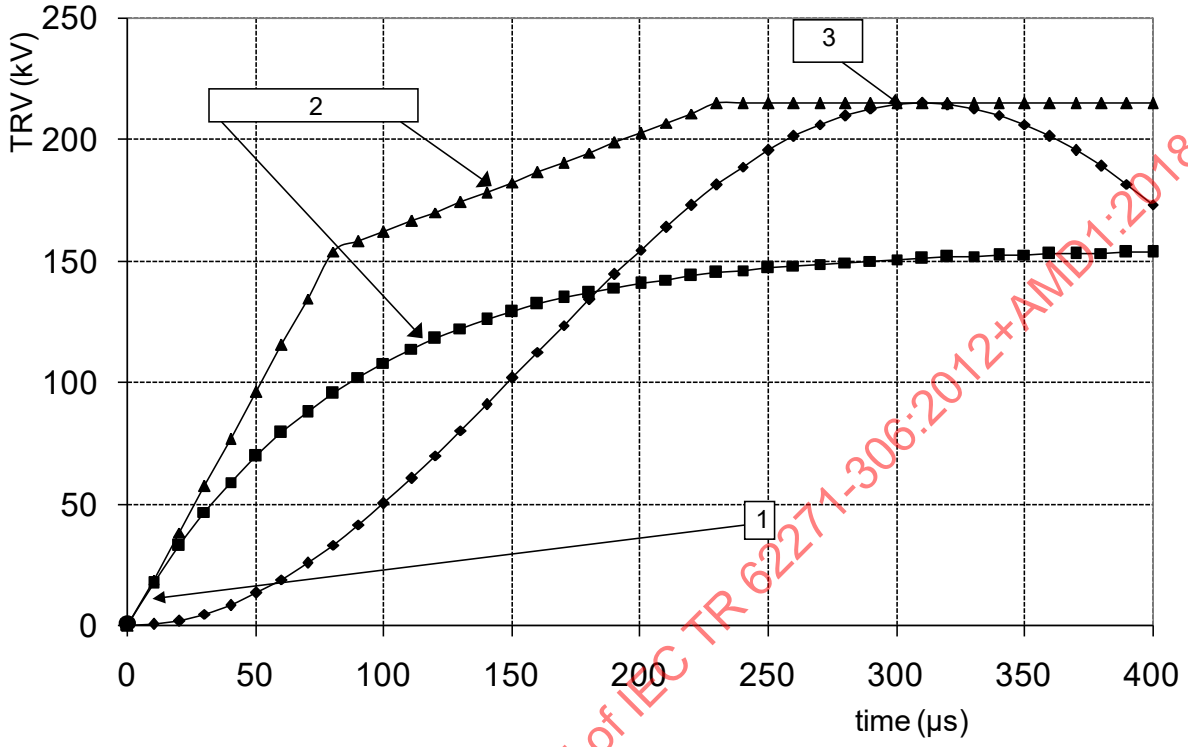

Key

▲—	Four parameter TRV	1	Both standards have the same rate-of-rise of recovery voltage and time delay
■—	Exponential TRV	2	The two standards differ in the middle region
◆—	1-cos TRV	3	Both standards have approximately the same peak

Figure 11 – Comparison of IEEE, IEC and harmonized TRVs, example for 145 kV at 100 % I_{sc} with k_{pp} = 1,3

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6.1.2.5 The importance of harmonization of TRV standards

Both methods of describing TRV and of specifying ratings have served the industry very well. This is supported by the fact that very few failures of circuit-breakers in service have been attributed to an excessive TRV stress, regardless of which of the two standards was used to design, test and apply the circuit-breakers.

WG 23 of IEC SC17A studied the TRV descriptions in the standards and also reviewed some of the literature describing the origins of these standards. The harmonizing changes recommended to the TRV descriptions in both standards were then considered equitable by WG 23 whose members represent both the IEEE Switchgear Committee and IEC SC 17A.

The recommended changes are summarized in Table 8 and explained in detail in 6.1.3.1.

Table 8 – Summary of recommended changes to harmonize IEC and IEEE TRV requirements

Item	Changes to IEEE
A1	Adopt the 4-parameter TRV as the rated TRV description at 100 % and 60 % I_{sc}, and Adopt the 2-parameter TRV as the rated TRV description at 30 % and 10 % I_{sc}
A2	Adopt the same RRRVs, time delays and delay line descriptions as IEC at 100 % and 60 % I_{sc}
A3	Adopt the peak voltage values of u_c (E_2 in IEEE) and times to peak of t_2 presently in IEC standards at 100 % and 60 % of rated I_{sc}
Item	**Changes to IEC**
B1	Adopt the 2-parameter TRV as the rated TRV description at 30 % I_{sc}
Item	**Changes to IEEE and IEC**
C1	Adopt new harmonized values for u_1 and t_1 as a compromise between IEEE and IEC to harmonize the 2 standards around the middle of the TRV wavefront where the major differences presently exists: Present IEC: u_1 = 1,0 per unit, with (t_2/ t_1) = 3; Present ANSI: u_1 = 0,5 per unit, with (t_2/t_1) = 5,5 approximately Harmonized: u_1 = 0,75 per unit, with (t_2/t_1) = 4
C2	Adopt the new compromise peak TRV voltage values of u_c (E_2) and times to peak of t_3 (T_2) at 30 % and 10 % of rated I_{sc}
C3	Use these new harmonized TRV values for the source side TRV under short-line fault conditions
C4	Use these new harmonized TRV values for the source side TRV under out-of-phase switching conditions
C5	Develop new common 2-parameter TRV values for special purpose fast rate of rise TRV conditions such as transformer fed faults based on the new trial use standard IEEE C37.06.1-1997

6.1.3 Revision of TRVs for rated voltages of 100 kV and above

6.1.3.1 TRVs for terminal faults

WG 23 recommended that IEC and IEEE adopt a common compromise value for u_1, the first TRV voltage parameter that occurs at time t_1. The recommended values are given in Table 9.

Table 9 – Recommended u_1 values

I % I_{sc}	u_1 p.u.
100	0,75
60	0,75

Where 1 p.u. for u_1 is defined as:

$1\,\text{p.u.} = k_{pp} \times \frac{U_r\sqrt{2}}{\sqrt{3}}$ and the first-pole-to-clear factor k_{pp} = 1,3 for the standard case of effectively grounded systems and k_{pp} = 1,5 for the special case of non-effectively earthed systems.

These values represented a compromise and, moreover, were also consistent with reported system data.

– IEC used a single value of u_1 = 1,0 p.u. for all currents. This was a simple compromise choice made in the original IEC or CIGRE working group. However, the system data reported in Figure 7 of report 13-10 presented at CIGRE session 1968 [6], shows that for

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currents of 25 kA and above, a u_1 value of 0,75 p.u. is adequate and 1,0 is too high. Therefore, the recommended change in IEC standards to 0,75 p.u. at 100 % and 60 % was made to bring things into better compliance with reported system data.

– IEEE did not specify a u_1 value. However, applying the 4-parameter method to the Ex-Cos envelope as shown in Figure 11 suggests an apparent u_1 of approximately 0,5 p.u. at 100 % and 60 % I_{sc}. At such values, there was a large perceived difference between ANSI and IEC.

Therefore, the recommended changes in both IEC and ANSI/IEEE standards of u_1 = 0,75 p.u. at 100 % I_{sc} and 60 % I_{sc} brought IEEE and IEC into harmonization and brought the standard TRV into better compliance with reported system data as well.

Moreover, a value of 0,75 preserves a simple relationship between u_1, t_1 and u_c, t_2 as follows:

At 100 % of rated I_{sc}:

– present IEC standard, with u_1 = 1,0 p.u. and RRRV = 2 kV/µs;

  $t_2 = 3 \times t_1$;

– proposed harmonized standard, with u_1 = 0,75 p.u. and RRRV = 2 kV/µs;

  $t_2 = 4 \times t_1$ results in the same t_2 values as presently used in IEC standards.

At 60 % of rated I_{sc}:

– present IEC standard, with u_1 = 1,0 per unit and RRRV = 3 kV/µs;

  $t_2 = 4{,}5 \times t_1$;

– proposed harmonized standard, with u_1 = 0,75 per unit and RRRV = 3 kV/µs;

  $t_2 = 6 \times t_1$ results in the same t_2 values as presently used in IEC standards.

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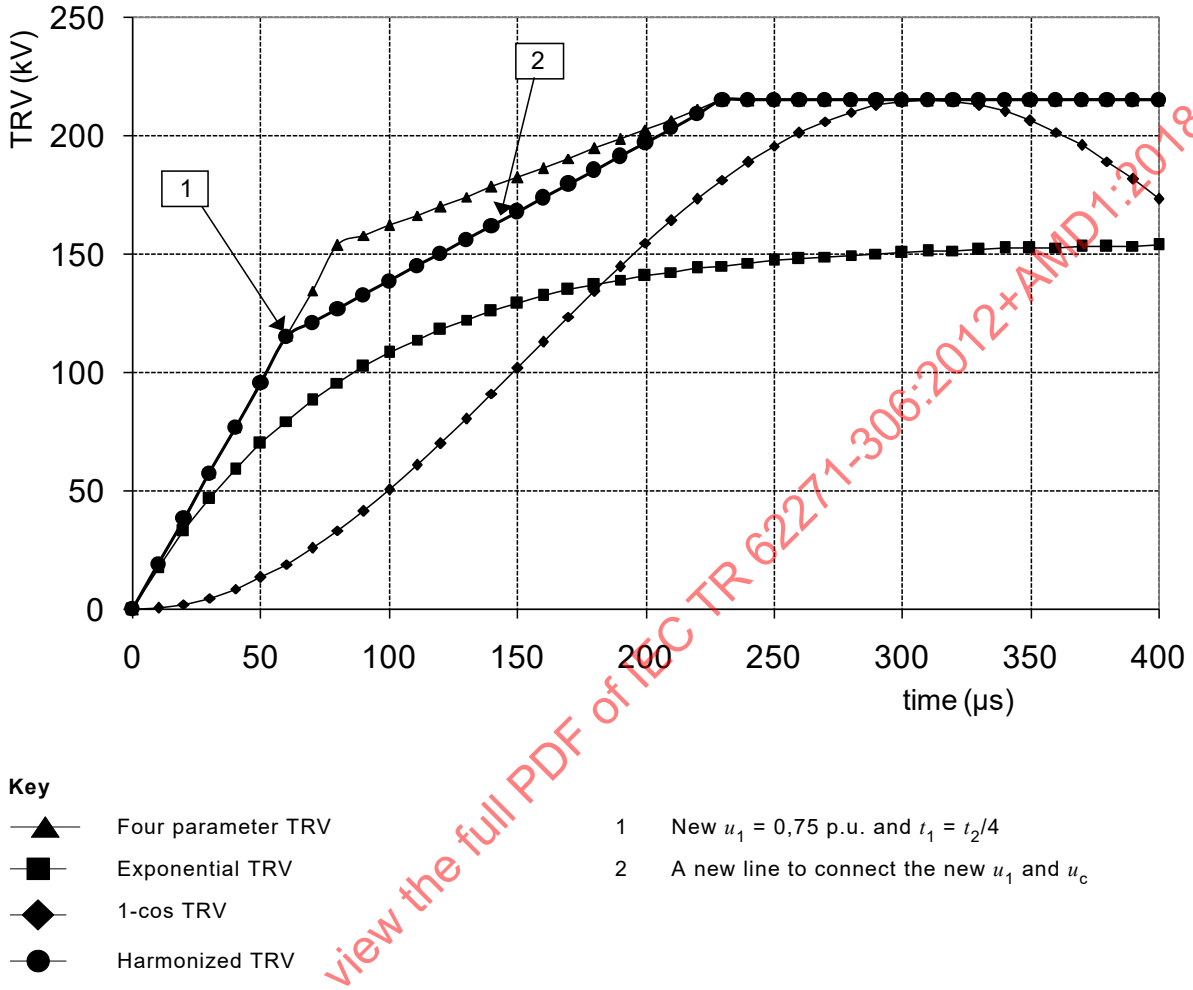

Figure 12 – Comparison of IEEE, IEC and harmonized TRVs with compromise values of u_1 and t_1, example for 145 kV at 100 % I_{sc} with k_{pp} = 1,3

After introduction of these first recommended changes, the two standards were further harmonized with the same values of RRRV for all terminal fault and short-line fault test duties.

In the past ANSI/IEEE used a first-pole-to-clear factor of 1,5 for all rated voltages. However, a change was adopted in 1999 to reduce the first-pole-to-clear factor to 1,3. This change was motivated by the following:

– a recognition that most power systems are effectively earthed at these voltages;

– a recognition that this change would move in the direction of harmonization with IEC, at least at the upper end of the spectrum of rated voltages.

The amplitude factor in IEC is 1,76; 1,54; 1,5 and 1,4 for T10, T30, T60 and T100, respectively for effectively earthed and non-effectively earthed neutral systems. These values have been adopted by IEEE in all cases for T60 and T100, and also for T10 and T30 in case of effectively earthed neutral systems and grounded faults. IEEE has kept the amplitude factors of ANSI C37.06 – 1979 for T10 and T30 in case of non-effectively earthed systems or ungrounded faults in effectively-earthed systems i.e. 1,64 for T10 and 1,58 for T30.

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6.1.3.2 TRVs on the supply side for short-line fault interruption

For the supply side in short-line fault conditions, IEC and IEEE adopted TRVs as defined already in IEC but with a lower u_1 value set in the same manner as described for T60 and T100.

6.1.3.3 TRVs for out-of-phase switching

For use in out-of-phase switching conditions, IEC and IEEE adopted TRVs as defined already in IEC but with a lower u_1 value set in the same manner as described for T60 and T100.

The first-pole-to-clear factor is 2,0 in both standards in case of effectively-earthed neutral systems, in IEEE it follows that this value is used for rated voltages 170 kV and above.

The first-pole-to-clear factor is 2,5 in both standards in case of non-effectively-earthed neutral systems.

6.1.4 Revision of TRVs for rated voltages less than 100 kV

6.1.4.1 General

Following extensive studies done by several CIGRE working groups from 1983 to 1998, IEC started in 2001 the revision of TRVs for circuit-breakers with rated voltages higher than 1 kV and less than 100 kV. This revision lead to TRVs defined in amendment 2 to edition 1.0 of IEC 62271-100.

At the same time the IEEE Switchgear Committee started revising the TRVs for high-voltage circuit-breakers in standards ANSI/IEEE C37.04, C37.06, C37.09 and C37.011. In the range of rated voltages less than 100 kV, the IEEE working groups in charge of the revision of their respective standards decide to adopt the revised IEC values. As a consequence, the TRVs proposed were expected to be fully harmonized between IEC and ANSI/IEEE standards in this rated voltage range.

6.1.4.2 Revision of IEC 62271-100

In IEC the input coming from former Working Groups (WGs) of CIGRE Study Committee (SC) A3 (High-voltage Equipment) was used. These working groups studied the necessity to adapt the TRV requirements for circuit-breakers rated less than 100 kV. In 1983, a CIGRE SC A3 Task Force reported on Transient Recovery Voltages in Medium Voltage Networks, the results of the study have been published in Electra 88 [7]. Another working group, WG 13.05, studied the TRVs associated with clearing transformer fed faults and transformer secondary faults. The results of the work of WG 13.05 were presented in Electra 102 [8]. In 1992 together with CIRED (Congrès International des Réseaux Electriques de Distribution), CIGRE SC A3 created WG CC-03 to investigate again the definition of TRVs for medium voltage switching devices. The results of these investigations were published in CIGRE Technical Brochure 134 [9], they are in line with earlier studies.

The IEC work lead to amendment 2 to the first edition of IEC 62271-100. The main feature is the distinction between two types of systems that can be met in the range considered of rated voltages higher than 1 kV and less than 100 kV:

– Cable-systems have a TRV during breaking of terminal fault at 100 % of short-circuit breaking current that does not exceed the two-parameter envelope shown in 3. Standard values of TRVs for cable-systems are as in the first edition of IEC 62271-100.

  In practice, a circuit-breaker in an outdoor substation with cable connection to overhead lines is considered to be in a cable system if the total length of cable connected on the supply side of the circuit-breaker is at least 100 m. It has to be noted also that the capacitance of cable systems on the supply side of circuit-breakers can be provided by cables and/or capacitors and/or insulated bus.

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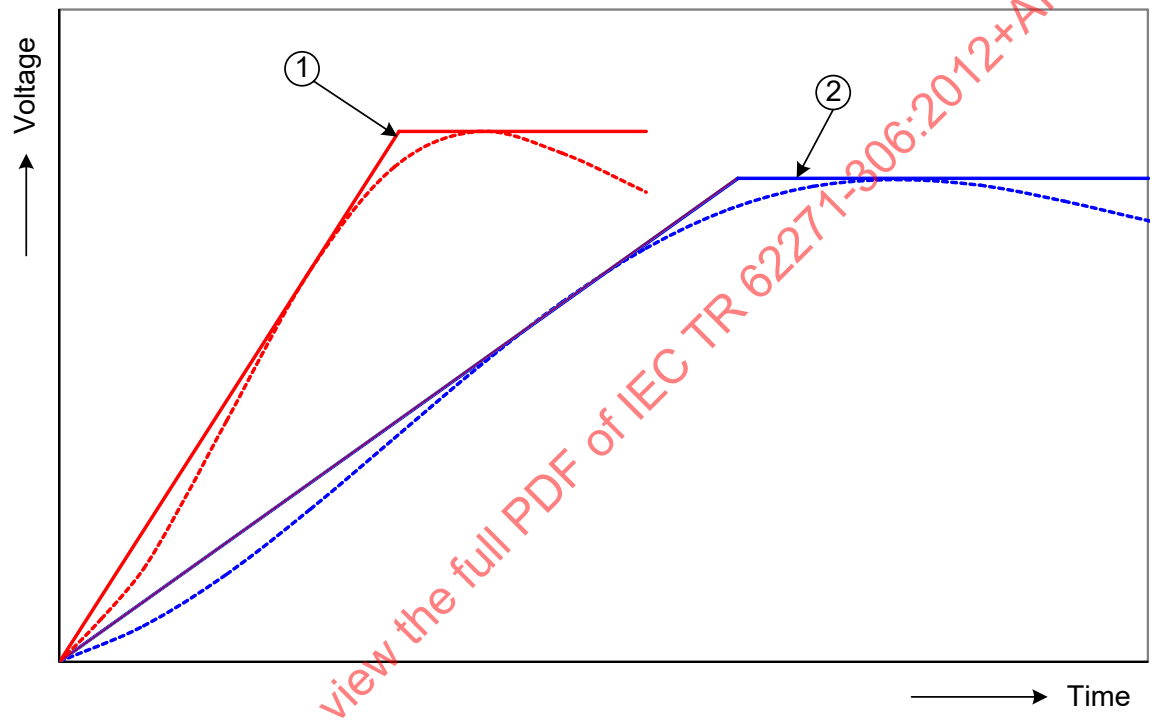
– Line systems have a TRV during breaking of terminal fault at 100 % of short-circuit breaking current higher than the envelope defined for cable systems but not exceeding the two-parameter envelope shown in Figure 13. For the purpose of harmonization, standard values of TRVs for line-systems are those defined in ANSI/IEEE C37.06 for outdoor circuit-breakers.

  In line-systems, no cable is connected on the supply side of the circuit-breaker, with the possible exception of a short length of cable between the circuit-breaker and the line(s) or the supply transformer. Systems with transmission lines directly connected to a busbar, without intervening cable connections, are typical examples of line systems.

Figure 13 shows the comparison of TRVs for cable-systems and line-systems. The RRRV for line systems is approximately twice the value for cable-systems.



Key

1 Envelope of a line system TRV

2 Envelope of a cable system TRV

Figure 13 – Comparison of TRV's for cable-systems and line-systems

Explanatory notes on the revision of TRVs for circuit-breakers of rated voltages less than 100 kV are given in Annex G.

6.1.4.3 Revision of ANSI/IEEE C37.04 and 06

In the process of harmonization of IEC and IEEE standards for high-voltage circuit-breakers, the IEEE Switchgear Committee has adopted the corresponding revision of TRVs. As illustrated by Figure 14, the aim is to have fully harmonized requirements with IEC in the voltage range between 1 kV and 100 kV.

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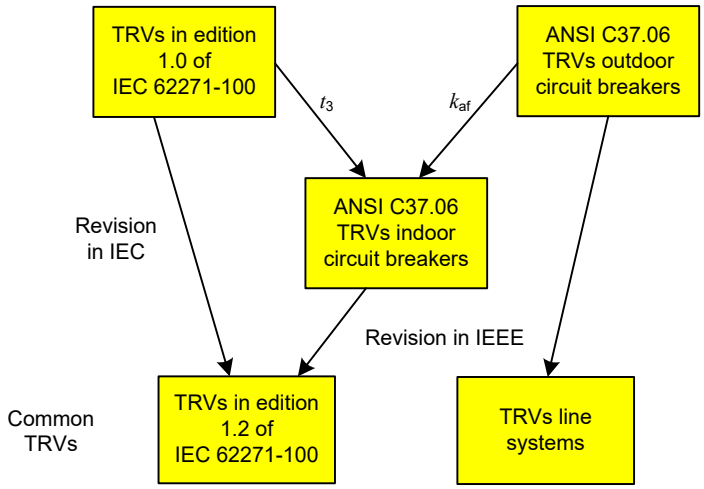

Figure 14 – Harmonization of TRVs for circuit-breakers < 100 kV

Following the approved revision of IEEE C37.04 [10] and IEEE C37.06 [11], the harmonization of TRVs in IEC and IEEE standards for high-voltage circuit-breaker was completed in 2009.

6.2 Initial Transient Recovery Voltage (ITRV)

6.2.1 Basis for specification

Due to travelling waves on the busbar and reflections from the first major discontinuity along the busbar, a high-frequency oscillation occurs which is similar to the one observed on a faulted line under short-line fault conditions. As the busbar is usually on the network side of the circuit-breaker this oscillation, which is called “Initial Transient Recovery Voltage (ITRV)” is superimposed to the very beginning of the terminal fault TRV.

The ITRV is mainly determined by the busbar and line bay configuration of the substation. Compared with the short-line fault, the first voltage peak is rather low, but the time to the first peak is extremely short, that is, within the first 1,5 μs after current zero. Therefore the thermal mode of interruption may be influenced.

CIGRE WG 13-01 studied nearly all the basic network configurations and established the basic considerations with representative figures which served as the basis for ITRV specification [12] [13]:

– the initial part of ITRV depends only on the surge impedance of the connection and on the current;
– based on the dimensions of the busbar and the connections to them a surge impedance of 260 Ω is considered as a good estimate for practical applications with rated voltages up to 550 kV;
– the time to the first peak of ITRV is twice the travelling time of the wave to the main discontinuity. It depends on the dimensions of the substation, which is related to the rated voltage (see Table 10) and thus on the arrangement of the busbar;
– in practice, the main discontinuity is either a division in two branches of the busbar or the presence of a capacitance of more than 1 000 pF;
– the velocity of the wave propagation along the busbar was found to be about 260 m/μs.

6.2.2 Applicability

As the ITRV is proportional to the busbar surge impedance and to the current, the ITRV requirements can then be neglected in the following cases:

– for all circuit-breakers with a rated short-circuit breaking current of less than 25 kA;

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– for circuit-breakers installed in metal enclosed gas insulated switchgear (GIS) because of the low surge impedance;

– for circuit-breakers with a rated voltage below 100 kV because of the small dimensions of the busbars.

– for circuit-breakers directly connected to a busbar with a connection having a capacitance higher than 800 pF. The value of 800 pF was chosen such that the corresponding time constant is higher than the arc time constant for high current interruption in SF_6. The arc time constant is approximately 0,3 µs.

If a circuit-breaker with a rated voltage equal or less than 800 kV has a short-line fault rating, the ITRV requirements are covered if the short-line fault tests are carried out using a line with insignificant time delay (see 6.104.5.2 and 6.109.3 of IEC 62271-100:2008) unless both terminals are not identical from an electrical point of view (for instance when an additional capacitance is used as mentioned in the note). When terminals are not identical from an electrical point of view, test circuits which produce an equivalent TRV stress across the circuit-breaker may be used.

For circuit-breakers with a rated voltage higher than 800 kV, the ITRV requirements are considered to be covered if the short-line fault tests are carried out using a line with insignificant time delay and a surge impedance of 450 Ω unless both terminals are not identical from an electrical point of view (for instance when an additional capacitance is used as mentioned in the NOTE). When terminals are not identical from an electrical point of view, test circuits which produce an equivalent TRV stress across the circuit-breaker may be used.

NOTE Where the breaking capability of the circuit-breaker is not sufficient to interrupt a short-line fault, additional capacitance at the line side of the circuit-breaker or parallel to the breaking unit(s) can be used, both during the test and in service. The value and the location of this additional capacitance used during the tests should be stated in the test report.

Depending on the size of the additional capacitance (in pF) in relation to the circuit of interest (i.e. test circuit or service conditions), the line side time delay increases while the surge impedance of the line may be reduced. The latter will result in a lower rate-of-rise of the line side TRV.

During type testing the prospective TRV (given in Table 8 of IEC 62271-100:2008) is evaluated without the circuit-breaker or its additional capacitance present. It should be observed that the TRV values measured during the test will be different as a result of the influence of the circuit-breaker and its additional capacitance.

6.2.3 Test duties where ITRV is required

As interruption is influenced by ITRV mainly for high values of the short-circuit current, testing under ITRV conditions is required for T100a, T100s and L_{90}.

If the circuit-breaker has a short-line fault rating, the ITRV requirements are considered to be covered if the short-line fault tests are carried out using a line with insignificant time delay, unless both terminals are not identical from an electrical point of view (for instance when an additional capacitance is used).

6.2.4 ITRV waveshape

The ITRV is defined by the voltage u_i and the time t_i. As shown on Figure 12b of IEC 62271-100:2008, reproduced hereafter as Figure 15.

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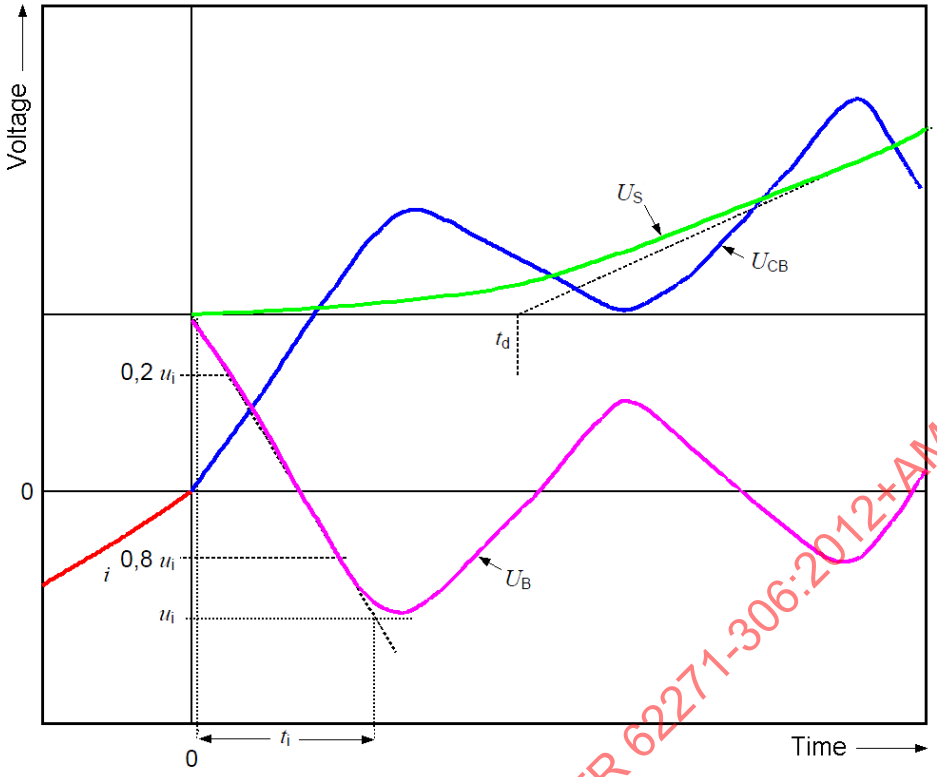

Key

i	Short-circuit current	U_{CB}	TRV across the circuit-breaker
u_i	Peak voltage of ITRV	U_B	Inherent busbar TRV
t_i	Time co-ordinate of ITRV	U_S	Inherent source side voltage TRV
t_d	Source side time delay		

Figure 15 – Representation of ITRV and terminal fault TRV

The rate of rise of the ITRV is dependent on the interrupted short-circuit current and its amplitude depends upon the distance to the first discontinuity along the busbar.

The inherent waveshape shall follow a straight line drawn using the 20 % and the 80 % point of the ITRV peak voltage u_i and the required rate of rise of the ITRV.

6.2.5 Standard values of ITRV

A multiplying factor f_i is used to determine the amplitude of the first peak u_i as function of the r.m.s value of the short-circuit breaking current.

Values of time to peak t_i are given in Table 7 of IEC 62271-100:2008 (reproduced here for convenience of reading as Table 10). These values were developed from the average distances from the breaker to the first discontinuity for the various system voltages [12].

The standard values cover both three-phase and single-phase faults. They are based on the assumption that the busbar, including the elements connected to it (supports, current and voltage transformers, disconnectors, etc.), can be roughly represented by a resulting surge impedance Z_i of about 260 Ω in the case of a rated voltage lower than 800 kV and by a resulting surge impedance Z_i of about 325 Ω in the case of a rated voltage of 800 kV. The relation between f_i and t_i is then:

$$f_i = t_i \times Z_i \times \omega \times \sqrt{2}$$

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where

$\omega = 2\pi f_r$ is the angular frequency corresponding to the rated frequency of the circuit-breaker.

Table 10 – Standard values of initial transient recovery voltage – Rated voltages 100 kV and above

Rated voltage U_r kV	Multiplying factor to determine u_i as function of the r.m.s. value of the short-circuit breaking current I_{sc} [a] f_i kV/kA		Time t_i µs
	50 Hz	60 Hz	
100	0,046	0,056	0,4
123	0,046	0,056	0,4
145	0,046	0,056	0,4
170	0,058	0,070	0,5
245	0,069	0,084	0,6
300	0,081	0,098	0,7
362	0,092	0,112	0,8
420	0,092	0,112	0,8
550	0,116	0,139	1,0
800	0,159	0,191	1,1
1 100	0,173	0,208	1,5
1 200	0,173	0,208	1,5

[a] The actual initial peak voltages are obtained by multiplying the values in these columns by the r.m.s. value of the short-circuit breaking current.

6.3 Testing

6.3.1 ITRV measurement

The ITRV should be handled as for the short-line fault TRV. Consequently it is necessary to measure the inherent ITRV circuit value.

As connections between the ITRV circuit and the supply circuit can also contribute to the initial part of the TRV, the inherent ITRV is that of the complete circuit from the circuit-breaker terminal to the first discontinuity i.e. the delay capacitor. Other contributions from the supply circuit, apart from ITRV and the normal two or four parameters TRV, must be damped by appropriate RC circuits.

As ITRV is characterized by a very high frequency in the MHz range, caution is recommended when measuring its inherent value. Diodes used in current injection methods must have short characteristic times (duration during which it differs notably from an ideal circuit-breaker), otherwise measurement could show a falsely damped ITRV with reduced RRRV [14].

The inherent waveshape shall mostly follow a straight reference line drawn from the beginning of the ITRV to the point defined by u_i and t_i. The inherent ITRV waveshape shall follow this reference line from 20 % to 80 % of the required ITRV peak value (see Figure 15). Deviations from the reference line are permitted for an ITRV amplitude below 20 % and above 80 % of the specified ITRV peak value.

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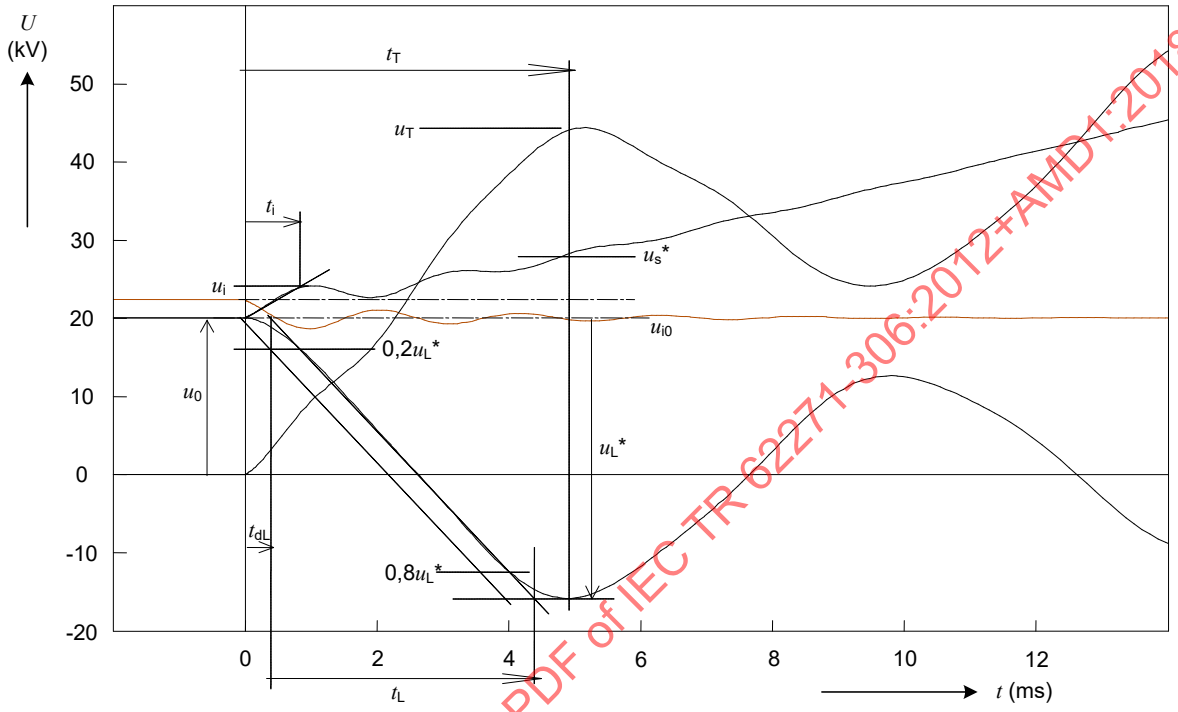
6.3.2 SLF with ITRV

Where short-line fault duties are to be performed, it may be convenient to combine the ITRV and SLF requirements in the line side circuit.

Figure 16 shows a typical graph of line and source side TRV in the case of line side TRV with time delay and source side with ITRV.



Key

t_{dL}	Line side time delay	u_{i0}	Busbar voltage drop
t_i	Time to peak of ITRV	u_L*	Line side TRV
u_0	Induced voltage drop across the line inductance	u_s*	Source side TRV
u_i	First peak of the ITRV	u_T	First peak of TRV across the circuit-breaker

Figure 16 – Typical graph of line side TRV with time delay and source side with ITRV

The first peak voltage across the circuit-breaker (u_T) is equal to sum of the line side TRV (u_L^*) and the source side TRV (u_S^*). Annex A of IEC 62271-100:2008 gives the calculation of these TRVs.

When the ITRV is combined with the transient voltage of a short line having a time delay t_{dL} as specified in Table 4 of IEC 62271-100:2008, the total stress is, for practical considerations, considered to be equal to the stress of a short line with insignificant time delay.

Further justification of the equivalence can be found in [15].

Subclause 6.109.3 of Amendment 1 to IEC 62271-100:2008 states the following.

Where applicable, a circuit-breaker with rated voltage higher than 800 kV can be tested with a line having an insignificant time delay and a surge impedance of 450 Ω (see 6.104.5.1 of IEC 62271-100:2008). If the circuit-breaker fails during this test procedure after a time corresponding to the first peak of ITRV, the test can be repeated with the required test circuit

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having the specified ITRV and a line having a surge impedance of 330 Ω and the specified time delay (t_{dL}). For both cases it is not required to perform T100s and T100a with circuits reproducing the rated ITRV.

6.3.3 Unit testing

As for SLF, ITRV circuit inductance must be divided by the number of breaks in series while time t_i is unchanged.

If the circuit-breaker has distribution capacitors, one capacitor shall be put in parallel to the unit under test.

6.4 General considerations regarding TRV

6.4.1 General

The purpose of 6.4 is to provide a background framework for some of the TRV requirements.

6.4.2 TRV waveshapes

In some cases, particularly in systems with a voltage 100 kV and above, and where the short-circuit currents are relatively large in relation to the maximum short-circuit current at the point under consideration, the transient recovery voltage contains first a period of high rate of rise, followed by a later period of lower rate of rise. This waveshape is generally adequately represented by an envelope consisting of three line segments defined by means of four parameters (see Figure 96).

The TRVs for terminal fault test-duties T100 and T60 represent cases where the major contribution of fault current is over transmission lines from multiple sources. The TRVs consist of the initial component at the fault bus and the additional component due to later arriving multiple reflected waves at the fault bus. The TRVs are overdamped (exponential) owing to the effect of the surge impedances of the lines and represented by four parameters to cover both of the above components. For terminal fault test duties T30 and T10 TRV cases, the fault current is from a single source and damping is determined by the involved circuit elements. The TRVs are underdamped (oscillatory) and thus represented by two parameters.

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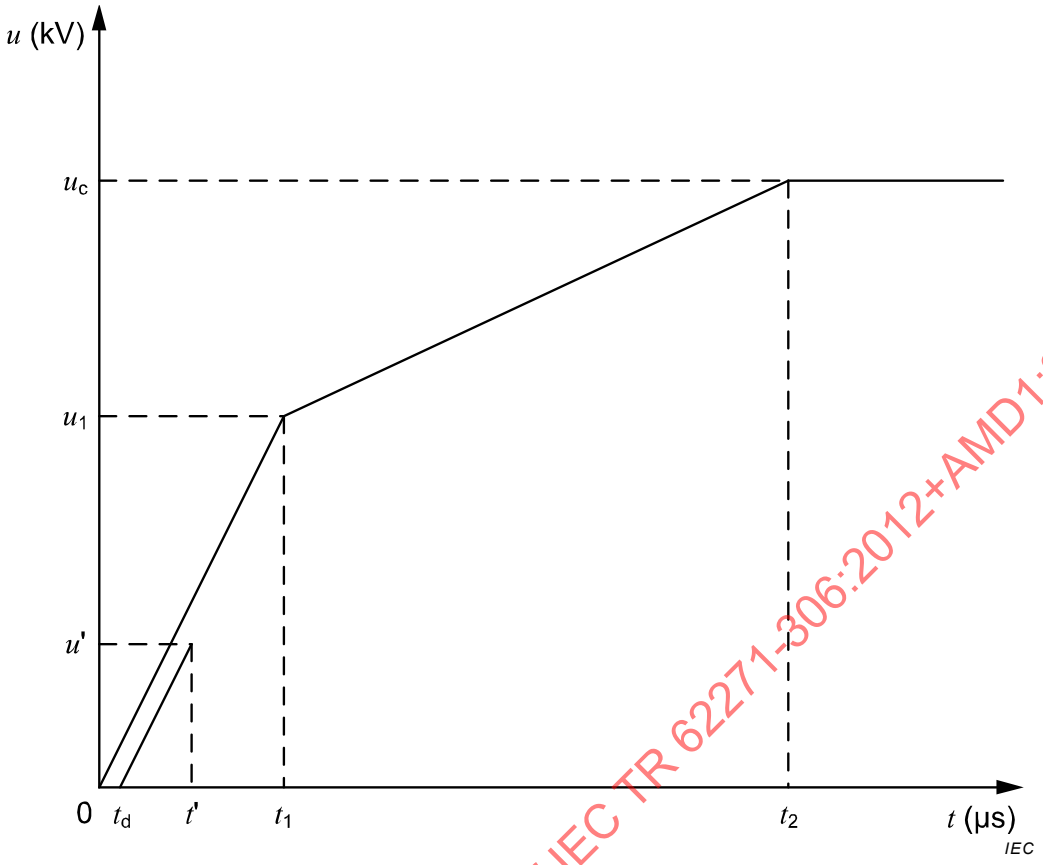

Figure 96 – Representation of a four-parameter TRV and a delay line

In other cases, particularly in systems with a voltage less than 100 kV, or in systems with a voltage greater than 100 kV in conditions where the short-circuit currents are relatively small in relation to the maximum short-circuit currents limited by transformers, the transient recovery voltage approximates to a damped single frequency oscillation. This waveshape is adequately represented by an envelope consisting of two line segments defined by means of two parameters (see Figure 97).

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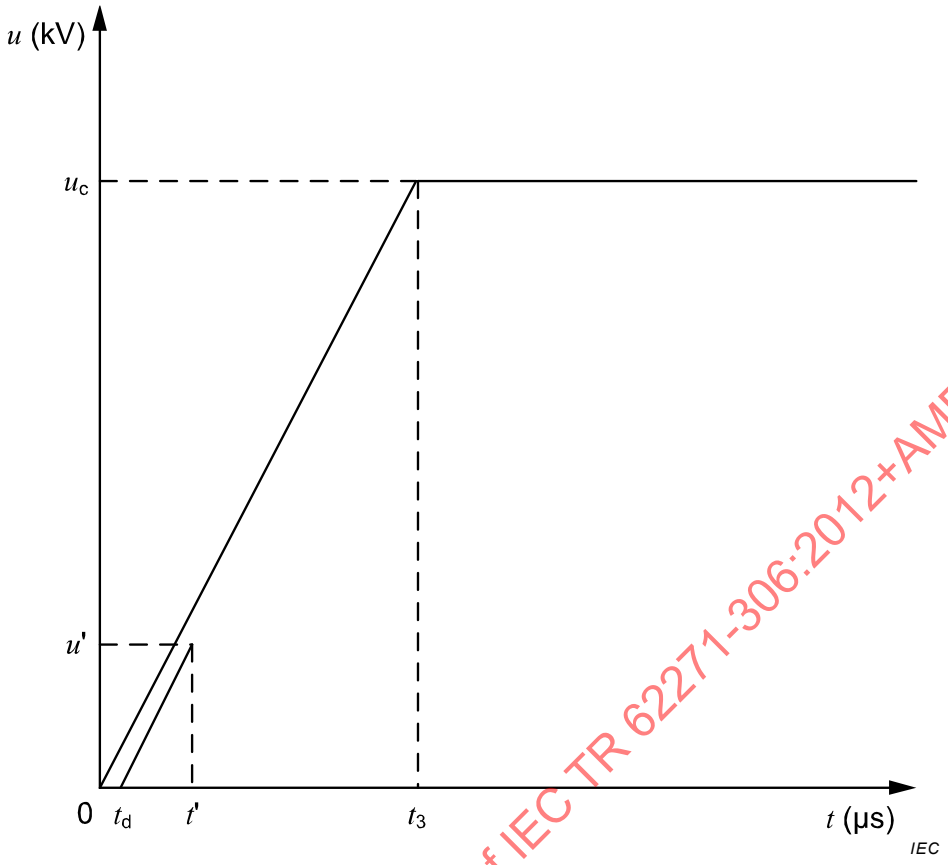

Figure 97 – Representation of a specified TRV by a two-parameter reference line and a delay line

Such a representation in terms of two parameters is a special case of representation in terms of four parameters.

The influence of local capacitance on the source side of the circuit-breaker produces a slower rate of rise of the voltage during the first few microseconds of the TRV. This is taken into account by introducing a time delay.

6.4.3 Earthing of the system

The system may be earthed in different ways depending on system voltage and application. The following definitions are used (Clause 3 of IEC 62271-100:2008 and as noted below):

solidly earthed (neutral) system (3.1.106 of IEC 62271-100:2008)
a system whose neutral point(s) is (are) directly earthed

[SOURCE: IEC 60050-601:1985, 601-02-25]

effectively earthed neutral system (3.1.128 of IEC 62271-100:2008)
system earthed through a sufficiently low impedance such that for all system conditions the ratio of the zero-sequence reactance to the positive-sequence reactance (X_0/X_1) is positive and less than three, and the ratio of the zero-sequence resistance to the positive-sequence reactance (R_0/X_1) is positive and less than one. Normally such systems are solidly earthed (neutral) systems or low impedance earthed (neutral) systems.

Note 1 to entry: For the correct assessment of the earthing conditions not only the physical earthing conditions around the relevant location but the total system is to be considered.

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non-effectively earthed neutral system (3.1.129 of IEC 62271-100:2008)
system other than effectively earthed neutral system, not meeting the conditions given in 3.1.128 of IEC 62271-100:2008. Normally such systems are isolated neutral systems, high impedance earthed (neutral) systems or resonant earthed (neutral) systems

Note 1 to entry: For the correct assessment of the earthing conditions not only the physical earthing conditions around the relevant location but the total system is to be considered.

6.4.4 Power frequency recovery voltage and first-pole-to-clear factor

6.4.4.1 General

The first-pole-to-clear factor (k_{pp}) is a function of the earthing arrangements of the system. As defined in 3.7.152 of IEC 62271-100:2008, it is the ratio of the power frequency voltage across the interrupting pole before current interruption in the other poles, to the power frequency voltage occurring across the pole or poles after interruption in all three poles. For non-effectively earthed neutral systems, this ratio is or tends towards 1,5. For rated voltages less than 170 kV, such systems are quite common, particular within Europe and Japan.

For effectively earthed neutral systems, the realistic and practical value is dependent upon the sequence impedances of the actual earth paths from the location of the fault to the various system neutral points (the ratio X_0/X_1). The value used in IEC 62271-100 is taken to be ≤ 3 (see Equation (144)). The X_0/X_1 value is a standard value confirmed by system studies of various networks. Hence, for rating purposes, IEC 62271-100 considers two values for the three-phase short-circuit condition. These are adequate for the many, different, system earthing arrangements:

a) the non-effectively earthed, to cover all unearthed systems and those with some deliberate additional impedance in the neutral system. A standardised value for k_{pp} of 1,5 is used for all such systems;

b) all effectively earthed systems where it is accepted that some impedance exists. For standardization purposes for power systems operating at 800 kV and below the value for k_{pp} used is 1,3. For ultra-high-voltage (UHV) power systems operating above 800 kV, k_{pp} is 1,2 based on an X_0/X_1 ratio of 2.

For single-phase-to-earth faults in solidly or effectively earthed neutral systems, the pole factor k_{pp} is 1,0.

At transmission voltages, there has been an increase in interconnection and transformation, particularly in major urban systems. The high number of transformer neutrals connected effectively to earth causes the value of 1,3 to be questioned. Although this has been considered, the text of IEC 62271-100 does not take these developments into account. It is important for users with such systems to note that as k_{pp} decreases towards unity the value of the second-pole-to-clear factor will fall. In addition, the value of the phase currents will change. The three phases become three independent single-phases each with k_{pp} approaching 1,0. In general the users of such systems are aware of this possibility and of the need to consider the actual system conditions when assessing the suitability of their specified requirements and the test evidence they are offered against these.

For rated voltages higher than 800 kV, systems are characterized by long transmission lines and large transformers that contribute a relatively large part of the total short-circuit current. The first-pole-to-clear factor is function of the X_0/X_1 ratio that is in this case equal to or lower than 2,0, as a consequence k_{pp} is equal to or less than 1,2 and has been standardized to 1,2.

Where the ratio of three-phase to single-phase earth fault current is 1,0, k_{pp} is also 1,0. However, although this is normally assumed to be adequately covered by the use of the three-phase requirements and the associated k_{pp} of 1,2 or 1,3, it is important that evidence is provided to demonstrate the extended arc condition of the single-phase fault. In accordance with IEC 62271-100, a full extinguishing window shall be demonstrated.

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It should be noted that in accordance with 6.108 of IEC 62271-100:2008, specific recovery voltage conditions are required to demonstrate the ability of a circuit-breaker to clear double earth faults.

Regarding earthing of the test circuit, reference is made to 6.103.3 of IEC 62271-100:2008.

6.4.4.2 Equations for the first, second and third-pole-to-clear factors

The equation for the first-pole-to-clear factor is:

$$k_{pp} = \frac{3X_0}{X_1 + 2X_0} \quad (144)$$

where X_0 is the zero sequence, and X_1 the positive sequence reactance of the system. Table 39 gives the k_{pp} values for various earthing arrangements based on the definitions given in 6.4.1.

Table 39 – First-pole-to-clear factors k_{pp}

Earthing arrangement	X_0/X_1	k_{pp}	System voltage
Solidly earthed	1	1	All
Effectively earthed	2	1,2	> 800 kV
Effectively earthed	3	1,3	≤ 800 kV
Non-effectively earthed	∞	1,5	≤ 170 kV
NOTE Calculation of k_{pp} for the effectively earthed case (X_0/X_1 = 3) gives k_{pp} = 1,286 which is then rounded to 1,3.			

Following interruption of the first pole, the remaining two phases continue to conduct fault current.

In systems with non-effectively earthed neutrals the second and third poles interrupt in series under the phase-to-phase voltage so that for the second and third pole,

$$k_p = \frac{\sqrt{3}}{2},$$

where k_p is the pole-to-clear factor of the individual poles.

In systems with effectively earthed neutrals the second pole clears with a pole-to-clear factor of,

$$k_p = \frac{\sqrt{3(X_0^2 + X_0X_1 + X_1^2)}}{X_0 + 2X_1} \quad (145)$$

NOTE In Equations (144) and (145) the resistances are neglected.

Equation (145) can be expressed as a function of the ratio $\alpha = X_0/X_1$:

$$k_p = \frac{\sqrt{3}\sqrt{\alpha^2 + \alpha + 1}}{2 + \alpha}$$

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For the third-pole-to-clear in an effectively earthed system k_p = 1. Table 40 gives k_p for each clearing pole as a function of X_0/X_1 as appropriate.

Table 40 – Pole-to-clear factors for each clearing pole

X_0/X_1	Pole-to-clear factor		
Ratio	**First**	**Second**	**Third**
1	1,0	1,00	1,0
2	1,2	1,15	1,0
3	1,3	1,26*	1,0
∞	1,5	0,866	0,866
* Equation (145) assumes that system impedances are inductances only.			

The respective multiplying factors for the peak value of the TRV (u_c) are given in Table 6 of IEC 62271-100:2008. It is important to note that the amplitude factor is the same for each pole. The multiplying factors are as applied to the power frequency voltages.

6.4.4.3 Standardised values for the second- and third- pole-to-clear factors

As discussed above, IEC 62271-100 has standardised values for the second and third-pole to clear factors for three-phase testing. Subclause 13.3 deals with this topic in relation to demonstration of arcing times for these poles and the appropriate pole factors relevant to each opening pole. It is important to note that on systems where the neutral earthing is solid, both the first-pole-to-clear factor of 1,3 and the values provided above for second pole-to-clear factors are lower. This is likely to be a rare occurrence, generally associated with urban systems where there are numerous effectively earthed transformers in close proximity. Where such differences are significant, the user is generally aware that it may be necessary to specify system-specific requirements and tests (e.g. extinguishing window and single-phase short-circuit current).

Circuit-breakers are rated on the basis of their ability to interrupt a three-phase to earth fault in either an effectively or non-effectively earthed neutral systems. Taking the former case, the three poles clear in sequence:

- The first pole clears with k_{pp} given by Equation (144) leaving a two-phase to earth fault.
- The second pole clears with k_p given by Equation (145) leaving a single-phase to earth fault. For the case of a two-phase to earth, the k_{pp} for the first clearing pole is also given by Equation (145).
- Third pole with k_p = 1 which is also applicable to the single-phase to earth fault case.

Similar logic can be applied to faults in non-effectively earthed neutral systems. A summary of the pole-to-clear factors for the different fault cases is given in Table 41.

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Table 41 – Pole-to-clear factors for other types of faults in non-effectively earthed neutral systems

Type of fault	First-pole-to-clear	Second-pole-to-clear	Third-pole-to-clear
Phase-to-earth	1	-	-
Two-phase not involving earth	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	-
Two-phase-to-earth	$k_p = \frac{\sqrt{3}\sqrt{\alpha^2+\alpha+1}}{2+\alpha}$	1	-
Three-phase not involving earth	1,5	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$	Simultaneous clearing of both poles: $k_p = \frac{\sqrt{3}}{2}$

6.4.5 TRV characteristics

6.4.5.1 Terminal fault TRVs for rated voltages higher than 1 kV and less than 100 kV

6.4.5.1.1 General

Following the decision taken at the SC17A meeting in Beijing (CN) in October, 2002, IEC SC 17A/WG35 has prepared a proposal for the revision of TRVs for circuit-breakers rated above 1 kV and less than 100 kV.

This proposal used the input coming from former Working groups of CIGRE Study Committee A3 (Switching Equipment) that have studied the necessity to adapt the TRV requirements for circuit-breakers rated less than 100 kV. In 1983, a CIGRE SC A3 Task Force reported on Transient Recovery Voltages in Medium Voltage Networks. The results of the study have been published in Electra 88. Another CIGRE working group, WG 13.05, studied the TRVs generated by clearing transformer fed faults and transformer secondary faults. The results have been presented in Electra 102 (1985). In 1992, together with CIRED, CIGRE SC A3 created working group CC-03 to investigate again the definition of TRVs for medium voltage switchgear. The outcome of these investigations has been published in CIGRE Technical Brochure 134 (1998) and is in line with earlier studies.

The first edition of IEC 62271-100 (IEC 62271-100:2001) was amended in 2006 (Amendment 2) to include the new TRV values. The modifications can be summarized as follows:

a) In order to cover applications in all types of networks (distribution, industrial and sub-transmission) for rated voltages higher than 1 kV and less than 100 kV, and for standardization purposes, two types of systems and two classes of circuit-breakers are defined:
   - cable systems:

     cable-systems are defined in 3.1.132 of IEC 62271-100:2008;
   - line systems:

     line systems are defined in 3.1.133 of IEC 62271-100:2008;
   - Circuit-breaker class S1: circuit-breaker to be used in a cable system;
   - Circuit-breaker class S2: circuit-breaker to be used in a line system.

b) A particular test duty T30 is specified for the special case of circuit-breakers intended to be connected to a transformer with a connection of small capacitance (cable length less than 20 m), in order to verify their capability to interrupt transformer-limited faults. This is covered in Annex M of IEC 62271-100:2008.

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In the general case where the capacitance of the connection is high enough, the normal test duty T30 demonstrates the capability to interrupt transformer-limited faults.

6.4.5.1.2 Terminal fault TRV for circuit-breakers in line systems

6.4.5.1.2.1 General

In North America, line systems are prevalent at 72,5 kV and below. Therefore, the TRV ratings as listed in Table 2 of ANSI C37.06-2000 were the basis to define the new Table 25 of IEC 62271-100:2008. The values for t_3 are 0,88 times the T_2 values specified in ANSI.

NOTE 1 The factor 0,88 is derived from a pure "1-cos"-waveshape multiplied with ½ amplitude factor. The standard TRV wave-shape "1-cos" in ANSI C37-06-2000 for rated voltages less than 100 kV did not coincide with the precise mathematical equation for parallel or series damped circuits, for which another ratio t_3/T_2 is applicable.

NOTE 2 TRV parameters are defined in the standard for rated voltages of 15 kV to 72,5 kV, for rated voltages less than 15 kV the TRV parameters can be derived using k_{pp} = 1,5, the values of amplitude factor, time t_3 and time delay given in 6.4.1.2.2.2, 6.4.1.2.2.3 and 6.4.1.2.2.4.

6.4.5.1.2.2 Amplitude factor

For T100, T60, T30 and T10 the following values were taken from ANSI C37.06-2000:

– 1,54 for T100;
– 1,65 for T60;
– 1,74 for T30;
– 1,8 for T10.

6.4.5.1.2.3 Time t_3

The rate-of-rise of recovery voltage (RRRV) is calculated using Equation (146),

$$\text{RRRV} = 0{,}4 U_r^{0{,}305} \tag{146}$$

Time t_3 for terminal fault is equal to $4{,}65 \times U_r^{0{,}7}$, with t_3 in µs and U_r in kV. Equation (146) was derived from the values given in Table 2 of ANSI C37.06-2000 for rated voltages 15,5 kV, 25,8 kV, 48,3 kV and 72,5 kV. The same equation is used for other rated voltages.

6.4.5.1.2.4 Time delay

The time delay in Table 25 of IEC 62271-100:2008 is derived using the following equation, t_d = 0,05 × t_3, as in the first edition of IEC 62271-100:2001 for rated voltages 48,3 kV – 52 kV and 72,5 kV. The equation has been extended to the lower rated voltages as no change in the initial part of the TRV wave-shape is expected (the initial part is exponential, even with the short line lengths that can be met in distribution and sub-transmission systems). This requirement is not judged excessive, as in the worst case (U_r = 15 kV), the time delay value of 2 µs is as specified for circuit-breakers with rated voltages higher than 72,5 kV.

It recognizes the fact that this time delay can be critical during short-line fault testing and test duty T100 with ITRV and has therefore to be taken into account. However, as shown in Tables 13 and 14 of the first edition of IEC 62271-100 published in 2001, such verification can be made when performing short-line fault tests. Therefore, as it is already the case for rated voltages higher than 38 kV, it is allowed to have a longer time delay during testing of T100, up to 0,15 × t_3, provided that short-line fault tests are performed. This possibility is indicated in Table 25 of IEC 62271-100:2008.

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6.4.5.1.3 Terminal fault TRV for circuit-breakers in cable systems

6.4.5.1.3.1 Amplitude factor

For T60, the value of 1,5 in the first edition of IEC 62271-100:2001 is kept, due to the positive experience obtained.

For T30 and T10, the amplitude factor has been raised from 1,5 to respectively 1,6 and 1,7, as the contribution to TRV comes mainly from the voltage variation across transformer(s), which has low damping; this combined with source voltage results in a TRV with a relatively high amplitude factor.

For T100, the value of 1,4 in the first edition of IEC 62271-100 published in 2001 is retained owing to the positive experience with past editions of this standard.

6.4.5.1.3.2 Time delay

The time delay t_d is as given in the first edition of IEC 62271-100 published in 2001 for rated voltages less than 52 kV, t_d = 0,15 × t_3. The equation is generalized to all cable systems (rated voltage less than 100 kV).

6.4.5.1.4 Terminal fault TRV for rated voltages equal to or higher than 100 kV

6.4.5.1.4.1 Amplitude factor

The values of the amplitude factors are given in IEC 62271-100. These values were adopted into IEC 62271-100 as a result of system studies and generally remain acceptable.

6.4.5.1.4.2 Rate-of-rise of recovery voltage and time delay

The values for the rate-of-rise-of-recovery-voltage (RRRV) for the first-pole-to-clear, and the associated time delay values, were derived from system studies, supported by system tests performed in and before the mid-1970s. The values adopted (2 kV/µs etc.) have been shown by this work to be adequate for all developed systems, and are generally acceptable for others. IEC 62271-100 gives multipliers for the RRRV for the second and third poles-to-clear. These values were derived by calculation.

6.4.5.1.5 Basis for the current TRV values of test-duty T10

Test-duty T10 is detailed in IEC 62271-100 and represents the following cases:

– a transformer limited fault condition with the circuit-breaker under consideration clearing a fault on the remote side of the transformer.

  In such circumstances, the fault current is limited by the impedance of the transformer to a value, chosen for standardization purposes, of approximately 10 %. The value of 10 % is historic, having been established from system studies and modelling using the typical impedance values of transformers of standardised ratings.

  For this duty, the fault-current is limited by the value of the impedance of the transformer. The TRV is also dominated by the transformer characteristics which give it a (1-cos) wave-shape form. The values given in IEC 62271-100 for amplitude factor, time coordinates and delay line have been established from system studies and modelling during the 1960s and before. The present values are accepted as being adequate for the vast majority of systems;

– a long line fault for circuit-breakers having a rated voltage of 245 kV and above

  For rated voltages below 245 kV, k_{pp} = 1,5 in view of the fact that the contribution of transformers to the short-circuit current is relatively larger at smaller values of the short-circuit current. Additionally, a comparatively large number of transformers having an unearthed neutral are in service in earthed neutral systems. As the damping of the TRV oscillation on a high-voltage transformer is less than in a network, an amplitude factor of

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1,7 has been standardised except for line systems, with a voltage reduction across the transformer of 10 % for voltages of 100 kV and above.

Thus, the TRV peak u_c for test-duty T10 is $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ with the following parameters:

a) for rated voltages below 100 kV:
   1) for circuit-breakers in cable systems
      k_{pp} = 1,5 and k_{af} = 1,7.
   2) for circuit-breakers in line systems
      k_{pp} = 1,5 and k_{af} = 1,8.
b) for rated voltages of 100 kV up to and including 170 kV:
   k_{pp} = 1,5 and k_{af} = 0,9 × 1,7 = 1,53.
c) for rated voltages of 245 kV up to and including 800 kV:
   k_{pp} = 1,3 and k_{af} = 1,76.
d) for rated voltages above 800 kV:
   k_{pp} = 1,2 and k_{af} =1,76.

6.4.6 Short-line fault TRV

6.4.6.1 General

Short-line fault (SLF) is a mandatory duty for circuit-breakers with rated voltages 15 kV and above that are directly connected to overhead lines. As specified already in IEC 62271-100:2001 for circuit-breakers rated 48,3 kV and above, the rated short-circuit current shall be higher than 12,5 kA (i.e. $I_{sc} \geq 16$ kA).

As it is considered that there are only few line systems below 15 kV, no short-line fault breaking capability is required for rated voltages below 15 kV. In the rare cases where a circuit-breaker with a voltage rating below 15 kV is directly connected to an overhead line, no short-line fault requirement is necessary as the line contribution to the TRV would be too low to produce a significant stress.

NOTE For class S2 circuit-breakers, short-line fault test-duty L90 is not required as it would lead to an unrealistic short length of faulted line.

The short-line fault test specified is regarded as covering three-phase short-line faults as well as two-phase and single-phase faults for the following reasons:

– the representative surge impedance, seen from the terminals of the clearing pole, is such that for all cases the RRRV for all three poles to clear is covered by the specified characteristics listed in Table 8 of IEC 62271-100:2008;
– the single-phase short-line fault test, with an interrupting window of (180°−dα), covers the requirement for the multi-phase fault cases for effectively-earthed and non-effectively earthed systems;
– the withstand of the peak value of TRV during three-phase fault interruption is demonstrated by terminal fault test duty T100.

6.4.6.2 Rated voltage less than 100 kV

6.4.6.2.1 General

In IEC 62271-100:2001, short-line fault requirements have been specified for circuit-breakers with a rated voltage of 52 kV and 72,5 kV, in the range of rated voltages considered in this edition, and directly connected to overhead-lines.

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In IEC 62271-100:2008, short-line fault requirements are specified for class S2 circuit-breakers with a rated voltage of 15 kV and above and directly connected (with busbars) to overhead-lines, irrespective of the type of network on the source side.

As the network and substation topology and layout for 48,3 kV is identical to those of 52 kV and 72,5 kV systems, the short-line test duty for 48,3 kV is specified in a way similar to 52 kV and 72,5 kV.

For rated voltages of 15 kV to 38 kV, the characteristics and procedure are slightly different. As normally no equipment is connected to the line side of the circuit-breaker, the line characteristics are adapted to virtually no delay capacitance: $t_{dL} < 0,1$ µs. As the line length to the fault location should correspond to realistic distances, the test duty L_{90} has been dropped and the tolerances on the line length for L_{75} have been adapted.

Time t_3 and the amplitude factor of the supply circuit is the same as for terminal fault test-duty T100.

6.4.6.2.2 Rated voltage equal to or higher than 100 kV

The amplitude factor and the inherent value of the RRRV of the supply circuit are as specified for terminal fault test duty T100. During a SLF interruption the RRRV on the supply side is equal to the inherent value of RRRV for the supply circuit multiplied by the ratio of the SLF current divided by the rated short-circuit breaking current.

6.4.7 Out-of-phase TRV

Not enough system information is available to revise TRV parameters for breaking in the out-of-phase condition. CIGRE SC A3 has been asked to investigate the system and service conditions leading to out-of-phase current clearing. Therefore, the TRVs for out-of-phase breaking are basically unchanged.

The values of t_3 for out-of-phase are in all cases two times the value for terminal fault T100.

6.4.8 TRV for series reactor fault

Due to the very small inherent capacitance of a number of current-limiting reactors, the natural frequency of transients involving these reactors can be very high. A circuit-breaker installed immediately in series with such type of reactor will face a high-frequency TRV when clearing a terminal fault (reactor at supply side of circuit-breaker) or clearing a fault behind the reactor (reactor at load side of circuit-breaker). The resulting TRV frequency generally exceeds by far the standardized TRV values.

In these cases, it is necessary to take mitigation measures, such as the application of capacitors in parallel to the reactors or connected to earth. The available mitigation measures are very effective and cost efficient [125]. It is strongly recommended to use them, unless it can be demonstrated by tests that a circuit-breaker can successfully clear faults with the required high-frequency TRV.

Considering the economical aspect as well as service experience with TRV mitigation measures, there is no need for special requirements in IEC 62271-100 for circuit-breakers for this type of application.

More information is given in IEEE Std. C37.011 [126].

6.4.9 TRV for last clearing poles / tests circuit topology

In Table 2 of IEC 62271-100:2001, multipliers for transient recovery voltage values for second and third clearing poles are given for circuit-breakers with rated voltages higher than 72,5 kV.

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Under NOTE 1, it is stated that for voltages equal to or lower than 72,5 kV, the values are under consideration.

For circuit-breakers with rated voltages equal to or lower than 72,5 kV, as not enough information is available to define values other than those specified for higher rated voltages, IEC SC17A has decided during its meeting in Montreal (CA), October 2003, to extend the validity of Table 2 to all rated voltages higher than 1 kV.

6.5 Calculation of TRVs

6.5.1 General

TRV parameters are defined as a function of the rated voltage (U_r), the rated first-pole-to-clear factor (k_{pp}) and the amplitude factor (k_{af}). k_{pp} is a function of the earthing of the system neutral. The rated values of k_{pp} are:

– 1,2 for terminal fault breaking by circuit-breakers with rated voltages higher than 800 kV in effectively earthed neutral systems;

– 1,3 for terminal fault breaking by circuit-breakers for rated voltages up to and including 800 kV in effectively earthed neutral systems;

– 1,5 for terminal fault breaking by circuit-breakers for rated voltages less than 245 kV in non-effectively earthed neutral systems.

6.5.2 Rated voltages less than 100 kV

A representation by two parameters of the prospective TRV is used for all test-duties.

– For circuit-breakers in cable systems.

  The TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ where k_{af} is equal to 1,4 for test-duty T100, 1,5 for test-duty T60, 1,6 for test duty T30 and 1,7 for test duty T10, 1,25 for out-of-phase breaking.

  Time t_3 for test-duty T100 is taken from Tables 24 and 43 of IEC 62271-100:2008 with IEC 62271-100:2008/AMD1:2012 and IEC 62271-100:2008/AMD2:2017. Time t_3 for test-duties T60, T30 and T10 is obtained by multiplying the time t_3 for test-duty T100 by 0,44 (for T60), 0,22 (for T30) and 0,22 (for T10).

– For circuit-breakers in line systems.

  TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \sqrt{2/3}$ where k_{af} is equal to 1,54 for test-duty T100 and the supply side circuit for short-line fault, 1,65 for test-duty T60, 1,74 for test duty T30 and 1,8 for test duty T10, 1,25 for out-of-phase breaking.

  Time t_3 for test-duty T100 is taken from Tables 25 and 44 of IEC 62271-100:2008 with IEC 62271-100:2008/AMD1:2012 and IEC 62271-100:2008/AMD2:2017. Time t_3 for test-duties T60, T30 and T10 is obtained by multiplying the time t_3 for test-duty T100 by 0,67 (for T60), 0,40 (for T30) and 0,40 (for T10).

– Time delay t_d for test-duty T100 is $0{,}15\,t_3$ for cable systems, $0{,}05\,t_3$ for line systems, $0{,}05\,t_3$ for the supply side circuit for short-line fault.

– Time delay t_d is $0{,}15\,t_3$ for test-duties T60, T30 and T10 and for out-of-phase breaking.

– Voltage $u' = u_c/3$.

– Time t' is derived from u', t_3 and t_d according to Figure 97, $t' = t_d + t_3/3$.

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6.5.3 Rated voltages from 100 kV to 800 kV

A representation by four parameters of the prospective TRV is used for test-duties T100 and T60, and the supply circuit of SLF for test duties L_{90} and L_{75} and for out-of-phase test duties OP1 and OP2 and by two parameters for test-duties T30 and T10.

– First reference voltage $u_1 = 0{,}75 \times k_{pp} \times U_r \times \sqrt{2/3}$

– Time t_1 for terminal fault test duties is derived from u_1 and the specified value of the rate of rise u_1/t_1. For test duties OP1 and OP2, t_1 is two times t_1 for test duty T100 and the rate of rise is derived from u_1 and t_1.

– TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \times \sqrt{2/3}$

where k_{af} is equal to 1,4 for test-duty T100 and for the supply side circuit for SLF, 1,5 for test-duty T60, 1,54 for test-duty T30, 0,9 × 1,7 for test-duty T10, and 1,25 for out-of-phase breaking.

– Time t_2 is equal to $4t_1$ for test-duty T100 and for the supply side circuit for short-line fault and between t_2 (for T100) and $2t_2$ (for T100) for out-of-phase breaking. Time t_2 is equal to $6t_1$ for T60.

– For test-duties T30 and T10, time t_3 is derived from u_c and the specified value of the rate of Figure 96. Time delay t_d is 2 µs for test-duty T100, between 2 µs and $0{,}3t_1$ for test-duty T60, between 2 µs and $0{,}1t_1$ for test duties OP1 and OP2. Time delay is 0,15 t_3 for test-duties T30 and T10. For the supply side circuit for short-line fault the time delay is equal to 2 µs. When short-line fault tests are performed, the time delay t_d for test-duty T100 can be extended up to 0,28 t_1. The relevant value of t_d to be used for testing is given in 6.104.5.2 to 6.104.5.5 of IEC 62271-100:2008.

– Voltage u' = $u_1/2$ for test-duties T100 and T60 and the supply side for SLF and out-of-phase breaking, and $u_c/3$ for test-duties T30 and T10.

– Time t' is derived from u', u_1/t_1 and t_d for test-duties T100, T60 and the supply circuit for SLF and out-of-phase breaking, and in accordance with Figure 96; and from u', u_c/t_3 and t_d for test-duties T30 and T10 in accordance with Figure 97.

6.5.4 Rated voltages higher than 800 kV

A representation by four parameters of the prospective TRV is used for test-duties T100 and T60, and the supply circuit of SLF for test duties L_{90} and L_{75} and by two parameters for test-duties T30, T10 and for out-of-phase test duties OP1 and OP2.

– First reference voltage $u_1 = 0{,}75 \times k_{pp} \times U_r \times \sqrt{2/3}$

– Time t_1 for terminal fault test duties is derived from u_1 and the specified value of the rate of rise u_1/t_1.

– Time t_3 for out-of-phase test duties OP1 and OP2 is derived from u_c and the specified value of the rate of rise.

– TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \times \sqrt{2/3}$

where k_{af} is equal to 1,5 for test-duty T100 and for the supply side circuit for SLF, 1,5 for test-duty T60, 1,54 for test-duty T30, 1,76 for test-duty T10, and 1,25 for out-of-phase breaking.

– Time t_2 is equal to 3 t_1 for test-duty T100 and for the supply side circuit for short-line fault. Time t_2 is equal to 4,5 t_1 for T60.

– For test-duties T30 and T10, time t_3 is derived from u_c and the specified value of the rate of rise u_c/t_3.

– Time delay t_d is 2 µs for test-duty T100, between 2 µs and 0,3 t_1 for test-duty T60. Time delay is 0,15 t_3 for test duties T30 and T10, 0,05 t_3 for test duties OP1 and OP2. For the supply side circuit for short-line fault the time delay is equal to 2 µs. When short-line fault

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tests are performed, the time delay t_d for test-duty T100 can be extended up to 0,28 t_1. The relevant value of t_d to be used for testing is given in 6.104.5.2 to 6.104.5.5.

– Voltage u' = $u_1/2$ for test-duties T100 and T60 and the supply side for SLF, and $u_c/3$ for test-duties T30, T10 and out-of-phase test duties.

– Time t' is derived from u', u_1/t_1 and t_d for test-duties T100, T60 and the supply circuit for SLF, and in accordance with Figure 96; and from u', u_c/t_3 and t_d for test-duties T30, T10 and out-of-phase test duties in accordance with Figure 97.

7 Short-line faults

7.1 Short-line fault requirements

7.1.1 Basis for specification

Short-line fault (SLF) tests are made to prove the capability of a line circuit-breaker to break faults which occur from a few hundred meters up to several km down the line. They are due to numerous causes such as lightning, tree interfering with a line, etc.

These faults are characterised by a high short-circuit current and a rate of rise of the transient recovery voltage (RRRV) which is generally much higher than the values specified for other tests duties. The transient recovery voltage (TRV) applied to the circuit-breaker is a combination of a source side component, with a RRRV comparable to the value required for terminal fault tests, and a high frequency line side component.

The latter is caused by a travelling wave. This is initiated at the moment of current interruption and sent into the line to be reflected at the fault. The reflected wave is of triangular wave-shape and has a high RRRV which is imposed on the circuit-breaker open contacts on the line side.

The RRRV and the amplitude of the line side TRV as well as the magnitude of the short-circuit current depend on the distance of the fault location from the circuit-breaker, as well as the rated voltage and the source-side conditions.

In standardization it has been found advantageous to define the stress on the circuit-breaker in case of SLF by the relation between the corresponding short-circuit current I_L and the terminal fault current I_{sc} of T100 for the same source-side conditions: For example, in case of the 90 % short-line fault test duty L_{90}: $I_L = 0{,}9 \times I_{sc}$.

L_{90} corresponds to a fault distance of a few hundred meters to less than 2 km, the 75 % short-line fault test duty L_{75} to 1 km to 5 km.

An SLF interrupting capability is required for circuit-breakers designed for direct connection to overhead lines in systems having a rated voltage of 52 kV and above and a rated short-circuit current higher than 12,5 kA. This is explained below in the technical comment.

When required, SLF test duties are applicable to all types of circuit-breakers, regardless of their interrupting medium or technology. They must break short-line faults occurring at any practical value of line length. As explained in SLF testing (7.2.3.1) the range of currents specified is such that critical values for all kinds of interrupting medium and circuit-breaker technologies are likely to be covered.

The procedure to calculate the line side and source side transient recovery voltages under conditions of a short-line fault is described in detail in Annex A of IEC 62271-100:2008.

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7.1.2 Technical comment

For rated short-circuit currents lower than or equal to 12,5 kA the requirements in terms of RRRV and current (or di/dt) are considered to be covered by the basic terminal fault test duties.

For example, during SLF test duty L_{90} a circuit-breaker rated 100 kV, 12,5 kA – 50 Hz would have to withstand a RRRV of 2,25 kV/μs while interrupting 11,25 kA (di/dt = 5 A/μs). Under terminal fault test duty T100 at 100 % of 12,5kA (di/dt = 5,5 A/μs) it is tested to withstand a RRRV of 2 kV/μs.

As stated in 7.1.1, short-line faults tests apply to circuit-breakers directly connected to overhead lines. Direct connection is defined as a connection between the circuit-breaker and overhead line having a capacitance less than 5 nF. A time delay of more than 2 μs is obtained when a capacitance of 5 nF is added between the circuit-breaker and a line having a surge impedance of 450 Ω ($t_d = C \times Z = 5 \times 10^{-9} \times 450 = 2{,}25$ μs). It follows that the initial part of TRV is covered by terminal fault test duty T100s and the SLF test duty is not required in this case. For voltages lower than 52 kV the situation is discussed in CIGRE Technical Brochure 134 [128] where it is recognised that the majority of connections to line circuits is made via cables, and in these systems SLF tests are generally not necessary. In the case of systems with overhead lines connected directly to the circuit-breaker without any length of cable, it is recommended to verify the SLF interrupting capability of the circuit-breaker.

7.1.3 Single-phase faults

SLF testing of circuit-breakers is based on single-phase faults because these faults are by far the most frequent. In addition, in effectively earthed systems, it corresponds to the condition of the last pole-to-clear which is the more severe condition for a three-phase fault.

This test condition covers also the case of the first-pole-to-clear of a three-phase fault in non-effectively earthed systems.

7.1.4 Surge impedance of the line

7.1.4.1 Surge impedance selection

For standardization purposes a surge impedance of 450 Ω adequately covers overhead line configurations up to and including 800 kV (see [16]).

For rated voltages of 1 100 kV and 1 200 kV, the surge impedance is 330 Ω.

7.1.4.2 Technical comment

The surge impedance is a function of many characteristics of a line (diameter, number, spacing, height of conductors), circuit configuration (single or double), earth resistivity and presence/type of earth wire.

For a symmetrical transmission line, the surge impedance for a single-phase fault (or the surge impedance for the last pole to clear a three-phase fault) is related to the positive and zero sequence surge impedances in the following way:

$$Z = \frac{2Z_1 + Z_0}{3} \tag{13}$$

where

Z_1 is the positive sequence surge impedance;

Z_0 is the zero sequence surge impedance.

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Typical values are given in 7.4.

Subclause 7.4 shows that for single circuit arrangements, the surge impedance is maximum when a pole clears when the others are already opened. This is also the case for double circuit constructions.

On transmission lines of system rated voltages up to and including 800 kV using bundled sub-conductor phase construction, the sub-conductors of a faulted phase are attracted together to constrict the effective diameter of the bundle during fault conditions. This changes the line impedance for that phase during the duration of the fault. This fact has been taken into account when evaluating and standardising the value of surge impedance. For rated voltages of 1 100 and 1 200 kV the value of 330 Ω is based on the fact that the individual conductors in the bundle do not make contact under the influence of a short-circuit.

Calculations performed on 420 kV lines have shown that the surge impedance is between 434 Ω and 456 Ω when bundle contraction during fault is considered [16].

Therefore, in the 4th edition of IEC 60056 a single value of 450 Ω was standardised irrespective of the number of conductors per phase as short-circuit conditions were similar to those of a single conductor line.

Even though values for single conductor lines could be found to be slightly higher, a surge impedance of 450 Ω adequately covers all practical cases for rated voltages up to and including 800 kV and 330 Ω for 1 100 kV and 1 200 kV, because when evaluating SLF parameters only the worst conditions are considered [17]:

– three-phase short-line fault at a critical distance;
– it is assumed that the supply has a single-phase short-circuit current equal to 100 % of the rated (3-phase) short-circuit current. In practice this is unlikely to happen as 100 % generation is generally not available and the single-phase short-circuit current is in many cases lower than the three-phase short-circuit current (see 7.2.6);
– in addition it is assumed that the impedance of earth return is negligible, whereas in practice this impedance effectively reduces the short-circuit current and the rate-of-rise of recovery voltage.

7.1.5 Peak voltage factor

7.1.5.1 Definition and selection of value

The peak factor (k) is the ratio of amplitudes of the first peak of the TRV on the line side (u_L*) to the peak voltage at the circuit-breaker terminals prior to interruption (u_0) (see Figure 16 of IEC 62271-100:2008).

As shown in 7.1.5.2 and 7.4, the standardised value of 1,6 adequately covers all practical values.

7.1.5.2 Technical comment

The peak factor (k) is given by:

$$k = \frac{u_L^*}{u_0} \tag{14}$$

The rate of rise of recovery voltage on the line side is equal to the product $Z \times \frac{di}{dt}$,

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where

Z is the surge impedance;

$\frac{\mathrm{d}i}{\mathrm{d}t} = \omega \times I_{\mathrm{L}} \times \sqrt{2}$ is the current derivative before interruption.

The time to the first peak u_{L}* is equal to two times the reflection time from the circuit-breaker to the fault point (time necessary for the travelling wave to reach the fault and be reflected back to the circuit-breaker):

$$\frac{2\lambda}{v} = t_{\mathrm{L}}$$

where

λ is the distance from the opening circuit-breaker to the fault;

v is the velocity of light.

The rate-of-rise of recovery voltage is then given by:

$$\frac{u_{\mathrm{L}}^{*}}{t_{\mathrm{L}}} = Z\frac{\mathrm{d}i}{\mathrm{d}t}$$

It follows that the first peak of the line side TRV is given by:

$$u_{\mathrm{L}}^{*} = Z\frac{\mathrm{d}i}{\mathrm{d}t} \times \frac{2\lambda}{v} \tag{15}$$

$$u_0 = X_{\mathrm{L}} \times \lambda \times I_{\mathrm{L}}\sqrt{2} \tag{16}$$

where

X_{L} is the line reactance per unit length.

From Equations (14), (15) and (16):

$$k = \frac{2\omega Z}{X_{\mathrm{L}} \times v} \tag{17}$$

$$X_{\mathrm{L}} = \frac{(2L_{1\mathrm{w}} + L_{0\mathrm{w}})\omega}{3} \tag{18}$$

where

$L_{1\mathrm{w}}$ is the positive sequence power frequency line inductance per unit length;

$L_{0\mathrm{w}}$ is the zero sequence power frequency line inductance per unit length.

$$Z_1 = \sqrt{\frac{L_1}{C_1}} \tag{19}$$

$$v = \frac{1}{\sqrt{L_1 C_1}} \tag{20}$$

where

L_1 is the high-frequency positive sequence line inductance per unit length;

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C_1 is the high-frequency positive sequence line capacitance per unit length.

From Equations (19) and (20):

$$\frac{Z_1}{v} = L_1 \tag{21}$$

Combining Equation (17) with Equation (13), (18) and (21) gives:

$$k = \frac{2L_1(2 + \frac{Z_0}{Z_1})}{2L_{1w} + L_{0w}} \tag{22}$$

If the high-frequency inductance L_1 is equal to the power frequency inductance of the line L_{1w}, Equation (22) simplifies to:

$$k = \frac{2(2 + \frac{Z_0}{Z_1})}{2 + \frac{L_{0w}}{L_{1w}}} \tag{23}$$

if $\frac{L_{0w}}{L_{1w}} = 3$ is assumed for high-voltage networks,

$$k = 0{,}4(2 + \frac{Z_0}{Z_1}) \tag{24}$$

In practice the high frequency inductance L_1 is lower than the power frequency value L_{1w}, and losses which are always present have been neglected in the calculation. For these reasons the peak factor obtained by Equation (23) is a conservative value.

Subclause 7.4 gives values of peak factors calculated for HV networks 72,5 kV to 550 kV. All the values obtained are equal or lower than 1,55. The specified value of 1,6 is therefore conservative.

7.1.6 Rate-of-Rise of Recovery Voltage (RRRV) factor "*s*"

7.1.6.1 General

The RRRV on the line side is given by $Z\frac{\mathrm{d}i}{\mathrm{d}t}$ or $Z \times \omega \times I_L\sqrt{2}$. For practical applications it is sometimes useful to express the RRRV as follows:

$$\text{RRRV} = s \times I_L, \text{ with } s = Z \times \omega\sqrt{2} \text{ and } \omega = 2\pi f_r$$

For rated frequencies (f_r) of 50 Hz and 60 Hz, and with Z= 450 Ω, the RRRV factor s is then equal to:

f_r = 50 Hz s = 0,20 kV/μskA

f_r = 60 Hz s = 0,24 kV/μskA

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7.2 SLF testing

7.2.1 Test voltage

As SLF tests are based on single-phase faults, the test voltage is equal to the phase to earth voltage i.e. the rated voltage divided by √3, with a first-pole-to-clear factor k_{pp} = 1,0.

7.2.2 Operating sequence

SLF is mainly a single-phase fault on a line. During network operation the fault is cleared by a circuit-breaker performing its rated operating duty: an auto-reclosing duty as usual for overhead line networks.

In order to reproduce service conditions, IEC 62271-100 requires circuit-breakers to perform their rated operating duty during testing.

7.2.3 Test duties

7.2.3.1 General

The severity of SLF tests depends on the position of the fault along the line length as it determines the magnitude of the current (and di/dt) and the transient recovery voltage characteristics: RRRV (proportional to di/dt) and first peak value (proportional to the reflection time from the circuit-breaker to the fault). Circuit-breakers must break short-line faults with any practical values of line length corresponding to fault currents ranging from tens of percent to about 90 % of the rated short-circuit current.

For example for a 145 kV, 40 kA, 60 Hz circuit-breaker, a short-line-fault test at 90 % of the rated short-circuit current corresponds in practice to a fault on the line occurring 330 m away from the circuit-breaker.

The critical percentage of short-circuit current is dependent on the interrupting medium of the circuit-breaker.

An arc in SF_6 has a very short time constant (less than 0,5 μs) i.e. its resistance or conductance changes rapidly during the transient recovery period. Therefore interruption is affected by the very high frequencies of TRV met in L_{90} test duty and the associated high values of the short-circuit current [18].

An arc in high pressure air has a longer time constant (typically 10 times the value in SF_6), so interruption is mostly affected by the lower frequencies and higher amplitudes met in L_{75}.

Other technologies such as oil or vacuum circuit-breakers have proved to be insensitive to short-line fault conditions, as long as they have the corresponding terminal fault breaking capability.

In order to cover the possible critical values of short-circuit current, two ranges of currents are specified for short-line fault tests, in percentage of the rated short-circuit current:

– test duty L_{90} with 90 % (-0 %, +2 %) of I_{sc};
– test duty L_{75} with 75 % (-4 %, +4 %) of I_{sc}.

If there is a significant increase of arcing time when the current is reduced from 90 % I_{sc} to 75 % I_{sc}, an additional series of tests with 60 % (± 5 %) I_{sc} (L_{60}) is required to confirm that there is no critical current in the 60 % to 75 % region.

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7.2.3.2 Technical comment

Compared to terminal fault conditions and assuming the same source side impedance as in the case of a 100 % terminal fault (T100) the short-circuit current in a short-line fault is lower as the line between circuit-breaker and fault introduces an additional impedance into the total circuit.

Standard values of the current I_L related to line length are specified corresponding to a reduction of the a.c. component of the rated short-circuit current to 90 % (L_{90}) and 75 % (L_{75}).

In IEC 62271-100 the line length has been standardised.

As the line length represented in a test may differ from the standardised value, within a tolerance given in Annex B of IEC 62271-100:2008, the short-circuit current during tests may vary in the following ranges for circuit-breakers having rated voltages of 48,3 kV and above:

L_{90}:	I_L = 90 % of I_{sc}	(line length = standardised value)
	I_L = 92 % of I_{sc}	(line length = standardised value – 20%)
L_{75}:	I_L = 71 % of I_{sc}	(line length = standardised value + 20%)
	I_L = 79 % of I_{sc}	(line length = standardised value – 20%)

In cases (see c) of 6.109.4 of IEC 62271-100:2008) where a test duty L_{60} is required:

L_{60}:	I_L = 55 % of I_{sc}	(line length = standardised value + 20%)
	I_L = 65 % of I_{sc}	(line length = standardised value – 20%)

These values are derived from calculations given in 7.5.

NOTE Since the network topology and layout for 48,3 kV is identical to those of 52 kV and 72,5 kV, the value of 48,3 kV has been chosen as the lower value.

For circuit-breakers with voltage ratings equal to or higher than 15 kV and lower than 48,3 kV only test duty L_{75} has to be performed with a line length equal to the standardized value with a tolerance of +0 % and -20 %.

7.2.4 Test current asymmetry

7.2.4.1 General

The test current is symmetrical at contact separation (with a d.c. component less than 20 %) because the most severe condition is obtained in the thermal phase of interruption when the current derivative ($\frac{di}{dt}$) and the RRRV ($Z\frac{di}{dt}$) are maximum.

7.2.4.2 Technical comment

It is recognised that lightning strikes are the most likely events leading to a short-line fault. As these are random events in relation to the point on the voltage cycle they will generally lead to asymmetrical currents. However the d.c. component of this current decreases more rapidly for a line fault than for other faults due to the high value of resistance in the earth return circuit. Therefore for the most likely system condition giving SLF, although asymmetrical at initiation, will approach the symmetrical condition or at least a low degree of asymmetry, by the time of current interruption by the circuit-breaker.

Based on the above SLF breaking tests need not be asymmetrical. As a result the simpler test regime of symmetrical testing has been standardised on for this duty.

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SLF breaking tests with asymmetrical currents are also not required because when compared with symmetrical conditions, the $\frac{di}{dt}$ at current zero and RRRV ($Z\frac{di}{dt}$) applied on circuit-breakers are reduced.

7.2.5 Line side time delay

The local capacitance always present in a substation between the circuit-breaker and the line introduce a time delay t_{dL} in the initial part of the line side TRV. This capacitance represents the typical capacitance that can be met in actual networks. It is for example introduced by supports and stray capacitance of the connection between the circuit-breaker and the faulted line.

For rated voltages equal and lower than 170 kV, the time delay t_{dL} is standardised to 0,2 μs.

For rated voltages equal to and higher than 245 kV, it is standardised to 0,5 μs.

These values correspond to a line side phase to earth capacitance C_{dL} equal to 445 pF and 1 110 pF, respectively.

NOTE In order to cover the ITRV requirement, where it is specified on the supply side (see 6.104.5.2 and 6.109.3 of IEC 62271-100:2008), the SLF tests are generally performed with an insignificant time delay (less than 0,1 μs) on the line side. ITRV specification is not applicable to circuit-breakers in Gas Insulated Substations.

7.2.6 Supply side circuit

7.2.6.1 Supply side circuit definition

The short-circuit impedance of the supply side circuit is such that the rated short-circuit current is obtained in terminal fault conditions. This is due to the fact that the single-phase short-circuit current is assumed to be equal to the three-phase short-circuit current.

For rated voltages equal to or higher than 15 kV and less than 100 kV, it is assumed that the TRV frequency and the amplitude factor of the supply circuit are the same as for a three-phase terminal fault. It follows that the RRRV of the supply side circuit is equal to the RRRV of the circuit for terminal fault test duty T100s divided by 1,5, and the amplitude factor is 1,54.

For rated voltages equal to 100 kV and above, the supply side RRRV is equal to the RRRV specified for three-phase faults.

The supply side TRV is adjusted to obtain the crest value according to the first-pole-to-clear factor 1,0 and amplitude factor 1,4. The RRRV of 2,0 kV/μs is retained. The time parameters (t_3 or t_1 and t_2) are adjusted accordingly.

7.2.6.2 Technical comment

System studies have shown that the supply side RRRV is, as a first approximation, equal to the RRRV defined for three-phase faults [19]. Such an approximation is justified as the RRRV is equal to the product $Z\frac{di}{dt}$, with the supply side surge impedance Z and the current derivative ($\frac{di}{dt}$) having similar values for single-phase and three-phase conditions.

Generally speaking the supply side RRRV for single-phase faults is slightly lower than for three-phase faults. This has been supported by TRV studies in 420 kV networks [19]. However, as there is a large scatter of values, the RRRV for a single phase terminal fault, corresponding to the supply side TRV in the case of a short-line fault, has been standardised

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to be the same value 2 kV/μs for rated voltages equal or higher than 100 kV as defined for three-phase faults.

During a SLF breaking operation, the voltage at the circuit-breaker terminals at current zero is equal to the voltage drop on the faulted line and is not zero as would be the case under terminal fault conditions. It follows that the TRV voltages on the supply side during SLF interruption are accordingly lower than the inherent values defined previously.

During test duties L_{90} and L_{75}, and neglecting the influence of the circuit-breaker, the source side TRV peak is reduced by a factor 1,36/1,4 and 1,30/1,4, respectively. The derivation of TRV peak values is explained in Annex A of IEC 62271-100:2008.

7.3 Additional explanations on SLF

7.3.1 Surge impedance evaluation

7.3.1.1 General

The surge impedance is the ratio of the TRV slope ($\frac{\mathrm{d}u}{\mathrm{d}t}$ or RRRV) divided by the current derivative $\frac{\mathrm{d}i}{\mathrm{d}t}$. The RRRV is defined as the slope between the points corresponding to 20 % and 80 % of the line side TRV peak of the inherent test circuit response.

7.3.1.2 Technical comment

In the case of very short lines between the opening circuit-breaker and the fault, with $t_L < 5\ t_{dL}$, the wave shape of the line side TRV is deformed and cannot be compared to a triangular shape with an initial time delay.

The curves presented in 7.6 show that for a correct evaluation of the surge impedance it is necessary to define the rate of rise of the line side recovery voltage as the slope between the points corresponding to 20 % and 80 % of the peak voltage, as in this region the shape is not influenced by the time delaying capacitance.

Although the previous 10 % to 90 % method leads also to correct values where $t_L \geq 5t_{dL}$, this 20 % to 80 % method is generalised for the evaluation of inherent line side TRVs in the 1st edition of IEC 62271-100.

7.3.2 Influence of additional capacitors on SLF interruption

7.3.2.1 General

Additional capacitance connected between the circuit-breaker terminals (grading capacitor or capacitor used to assist the interruption) or line-to-earth, has two effects:

– it decreases the oscillation frequency and the RRRV of the line side TRV;
– it increases the time delay of the line side TRV.

Both effects tend to ease the interruption, and capacitors are sometimes used to increase the short-line fault breaking capability of circuit-breakers.

Historically resistors where used in air-blast circuit-breakers resistors to reduce the RRRV and facilitate the interruption. RRRV is reduced by a factor $\frac{R}{R+Z}$ where R is the resistor value and Z the surge impedance of the line.

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7.3.2.2 Reduction of the line side RRRV by a phase to earth capacitor

As SF_6 circuit-breakers are more sensitive to the initial part of the TRV (first μs) the use of additional capacitors has proved to be more efficient.

When capacitors mounted across the circuit-breaker terminals are used to meet a SLF breaking capability, caution is recommended as high values of capacitance could lead to ferro-resonance with electromagnetic instrument transformers connected between the circuit-breaker and a de-energized line or connected to a supposedly de-energized bus.

If the capacitor is connected phase to earth on the line side, the reduction of the line side RRRV can be estimated by a simple calculation:

Definitions:

C_{add} is the additional line-to-earth capacitance;

L is the line inductance;

Z is the line surge impedance;

C_L is the total line capacitance = $\frac{L}{Z^2}$;

C_e is the equivalent line capacitance.

The equivalent line capacitance C_e is defined as the capacitance which, together with the inductance L, gives the line frequency of oscillation:

$$f_L = \frac{1}{2\pi\sqrt{LC_e}} \tag{25}$$

The period of oscillation is equal to $\frac{2u_L^*}{\left(\frac{du}{dt}\right)_L}$ with:

$$u_L^* = 2X_L \times I_L\sqrt{2} \quad \text{and} \quad \left(\frac{du}{dt}\right)_L = Z \times \omega \times I_L\sqrt{2}$$

It follows that:

$$f_L = \frac{Z \times \omega}{4X_L} \tag{26}$$

From Equations (25) and (26):

$$C_e = \frac{4L}{\pi^2 \times Z^2} = \frac{4C_L}{\pi^2} = 0{,}4C_L \tag{27}$$

If an additional capacitance is added at the line entrance, the RRRV on the line side is reduced in the same manner as the line frequency of oscillation:

$$\frac{du}{dt} = Z \times \omega \times I_L\sqrt{2}\,\frac{2\pi\sqrt{LC_e}}{2\pi\sqrt{L(C_e + C_{add})}}$$

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Using Equation (27) gives:

$$\frac{\mathrm{d}u}{\mathrm{d}t} = Z \times \omega \times I_{\mathrm{L}} \sqrt{2}\, \frac{\sqrt{C_{\mathrm{L}}}}{\sqrt{C_{\mathrm{L}} + 2{,}5 C_{\mathrm{add}}}}\,, \text{ or } \frac{\mathrm{d}u}{\mathrm{d}t} = Z \times \omega \times I_{\mathrm{L}} \sqrt{2} \sqrt{\frac{C_{\mathrm{L}}}{C_{\mathrm{L}} + 2{,}5 C_{\mathrm{add}}}} \qquad (28)$$

with $C_{\mathrm{L}} = \frac{L}{Z^2}$

Equation (28) can be used in practice to estimate the effect of a phase-to-earth capacitance C_{add} on the line side rate of rise of recovery voltage.

The method presented in 7.6 can also be used to evaluate the effect of a capacitance on the line side TRV in more detail. The time delay t_{dL} is calculated by taking into account the total capacitance on the line side, i.e. line capacitance plus additional capacitance from the circuit-breaker (see Figure 17).

The reduction of the line side RRRV by a phase to earth capacitor is especially important to be reproduced in synthetic testing where the capacitor must be installed in parallel to the line. If, for practical reasons the capacitor is connected in parallel to the circuit-breaker, then its value shall be calculated (by Electromagnetic Transient Program or equivalent) to produce an equivalent TRV.

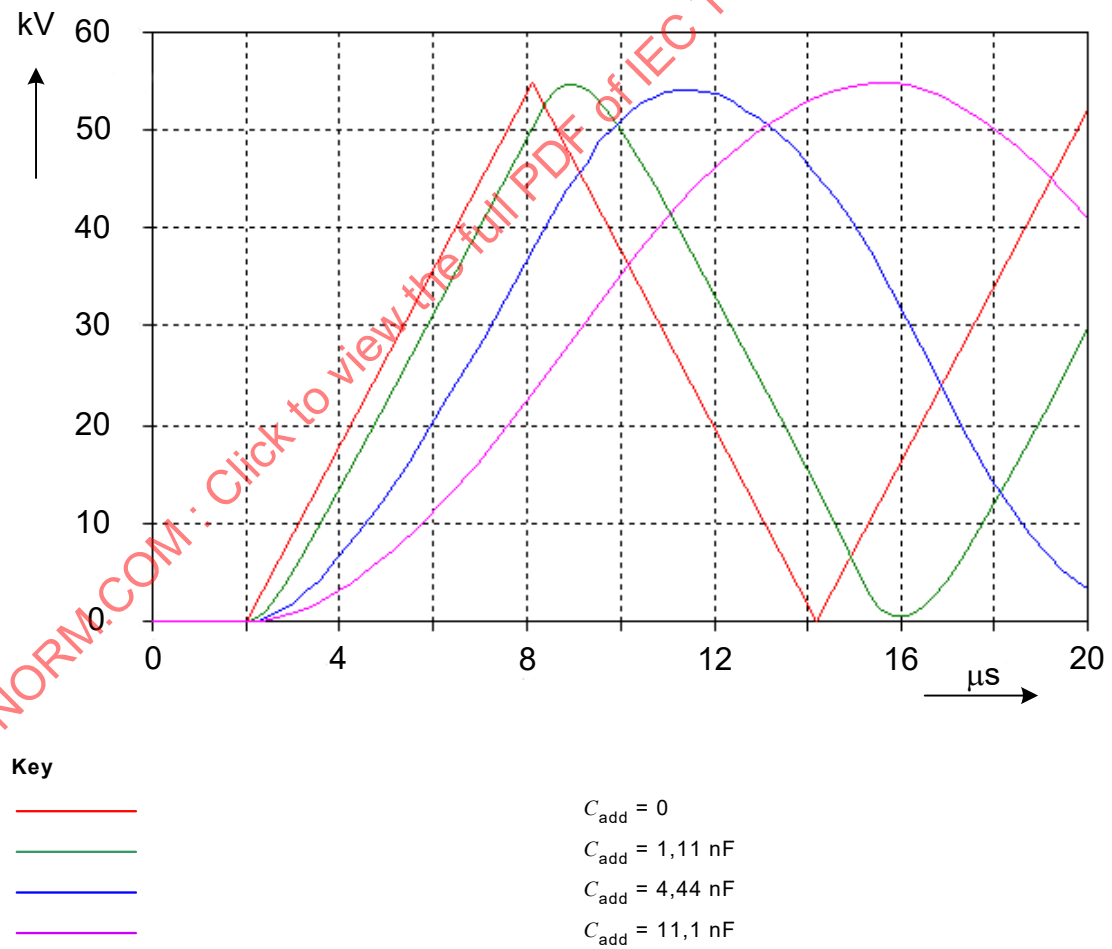

Figure 17 – Effects of capacitor size on the short-line fault component of recovery voltage with a fault 915 m from circuit-breaker

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7.3.2.3 Influence of the location of phase-to-earth capacitors

In a substation it can be advantageous to take into account the existing phase-to-earth capacitances between the circuit-breaker and the line (such as cables, GIS bus, CVTs) in order to define the necessary additional value of the phase-to-earth capacitor which has to be delivered with the circuit-breaker. However caution is recommended if the circuit-breaker is to be moved to a different location.

For maximum effectiveness the capacitor should be close to the circuit-breaker terminal.

CVTs due to their inherent capacitance have an influence on the TRV, but as shown in Figure 18, taken from [20], caution is necessary because to be of benefit they shall be close enough to the circuit-breaker to influence current interruption. Figure 18 shows that if the capacitor is located too far from the circuit-breaker, the time delay of the recovery voltage is decreased and the amplitude of the first voltage jump is increased, both effects resulting in a lowering of the benefit of the capacitance to the circuit-breaker interruption capability.

Based on these considerations if a smaller value of the phase-to-earth capacitor is used compared to that applied for type testing to take the existing phase-to-ground capacitance in the substation into account, it is recommended to calculate its final value by Electromagnetic Transient Program or equivalent to produce an equivalent TRV of the lumped capacitor used for testing.

This calculation has to be repeated if the location of the circuit-breaker or the substation configuration changes (a CVT is substituted by another one having a different capacitance, a cable is substituted by a bus bar connection).

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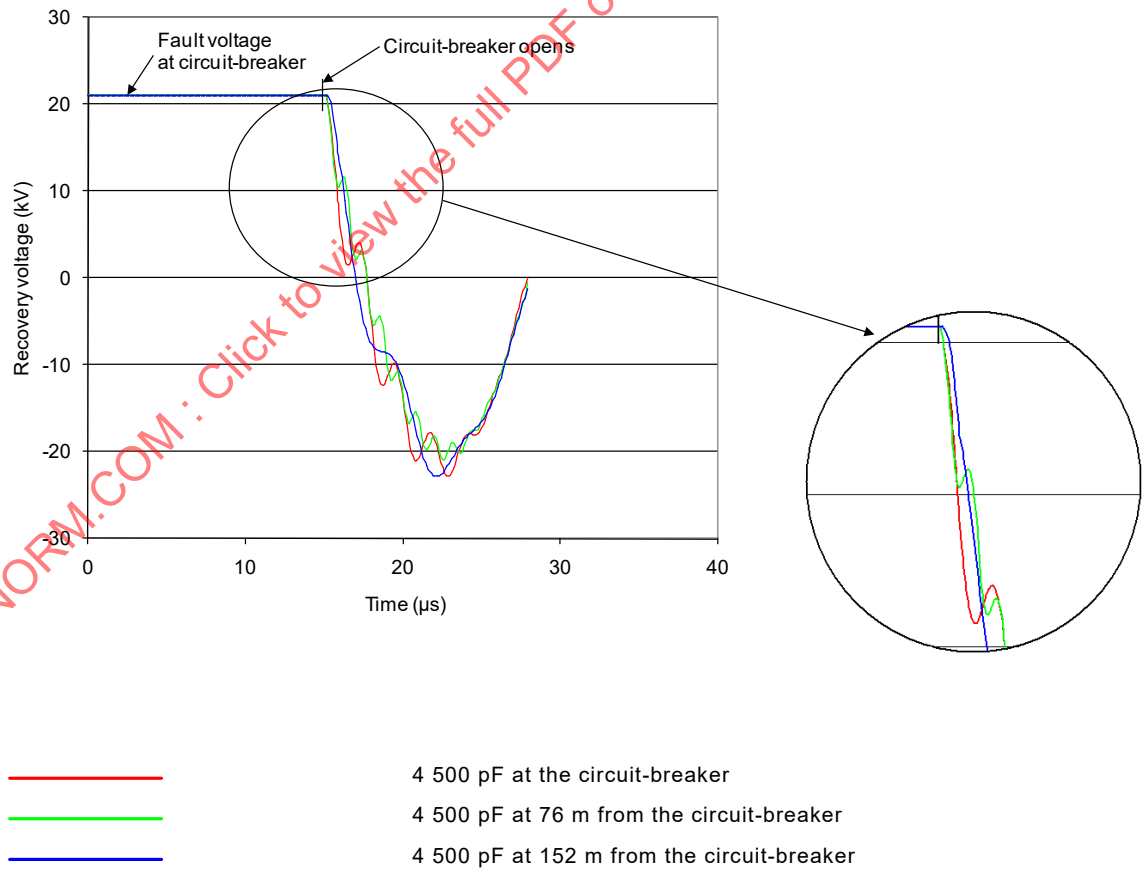


Figure 18 – Effect of capacitor location on short-line fault component of transient recovery voltage with a fault 760 m from circuit-breaker

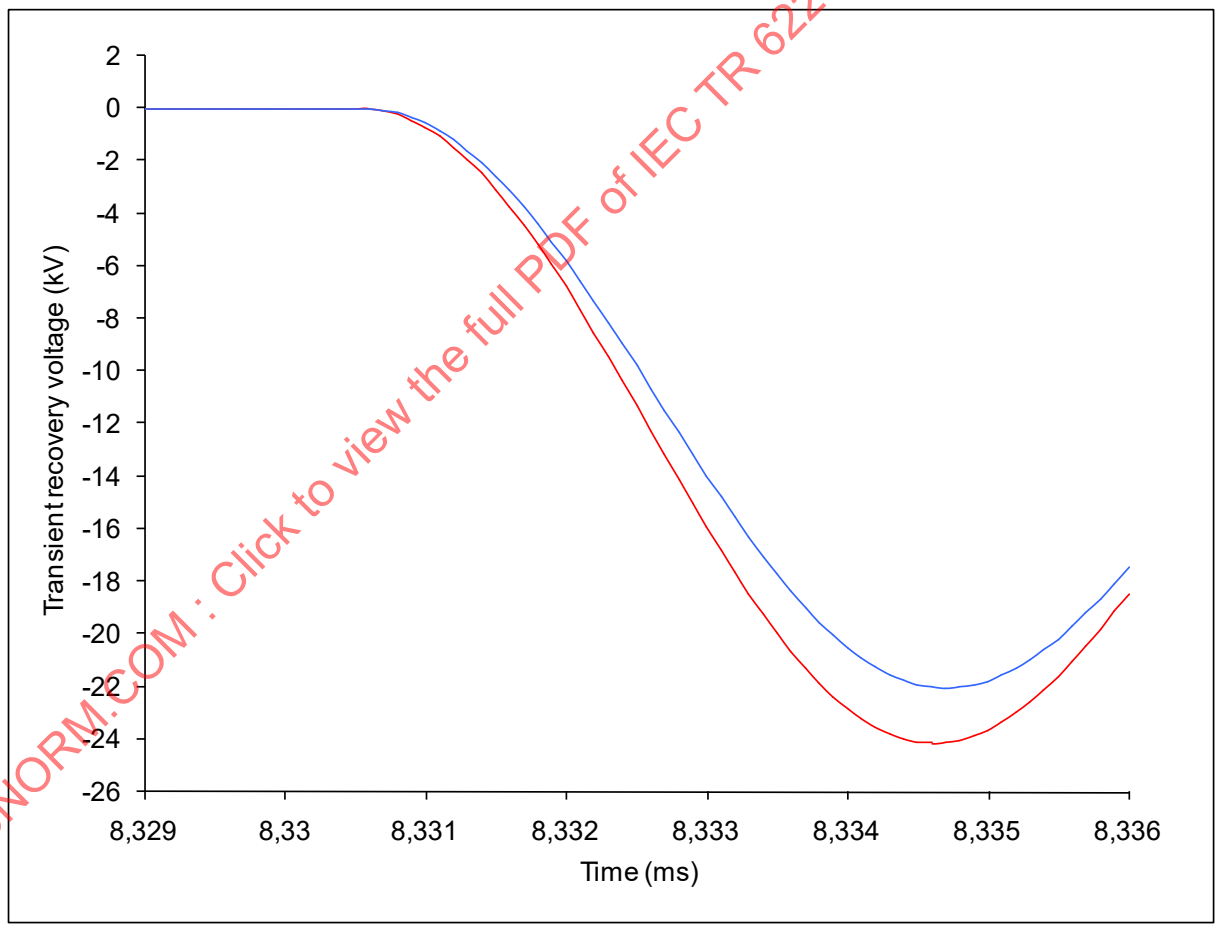
7.3.2.4 Relative influence of phase to earth and parallel capacitors

When circuit-breakers are fitted with capacitors between terminals (grading capacitors for example) the frequency of the line side oscillation is reduced in a similar way as with a phase to earth capacitor, but the effect of a given value of capacitance is different as the TRV is affected on both sides of the circuit-breaker. A lower value of capacitor is needed to obtain a given reduction of the TRV if it is connected between the terminals instead of phase-to-earth.

Figure 19 shows the TRV calculated obtained during a L_{90} test duty on a 145 kV, 50 kA, 60 Hz circuit-breaker with an additional capacitor of 3 nF connected phase-to-earth (curve 1: maximum slope from the instant of interruption = 6,91 kV/μs) or between terminals (curve 2: maximum slope from the instant of interruption = 6,18 kV/μs).

As the effects of parallel (between terminals) or phase-to-earth capacitors are not the same, it is important to indicate in the type test report the position of any additional capacitor. The relevant capacitance is the one measured at the circuit-breaker line side terminal. The capacitance used for measurements is already taken into account in the adjustment of the line side TRV.

It should be noted that the parallel capacitor is part of the circuit-breaker and that the TRV modified by the capacitor does not need to be compensated.



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Key

Red trace	Additional capacitor of 3 nF connected phase-to-earth
Blue trace	Additional capacitor of 3 nF connected between terminals

Figure 19 – TRV obtained during a L_{90} test duty on a 145 kV, 50 kA, 60 Hz circuit-breaker

7.4 Comparison of surge impedances

Table 11 shows a comparison of the typical values of the surge impedances for single-phase fault (or the third pole to clear a three-phase fault) and the first pole to clear a three-phase fault.

Table 11 – Comparison of typical values of surge impedances for a single-phase fault (or third pole to clear a three-phase fault) and the first pole to clear a three-phase fault

U_r (kV)	123		245		420	
Z_1 (Ω)	375	350	365	300	240	235
Z_0 (Ω)	680	655	585	465	450	445
peak factor k (p.u.)	1,55	1,55	1,52	1,43	1,41	1,34
Z single-phase fault (Ω)	476	452	438	355	310	305
Z 1st pole to clear a three-phase fault (Ω)	440	414	416	340	284	279
Z is the surge impedance. Z_1 is the positive sequence surge impedance. Z_0 is the zero sequence surge impedance.						

7.5 Test current and line length tolerances for short-line fault testing

The line reactance corresponding to the standardised line length can be calculated as follows:

$$X_{\text{L, stand}} = \frac{1 - \frac{I_{\text{L, stand}}}{I_{\text{sc}}}}{\frac{I_{\text{L, stand}}}{I_{\text{sc}}}} X_{\text{source}}$$

where

$I_{\text{L,stand}}$ is the short-line fault breaking current corresponding to the standardised line length;

I_{sc} is the rated short-circuit current;

$X_{\text{L,stand}}$ is the line reactance corresponding to the standardised line length;

X_{source} is the reactance corresponding to the rated short-circuit breaking current.

If the reactance of the line applied in practice differs from the reactance corresponding to the standardised line length within the tolerances of –20 % for L_{90} and ±20 % for L_{75} and L_{60}, as stated in 6.109.2 of IEC 62271-100:2008, the related current values can be calculated as follows:

$$I_{\text{L, act}} = \frac{U_r}{\sqrt{3}\left(X_{\text{L, act}} + X_{\text{source}}\right)}$$

where

$I_{\text{L,act}}$ is the short-line fault breaking current corresponding to the actual line length;

$X_{\text{L,act}}$ is the line reactance corresponding to the actual line length.

The actual line length is calculated considering the standardised line length and the percentage deviation of the actual line length from the standardised one:

$$I_{\text{act}} = I_{\text{stand}}\left(1 + \frac{d}{100}\right)$$

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where

l_{stand} is the standardised line length;

l_{act} is the actual line length;

d is the deviation of the actual line length from the standardised line length in percent.

The actual line reactance is calculated using the following equation:

$$X_{L,\,act} = X_{L,\,stand} \times \frac{I_{act}}{I_{stand}} = X_{L,\,stand}\left(1 + \frac{d}{100}\right)$$

The actual percentage short-line fault breaking current $I_{perc,act}$ is determined by the following equation:

$$I_{perc,\,act} = \frac{I_{L,\,act}}{I_{sc}} \times 100 = \frac{I_{perc,\,stand}}{1 + \frac{d}{100}\left(1 - \frac{I_{perc,\,stand}}{100}\right)}$$

In Table 42 the actual percentage short-line fault breaking currents are stated for each standardised short-line fault breaking current $I_{perc,stand}$ taking the maximum tolerances for the line length into account.

Table 42 – Actual percentage short-line fault breaking currents

Standardised short-line fault breaking current $I_{perc,stand}$ %	Deviation of the line length d %	Actual short-line fault breaking current $I_{perc,act}$ %
90	**–20**	**91,8**
90	**0**	**90**
75	**–20**	**78,9**
75	**+20**	**71,4**
60	**–20**	**65,2**
60	**+20**	**55,5**

7.6 TRV with parallel capacitance

The short-line fault TRV from an idealised distributed parameter line is known as a triangular wave shape. In the Laplace domain, this can be written as follows:

$$\mathrm{TRV}(s) = \frac{\omega IZ}{s^2}\left(1 - 2e^{-t_L s}\right) \quad (29)$$

where

t_L is the time to peak without capacitance;

ω is the angular frequency of the breaking current;

I is the breaking current peak;

Z is the surge impedance;

s is the Laplace operator.

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Equation (29) is valid for $0 \le t \le 2t_L$. If the TRV for $t > 2t_L$ is required, Equation (29) should be replaced by the following:

$$\mathrm{TRV}(s) = \frac{\omega IZ}{s^2}(1 - 2\mathrm{e}^{-t_L s} + 2\mathrm{e}^{-2t_L s} + \ldots\ldots) \tag{30}$$

In order to introduce damping of the wave, the term $2\mathrm{e}^{-t_L s}$ in Equation (29) should be replaced by $2k\mathrm{e}^{-t_L s}$, where $k < 1{,}0$.

The TRV can be represented by the product of the breaking (= injection) current and the impedance, also in the Laplace domain. The injection current in the Laplace domain can be approximated such as:

$$\frac{\omega I^2}{s^2} \quad \text{(corresponding to } \omega It \text{ in the time domain)}$$

Then the impedance of the distributed parameter line in Laplace domain is:

$$Z(1 - 2\mathrm{e}^{-t_L s}) \tag{31}$$

The lumped capacitance impedance in the Laplace domain is represented by:

$\frac{1}{Cs}$, where C = capacitance

The capacitance value includes both the lumped capacitance at the circuit-breaker terminal side producing the inherent t_{dL} of the line and the additional capacitance, if any.

Connecting the two impedances represented by Equations (30) and (31) in parallel, the following equation is obtained for the total impedance in the Laplace domain:

$$\frac{Z(1 - 2\mathrm{e}^{-t_L s})}{Cs\left(\frac{1}{Cs} + Z - 2Z\mathrm{e}^{-t_L s}\right)} = \frac{Z(1 - 2\mathrm{e}^{-t_L s})}{(1 + t_{dL} s) - 2t_{dL} s\mathrm{e}^{-t_L s}} \tag{32}$$

where $t_{dL} = ZC$.

t_{dL} is applicable also for conditions with parallel additional capacitances.

The product of the injection current ($\omega I/s^2$) and the impedance Equation (32) is the TRV with parallel capacitance in the Laplace domain:

$$\omega IZ \times \frac{1}{s^2} \times \frac{(1 - 2\mathrm{e}^{-t_L s})}{(1 + t_{dL} s) - 2t_{dL} s\mathrm{e}^{-t_L s}}$$

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$$= \omega IZ\left[\frac{1}{s^2}\times\frac{1}{1+t_{dL}s}-\frac{1}{s^2}\cdot\frac{2e^{-t_L s}}{(1+t_{dL}s)^2}+\ldots\ldots\ldots\right]$$

$$= \omega IZ\left[\frac{1}{s^2}-\frac{t_{dL}}{s}+\frac{t_{dL}^2}{1+t_{dL}s}-2e^{-t_L s}\left(\frac{1}{s^2}-\frac{2t_{dL}}{s}+\frac{2t_{dL}^2}{1+t_{dL}s}+\frac{t_{dL}^2}{(1+t_{dL}s)^2}\right)\right] \quad (33)$$

The second line of Equation (33) is valid for $t_L \le t \le 2t_L$ only.

By inverse Laplace transformation, SLF TRV with parallel capacitance in time domain is calculated as follows:

$0 \le t \le t_L$:

$$TRV_1(t) = \omega IZ\left[t + t_{dL}\left(e^{-\frac{t}{t_{dL}}}-1\right)\right] \quad (34)$$

$t_L \le t \le 2t_L$

$$TRV_2(t) = TRV_1(t) - 2\omega IZ\left[t'\left(e^{-\frac{t'}{t_{dL}}}+1\right)+2t_{dL}\left(e^{-\frac{t'}{t_{dL}}}-1\right)\right] \quad (35)$$

with $t' = t - t_L$.

Using equations (34) and (35), the correct waveshapes of SLF TRVs with line inherent t_{dL} and for conditions with additional parallel capacitance can be calculated.

For cases $t > 2t_L$, Equation (30) instead of Equation (29) should be applied. When damping is introduced, $2ke^{-t_L s}$ should be used instead of $2e^{-t_L s}$ in Equation (29) as mentioned before. The total calculation process is then slightly modified.

For every case, with or without parallel capacitance, the peak value of the TRV is quasi equal to ωIZt_L. Dividing Equations (34) and (35) by ωIZt_L, gives the following equations.

$$TRV(10) = \frac{t_{dL}}{t_L}\left[\frac{t}{t_{dL}}+\left(e^{-\frac{t}{t_{dL}}}-1\right)\right] \quad (36)$$

$$TRV(20) = TRV(10) - \frac{2t_{dL}}{t_L}\left[\frac{t'}{t_{dL}}\left(e^{\frac{-t'}{t_{dL}}}+1\right)+2\left(e^{\frac{-t'}{t_{dL}}}-1\right)\right] \quad (37)$$

The TRV wave shape given by Equations (36) and (37) can be normalised such that the peak value is unity and time unit is in t_{dL}. The parameter is t_L/t_{dL}.

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Figure 20 shows the results of a calculation for t_L/t_{dL} = 4,0. Multiplying the Y-axis value by ωIZt_L and X-axis value by t_{dL}, the actual wave shape is obtained.

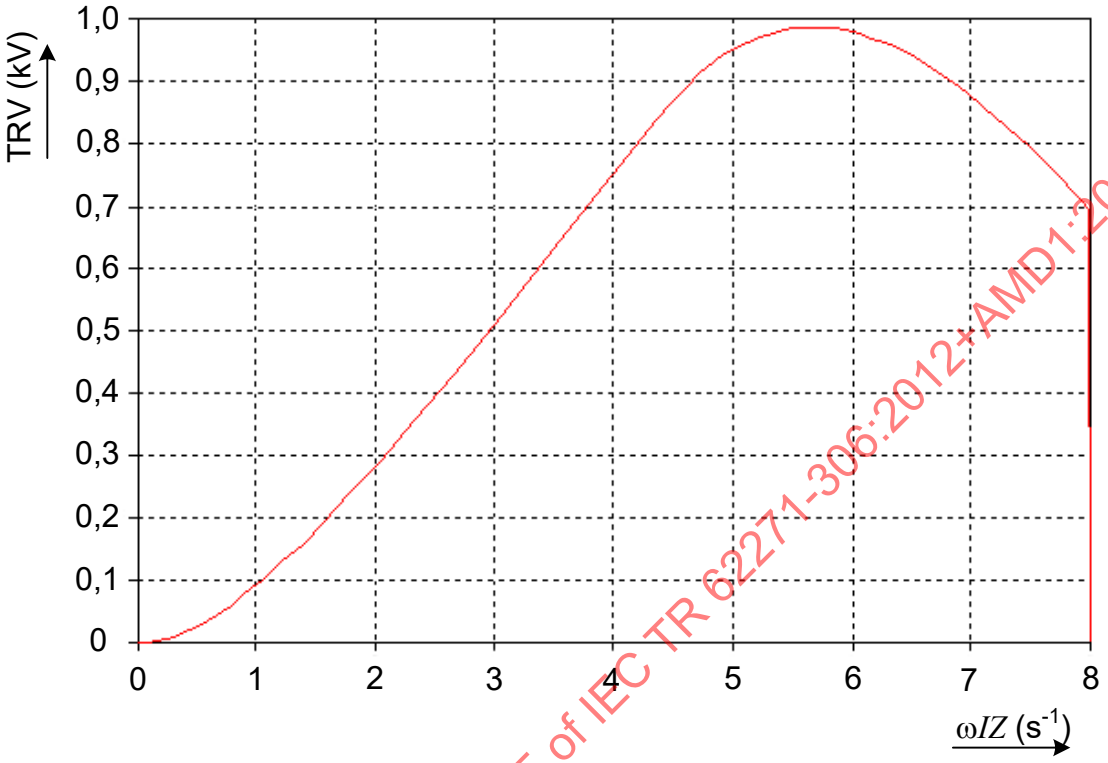

Figure 20 – TRV vs. ωIZ as function of t/t_{dL} when t_L/t_{dL} = 4,0

8 Out-of-phase switching

8.1 Reference system conditions

8.1.1 General

Although the out-of-phase switching condition is a rare occurrence, two cases are considered to illustrate the background to the standard requirements of IEC 62271-100.

Case A Instability of a system in service, due to overloading, load rejection, or other major disturbance such as that caused during a severe storm, etc.;

Case B Erroneous switching operation during synchronizing.

8.1.2 Case A

The system conditions illustrated above are often considered in power system stability studies. In such events, as the parts of the system separate the out-of-phase occurs across an impedance in a system, where it can be assumed a heavy load current exists. Out-of-phase breaking is initiated by a protective system detecting the voltage phase angle difference across the impedance and sending a tripping signal to the associated circuit-breakers. The first to open of these will experience the out-of-phase condition. Studies indicate that during such disturbances, the phase angles of the individual generators scatter so that it is unlikely that the two sections will have a simple, uniform phase angle between them. Also, a densely connected part of a system can rarely be separated to be out-of-phase with the rest of the system.

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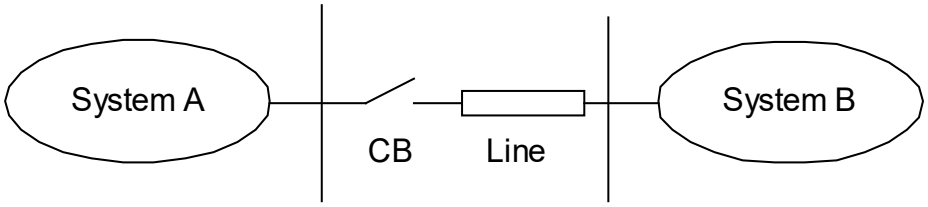

Figure 21 – Typical system configuration for out-of-phase breaking for case A

Figure 21 is a representation of a separating system where a line is the link between the two separate parts, i.e. system A and system B. The connecting line (or impedance such as a transformer) exists in between. Each of system A and B is considered to be corresponding to a system operating at its T30 to T60 short-circuit level.

Cases where the short-circuit power of both systems A and B correspond to T100 can be considered exceptional.

Cases with a weak sub-system on one side can be considered covered by case B with regard to TRV parameters.

8.1.3 Case B

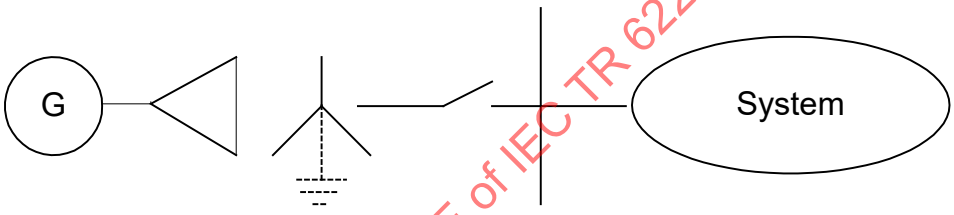

Figure 22 – Typical system configuration for out-of-phase breaking for Case B

Synchronizing between relatively strong systems can be considered a rare case and is covered by case A with regard to TRVs.

A more typical system layout for synchronizing is shown in Figure 22, where a generator interfaces with a system via a step up transformer. The right-hand side system short-circuit power can be considered to be corresponding to a T60 level. In such systems, a synchronizing operation is mostly performed at the high-voltage side of the step-up transformer. Typical characteristics are:

– generator sub-transient reactance is 0,3 p.u.;
– step-up transformer reactance is 0,1 p.u.

Present day maximum ratings of generator units are in the order of 600 MVA and 1 300 MVA for 245 kV and 550 kV, respectively. Introducing, also, the short-circuit reactance of the system, the out-of-phase breaking current (generator-side short-circuit current on the high-voltage side) is 0,5 kA up to 8 kA for most common applications.

The following points are also to be considered:

– due to the connection of the transformer windings, i.e., Δ on the LV side and Y on the HV side, for solidly earthed systems, the zero sequence reactance of the generator side is far lower than that of positive sequence, i.e. ca. 25 %. Therefore the pole-to-clear factor is maximum for the 3rd pole, and is 1,0;
– the recovery voltage of the generator after the fault current has been cleared is heavily damped, giving a damping factor in the order of 0,8;

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– statistically a 180 degree out-of-phase condition very rarely occurs in practice and an additional factor of 0,8 can be introduced.

8.2 TRV parameters introduced into Tables 1b and 1c of the first edition of IEC 62271-100

8.2.1 General

As rated TRV parameters in tables 1b, 1c and 1d of the first edition of IEC 62271-100 published in 2001, system requirements and experiences based on circuit-breaker characteristics and other duties, i.e. terminal faults, etc., are to be considered.

8.2.2 Case A

8.2.2.1 Breaking current

The breaking current listed is 25 % of the rated short-circuit breaking current.

As shown before, actual out-of-phase occurs between the portions of a system via a certain impedance. As already noted, it is unlikely that a perfect 180 degree of out-of-phase will ever occur. The value 25 % is taken to cover the majority of cases.

8.2.2.2 First-pole-to-clear factor

A first-pole-to-clear factor of 2,0/2,5 is specified by IEC 62271-100 for effectively/non-effectively earthed systems, respectively.

The theoretical maximum values are 2,6/3,0, but stability studies have shown that the phase angles of the individual generators are scattered. This fact has been taken into account by introducing a factor of 0,8. Furthermore, the majority of today's effectively earthed systems have a first-pole-to-clear factor of 1,15 at the most. Therefore, the values of 2,0/2,5 are considered to be conservative.

8.2.2.3 Amplitude factor

An amplitude factor of 1,25 is specified by IEC 62271-100.

The theoretical maximum value can be 1,4. However, due to the statistical displacement between the timings of the TRV peaks of the two parts of the system, a factor of 0,7 is introduced to cover the effect of the two randomly over-swinging parts, i.e.:

$$(2 + 2 \times 0{,}4 \times 0{,}7)/2 = 1{,}28$$

Considering the higher value of the first-pole-to-clear factor, the value 1,25 is appropriate.

8.2.2.4 RRRV

The rate-of-rise of recovery voltage is specified by IEC 62271-100 as 1,54 kV/μs or 1,67 kV/μs depending on the earthing conditions.

$u_1 = 0{,}75 \times (\sqrt{2}/\sqrt{3}) \times U_r \times k_{pp}$

– The value depends on the system layout and is common to other breaking duties, i.e. T100, T60, etc.

– The factor 0,75 was agreed between IEC SC 17A and the IEEE PES Switchgear Committee as a harmonised value.

$t_1 = u_1/\text{RRRV}$;

$u_c = (\sqrt{2}/\sqrt{3}) \times U_r \times$(first-pole-to-clear factor)$\times$(amplitude factor);

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The t_2 value mainly depends on the system scale and is to be common to the other duties, i.e. T100, T60, etc. The value specified for T100 is satisfactory as system requirement. Laboratory experience shows that the t_2 value introduces no significant influence on circuit-breaker performance.

Like the RRRV condition above, the case of direct connection to a line can be excluded for t_d values. The value of t_d also depends on the system layout and, based on experience, the T60 time delay can be applied as rated value with no detriment.

8.2.3 Case B

Simulation calculations have been performed and the results are shown in, Figure 23, Figure 24 and Figure 25. In this study a 1 500 MVA synchronous generator (at present the highest capacity available) is connected to a 550 kV system through a step-up transformer. The 550 kV system has a short-circuit current of 30 kA. The generator parameters used here are the actual parameters as supplied by the manufacturer:

– sub-transient reactance ca. 0,3 p.u.
– transformer short-circuit reactance ca. 0,1 p.u.

The following conditions apply:

– two parameter TRV waveshape;
– generator/transformer side contribution is predominant for the TRV across the circuit-breaker terminals due to higher voltage drop in these reactances;
– due to the step-up transformer winding connections (Δ/Y on the generator side/HV side, respectively), the positive sequence reactance is four times the zero sequence reactance. Hence the third-pole-to-clear sees a maximum TRV of 1,0 p.u. (as for a solidly earthed system);
– the generator side recovery voltage just after current interruption shows significant damping (in the order of 0,7 – 0,8) and then gradually recovers to the original value;
– due to the statistically rare occurrence of a full 180 degrees out-of-phase condition a factor of 0,8 is applied to the first-pole-to-clear factor, which, corresponds to an out-of-phase condition of up to 115 degrees depending on the neutral earthing conditions.

Based on these assumptions, for effectively earthed neutral systems, TRV parameters are well covered by those of T10. Specifying TRVs for case B is not necessary.

For non-effectively earthed neutral systems, u_c is higher than that of T10, but not higher than for case A. In actual systems of the voltage class applying non-solidly earthed neutral, it is necessary to consider the multi-frequency TRV wave shapes, and the voltage drop portion in the generator/transformer reactance, etc. Hence lower u_c and/or RRRV are probable. Based on that TRV ratings for case B are not considered necessary.

8.2.4 TRV parameters for out-of-phase testing

As mentioned before and from laboratory experience, t_2, t_d and t' values are viewed as less dominant on out-of-phase breaking phenomena provided the other test duties (T10 to T100, SLF, etc.) are performed. For rating purposes, the t_2 value is that of T100s as specified in Tables 1a, 1b, 1c and 1d of the first edition of IEC 62271-100. However, for convenience of testing and since the influence of t_2 is not considered critical, the testing values given in Tables 14a and 14b of the first edition of IEC 62271-100 extend this value up to two times that for T100s.

System requirement basis is considered appropriate.

t_d, t' Lowest side values as used for T60

Again the system basis is used.

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Figure 23, Figure 24 and Figure 25 represent a typical simulation result for a case B study.

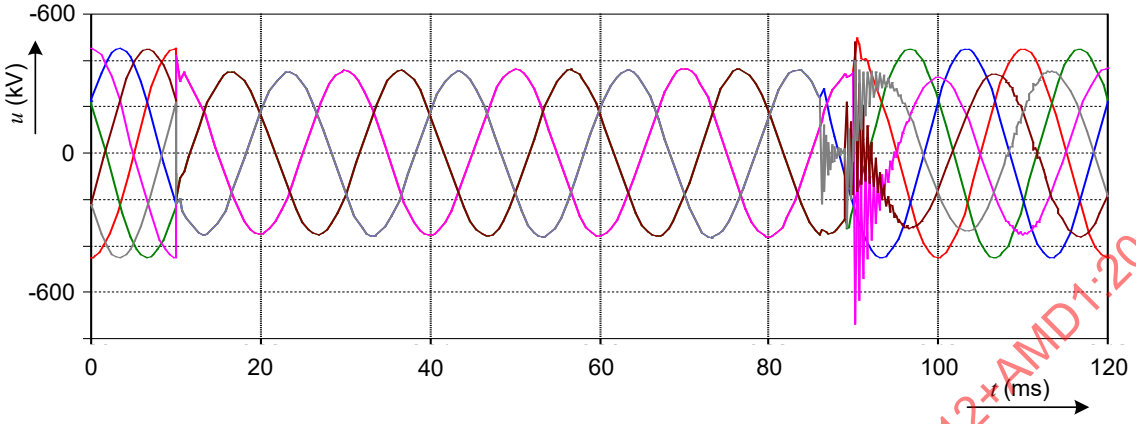

Figure 23 – Voltage on both sides during CO under out-of-phase conditions

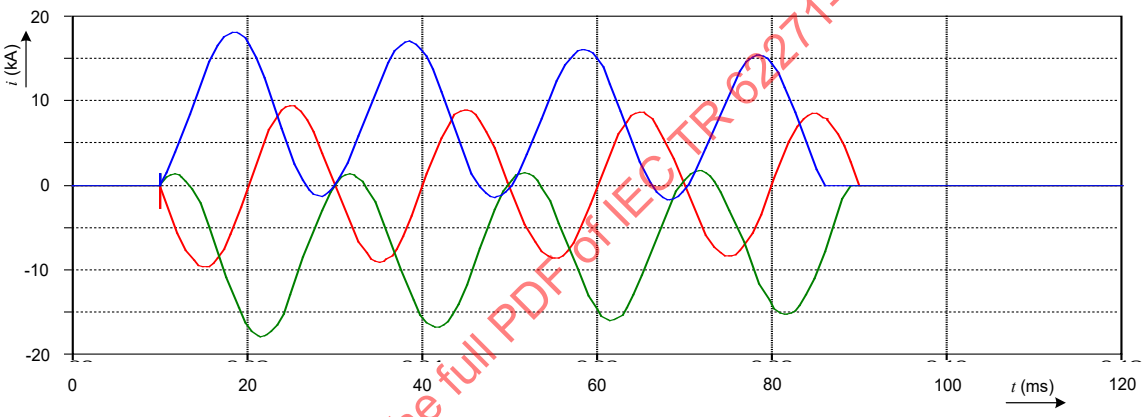

Figure 24 – Fault currents during CO under out-of-phase

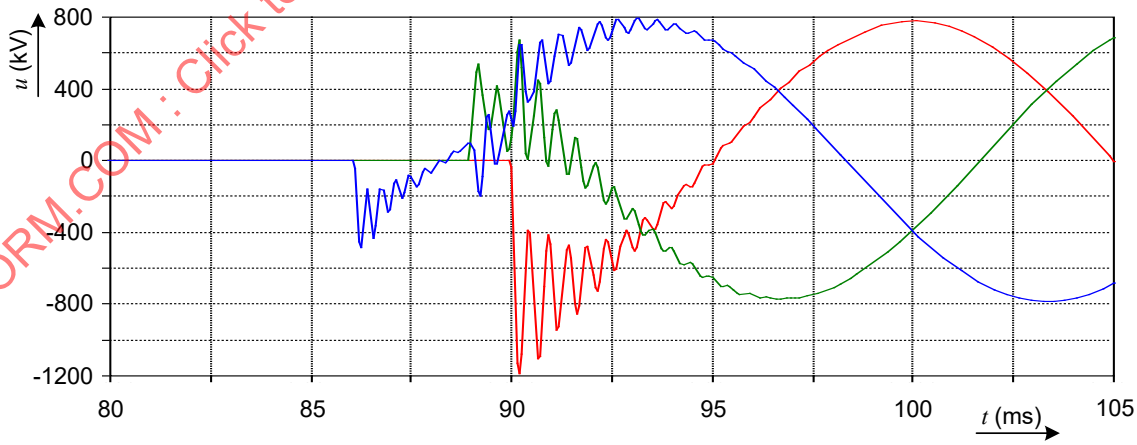

Figure 25 – TRVs for out-of-phase clearing (enlarged)

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9 Switching of capacitive currents

9.1 General

Preferred values for capacitive current switching are given in Table 9 of IEC 62271-100:2008. The values include both de-energisation and energisation of capacitive loads as follows:

– shunt capacitor banks in single and parallel configurations;

– no-load cables in single and parallel configurations;

– no-load transmission lines.

The values given in Table 9 of IEC 62271-100:2008 for inrush current peak and frequency are not linked to the back-to-back capacitor bank breaking current.

Capacitive currents are typically in the order of up to a few hundred amperes and interruption is generally considered a light duty for a circuit-breaker. However, restriking is an issue since it may lead to undesirable overvoltages or high-frequency transients affecting power quality and also may cause damage to the interrupting unit or units. Circuit-breakers are therefore rated according to their restriking probability, i.e. restrike performance class C1 or C2 as discussed in 3.3.

Energisation of capacitive loads is usually associated with transient voltages and currents. Those transients are the following:

– inrush currents;

– overvoltages caused by the system response to the voltage dip when energizing capacitor banks;

– overvoltages caused by travelling waves on transmission lines and cables.

These transients also present power quality issues and some form of mitigation may be necessary as discussed later. IEC 62271-100 contains preferred values of inrush current magnitude and frequency, namely 20 kA peak and 4 250 Hz.

Type testing is designed to be representative of the service conditions up to the point of either clearing, reigniting or restriking. Because the actual value of overvoltage and transient response is totally system-dependent, tests cannot replicate these effects. By providing a means of assessing the likelihood of restrike occurrence, the user can determine what best suits their application. It is assumed that since capacitor switching is not the only source of overvoltage, other protection systems are employed and in the case of unacceptable power quality for sensitive electronic equipment, a sufficiently low number of likely events are selected. A separate study of actions relative to power quality on energisation should also be made.

In the selection of the rating for the circuit-breaker for capacitive current switching, the following needs to be considered:

a) application, i.e. capacitor bank (single or back-to-back), cable or transmission line;

b) power frequency of the network;

c) earthing situation of the network;

d) neutral earthing of the capacitor bank, i.e. solidly earthed or isolated;

e) presence of single or two phase-to-earth faults.

Based on the application, the required restrike performance class of the circuit-breaker can be chosen (C1 or C2) and also the mechanical endurance class (M1 or M2). Network earthing, presence of single and two phase-to-earth faults are important factors that determine the recovery voltage across the circuit-breaker, which, in turn, determines the test voltage of the circuit-breaker.

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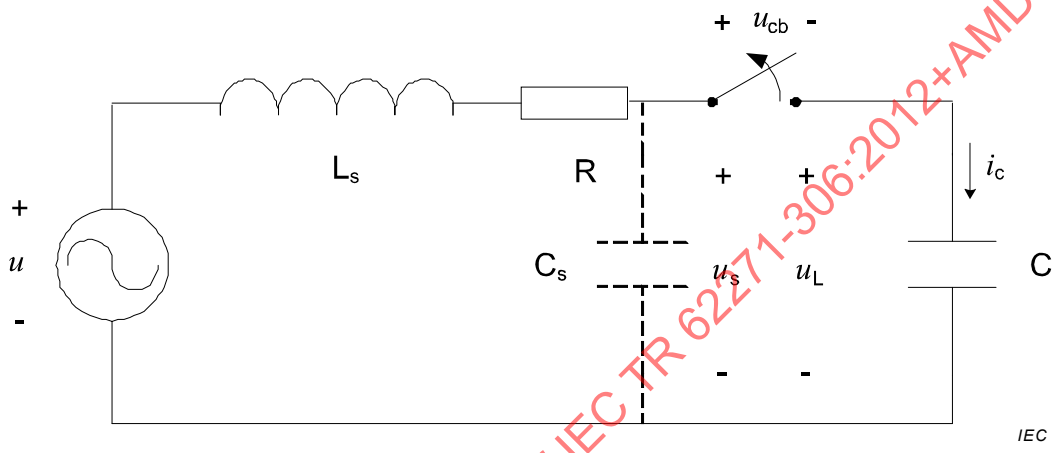
In 9.2, the general theory of capacitive current switching is given as well as the application and testing considerations.

9.2 General theory of capacitive current switching

9.2.1 De-energisation of a capacitive load

9.2.1.1 General

The single-phase equivalent circuit shown in Figure 98 may be used to illustrate the conditions when de-energising a capacitive load. The capacitive load is in this case represented by a concentrated capacitor.



Key

u	Source voltage (r.m.s.)	u_{cb}	Voltage across the circuit-breaker (r.m.s.)
L_s	Source inductance	u_L	Voltage across the capacitive load (r.m.s.)
R	Resistor representing the losses in the circuit	i_c	Capacitive current (r.m.s.)
C_s	Source side capacitance (stray capacitance)	C	Capacitive load (capacitor bank, transmission line or cable)
u_s	Source side voltage (r.m.s.)		

Figure 98 – Single-phase equivalent circuit for capacitive current interruption

9.2.1.2 Capacitive current

The capacitive current i_c flowing in the circuit is given by Equation (147):

$$i_c = \frac{\omega_s C \times u}{1 - \omega_s^2 L_s C} = \frac{\omega_s C \times u}{1 - \frac{\omega_s^2}{\omega_l^2}} \quad (147)$$

where

C is the capacitance of capacitor bank C (F).

$$\omega_s = 2\pi f_s ,$$

where

f_s is the system frequency (Hz).

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$$\omega_i = \frac{1}{\sqrt{L_s C}} = 2\pi f_i \ ,$$

where

f_i is the inrush current frequency in Hz (see also 9.2.3);

L_s is the inductance of the source inductance L_s (H).

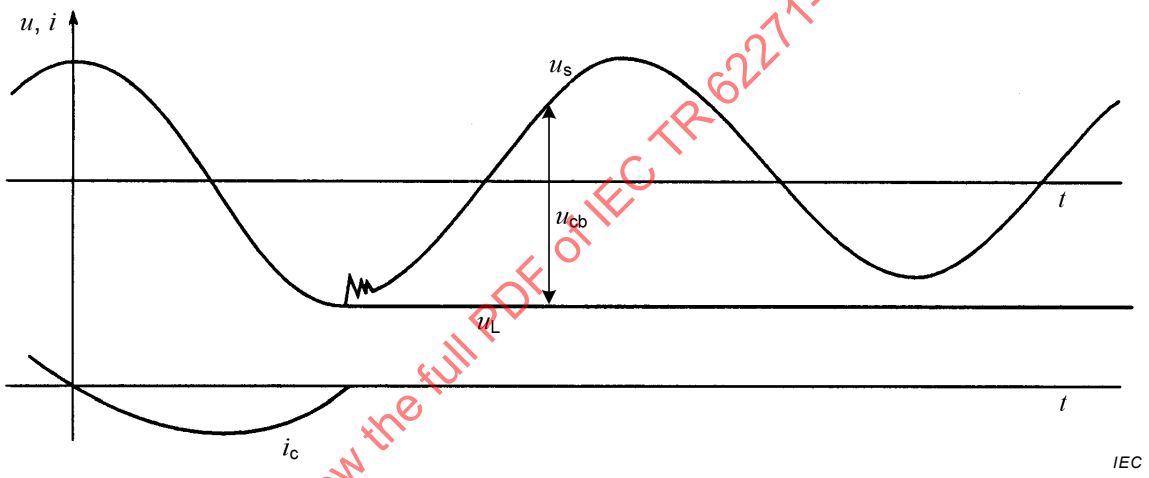
With $\omega_i >> \omega_s$, Equation (147) transforms to $i_c = \omega_s C \times u$.

In the determination of the power frequency capacitive current the influence of the resistance R is usually negligible and is ignored in Equation (147).

9.2.1.3 Recovery voltage

9.2.1.3.1 Recovery voltage in a single-phase circuit

Figure 99 shows the current and voltage shapes at interruption.



Key

i_c	Capacitive current
u_L	Voltage on the load side of the circuit-breaker
u_{cb}	Voltage across the circuit-breaker
u_s	Voltage on the source side of the circuit-breaker

Figure 99 – Voltage and current shapes at capacitive current interruption

After interruption of the current, the supply side voltage u_s will be more or less unaffected. There is only a minor decrease in amplitude, associated with the removal of the capacitive load. The transition to the new amplitude value is associated with a slight oscillation, the frequency of which is determined by L_s and C_s.

The interruption of the current leaves a trapped charge on the capacitor bank. The voltage u_L will remain constant at the value it had at current zero (namely the peak value of the supply voltage).

Together with the low-current amplitude to be interrupted, the low initial rate-of-rise of the recovery voltage makes it relatively easy for the circuit-breaker to interrupt. Some circuit-breakers may interrupt even if the current zero occurs immediately after contact separation. Half a cycle after current zero, the recovery voltage increases to an amplitude of twice the

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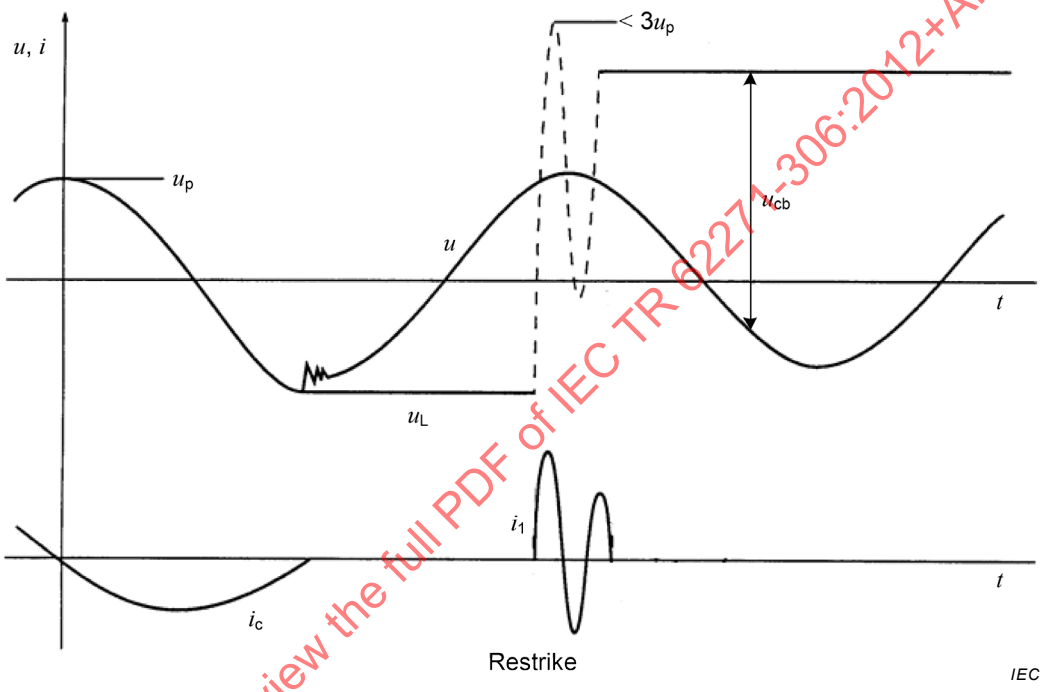
peak value of the supply voltage. Consequently, a rated frequency of 60 Hz is more severe than 50 Hz. The circuit-breaker may then not be able to withstand the high value of the recovery voltage across a relatively small contact gap. Dielectric breakdown may occur between the contacts and the current is re-established between the contacts.

Figure 100 shows current and voltage wave shapes in a case where voltage breakdown occurs relatively close to the recovery voltage peak. The load side voltage will swing up to a voltage that ideally (without damping present) reaches three times the supply voltage peak u_p. The oscillation frequency of the current and voltage after the breakdown is determined by L_s and C (assuming $C >> C_s$). The circuit-breaker may interrupt the oscillatory current at one of its current zeros, with the result that the voltage across the capacitor may attain a new constant value, perhaps higher than before. Further breakdowns associated with even higher overvoltages across the load may then occur (Figure 101).



Key

u_p	Peak of the source voltage
i_c	Power frequency capacitive current
i_1	Restrike current through the circuit-breaker
u_L	Voltage on the load side of the circuit-breaker
u_{cb}	Voltage across the circuit-breaker

Figure 100 – Voltage and current wave shapes in the case of a restrike

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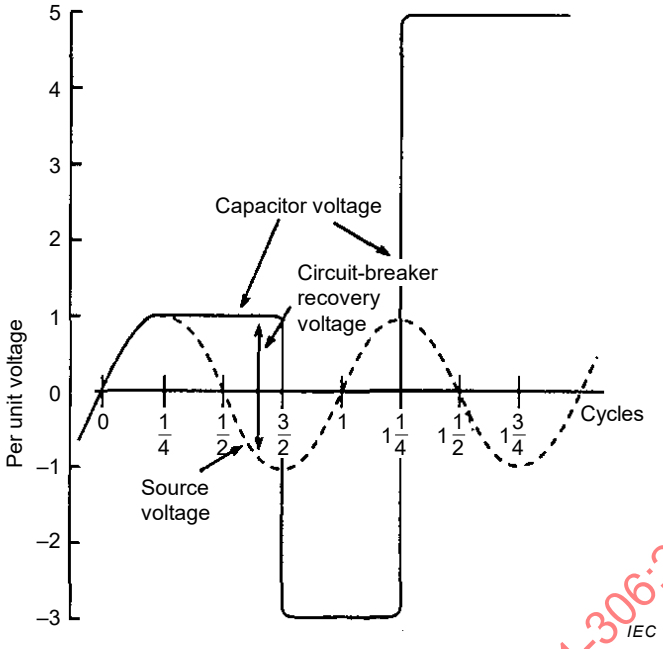

Key

1 p.u. is the peak value of the phase-to-earth voltage

Figure 101 – Voltage build-up by successive restrikes

Voltage breakdowns at capacitive current interruption are divided into two categories:

1) Re-ignitions: Voltage breakdown during the first 1/4 cycle following current interruption.
2) Restrikes: Voltage breakdown 1/4 of a cycle or more following current interruption.

The definitions of re-ignition and restrike are valid only when the recovery voltage has a 1-cosine frequency waveshape.

Restrikes will lead to overvoltages across the capacitive load (maximum 3 p.u. for a single restrike, where 1 p.u. is the peak value of the phase-to-earth voltage) while re-ignitions will not produce any overvoltages (theoretically maximum 1 p.u.). Re-ignitions are acceptable but may cause power quality problems.

In reality, there are no restrike-free circuit-breakers. It would take an infinite number of test shots to verify this. For this reason, the concept of restrike performance was introduced in IEC 62271-100.

Another phenomenon, which has been observed predominantly on vacuum circuit-breakers, may occur during three-phase capacitive current and short-circuit breaking current tests, but also at lower currents and voltages. This phenomenon is known as a *non-sustained disruptive discharge* (NSDD).

An NSDD is defined as a disruptive discharge associated with current interruption that does not result in the resumption of power frequency current or, in the case of capacitive current interruption does not result in current at the natural frequency of the circuit. An NSDD is considered as a late local breakdown across the interrupter and leads to a resumption of high-frequency current. The high-frequency oscillation is determined by stray capacitance and inductance locally across the interrupter. An example of an NSDD is given in Figure 102.

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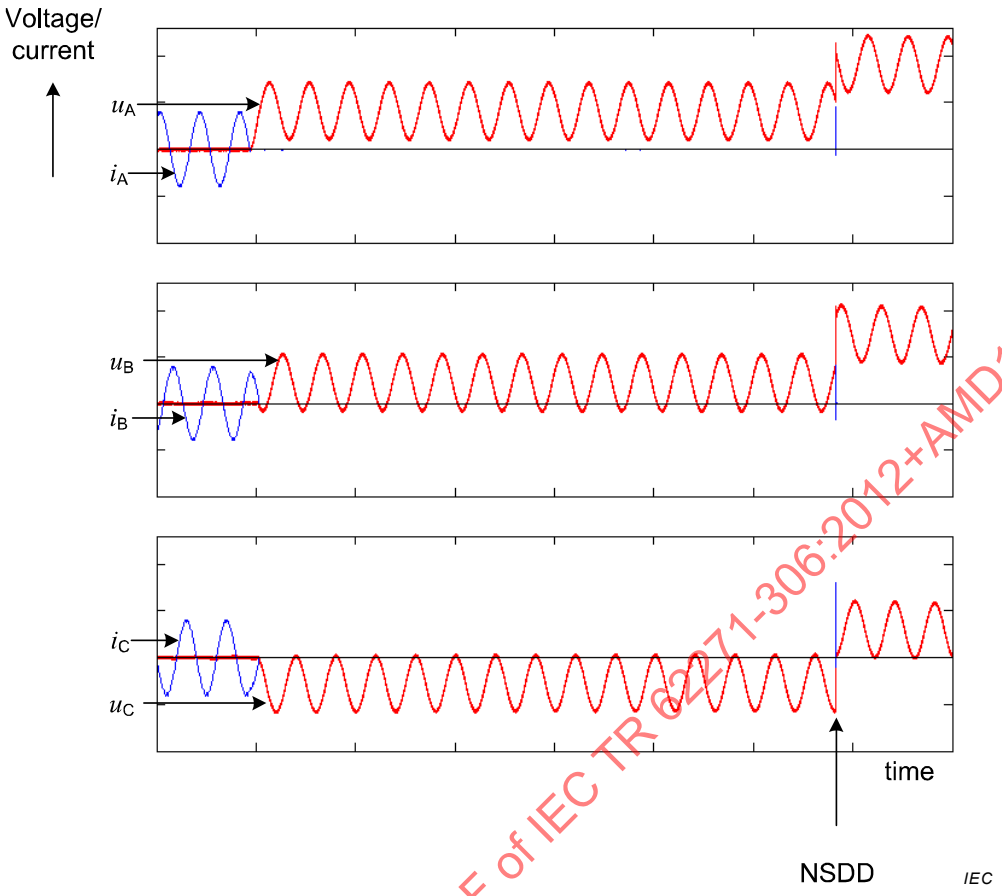

Key

i_A, i_B, i_C	Currents in phase A, B and C, respectively
u_A, u_B, u_C	Voltages across the contacts of phase A, B and C, respectively

Figure 102 – Example of an NSDD during capacitive current interruption

9.2.1.3.2 Recovery voltage in a three-phase circuit

The recovery voltages in three-phase circuits are more complicated than in the single-phase case. Figure 103 shows as an example the recovery voltage of the first-pole-to-clear in a case with a non-effectively earthed capacitive load. Due to the neutral shift, the recovery voltage initially has a shape that will lead to a peak value equal to three times the supply voltage peak (dotted line). The neutral shift is then 1,0 p.u. When the two last poles interrupt 90 electrical degrees after the first, there is however, a discontinuity in the slope (the neutral shift remains at 0,5 p.u.) and the final peak value for the first-pole-to-clear is 2,5 times the supply voltage peak (see also 9.6).

NOTE The recovery voltage peak of a circuit-breaker having a non-simultaneity between poles of more than ¼ cycle will be 3 times the supply voltage peak.

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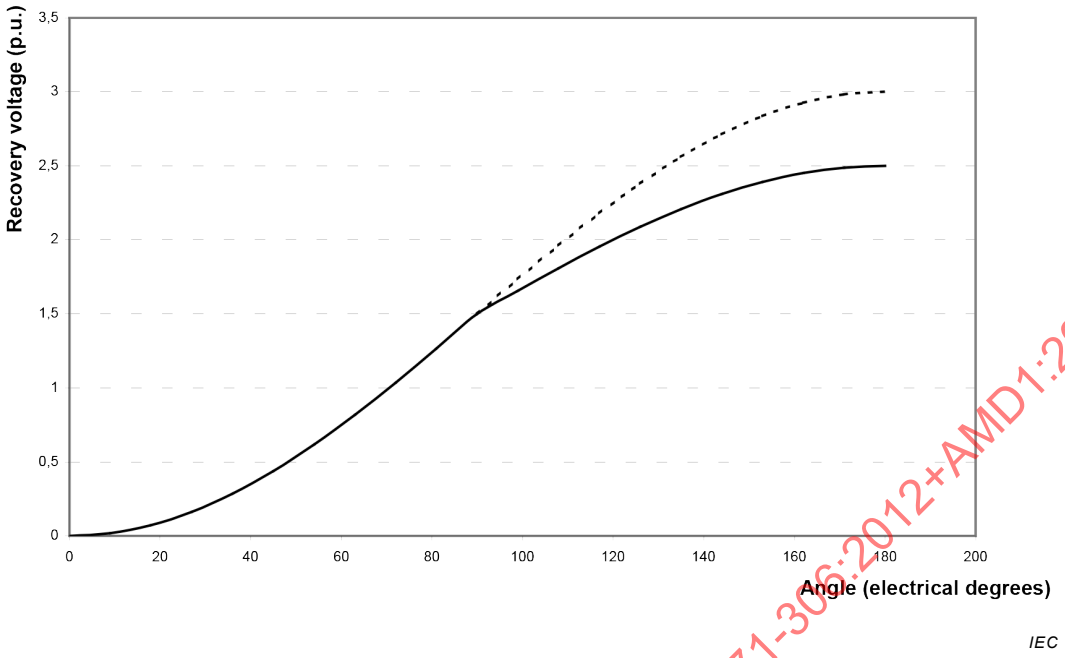

Figure 103 – Recovery voltage of the first-pole-to-clear at interruption of a three-phase non-effectively earthed capacitive load

9.2.2 Energisation of a capacitive load

With reference to Figure 98, L_s, R and C form a series RLC circuit. Applying a voltage u to such a circuit, the inrush current i can be calculated in general as follows:

$$u = Ri + L_s \frac{di}{dt} + \frac{q}{C}$$

Differentiating and treating u as a step voltage, i.e. energisation at the instant of the voltage peak:

$$\frac{d^2i}{dt^2} + \frac{R}{L_s}\frac{di}{dt} + \frac{1}{L_sC}i = 0 \qquad (148)$$

Equation (148) is a second order linear homogenous differential equation with three possible solutions depending on the degree of damping in the circuit. Taking $\alpha = R/2L_s$ and $\omega_0 = 1/\sqrt{L_sC}$, the three solutions are:

1) Overdamped $\alpha^2 > \omega_0^2$

$$i(t) = \frac{u}{L_s\sqrt{\alpha^2 - \omega_0^2}} e^{-\alpha t} \sinh\sqrt{\alpha^2 - \omega_0^2}\, t \qquad (149)$$

2) Critically damped $\alpha^2 = \omega_0^2$

$$i(t) = \frac{u}{L_s} te^{-\alpha t} \qquad (150)$$

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3) Underdamped $\omega_0^2 > \alpha^2$

$$i(t) = \frac{u}{L_s\sqrt{\omega_0^2 - \alpha^2}} e^{-\alpha t} \sin\sqrt{\omega_0^2 - \alpha^2}\, t \tag{151}$$

The resistance value R_{cd} that results in critical damping is given by:

$$R_{cd} = 2\sqrt{\frac{L_s}{C}} \tag{152}$$

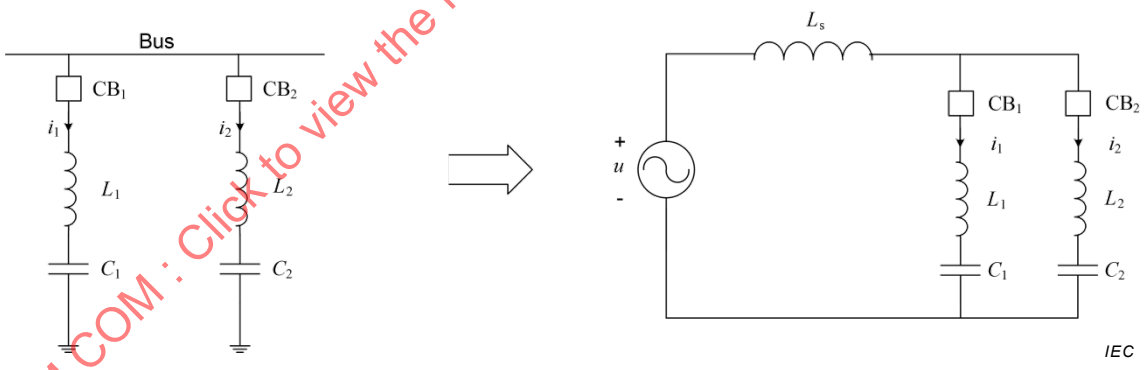
In most cases, the inrush current oscillation is underdamped and Equation (151) is of most interest. If closing resistors are applied to limit the inrush current, then Equation (149) or (150) may be applicable.

9.3 Capacitor bank switching

9.3.1 General

Since the use of capacitor banks for compensation purposes is increasing, it is common that more than one capacitor bank is connected to the same bus (back-to-back capacitor bank switching). This has no influence on the conditions at interruption. The current at closing, however, is affected to a high degree.

To describe the phenomena associated with capacitor bank switching, a general single-phase equivalent circuit is shown in Figure 104 showing a single-line diagram of the case where two capacitor banks (C_1 and C_2) are connected in back-to-back to a busbar. L_1 and L_2 represent the stray inductance (or stray inductance plus additional damping inductance). The inductance L_s of the source network will be several orders of magnitude higher than that of L_1 or L_2.



Key

CB_1	circuit breaker considered
CB_2	circuit breaker, open for single capacitor bank switching by CB_1, closed for back-to-back capacitor bank switching by CB_1
L_s	source inductance
L_1, L_2	inductance between capacitor bank 1 and 2 and bus, respectively
C_1, C_2	capacitor bank 1 and 2
i_1, i_2	capacitive currents
u	source voltage

Figure 104 – General circuit for capacitor bank switching

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Single capacitor bank switching occurs when C_1 is switched and C_2 is not connected in the circuit described in Figure 104. The circuit consists then of the source inductance L_s in series with the capacitor bank C_1. The inductance L_1 can be disregarded here, since the value of the source inductance L_s>>L_1.

Back-to-back capacitor bank switching occurs when switching C_1, with C_2 being in service, or vice versa.

The conditions for single and back-to-back capacitor bank switching are given in 9.3.3.1 and 9.3.3.2. In some cases, energised capacitor banks in nearby substations may contribute to the inrush current such that a back-to-back situation occurs.

Especially, the second case may give rise to an inrush current of very high amplitude and frequency, which may have to be limited in order not to be harmful to the circuit-breaker, the capacitor banks and/or the network. The magnitude and frequency of this inrush current is a function of the following:

a) applied voltage (point on the voltage wave at closing); the magnitude will be maximum on closing at the voltage peak;

b) capacitance of the circuit;

c) inductance in the circuit (amount and location);

d) any charge on the capacitor bank at the instant of closing;

e) any damping of the circuit due to closing resistors or other resistances in the circuit.

It is assumed that the capacitor bank is discharged prior to energisation. This is a reasonable assumption, as capacitor units are fitted with discharging resistors that will discharge the capacitor bank. Typical discharge times are in the order of 5 min.

The transient inrush current to a single bank is less than the available short-circuit current at the capacitor bank terminals. It rarely exceeds 20 times the rated current of the capacitor bank at a frequency that approaches 1 kHz. Since a circuit-breaker shall meet the making current requirements of the system, transient inrush current is not a limiting factor in single capacitor bank applications. For this reason making tests with inrush current are not required for single-capacitor bank switching.

When capacitor banks are switched back-to-back, transient currents of prospective high magnitude and with a high natural frequency may flow between the banks on closing of the circuit-breaker. The effects are similar to that of a restrike on opening. This oscillatory current is limited only by the impedance of the capacitor bank and the circuit between the energised bank or banks and the switched bank. This transient current usually decays to zero in a fraction of a cycle of the system frequency. In the case of back-to-back switching, the component supplied by the source is at a lower frequency and so small that it may be neglected.

9.3.2 De-energisation of capacitor banks

De-energisation of capacitor banks follows the theory outlined in 9.2.2.

9.3.3 Energisation of capacitor banks

9.3.3.1 Single capacitor bank

Energising a single capacitor bank is equal to energisation of capacitor bank C_1 when capacitor bank C_2 is not connected in the circuit described in Figure 104. The circuit consists then of the source inductance L_s in series with the capacitor bank C_1. L_1 can be disregarded here, since the inductance of the source is several orders of magnitude higher than that of L_1 (i.e. L_s >> L_1). In this case, the peak of the inrush current ($i_{i\ peak}$) and inrush current frequency (f_i) are limited by the source impedance L_s.

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A bank of shunt capacitors is considered single when the inrush current on energisation is limited by the inductance of the source and the capacitance of the bank being energised. A capacitor bank is also considered single if the maximum rate of change, with respect to time, of transient inrush current on energisation of an uncharged bank does not exceed the maximum rate of change of the rated short-circuit current at the voltage at which the current is applied. The limiting value is equal to

$$\left(\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}\right)_{\max} = \omega_\mathrm{s} I_\mathrm{sc}\sqrt{2} \tag{153}$$

where

$\frac{\mathrm{d}i_\mathrm{i}}{\mathrm{d}t}$ is the rate of change of inrush current, A/s;

I_sc is the rated short-circuit current, in A r.m.s;

$\omega_\mathrm{s} = 2\pi f_\mathrm{s}$ is the angular frequency, in rad/s and f_s is the power frequency, in Hz.

Assuming that bank 1 is to be connected to the busbar and bank 2 is not connected, from Equation (151):

$$i_\mathrm{i} = \frac{\hat{u}}{L\sqrt{\omega_0^2 - \alpha^2}} e^{-\alpha t} \sin\left(\sqrt{\omega_0^2 - \alpha^2}\right)t \tag{154}$$

where $L = L_\mathrm{s} + L_1$ and $\omega_0 = 1/\sqrt{LC_1}$

If ω_0 >> α, then Equation (154) can be re-written in the simplified form:

$$i_\mathrm{i} = \frac{\hat{u}}{Z} e^{-\alpha t} \sin \omega_0 t \tag{155}$$

where $Z = \sqrt{\frac{L}{C_1}}$

The two quantities of interest for circuit-breaker application are the peak value of the inrush current $i_{\mathrm{i\ peak}}$ and its frequency f_i:

$$i_{\mathrm{i\,peak}} = \frac{\sqrt{2}u}{Z} \tag{156}$$

$$f_\mathrm{i} = \frac{1}{2\pi\sqrt{L_\mathrm{s}C_1}} \tag{157}$$

where $Z = \sqrt{\frac{L_\mathrm{s}}{C_1}}$ and $L_\mathrm{s} >> L_1$ is assumed.

9.3.3.2 Back-to-back capacitor bank switching

The inrush current of a single bank will be increased when other capacitor banks or parallel cables are connected to the same bus.

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If, in Figure 104, bank 1 is connected to the busbar and initially uncharged bank 2 is to be connected, the inrush current associated with the charging of bank 2 is supplied by bank 1 (back-to-back switching).

Equations (156) and (157) are applicable and adjusted as follows:

$$i_{\mathrm{i}} = \frac{\sqrt{2}u}{Z_{\mathrm{eq}}} \tag{158}$$

$$f_{\mathrm{i}} = \frac{1}{2\pi\sqrt{L_{\mathrm{eq}}C_{\mathrm{eq}}}} \tag{159}$$

where $Z_{\mathrm{eq}} = \sqrt{L_{\mathrm{eq}} / C_{\mathrm{eq}}}$, $L_{\mathrm{eq}} = L_1 + L_2$ and $C_{\mathrm{eq}} = \frac{C_1 C_2}{C_1 + C_2}$

Equations (158) and (159) can be applied in general to multiple bank switching cases. Assume that bank C with series inductance L is to be switched in with banks C_1 to C_{n} and associated series inductances L_1 to L_{n} already in service. The simplified calculation procedure is as follows:

a) Ignore the capacitances and calculate L_{eq}

$$L_{\mathrm{eq}} = L + L'$$

where $L' = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + \ldots\ldots \frac{1}{L_n}}$

b) Ignore the inductances and calculate C_{eq}

$$C_{\mathrm{eq}} = \frac{CC'}{C + C'}$$

where $C' = C_1 + C_2 + \ldots\ldots + C_n$

Typical amplitudes of the inrush currents for back-to-back energisation of capacitor banks are several kA with frequencies of 2 kHz to 5 kHz. Typical values are given in Table 9 of IEC 62271-100:2008. Capacitors can normally withstand amplitudes up to 100 times their rated current.

If the inrush current amplitude and frequency exceed those stated in Table 9 of IEC 62271-100:2008, it may be necessary to limit them. This can be done by insertion of additional series inductance in the circuit, or by using pre-insertion resistors (see 9.5.3). Another possibility is to use controlled switching.

9.4 No-load cable switching

9.4.1 General

To describe the phenomena associated with no-load cable switching, a general single-phase equivalent circuit is shown in Figure 105, showing the case where two cables (cable 1 and cable 2) are connected back-to-back to a system. The cables are represented by their capacitance C_1 and C_2 and their surge impedances Z_1 and Z_2, respectively.

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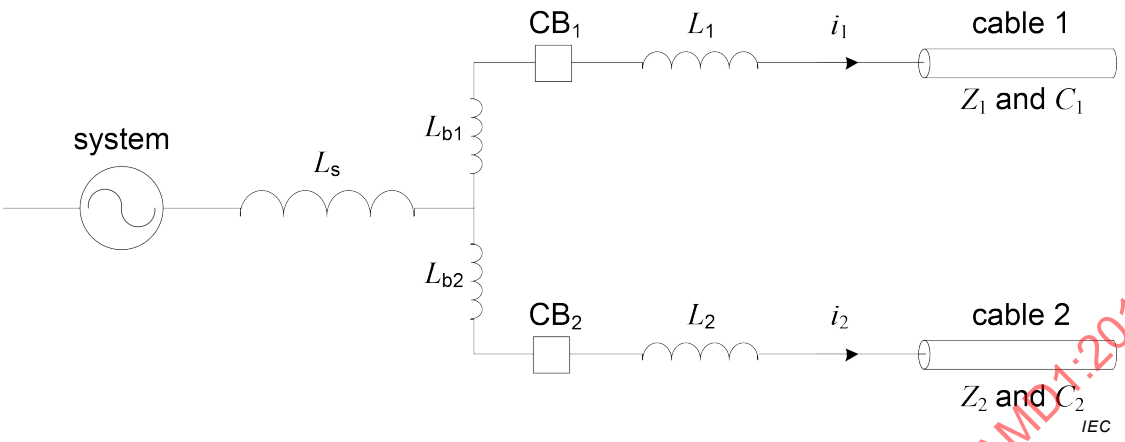

Key

CB_1	circuit-breaker
CB_2	circuit-breaker, open for single cable switching, closed for back-to-back switching
L_s	source inductance
L_1, L_2	inductance between cables 1 and 2 and the bus
Z_1, Z_2	surge impedance of cables 1 and 2 (Ω)
C_1, C_2	capacitance of cables 1 and 2 (F)
L_{b1}, L_{b2}	inductance of the bus connecting the cables

Figure 105 – Typical circuit for no-load cable switching

Single cable switching occurs when cable 1 is switched and cable 2 is not connected in the circuit described in Figure 10. The circuit then consists of the source inductance L_s in series with the bus inductance L_{b1} and the inductance L_1 between bus and cable.

Back-to-back cable switching occurs when cable 1 is switched, with cable 2 being in service.

Three phase cables can be individually screened (Figure 106) or belted (Figure 107). As the equivalent circuits show, individually screened cables represent a load similar to earthed capacitor banks and belted cables a load similar to unearthed capacitor banks.

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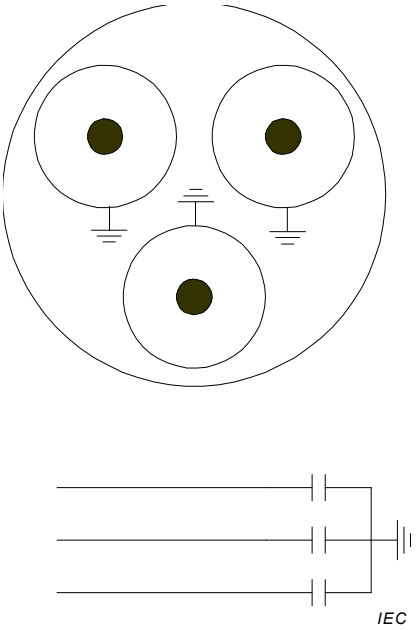

Figure 106 – Individually screened cable with equivalent circuit

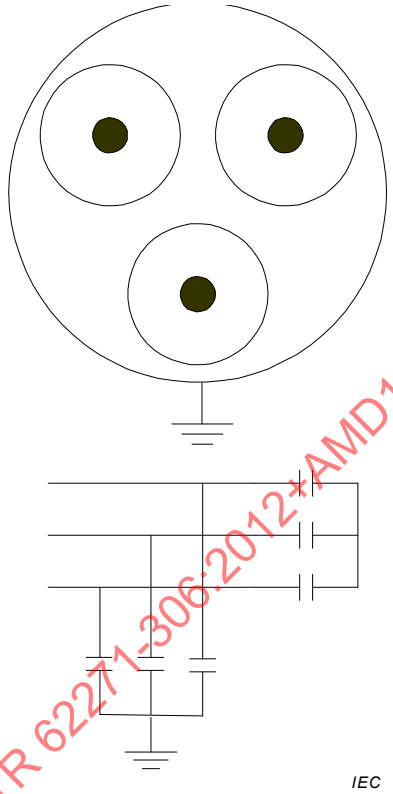

Figure 107 – Belted cable with equivalent circuit

9.4.2 De-energisation of no-load cables

9.4.2.1 General

A cable represents a distributed capacitive load. For de-energisation of a no-load cable, the principles discussed for capacitor bank switching are equally applicable with some variations as discussed later in Subclause 9.4.2. For example, in transient calculations, the cable surge impedance is applicable rather than its capacitance.

9.4.2.2 Cable charging current

The cable charging current is a function of the following characteristics:

a) system voltage;

b) cable geometry;

c) insulation dielectric constant;

d) cable length.

The shunt capacitive reactance can be obtained from the cable manufacturer, or if the physical constants of the cable are known, the shunt capacitive reactance can be calculated. Figure 108 shows the cross-section of a high-voltage cable.

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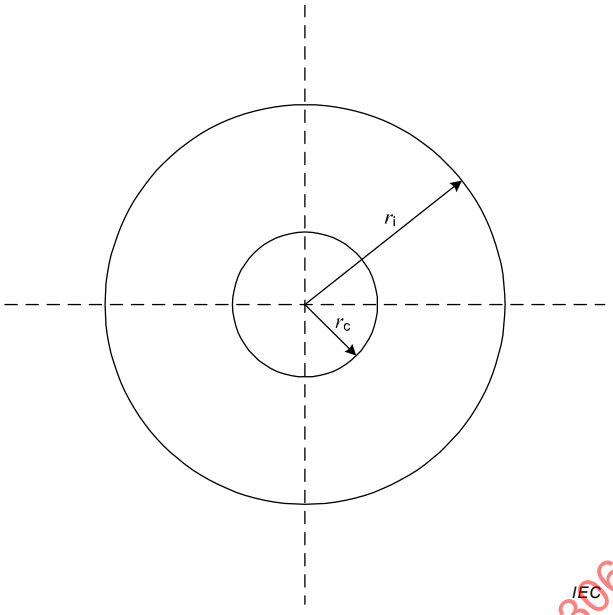

Key

r_c	Conductor radius (m)
r_i	Inside diameter of the shield

Figure 108 – Cross-section of a high-voltage cable

The shunt capacitance per unit length of a cable is expressed in Equation (160).

$$C = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln(\frac{r_i}{r_c})} \text{ F/m} \quad (160)$$

The series inductance per unit length of a cable is expressed in Equation (161).

$$L = \frac{\mu_0\mu_r}{2\pi}\ln(\frac{r_i}{r_c}) \text{ H/m} \quad (161)$$

For single-conductor and three-conductor shielded cables (for the different cable configurations see Figure 106 and Figure 107) the shunt capacitive reactance per km (X_c) can be written as shown in Equation (162).

$$X_c = \frac{1}{\omega_s C} = \frac{\ln(\frac{r_i}{r_c})}{l \times \omega_s \times 2\pi\varepsilon_0\varepsilon_r} (\text{M}\Omega) \quad (162)$$

Using the relationship $\ln(x) = 2{,}3\lg(x)$ and l = 1 000 m = 1 km, Equation (162) transforms to Equation (163).

$$X_c = \frac{6{,}58}{f_s\varepsilon_r}\lg\frac{r_i}{r_c} \text{ (M}\Omega \text{ per phase, see NOTE and Figure 108)} \quad (163)$$

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where

f_s is the system frequency (Hz);

ε_0 is the dielectric constant of vacuum, $\varepsilon_0 = 8{,}85\times10^{-12}$ (F/m);

ε_r is the relative dielectric constant of cable dielectric material;

r_i is the inside radius of shield (mm);

r_c is the conductor radius (mm);

l is the cable length (m);

μ_0 is the magnetic permeability of vacuum, $\mu_0 = 4\pi \times 10^{-7}$ (H/m);

μ_r is the relative magnetic permeability of the cable dielectric material ($\mu_r \approx 1$);

ω_s is the angular power frequency, $\omega_s = 2\pi f_s$ (rad/s);

f_s is the power frequency (Hz);

ln is the natural logarithm based on e, $^{e}\log x$;

lg is the logarithm based on 10, $^{10}\log x$.

NOTE When using the quantity MΩ per phase per km, the shunt capacitive reactance in MΩ for more than 1 km decreases because the capacitance increases. For more than 1 km of cable, therefore, the value of shunt capacitive reactance as given above is divided by the number of km of cable.

Using the capacitive reactance, the cable charging current can be calculated and compared with the rated cable charging current of the circuit-breaker given in IEC 62271-100. If the calculation exceeds the rating, the manufacturer should be consulted. Before an application can be made, the inrush current rating should also be checked (see 9.4.3).

The surge impedance (Z) of a single-conductor and three-conductor shielded cables can be expressed using Equation (164).

$$Z = \sqrt{\frac{L}{C}} = \sqrt{\frac{\frac{\mu_0\mu_r}{2\pi}\ln(\frac{r_i}{r_c})}{\frac{2\pi\varepsilon_0\varepsilon_r}{\ln(\frac{r_i}{r_c})}}} = \sqrt{\frac{4\pi\times10^{-7}}{4\pi^2 8.85\times10^{-12}\varepsilon_r}}\times\ln(\frac{r_i}{r_c}) = \frac{138}{\sqrt{\varepsilon_r}}\times\log\left(\frac{r_i}{r_c}\right) \quad (\Omega) \qquad (164)$$

Typical values of ε_r range from 2,3 (polyethylene) to 4 (fluid impregnated paper); a typical value for Z is 50 Ω.

9.4.2.3 Recovery voltage

The recovery voltage is similar to that of a capacitor bank (see 9.2.2.3).

9.4.3 Energisation of no-load cables

9.4.3.1 General

A circuit breaker may be required to energize a no-load cable during its normal operating duties. Prior to energisation the cable is usually at ground potential, but can have a trapped charge from a previous switching operation. A cable may be switched from a bus that does not have other cables energized (single cable) or against a bus that has one or more cables energized (i.e. back-to-back cable).

The energisation of a cable by the closing of a circuit breaker will result in a transient inrush current. The magnitude and rate of change of this inrush current is a function of the following:

– applied voltage (including the point on the voltage wave at closing);

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– cable surge impedance;
– cable capacitive reactance;
– inductance in the circuit (amount and location);
– any charges on the cable at the instant of closing;
– any damping of the circuit because of closing resistors or other resistance in the circuit.

The transient inrush current to a single cable is less than the available short-circuit current at the circuit breaker terminals. Because a circuit breaker shall meet the making current requirements of the system, transient inrush current is not a limiting factor in single cable applications.

When cables are switched back-to-back (that is, when one cable is switched while other cables are connected to the same bus), transient currents of high magnitude and initial high rate of change may flow between cables when the switching circuit-breaker is closed or restrikes on opening. This surge current is limited by the cable surge impedances and any inductance connected between the energised cable(s) and the switched cable. This transient current usually decays to zero in a fraction of a cycle of the system frequency. During back-to-back cable switching, the component of current supplied by the source is at a lower rate of change and so small that it may be neglected. Due to the very high damping of the inrush current, the switching of parallel cables usually does not represent a problem for modern circuit-breakers. Therefore no problems are expected for back-to-back cable configurations. The case of back-to-back cable switching is not addressed in IEC 62271-100.

Cables are considered being switched back-to-back if the maximum rate of change of transient inrush current on energizing an uncharged cable exceeds that specified for a single cable.

9.4.3.2 Single cable energisation

A cable is defined as single if the maximum rate of change, with respect to time, of transient inrush current on energizing an uncharged cable does not exceed the rate of change of current associated with the rated short-circuit current. This limiting value is numerically equal to

$$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max} = \omega_{\mathrm{s}}\sqrt{2}\,I_{\mathrm{sc}} = 2\pi f_{\mathrm{s}}\sqrt{2}\,I_{\mathrm{sc}} \qquad (165)$$

where

$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max}$ is the maximum rate of change of inrush current in A/s;

I_{sc} is the rated r.m.s. short-circuit current, in A;

$\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$ is the angular frequency in rad/s, where f_{s} is the power frequency in Hz.

By this definition, it is possible to have cable circuits that are physically back-to-back, but are considered single for application purposes provided a large inductance is located between the two cable circuits. The inductance should be large enough so that by itself it would limit fault current to a value less than or equal to the circuit-breaker rating.

In switching a single cable, if the source inductance is greater than 10 times the cable inductance, the cable can be represented as a capacitor. Otherwise, under transient conditions the cable can be represented by its surge impedance.

To calculate the inrush current for a single cable, Figure 105 may be used, with circuit-breaker CB_2 open.

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$$i_i(t) = \frac{U_m - U_t}{Z_1}\left[1 - \exp(-\frac{Z_1}{L}t)\right] \quad (166)$$

where

$$i_{i\,peak} = \frac{U_m - U_t}{Z_1}$$

U_m is the crest of applied voltage;
U_t is the trapped voltage on the cable being switched;
f_s is the source frequency (power frequency);
i_i is the inrush current;
$i_{i\,peak}$ is the peak of the inrush current;
Z_1 is the cable surge impedance;
L is the source inductance.

The initial rate-of-rise (di/dt at t = 0) of the inrush current is $\frac{U_m - U_t}{L}$. For application purposes, $i_{i\,peak}$ should be compared to the value given in Table 9 of IEC 62271-100:2008.

The cable inrush current is not oscillatory in the usual frequency-related sense, but the initial slope can be used to determine an equivalent frequency that can be compared with the inrush frequency. In general,

$$\left(\frac{di_i}{dt}\right) = 2\pi f_i I_i \quad (167)$$

where

$\left(\frac{di_i}{dt}\right)$ is the rate-of-change of inrush current in A/s;
f_i is the inrush current frequency;
I_i is the peak inrush current.

The equivalent frequency f_{eq} for a cable inrush current is then obtained as follows:

$2\pi f_{eq} I_i = \frac{U_m - U_t}{L}$ that gives $f_{eq} = \frac{U_m - U_t}{2\pi L I_i}$ and for proper circuit-breaker application, f_{eq} should be less than the preferred inrush current frequency.

9.4.3.3 Back-to-back cable energisation

Back-to-back cable switching occurs when cable 2 is in service and cable 1 is being energized in Figure 105. The values of the inductances of L_1, L_2, and L_{b1} and L_{b2} between the cables are often very small with respect to the inductance of L_s. In many cases they will be less than 1 % of the source inductance. They consist of the inductances from the cables to the circuit-breakers, the circuit-breaker inductances, and the bus inductance of the current path. Values of inductance depend upon the physical configuration and are hence site specific and unable to be standardized. However, a representative range is 0,66 µH to 1,0 µH per phase per m.

Neglecting the source contribution, the back-to-back cable switching case can be represented as shown in Figure 109.

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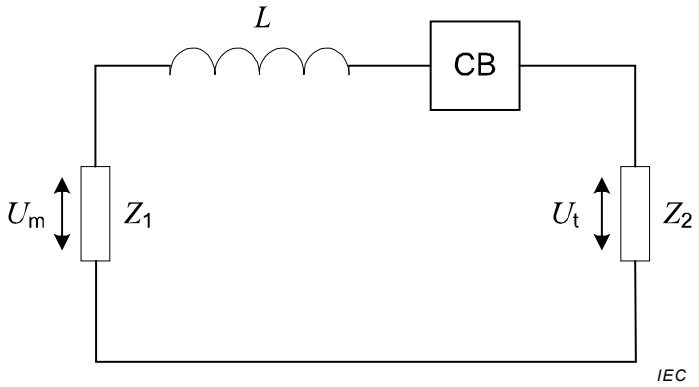

Key

U_m	Crest of applied voltage
U_t	Trapped voltage on cable being switched
Z_1, Z_2	Cable surge impedance
L	Total inductance between cable terminals
CB	Circuit-breaker

Figure 109 – Equivalent circuit for back-to-back cable switching

The initial pulse of current has a front expressed as

$$i(t) = \frac{U_m - U_t}{Z_1 + Z_2}\left[1 - \exp\left(-\frac{Z_1 + Z_2}{L}t\right)\right] \quad (168)$$

Assuming that the $L/(Z_1 + Z_2)$ time constant is less than 1/5 of the travel time of the cable out and back, the initial crest of the inrush current is then $(U_m - U_t)/(Z_1 + Z_2)$, which for application should be less than the rated peak inrush current.

The peak inrush current when energizing a cable with another already connected to the bus is given by

$$i_{i\,peak} = \frac{U_m - U_t}{Z_1 + Z_2} \quad (169)$$

and

$$f_{eq} = \frac{U_m - U_t}{\omega(L_1 + L_2)I_{ir}} \quad (170)$$

The inrush current when energizing a cable with an equal cable already connected to the bus is given by

$$i_{i\,peak} = \frac{U_m - U_t}{2Z}\ \text{(A)} \quad (171)$$

and

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$$f_{eq} = \frac{U_m - U_t}{\omega(L_1 + L_2)I_{ir}} \text{ (Hz)} \quad (172)$$

Differentiating the expression for the current at t = 0 will give the maximum initial rate of change of the inrush current, in Equation (173).

$$\left(\frac{di}{dt}\right)_0 = \frac{U_m - U_t}{L} \text{ (A/s)} \quad (173)$$

This can reach extreme values since the magnitude of L can be arbitrarily small.

Additional inductance may be added in series with the inductances making up L to meet the preferred inrush frequency.

9.4.4 Compensated cable energisation

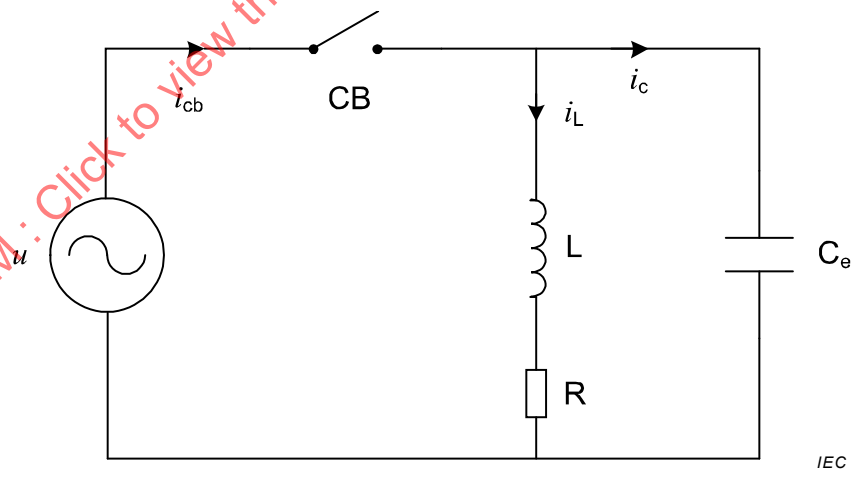
9.4.4.1 General

A circuit-breaker may be required to energise a no-load cable during its normal operating duties. Prior to energisation, the cable is usually at earth potential, but can have a trapped charge from a previous switching operation.

Besides these widely known effects, other phenomena may occur during cable energisation at rated voltages of 420 kV and above.

When operating the cable nearly fully compensated the phenomenon of delayed current zero crossings may occur. This phenomenon is similar to the one described at faults close to generators (see Annex B).

The simplified single-phase equivalent circuit is shown in Figure 110.



Key

u	Phase-to-earth voltage	R	Resistance to earth of compensating reactor
CB	Circuit-breaker	i_{cb}	Current through the circuit-breaker
C_e	Cable capacitance to earth	i_L	Current through the compensating reactor
L	Inductance to earth of compensating reactor	i_c	Current through the cable

Figure 110 – Equivalent circuit of a compensated cable

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When energizing the compensated cable by closing the circuit-breaker, the current starts flowing in the cable (i_c, momentary value of the current is not continuous and may change suddenly) and in the reactor (i_L, momentary value of the current is continuous due to the fact that di/dt at a inductance is zero at the instant of closing the circuit-breaker). The sum of both currents flows through the circuit-breaker (i_{cb}).

Due to the fact that the instantaneous current value in the reactor before energizing and the current value directly after energizing shall be identical ($di/dt = 0$), a DC equalizing current flows depending on the making angle and the instantaneous value of the making voltage, respectively. The change of the current through the inductance when closing the circuit-breaker causes a magnetic field. Due to the continuity requirement, this magnetic field is compensated. The equalizing magnetic field causes the DC equalizing current.

If the circuit-breaker is closed at voltage maximum, the equalizing current is zero and when closing at voltage zero, the equalizing current is at its maximum due to the 90° phase shift between voltage and current for an inductance.

This DC equalizing is superimposed on the inductive AC current of the reactor to the total reactor current i_L. Due to the resistance of the reactor, the DC current decays over time.

The following two different cases are distinguished: fully compensated cables and partly compensated cables.

9.4.4.2 Fully compensated cables

When operating a fully compensated cable, the inductive AC current and the capacitive AC current will be of the same amount. Hereby the capacitive current i_c has the opposite sign of the inductive current i_L.

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 111 for making at voltage maximum and full compensation.

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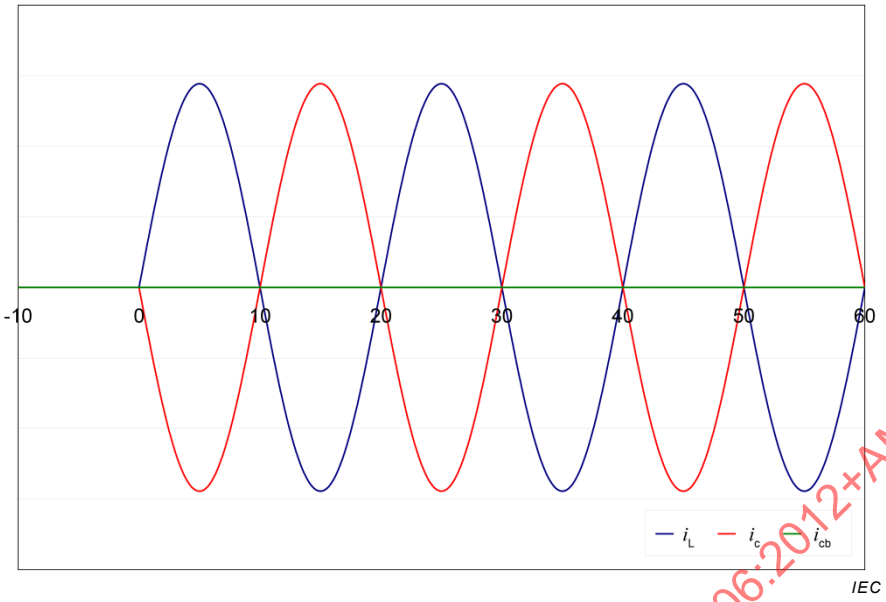

Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Dotted green line	Total current through the circuit-breaker i_{cb}

Figure 111 – Currents when making at voltage maximum and full compensation

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 112 for making at voltage zero and full compensation. The transient effects of the suddenly changing capacitive current when closing the circuit-breaker are not considered.

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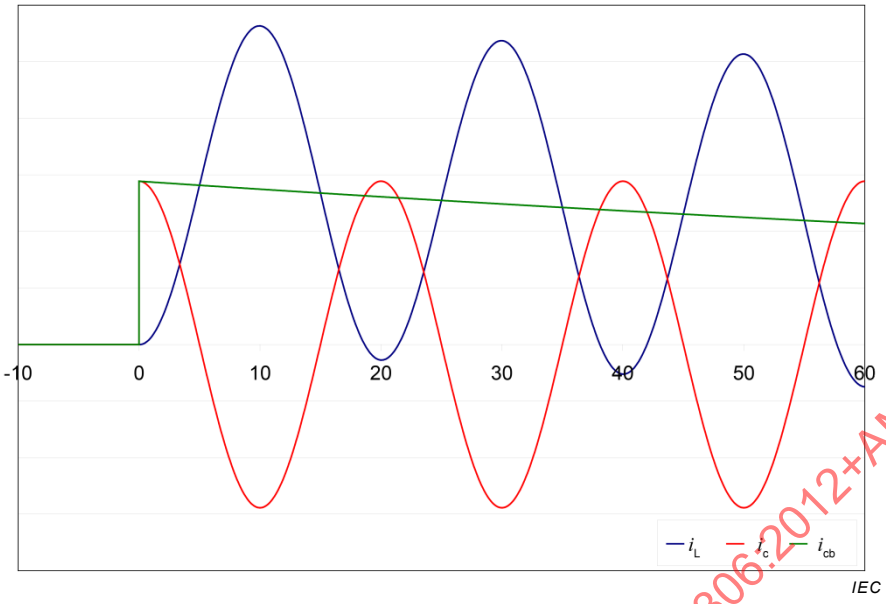

Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 112 – Currents when making at voltage zero and full compensation

It can be seen that the inductive current i_L and the capacitive current i_c in both cases always show zero crossings.

In the case of making at voltage maximum, the current through the circuit-breaker for a fully compensated cable is zero due to the fact that the inductive current i_L and the capacitive current i_c have the same magnitude and opposite polarity.

In the case of making at voltage zero, the current through the circuit-breaker does not show zero crossings for several periods. If within this time period the circuit-breaker is tripped, it may have severe difficulties to interrupt the current. This will be described in detail further in this subclause.

9.4.4.3 Partly compensated cables

If the cable is partly compensated (undercompensated), the inductive AC current is smaller than the capacitive AC current. The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 113 for making at voltage maximum and partial compensation (e.g. 80 %).

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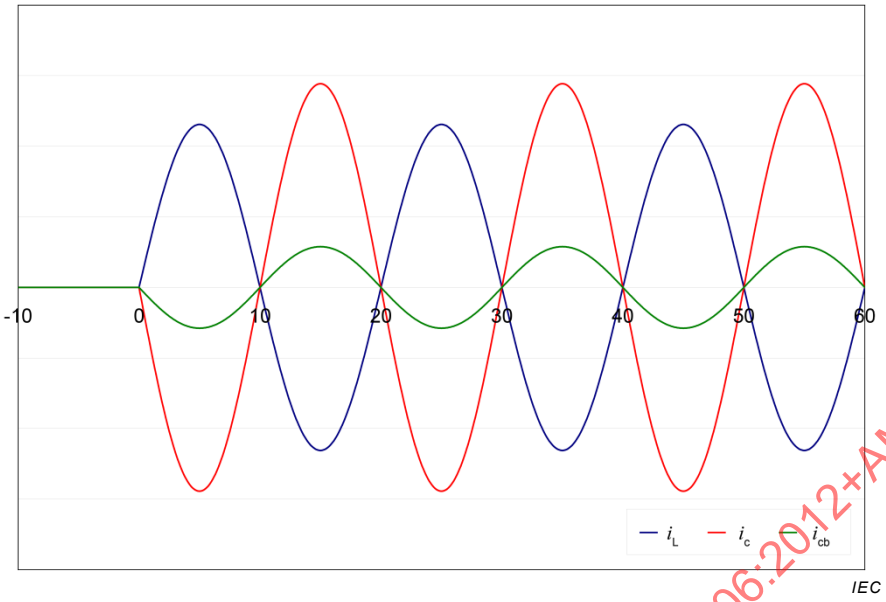
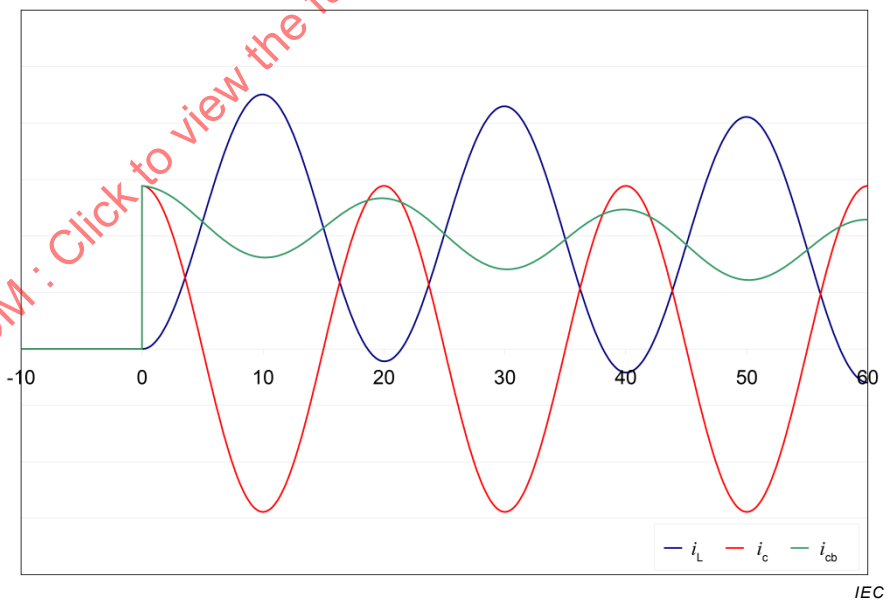


Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 113 – Currents when making at voltage maximum and partial compensation

The idealized graphs of the inductive current i_L, the capacitive current i_c and the total current through the circuit-breaker i_{cb} are shown in Figure 114 for making at voltage zero and partial compensation (e.g. 80 %). The transient effects of the suddenly changing capacitive current when closing the circuit-breaker are not considered.



Key

Blue trace	Inductive current i_L
Red trace	Capacitive current i_c
Green trace	Total current through the circuit-breaker i_{cb}

Figure 114 – Currents when making at voltage zero and partial compensation

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Also, in the case of undercompensated operated cables, it can be seen that the inductive current i_L and the capacitive current i_c in all cases always show zero crossings.

In the case of making at voltage zero, the current through the circuit-breaker also does not show zero crossings for several periods even if the amplitude of the DC equalizing current is smaller due to the lower inductive current at partial compensation.

9.4.4.4 Summary

The amplitude of the DC equalizing current depends on the degree of compensation and the instant of making. The duration of the time period of missing current zero crossings depends on the X/R ratio, the damping of the compensation reactor and the degree of compensation.

In the past, the resistance of the compensation reactors was comparably high. Therefore the X/R ratio (related to the DC time constant τ) was low and the DC equalizing current was damped fast enough to create current zeros. Nowadays, the resistance of the compensation reactors is reduced further in order to minimize the ohmic losses.

The phenomenon of delayed current zero crossings may become problematic if the circuit-breaker is tripped during the time period of missing zero crossings. To solve this problem two basic approaches are possible:

a) prevention of the occurrence of currents with delayed zero crossings;

b) choice of a circuit-breaker suitable for the application.

To prevent currents with delayed zero crossings, the making should always occur around the voltage maximum in each phase. This can be done using controlled closing (point-on-wave closing). Controlled closing ensures that the making occurs in all phases at or near voltage maximum. The disadvantage of this method is the occurrence of switching overvoltages.

If the making at voltage zero cannot be prevented, the decay of the DC equalizing currents can be increased by using circuit-breaker types equipped with pre-insertion resistors. Owing to the additional resistance, the X/R ratio is decreased and hence the first zero crossing of the current i_{cb} occurs significantly earlier. The resistance value of the pre-insertion resistor should be dimensioned in a way that the first zero crossing occurs about 10 ms after making. In this case, a successful opening operation can also be ensured for the worst-case (e.g. opening command is already given during closing of the circuit-breaker). For each application an individual calculation should be performed due to the different parameters of reactor and network parameters as well as a different degree of compensation.

If no suitable resistance value can be determined or controlled switching is not possible, the current shows delayed zero crossings. Hence a suitable circuit-breaker type should be chosen to ensure a successful current interruption at all cases. The arc in the circuit-breaker during the breaking operation represents a non-linear resistance, which also leads to a decreased X/R ratio, and therefore to an earlier occurrence of zero crossings. With special tests, the parameters for an arc model can be determined for each circuit-breaker type. Using this arc model, the influence on the current i_{cb} can be determined. Depending on the amplitude and time constant of the DC equalizing current circuit-breaker types with high arc voltages may be necessary. Also with this method, for each application an individual calculation should be performed due to the different parameters of reactor and network parameters, different parameters of the circuit-breaker arc as well as a different degree of compensation.

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9.5 No-load transmission line switching

9.5.1 De-energisation of uncompensated transmission lines

9.5.1.1 Line charging current

A no-load overhead line can generally be represented by a capacitance. In the case of short lines (< 200 km), this capacitance can be considered concentrated, but in the case of long lines, it should be considered distributed. Typical capacitance values vary from 9 nF/km per phase for single conductor overhead lines to 14 nF/km per phase for four-conductor bundle overhead lines (see also [127]).

Owing to the distributed nature of the inductance and the capacitance of the line, the peak value of the power frequency voltage at the remote (or receiving) end is higher than that at the circuit breaker (sending) end of the line. This effect is called the *Ferranti effect*. For a line length of 500 km, the voltage increase is approximately 4 % and approximately 1 % for a line of 200 km. That is why the Ferranti effect is not considered for line lengths below 200 km.

Figure 115 gives an approximation of the line charging current per km of different line configurations at 60 Hz. If the estimated current is greater than 90 % of the preferred line current rating, a more accurate calculation based on the actual line configuration and methods similar to that discussed in Gabrielle, et al. [127] should be used.

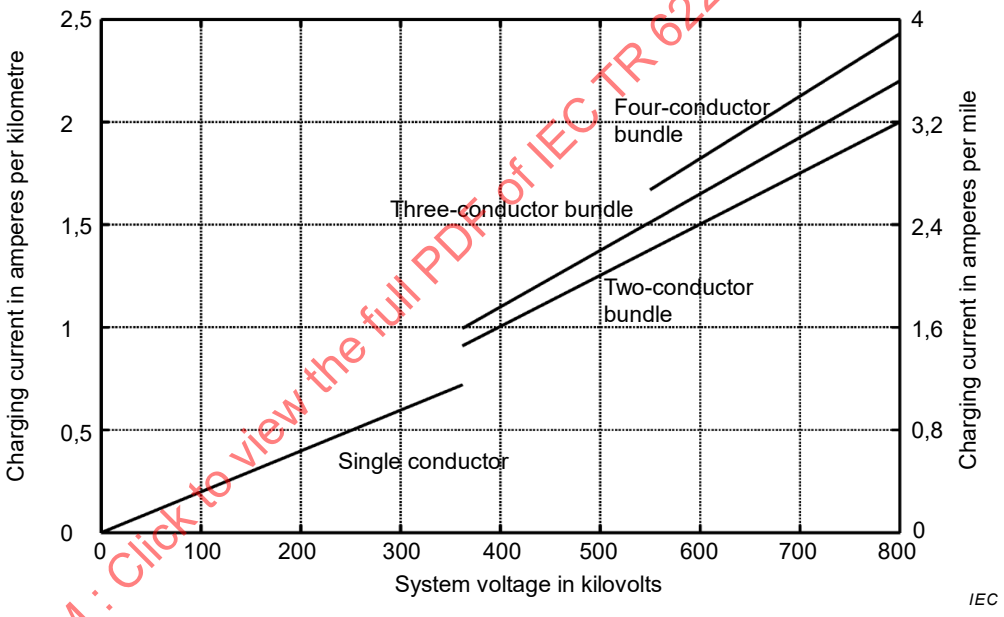

Figure 115 – RMS charging current versus system voltage for different line configurations at 60 Hz

From Figure 115, the capacitive reactance can be derived as follows.

Assume a system with a rated voltage of 245 kV, 60 Hz. The charging current is 0,5 A/km. The linear capacitive reactance X_C' is then:

$$X_c' = \frac{1}{\omega C'} = \frac{U}{I'} = \frac{245\,000\ \text{V}}{\sqrt{3} \times 0{,}5\ \text{A/km}} = 0{,}283\ \text{M}\Omega\ \text{km}\ ,$$

where

X_c' is the linear capacitive reactance of the line (MΩ km);

C' is the capacitance of the line (F/km);

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I' is the charging current of the line (A/km);

U is the system voltage (kV).

For a 50 Hz system frequency, the corresponding value of X_c' would be

$$0{,}283 \times \frac{60}{50} = 0{,}34\,\text{M}\Omega\,\text{km}$$

To calculate the reactance X_c of a line with a given length l, the linear reactance X_c' has to be divided by the length:

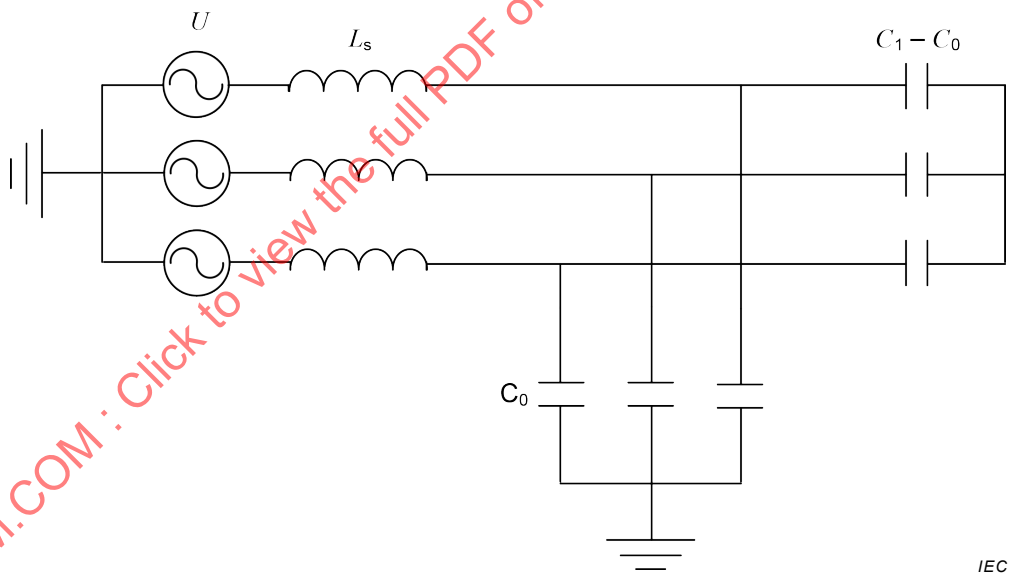
$$X_c = \frac{X_c'}{l}$$

Assume a length of 100 km for the example above. The reactance X_c is then:

$$X_c = \frac{X_c'}{l} = \frac{0{,}283\,\text{M}\Omega\text{km}}{100\,\text{km}} = 2{,}83\,\text{k}\Omega\,.$$

9.5.1.2 Recovery voltage

Transmission lines have capacitance both between phases and to ground. Figure 116 shows a general circuit that can be used to analyse the phenomena associated with no-load transmission line switching.



Key

U	Source voltage
L_s	Source inductance
C_0	Zero sequence capacitance
C_1	Positive sequence capacitance

Figure 116 – General circuit for no-load transmission line switching

Overhead lines in transmission systems typically have C_1/C_0 ratios in the order of 2,0. Figure 117 shows the peak value of the recovery voltage in the first-pole-to-clear as a function of the capacitance ratio C_1/C_0 (positive to zero sequence capacitance). The recovery

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voltage peak is the differential voltage of the source and line sides, including the effects of coupled voltage on the first cleared pole. In this case Figure 117 shows that the recovery voltage peak is approximately 2,4 p.u. It follows that the voltage factor for single-phase testing to cover three-phase interruption is equal to 1,2. It has been assumed that the amplitude approaches 3 p.u. This is the case without capacitance to earth and delayed interruption of the second phase. An example of the voltages in such a case is given in Figure 103. The other extreme, C_1 = C_0, is the case where each phase has capacitance to earth only. The recovery voltage peak is then 2 p.u. as in a single-phase case.

Overhead lines in transmission systems typically have capacitance both between phases and to earth. Figure 103 and Figure 117 assume that the second and third poles interrupt 90° after the first.

When the characteristics of the voltage in service (shape and peak value) are deviating from those of the test voltage, the restrike probability may increase. For example, if the line is compensated, the line side component is not a trapped voltage resulting from the trapped charge, but a voltage oscillating with a frequency determined by the compensating reactors and the line side capacitance (see 9.5.2).

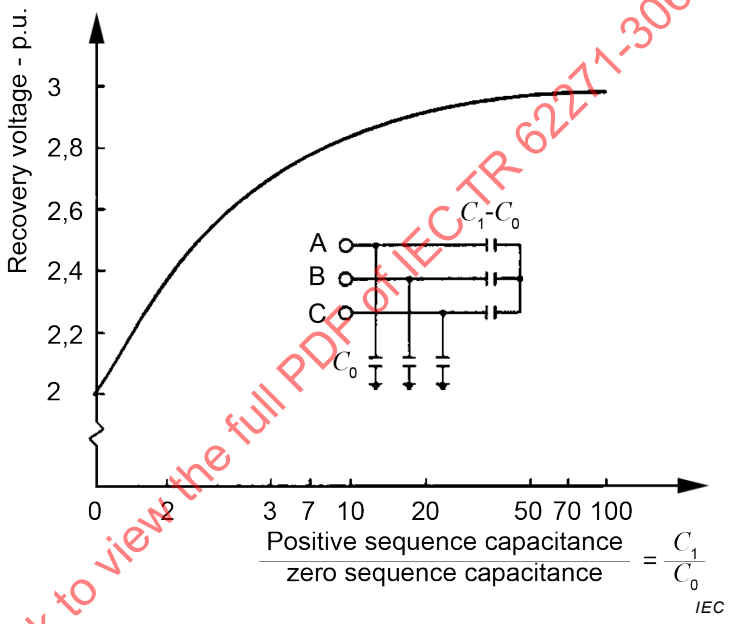

Figure 117 – Recovery voltage peak in the first-pole-to-clear as a function of C_1/C_0, delayed interruption of the second phase

If the C_1/C_0 ratio is greater than 2, higher voltages may be coupled to the first pole-to-clear, resulting in increased probability of restrike. In this case, the manufacturer should also be consulted since circuit-breaker designs are sensitive to both current magnitude and recovery voltage waveshapes.

9.5.2 De-energisation of compensated transmission lines

9.5.2.1 General

Long overhead lines are often compensated with shunt reactors to reduce the charging current of the line. The compensation factor (k_L) of an overhead line is given by the ratio of the capacitive reactance ($X_{C,line}$) to the inductive reactance ($X_{L,reactor}$) of the compensating reactor, in Equation (174):

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$$k_L = \frac{X_{C,line}}{X_{L,reactor}} \quad (174)$$

If $X_{L,reactor} > X_{C,line}$, the line is undercompensated, a line with $X_{L,reactor} < X_{C,\ line}$ is called overcompensated.

9.5.2.2 Line charging current

The compensated line charging current is given by $I_{Lc} = I_c'(1-k_L)$

where

I_{Lc} is the line charging current of the compensated line;

I_c' is the line charging current of uncompensated line;

k_L is the compensation factor.

Assuming a line compensated at 60 % (i.e. k_L = 0,60), the line charging current is $I_{lc} = I_c' \times (1 - 0{,}6) = 0{,}4 I_c'$, or 40 % of the uncompensated value.

9.5.2.3 Recovery voltage

If the line is compensated, the line side component of the recovery voltage is no longer a DC voltage, but an oscillation of which the frequency is determined by the compensating reactor and the line capacitance.

The resonant frequency is approximated by:

$$f_L \approx \frac{1}{2\pi\sqrt{LC}} = f_s \sqrt{\frac{X_{C,line}}{X_{L,reactor}}} = f_s \sqrt{k_L} \quad (175)$$

where

f_L is the resonance frequency of the compensated line (Hz);

L is the inductance of the reactor (H);

C is the total capacitance of the line (F);

f_s is the system frequency (Hz);

k_L is the compensation factor.

In other words: the resonance frequency of a compensated line is dependent on the degree of compensation. Since the compensation usually is less than 1, this resonance frequency is less than the system frequency, resulting in a reduction of the rate-of-rise of the recovery voltage. Typical current and voltage waveshapes are given in Figure 118.

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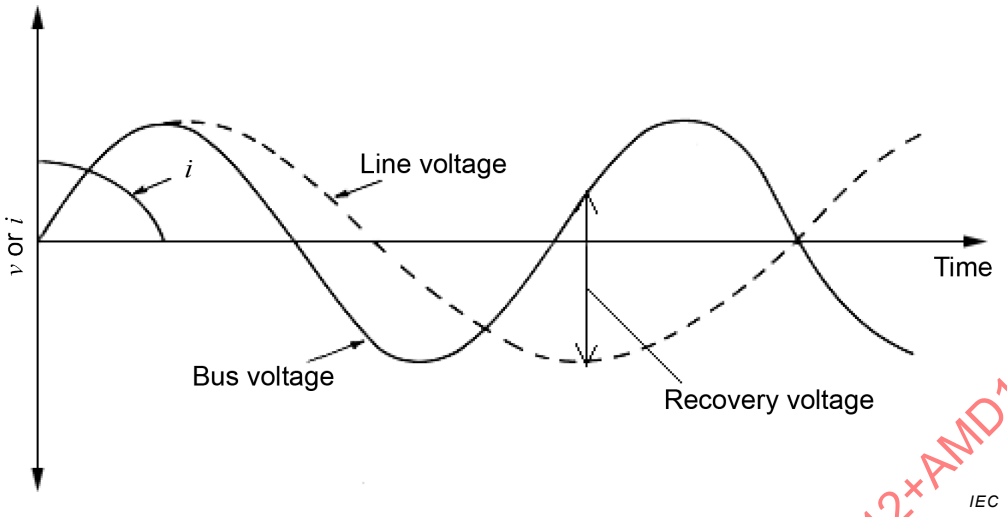

Figure 118 – Typical current and voltage relations for a compensated line

The first half-cycle of recovery voltage is, for this example, as shown in Figure 119. Compensation thus results in a decrease of the probability of restrike at a particular current. Under these conditions, improved performance may result, the circuit-breaker having a lower probability of restrike. The manufacturer should be consulted on applications which markedly alter the recovery voltage.

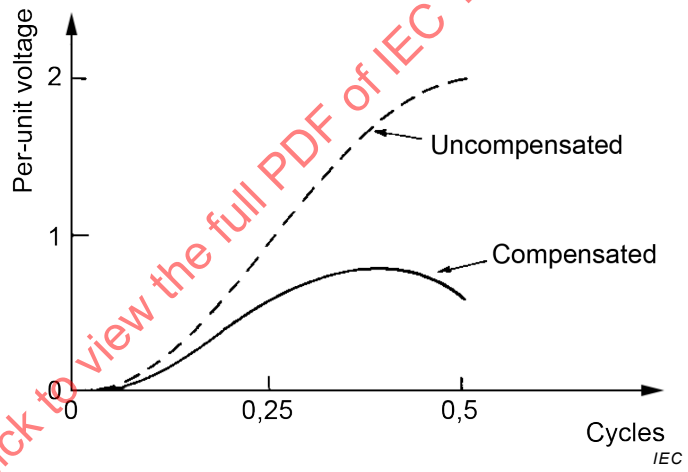

Figure 119 – Half cycle of recovery voltage

9.5.3 Energisation and re-energising transmission lines

9.5.3.1 General

For this case inrush currents are of no significance due to the high surge impedance of the lines. However, overvoltages are an issue due to travelling waves on the lines. Typically, the line is uncharged when being switched but voltage doubling is possible due to reflections from the open end of the line. A worst case can occur during high-speed reclosing when a restrike occurs at a source voltage peak of opposite polarity to the trapped charge on the line.

At voltages of 300 kV and above, mitigation measures are applied to limit the above switching overvoltages. The measures include opening resistors, metal oxide surge arresters and controlled switching.

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When a transmission line is switched onto an energised network, a voltage wave is imposed on the line. The resulting phenomena are similar to those of energizing a cable. The imposed wave will be reflected at the far end of the line and when the line is open at the far end (or terminated by a high-impedance load for high frequencies), the reflected wave results in doubling of the amplitude as shown in Figure 120.

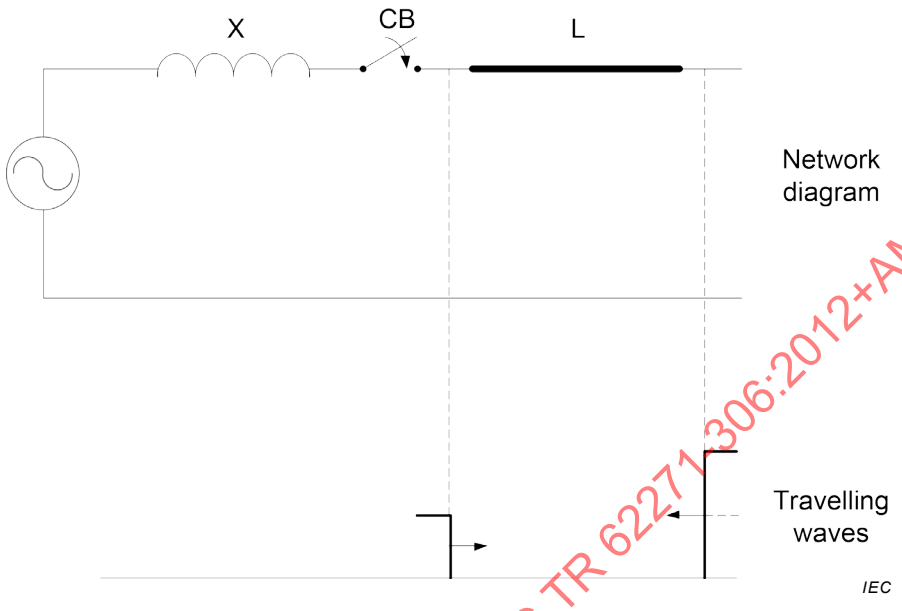

Figure 120 – Energisation of no-load lines: basic phenomena

An even higher voltage is obtained when the line has a trapped charge before being energized and the circuit-breaker happens to close at an instant when the polarity of the network voltage is opposite to that of the voltage that was present on the line. The voltage on the line can, after reflection of the wave, theoretically be up to three times the network voltage. This situation can occur in conjunction with auto-reclosing of a line.

Even higher voltages can develop on a three-phase line, when the three circuit-breaker poles are not closing simultaneously. A wave on one phase will then generate induced waves on the other phases and under unfavourable circumstances this can lead to a further rise in voltage on another phase.

9.5.3.2 Reclosing on a compensated transmission line

Similar phenomena as described under 9.4.4.2 also apply to fully compensated lines. Especially during reclosing of the healthy phases after the interruption of a single-phase short-circuit, the circuit-breaker may close at or near source voltage zero. This will result in delayed current zero crossings. Not all circuit-breakers may be suited for this application. For further information, refer to Annex B.

9.5.3.3 Long transmission line switching considerations

Overhead lines exceeding 200 km, even those of simple construction type, present a special case not covered by the requirements of 6.111.7 of IEC 62271-100:2008 or its notes. Where such long lines are to be switched, consideration should be given to the higher value of peak recovery voltage present on interruption. Some idea of the ability of a particular circuit-breaker for making and breaking of this requirement can be gained by considering any out-of-phase switching evidence that may exist. Such evidence will usually provide adequate demonstration of the elevated recovery voltage. For full compliance, evidence will be required to satisfy the capacitive current switching requirements of 6.111 of IEC 62271-100:2008, but to the elevated values required by the specific application.

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Some users may be concerned about rare or occasional switching operations from one end on a series of long lines. This can occur during the early development stages of a system when intermediate substations may not be fully equipped or may even be by-passed. In such cases, it may be appropriate to consider the out-of-phase capability in relation to the combined load presented by the series of lines. If satisfactory for the current and voltage conditions, then specific testing for the severe capacitive current switching duty of IEC 62271-100 would not be necessary at the enhanced levels of the extended line. They would be required for the switching duty of the individual lines of the series, as normal.

9.6 Voltage factors for capacitive current switching tests

Depending on the capacity of a high-power laboratory, capacitive current switching tests may be performed as three-phase tests or single-phase tests. For the higher voltages (362 kV, 420 kV, 550 kV and 800 kV), unit tests are generally carried out.

Especially when single-phase tests are made to cover three-phase application, the test voltage should reflect the application of the circuit-breaker in the field. One of the factors influencing this is the earthing situation of the network. The other is the presence of single or two-phase faults (see 9.8 of this document and Annex S of IEC 62271-100:2008/AMD2:2017.

Subclause 6.111.7 of IEC 62271-100:2008 gives the following voltage factors for single-phase test voltage (see Table 43). In accordance with IEC 62271-100, the test voltage measured at the circuit-breaker location prior to interruption shall not be less than the rated voltage $U_r/\sqrt{3}$ and the voltage factors given in Table 43.

Table 43 – Voltage factors for single-phase capacitive current switching tests

Voltage factor k_c	Application
1,0	Tests corresponding to normal service in solidly earthed neutral systems without significant mutual influence of adjacent phases of the capacitive circuit, typically capacitor banks with solidly earthed neutral and screened cables.
1,2	Test on belted cables and line-charging current switching [a] corresponding to normal service conditions in solidly earthed neutral systems with mutual influence of adjacent phases of the capacitive circuit for rated voltages 52 kV and above.
1,4	1. breaking during normal service conditions in systems having a non-effectively earthed neutral including screened cables [b]; 2. breaking of capacitor banks having a non-effectively earthed neutral; 3. test on belted cables and line-charging current switching [b] corresponding to normal service conditions in effectively earthed systems for rated voltages less than 52 kV;
NOTE 1 The voltage factors for line-charging current switching tests of 1,2 and 1,4 are applicable to single-circuit line construction. Requirements for multiple overhead line constructions may be greater than these factors. NOTE 2 The 1,4 factor is a compromise and is valid for breaking of capacitive currents in non-effectively earthed systems, where the second and third-pole-to-clear interrupt 90° after the first. NOTE 3 When the non-simultaneity of contact separation in the different poles of the circuit-breaker exceeds 1/6th of a cycle of rated frequency, IEC 62271-100 recommends to raise the voltage factor or to make only three-phase tests. Such circuit-breakers fall outside the scope of the standard. [a] Under the condition that the line can be replaced partly or fully by a concentrated capacitor bank. [b] When a significant capacitance to earth on the source side is present, the factor will be reduced.	

The voltage factor 1,4 is explained as follows (see Figure 121):

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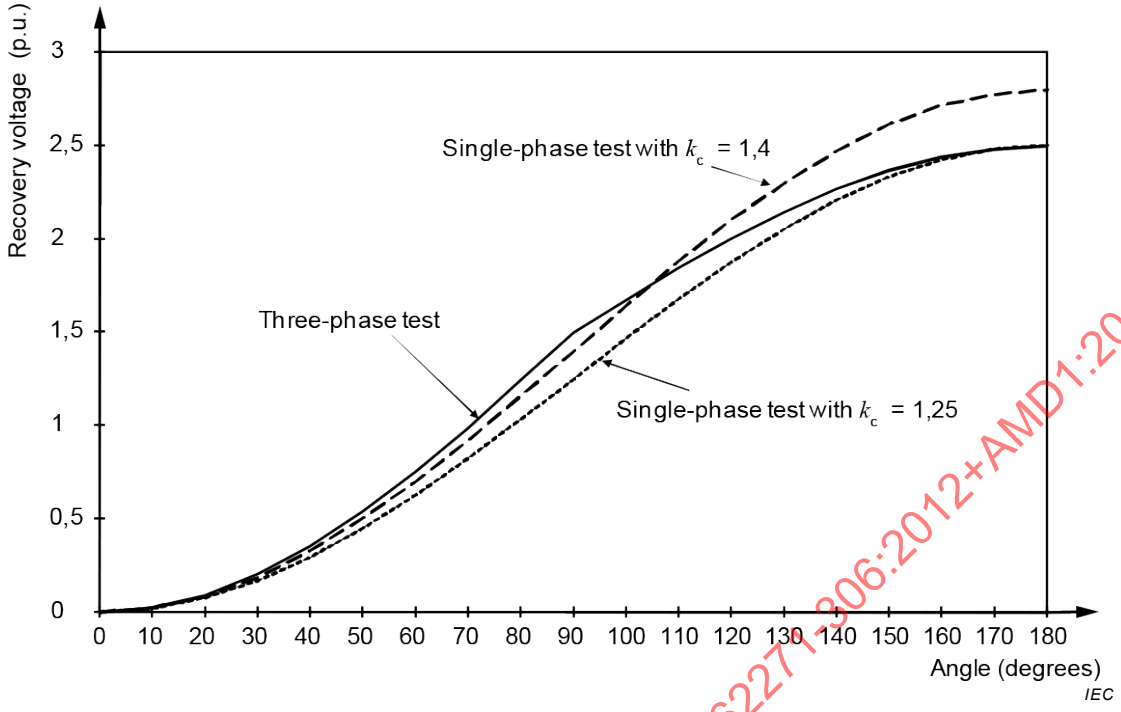

Figure 121 – Recovery voltage on first-pole-to-clear for three-phase interruption: capacitor bank with isolated neutral

When the current in the first pole is interrupted, the voltage across the circuit-breaker will rise as if the voltage factor would have been 1,5. When the second and third pole interrupt 90° later, there is a discontinuity and the recovery voltage across the first-pole-to-clear will follow a 1-cosine wave with a voltage factor of 1,25. The recovery voltage is indicated by the solid line in Figure 121. By using a voltage factor of 1,25 (dotted line in Figure 121), the initial portion of the recovery voltage across the first pole is not adequately covered. Using a voltage factor of 1,5 will result in too high a stress. A voltage factor of 1,4 as indicated by the dashed curve in Figure 121 is a compromise that adequately covers the actual recovery voltage.

Careful consideration should be given to these voltage factors when circuit-breakers are relocated to other parts of the system where the application is different from that of the original location.

As indicated in footnote a) to Table 43, the voltage factors given in Table 43 are associated with single circuit line constructions and are chosen to accommodate all known physical arrangements of the conductors of such circuits. Footnote b) to Table 43 indicates that energisation of the case of multiple overhead line constructions that have parallel circuits may require a voltage factor greater than 1,2 and 1,4. This is because such circuits are likely to have an enhancement to the line side residual voltage following interruption. This is associated with the coupling (pick-up) from the parallel circuit and may add a power frequency peak voltage of up to 0,2 p.u. This is dependent upon the geometry of the conductor systems of the two circuits.

In addition, the effect of these changes on the line side voltage, following interruption by the first-pole-to-clear, does affect the shape of the TRV across that opening pole. Consideration of this may require additional testing if the existing factor does not adequately cover the combined effects. Alternatively, the higher of the given values, e.g. 1,4 for 1,2, can be selected to encompass the specific waveshape.

On occasion, utilities have specified a voltage factor of 1,3 instead of 1,2 for double circuit lines.

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9.7 General application considerations

9.7.1 General

The capacitive current switching capability of the circuit-breaker is depending on its rated voltage, rated frequency, the particular application (i.e. overhead line, capacitor bank, etc.) and the earthing conditions of the network.

Caution should be exercised when applying older circuit-breakers that have not been rated to IEC 62271-100.

9.7.2 Maximum voltage for application

The operating voltage should not exceed the rated voltage since this is the upper limit for operation.

9.7.3 Rated frequency

The rated frequency for circuit-breakers is 50 Hz or 60 Hz. As described in 9.2.1.3, a rated frequency of 60 Hz results in a more severe stress on the circuit-breaker, since the voltage peak occurs earlier (at 8,3 ms) than in the case of 50 Hz (10 ms).

Special consideration should be given when comparing tests performed at 60 Hz to cover 50 Hz requirements or vice versa. At lower frequencies, the capacitance current switching ability will be adequate. The switching capability demonstrated at 60 Hz covers the requirements for 50 Hz with the same voltage factor.

9.7.4 Rated capacitive current

9.7.4.1 General

The preferred values of the rated capacitive switching current are given in Table 9 of IEC 62271-100:2008. Not all actual cases of capacitive current switching are covered by that table. The values for lines and cables cover most cases, the values of the current for capacitor banks (single and back-to-back) are typical for some capacitor banks in service.

9.7.4.2 Overhead lines and cables

Depending on length, the no-load current of lines and cables may exceed that given in Table 9 of IEC 62271-100:2008.

The following may serve as an example: the no-load current of a two bundle conductor 550 kV transmission line is approximately 1,1 A/km at 50 Hz and 1,3 A/km for 60 Hz.

Without considering the Ferranti effect (see 9.5.3.3), the charging current of a 500 km line would be 605 A at 50 Hz and 715 A at 60 Hz. Ferranti rise on a 500 km line would increase the charging current by about 4 % at 50 Hz and 6 % at 60 Hz. This is not covered by Table 9 of IEC 62271-100:2008.

The higher current does not pose a problem for circuit-breakers of present design, since the higher current tends to increase the minimum arcing time resulting in a wider contact gap when the recovery voltage reaches its peak. The possible peak recovery voltage present on interruption could be a problem (see 9.5.3.3).

9.7.4.3 Capacitor banks

The same remark as given under 9.7.4.2 applies to capacitor bank currents. The current is dependent on the size of the capacitor bank and, in certain cases, the capacitor bank

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considered may have a current rating higher than that given in Table 9 of IEC 62271-100:2008. This does not pose a problem for circuit-breakers of present design.

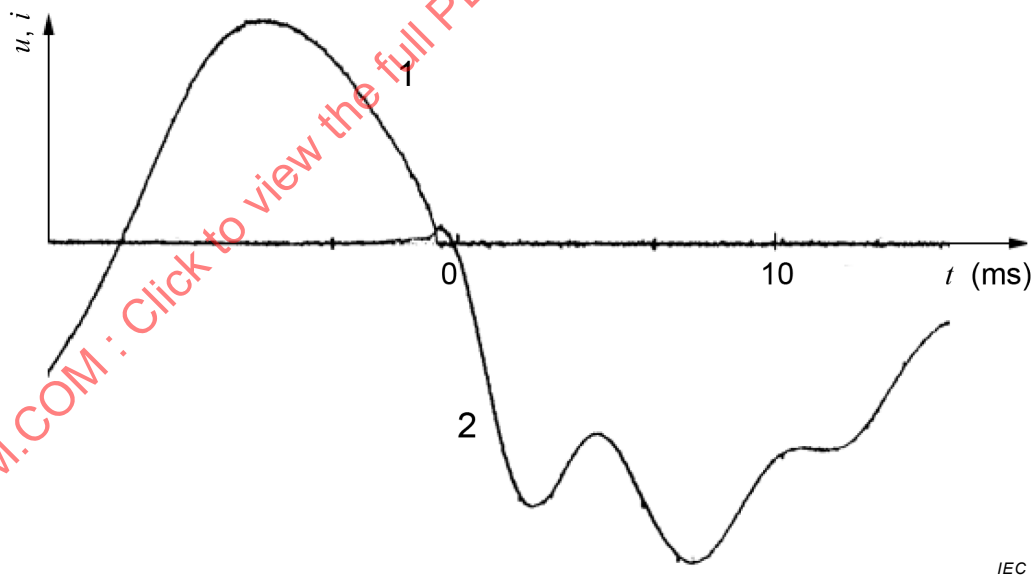
9.7.5 Voltage and earthing conditions of the network

Subclause 6.111.7 of IEC 62271-100:2008 gives the multiplication factors for single-phase tests for the different conditions, refer to 9.6. They range from 1,0 for solidly earthed systems to 1,7 for non-effectively earthed systems in the presence of single- or two-phase to earth faults.

Both user and manufacturer should be aware of these earthing conditions in order to specify the correct circuit-breaker suitable for the application.

Harmonic filter switching usually results in a recovery voltage that contains several harmonic components. The recovery voltage may have a shape as indicated in Figure 122. Careful system study should be done to define realistic requirements regarding the recovery voltage. In some cases, filter banks switching tests may need to be performed because capacitor bank switching tests do not cover the required recovery voltage waveshape. This needs to be considered when making the proper choice of circuit-breaker. From the voltage waveshape as indicated in Figure 122, it can be seen that the usual definition of re-ignition and restrike may no longer apply to a recovery voltage that does not have a 1-cosine waveshape.

In the case of a multi-frequency recovery voltage, the definition of re-ignition and restrike should be based on the amplitude of the breakdown voltage. If the amplitude is less than 1,0 p.u. of the system voltage, it is a re-ignition. If the amplitude is equal to or above 1,0 p.u. of the system voltage, it is a restrike. These definitions of restrike and re-ignition are generally acceptable but may lead to expensive solutions. More economical solutions may be obtained by permitting restrikes in a zone where tests have demonstrated that they are not harmful to the circuit-breaker.



Key

1 Current through circuit-breaker

2 Voltage across circuit-breaker

Figure 122 – Example of the recovery voltage across a filter bank circuit-breaker

9.7.6 Restrike performance

See 3.3.

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9.7.7 Class of circuit-breaker

The choice of the class of circuit-breaker is discussed in 3.3.

9.7.8 Transient overvoltages and overvoltage limitation

9.7.8.1 General

An important consideration for application of circuit-breakers for capacitive current switching is the transient overvoltage that may be generated by restrikes during the opening operation. The transient overvoltage factor is defined as the ratio of the transient voltage appearing between a circuit-breaker disconnected terminal and the neutral of the disconnected capacitance during opening to the operating line-to-neutral crest voltage prior to opening.

The selection of the class (see 9.7.7) of circuit-breaker to be applied should be coordinated with the insulation capability of other components on the system.

9.7.8.2 Overvoltages

9.7.8.2.1 General

When switching capacitive currents, transients are generated. These transients are associated with the restrikes when de-energising a capacitive load and with energisation of capacitive loads. These transients may cause:

– insulation degradation and possible failure of the substation equipment;
– operation of surge arresters;
– interference in the control wiring of the substation;
– increase in step potentials in substations;
– undesired tripping or damage to sensitive electronic equipment.

The magnetic fields associated with high inrush currents during back-to-back energisation of either the no-load transmission line conductors or the earthing grid during back-to-back switching can induce voltages in control cables by both capacitive and electromagnetic coupling. These induced voltages can be minimized by shielding the cables and using a radial configuration for circuits (circuits completely contained within one cable so that inductive loops are not formed).

9.7.8.2.2 Switching of capacitor banks

9.7.8.2.2.1 General

The switching of capacitor banks is associated with voltage and current transients. As most modern circuit-breakers have a very low probability of restrike, the majority of the switching transients will be generated when energizing capacitor bank(s). The effects of the transients will exhibit themselves locally and at remote locations on the power system.

The high-frequency transient inrush current associated with back-to-back switching can stress other equipment in the circuit as well as the circuit-breaker. Wound-type current transformers will have turn-to-turn insulation stressed because of the high rates of rise of current and the resulting voltage that is developed across inductance in the circuit.

9.7.8.2.2.2 Local effects

– voltage transients resulting in dielectric stresses on nearby equipment;
– electrical, mechanical and electromechanical forces caused by the inrush current.

9.7.8.2.2.3 Remote effects

– transfer of capacitively coupled fast transients through transformer windings;

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– reflections of travelling wave transients on open ended lines or transformer terminated lines;

– excitation of near resonant portions of the power system by the oscillatory transient frequency.

9.7.8.2.3 Switching of lines and cables

When energizing lines and cables, high overvoltages may be created depending on whether or not the line or cable was precharged as a result of a preceding breaking operation (i.e. in the case of an auto-reclosing). These overvoltages may result in damage of insulation.

9.7.8.3 Overvoltage limitation

There are several means available to reduce the overvoltages generated by the switching of capacitive currents:

– **current limiting reactors** are normally used to reduce the current transients associated with back-to-back switching. They do not limit the remote overvoltages.

– **pre-insertion resistors** limit the inrush current and remote overvoltages. It is a basic solution used on circuit-breakers. They are usually fitted on circuit-breakers and as such add to the complexity of the equipment. Depending on the design, the added complexity may or may not result in a reduced availability of the equipment (see also 9.7.16).

– **pre-insertion reactors** also limit the inrush current and remote overvoltages. They are usually fitted on circuit-switchers and their effect on complexity and availability of the equipment is sometimes equivalent to pre-insertion resistors, depending on the design of the devices.

– **controlled closing** reduces the magnitude of the inrush current depending on the point-on-wave of the voltage prior to the prestrike between the contacts. A simple way of reducing the transients is to let the circuit-breaker contacts close at a voltage zero. This method is called controlled closing. The controller also adds to the complexity of the equipment and can influence its availability.

9.7.9 No-load overhead lines

9.7.9.1 General

A circuit-breaker may be required to energise or de-energise a no-load transmission line during its normal operating duties. Prior to energisation, the line may or may not contain a trapped charge (see also 9.5.3). Consideration may need to be given to line energisation following load rejection (see [127]).

9.7.9.2 Line charging current

When considering the assigned line charging current rating, application is determined by the value of the line charging current. This current is a function of system voltage, line length, and line configuration (see also 9.5.1.1).

9.7.9.3 Compensated overhead lines

As described in 9.5.2 very long lines (> 200 km) are often compensated with shunt reactors to reduce the amount of charging current required of the system.

If the circuit-breaker rating is chosen based on I_{Lc}, the line could not be switched without the compensating reactor(s) connected. The voltage rise caused by the Ferranti effect and also the location of the reactor(s) will change the line current slightly.

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9.7.9.4 No-load line recovery voltage

The line-charging breaking current rating is assigned on the basis of a standard recovery voltage associated with this type of circuit. For solidly earthed systems, the no-load line charging current switching tests require a maximum voltage of 2,4 times (see also 9.5.1.2) the rated phase-to-earth voltage across the circuit-breaker one half-cycle after interruption (assumes $C_1 = 2C_0$ where C_1 is the positive-sequence capacitance and C_0 is the zero-sequence capacitance). This is the difference voltage of the source and line sides, including the effects of coupled voltage on the first-pole-to-clear. The test voltage requires a 1-cosine waveshape.

For double circuit lines with higher voltage factors refer to 9.6.

Deviations from the test voltage characteristics may increase or decrease the probability of the circuit-breaker restriking. As described in 9.5.2, a compensated line will have a lower rate-of-rise of the recovery voltage, which will reduce the restrike probability.

9.7.10 Capacitor banks

9.7.10.1 General

A circuit-breaker may be required to switch a capacitor bank from a bus that does not have other capacitor banks energised (single) or against a bus that has other capacitor banks energised (back-to-back). In the application of circuit-breakers for capacitor switching duty, consideration should be given to the preferred single shunt capacitor bank switching current, preferred back-to-back shunt capacitor bank switching current, preferred transient inrush current, and preferred transient inrush current frequency (see also 9.3.2 and 9.2.2).

9.7.10.2 Capacitor bank current

Circuit-breakers are to be applied according to the actual capacitive current they are required to interrupt. The rating should be selected to include the following effects.

a) *Voltage.* The reactive power rating of the capacitor bank, in kvar, is to be multiplied by the ratio of the maximum service voltage to the capacitor bank nameplate voltage when calculating the capacitive current at the applied voltage. This ratio can be as large as 1,1, since capacitors can be operated continuously up to 10 % above the capacitor rated voltage.

b) *Capacitor tolerance.* The manufacturing tolerance in capacitance is −0 to +15 % with a more frequent average of −0 to +5 %. A multiplier in the range of 1,05 to 1,15 should be used to adjust the nominal current to the value allowed by tolerance in capacitance.

c) *Harmonic component.* Capacitor banks provide a low-impedance path for the flow of harmonic currents. When capacitor banks are non-effectively earthed, no path is provided for zero-sequence harmonics (third, sixth, ninth, etc.), and the multiplier for harmonic currents is less. A multiplier of 1,1 is generally used for a solidly earthed neutral bank and 1,05 for a non-effectively earthed neutral.

In the absence of specific information on multipliers for the above factors, it will usually be conservative to use a total multiplier of 1,25 times the nominal capacitor current at rated capacitor voltage for non-effectively earthed neutral operation and 1,35 times the nominal current for solidly earthed neutral operation.

9.7.10.3 Methods for calculating transient inrush currents

9.7.10.3.1 General

The capacitor bank being switched is assumed uncharged, with closing at a voltage crest of the source voltage. The current used should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of

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capacitance. In the absence of specific information, a multiplier of 1,15 times normal capacitor current would give conservative results.

9.7.10.3.2 Single capacitor bank

A bank of shunt capacitors is considered single when the conditions described in 9.3.3.1 are fulfilled. Table 44 gives the equations that apply for calculation of the inrush current for single capacitor bank energisation, neglecting resistance.

Table 44 – Inrush current and frequency for switching capacitor banks

Duty	Quantity	Equation
Energisation of single bank	$i_{\text{i peak}}$ (A)	$\frac{\sqrt{2}U_{\text{r}}}{\sqrt{3}} \times \sqrt{\frac{C}{L_{\text{s}}}}$
	f_{i} (Hz)	$\frac{1}{2\pi\sqrt{L_{\text{s}}C}}$
Back-to-back switching	$i_{\text{i peak}}$ (A)	$\frac{\sqrt{2}U_{\text{r}}}{\sqrt{3}} \times \sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}}$
	f_{i} (Hz)	$\frac{1}{2\pi\sqrt{L_{\text{eq}}C_{\text{eq}}}}$

Key

U_{r}: rated voltage (V)*
C: bank capacitance (F)*
L_{s}: source inductance (H)*
C_{eq}: equivalent capacitance (F)**
L_{eq}: equivalent inductance (H)**
* See 9.3.3.1.
** See 9.3.3.2.

9.7.10.3.3 Back-to-back capacitor bank

The inrush current of a single bank will be increased when other capacitor banks are connected to the same bus (see also 9.3.3.2).

Table 44 gives the equations for calculating inrush current and frequency for back-to-back capacitor bank switching, neglecting resistance. These equations are based on the theory described in 9.2.2.

A typical circuit for back-to-back switching is shown in Figure 123. The inductance in the circuit that limits the transient oscillatory current is composed of the inductance of the bus between switching devices, L_{bus}, the inductance between the switching device and the capacitor banks, L_1 and L_2, and the inductance of the capacitor banks, L_{c1} and L_{c2} and any additional reactance inserted. The total inductance between capacitor banks, L_{c1} + L_1 + L_{bus} + L_2 + L_{c2}, is very small with respect to the inductance of the source L_{s}. In most cases, the total inductance between capacitor banks will be less than 1 % of the inductance of the source, and the contribution of transient current from the source can be neglected.

The inductance of the bus can be calculated similar to a transmission line using values from tables available from suppliers of bus conductors for different bus configurations (see 9.7.10.3.4).

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The inductance within the capacitor bank itself is not easy to obtain, but in general it is of the order of 10 µH for banks above 52 kV, and 5 µH for banks below 52 kV. Typical values of inductance per phase between back-to-back capacitor banks and bank inductance for various voltage levels are given in Table 45.

Table 45 – Typical values of inductance between capacitor banks

Rated maximum voltage (kV)	**Inductance per phase of busbar** (µH/m)	**Typical inductance between banks** [a] (µH)
17,5 and below	0,702	10 to 20
36	0,781	15 to 30
52	0,840	20 to 40
72,5	0,840	25 to 50
123	0,856	35 to 70
145	0,856	40 to 80
170	0,879	60 to 120
245	0,935	85 to 170

[a] Typical values of inductance per phase between capacitor banks. This does not include inductance of the capacitor bank itself. Values of 5 µH for banks below 52 kV and 10 µH for banks above 52 kV are typical for the inductance of the capacitor banks.

Inherent resistance of the circuit causes rapid decay of the transient current so that the first peak actually may only reach 90 % to 95 % of the maximum value calculated. These values are applicable to both solidly earthed or isolated capacitor banks and with Y or Δ connections. With a non-effectively earthed neutral, the current in the first two phases to close will be 87 % of calculated, but the current in the last phase will equal the value calculated. However, inherent resistance of the circuit will affect these currents by the factors indicated above.

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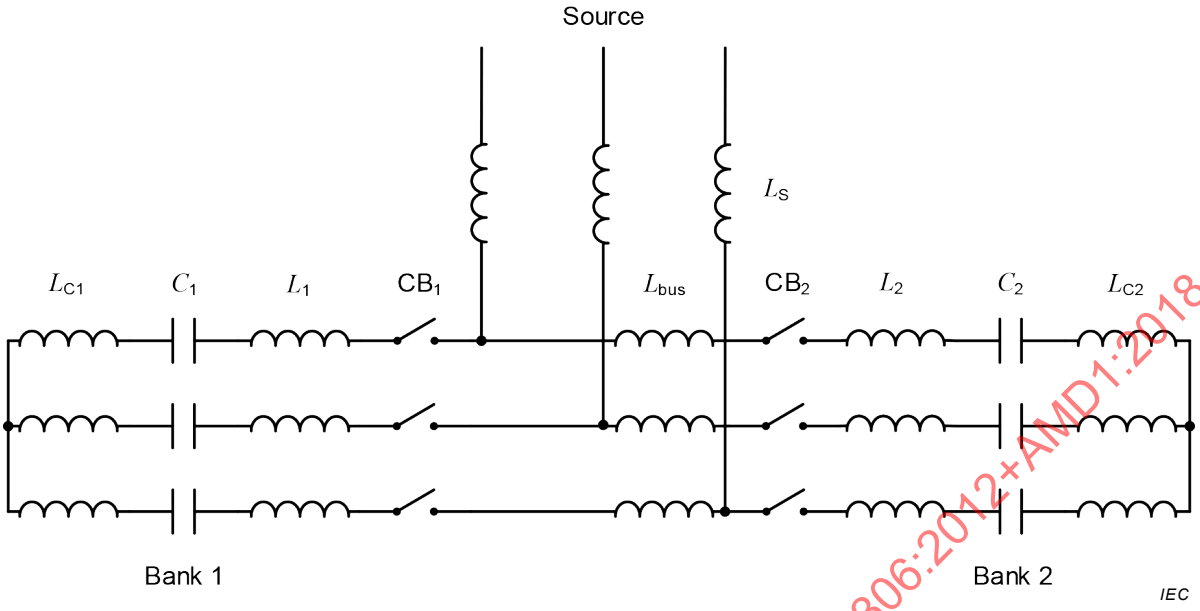

Key

CB_1	circuit-breaker energizing capacitor bank 1
CB_2	circuit-breaker energizing capacitor bank 2
L_S	source inductance
C_1	capacitor bank 1
C_2	capacitor bank 2
L_{C1}, L_{C2}	capacitor bank inductance
L_1, L_2	bus inductance between switching device and capacitor bank
L_{bus}	inductance of bus between switching devices

Figure 123 – Typical circuit for back-to-back switching

The equations in Table 44 for back-to-back switching will give correct results when switching a bank against another bank. However, when switching against several other banks connected to the bus, the correct value of equivalent inductance to be used for the combination of banks connected to the bus is not easily obtained. For example, when switching a bank against three other banks energised on the bus, the calculated current will be too high if an inductance of $L/3$ is used. On the other hand, using a value of $3L$ will result in a current that is too low. If exact solutions cannot be made, conservative results should be used in calculating inrush currents by using the inductance divided by the number of capacitor banks, recognizing that the results will be 20 % to 30 % higher (see also 9.3.3.2). When more than two banks are installed on the same bus, a more exact calculation of the inrush current parameters is obtained using an electromagnetic transient program.

9.7.10.3.4 Considerations for transient inrush currents

The inrush currents of different types of compact multi-section banks with minimum spacing between the individual sections may differ by as much as 20 %. Consequently, these inrush currents can be reduced significantly by increasing the lengths (inductance) of the circuits between the sections.

Another effective measure to reduce transient inrush currents is to add inductance in the circuit between the capacitor banks.

In IEC 62271-100:2001, the equivalency rule between the test performed and the service conditions was based on the product of inrush current peak and frequency, $i_{i\ peak} \times f_i$ (kAkHz). Calculations have shown that the arc energy during a making operation is independent of the inrush current frequency for cases where the pre-arcing time is greater than half a period of the inrush current frequency. This is usually the case for back-to-back

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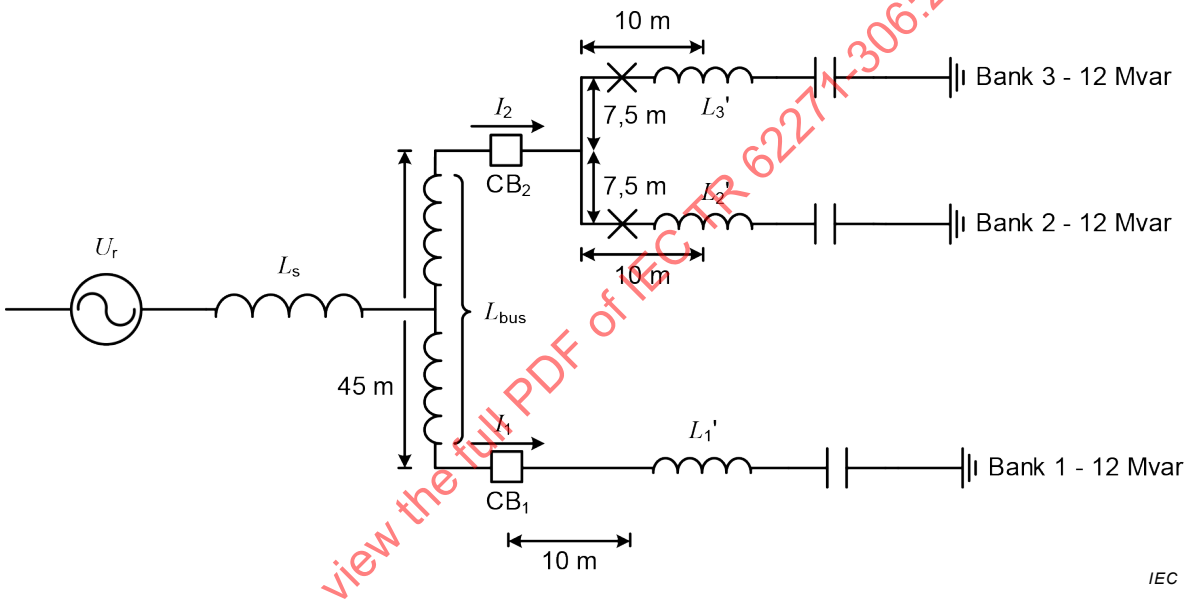
capacitor bank switching. For back-to-back capacitor bank switching, the arc energy during a making operation is only a function of the inrush current peak. On the other hand, it is well known that the shape of the wear on the arcing contacts as well as the effect of the pressure shock waves are somewhat frequency-dependent and should not be disregarded. Because of the latter, an upper tolerance of +130 % has been specified on the permissible inrush current frequency that can be used in service. In other words: the inrush current frequency used during the tests should not be lower than 77 % of the inrush current frequency foreseen in service. This concept is limited to inrush current frequencies up to 6 kHz since the information available for higher frequencies is limited.

Although circuit-breakers have usually been tested with inrush current peaks up to 20 kA and 4,25 kHz, system designers should endeavour to keep the inrush currents far below this value for system quality reasons.

The following example will illustrate the use of the equations in Table 44.

A 123 kV system is assumed as shown in Figure 124.



Key

U_r	123 kV (the rated capacitor bank voltage is 115 kV)
L_S	Source inductance is 3,77 Ω, 10 mH (f_s = 60 Hz)
L_1', L_2', L_3'	Inductance between circuit-breaker and capacitor bank; including inductance of capacitor bank
L_{bus}	Inductance of bus between switching devices
CB$_1$, CB$_2$	Circuit-breakers
	Short-circuit of source: 18 600 A at 123 kV

Figure 124 – Example of 123 kV system

The capacitor banks shown have a nominal rating of 12 Mvar (capacitors rated 100 kvar, 13,28 kV, 5 series sections with eight capacitors in parallel per phase). Nominal current per bank is 60 A. In determining the rating of the circuit-breaker required, the increase in current due to applied voltage, capacitance tolerance, and harmonics should be considered. The increase in current at maximum rated voltage is: maximum voltage to capacitor rated voltage = 123/115 = 1,07. Assume a positive tolerance of capacitors of +10 %, multiplier of 1,1 and assume a multiplier for harmonic content for a solidly earthed neutral bank of 1,1.

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The total multiplier used to determine the single and back-to-back current rating is 1,07 × 1,1 × 1,1 = 1,29, giving a current of 1,29 x 60 = 78 A. With capacitor banks 2 and 3 energised, the current through CB_2 is 156 A.

The circuit-breakers intended for this duty have the following ratings: rated voltage 123 kV, rated current 1 600 A, rated short-circuit current 40 kA, rated single and back-to-back capacitive switching current 400 A.

The transient inrush current and frequency are calculated using the equations in Table 44. In the example, L_1', L_2' and L_3' are the inductances between the respective capacitor banks and the circuit-breakers, including the inductance of the capacitor bank. L_{bus} is the inductance of the bus between the circuit-breakers.

The inductance values in Table 45 can be used or values can be calculated for the actual bus configuration used. In the example given below, the added reactance between the circuit-breaker and capacitor bank is:

L_1' = 20,0 µH

L_2' = L_3' = 27,1 µH

The inductance of the busbar L_{bus} = 38,5 µH.

In determining inrush current and frequency, the currents I_1 and I_2 as used in Table 44 should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of capacitance. In the example, the multiplier to be used is 1,07 × 1,1 = 1,18. The currents are I_1 = 60 × 1,18 = 71 A and I_2 = 71 A or 142 A, depending on whether bank 2 or 3 or both banks are energised.

Case I. Energisation of capacitor bank 1 with banks 2 and 3 not energised (single bank switching).

Bank capacitance C for calculation:

$$C = 1{,}1 \times \frac{\text{Mvar}}{\omega U_r^2}\,(\text{F}) \text{ with } U_r \text{ in kV} \rightarrow C = 1{,}1 \times \frac{12}{377 \text{ x } (115)^2} = 2{,}65\ \mu\text{F}$$

L_s = 10 mH

$$i_{ipeak} = \frac{\sqrt{2}\left(123 \times 10^3\right)}{\sqrt{3}} \times \sqrt{\frac{2{,}65 \times 10^{-6}}{10 \times 10^{-3}}} = 1\ 635\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{10 \times 10^{-3} \times 2{,}65 \times 10^{-6}}} = 977\ \text{Hz}$$

This is less than the maximum rate of change for a rated short-circuit current of 40 kA which is equal to $2\pi f_s \sqrt{2} I_{sc} = 21{,}3$ A/µs and therefore meets the requirements of single capacitor bank switching.

Case II. Energisation of bank 1 with bank 2 energised on the bus (back-to-back switching against an equal size bank).

$$C_{eq} = \frac{2{,}65}{2} = 1{,}325\ \mu\text{F}$$

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L_{eq} = 20 + 38,5 + 27,1 = 85,6 µH

$$i_{ipeak} = \frac{\sqrt{2}(123\times10^{3})}{\sqrt{3}} \times \sqrt{\frac{1{,}325\times10^{-6}}{85{,}6\times10^{-6}}} = 12\,495\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{85{,}6\times10^{-6}\times1{,}325\times10^{-6}}} = 14\,944\ \text{Hz}$$

The calculated back-to-back inrush current and frequency should be compared with the back-to-back switching capability listed in Table 5 of IEC 62271-100:2008. For a maximum voltage of 123 kV, the assumed rated values are 20 kA for the peak current and 4,25 kHz for the inrush current frequency. The calculated value of the inrush current peak is within this rating, the inrush current frequency exceeds that assumed and inductance should be added between the capacitor banks to reduce the inrush current frequency. Adding an inductance of 1 mH will limit the inrush current to 3,5 kA and the frequency to 4,18 kHz, both of which are below the assumed capability.

Case III. Energisation of bank 1 with banks 2 and 3 energised on the bus.

$$C_{eq} = \frac{(2{,}65+2{,}65)2{,}65}{(2{,}65+2{,}65)+2{,}65} = 1{,}76\ \mu\text{F}$$

$$L_{eq} = \frac{(27{,}1)}{2} + 38{,}52 + 20 = 72{,}07\ \mu\text{H}$$

$$i_{ipeak} = \frac{\sqrt{2}(123\times10^{3})}{\sqrt{2}} \times \sqrt{\frac{1{,}76\times10^{-6}}{72{,}07\times10^{-6}}} = 15\,694\ \text{A}$$

$$f_i = \frac{1}{2\pi\sqrt{72{,}07\times10^{-6}\times1{,}76\times10^{-6}}} = 14\,131\ \text{Hz}$$

Of the calculated values of inrush current peak and frequency, the frequency of 14,1 kHz exceeds the assumed back-to-back switching capability of 4,25 kHz listed in Table 9 of IEC 62271-100:2008. As in the previous case of switching identical banks, adding an inductance of 0,71 mH will limit the inrush current peak to 4,7 kA and the inrush current frequency to 4,3 kHz, both of which are below the assumed back-to-back switching capability of a 123 kV circuit-breaker.

Based on the system and conditions studied, a circuit-breaker having the following ratings would be applied: rated short-circuit current of 40 kA and rated single capacitor bank switching current of 400 A. The assumed back-to-back rating of 20 kA and 4,25 kHz that goes with this rating will be exceeded unless additional inductance is added between the capacitor banks. A value of 0,71 mH is sufficient to keep within the assumed ratings available.

9.7.11 Switching through transformers

Circuit-breakers may be required in some applications to switch capacitors, lines, or cables through an interposed transformer. The current switched by the circuit-breaker will be N times the capacitor, line, or cable current on the other side of the transformer, where N is the transformer turns ratio.

Switching charging current through a transformer may be less difficult than switching the same current directly. The capacitive elements of the circuit will oscillate with the transformer

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inductance, which may also saturate, producing a less severe transient recovery voltage and a lower probability of restrike. If a restrike should occur, the additional inductance will help to limit the inrush current. Saturation may also occur when de-energizing a remote transformer that is fed through a long cable. The stress on the transformer is not considered harmful.

If the value of N is greater than 1, switching through a transformer will have the effect of increasing the current being switched. De-energizing no-load overhead lines with lower voltage circuit-breakers can result in effective line charging currents in the 750 A to 1 000 A range. The capacitive switching rating of circuit-breakers which may be exposed to this type of duty should be carefully checked before application is made.

Figure 125 shows the voltage and current relations that are the result of a single-phase simulation of capacitor switching through an interposed transformer. It can be seen that due to the reduced recovery voltage, the increased current is not a problem for the circuit-breaker.

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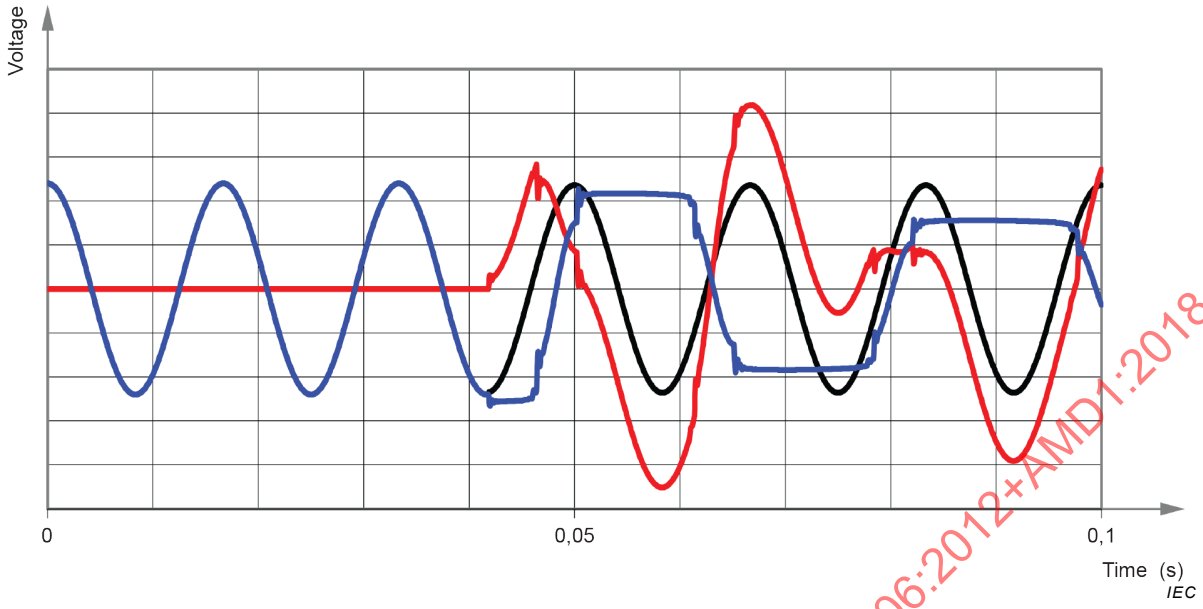
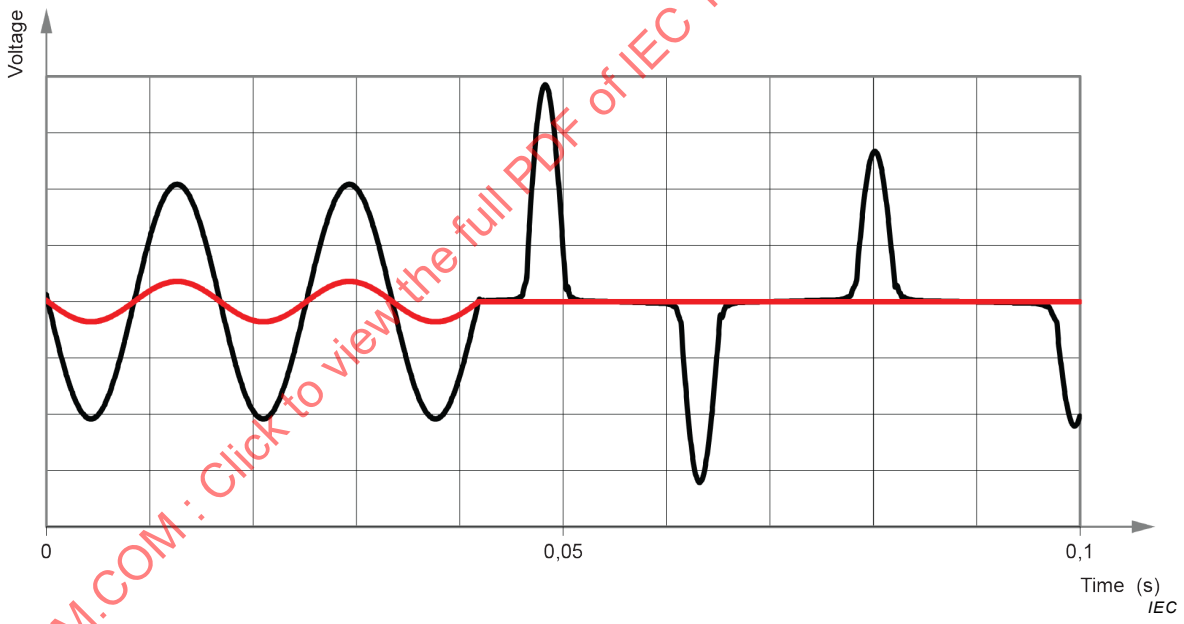


Black line	Source voltage
Blue line	Voltage on the load side of the circuit-breaker
Red line	Voltage across the circuit-breaker

Figure 125a – Voltage relations



Black line	Capacitor bank current (low voltage side of the transformer)
Red line	Current through the circuit-breaker

Figure 125b – Current relations

Figure 125 – Voltage and current relations for capacitor switching through interposed transformer

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9.7.12 Effect of transient currents

9.7.12.1 General

In the application of circuit-breakers in stations having banks of capacitors, it may be necessary to investigate the effects of transient currents and other special situations upon

circuit-breakers other than those specially equipped for and assigned to the routine capacitor switching.

The transient currents of capacitor banks may be considered in two aspects: the inrush currents energisation of the banks and the discharge currents into faults. Where the quantity of parallel capacitor banks installed in a station is large, the transient currents may have significant effects upon the circuit-breaker.

The transient currents may have large peaks and high frequencies which may affect circuit-breakers in the following ways:

a) a circuit-breaker may be subjected to a transient inrush current that exceeds its rating. This may occur with the circuit-breaker in the closed position or when closing into solidly earthed faults;

b) the transient inrush current may have sufficient magnitude and rate of change to flash over the secondaries of current transformers or the associated control wiring.

Circuit-breakers located in a position such as a tie circuit-breaker between bus sections (bus section or bus coupler) may be exposed to the transient inrush currents from energizing banks of capacitors when they are located on bus sections on both sides of the circuit-breaker (see Figure 126, CB_1).

The inrush current will seldom exceed the capability of the circuit-breaker. However, a check may be required to determine if the rate of change of inrush current will cause overvoltages on the secondary of current transformers on the circuit-breaker or in the current path between the capacitor banks.

9.7.12.2 Exposure to total capacitor bank discharge current

In a substation where parallel capacitor banks are located near or on a busbar, any circuit-breaker connected to the bus may be exposed during faults to the total discharge current of all the banks located behind the circuit-breaker. In Figure 126, CB_2 will be subjected to this total discharge current with a fault occurring at location A. The worst case, or highest capacitor discharge current, occurs with a bolted three-phase fault where capacitor banks are non-effectively earthed and for a case of a three phase-to-earth or a line-to-earth fault where capacitor banks are solidly earthed.

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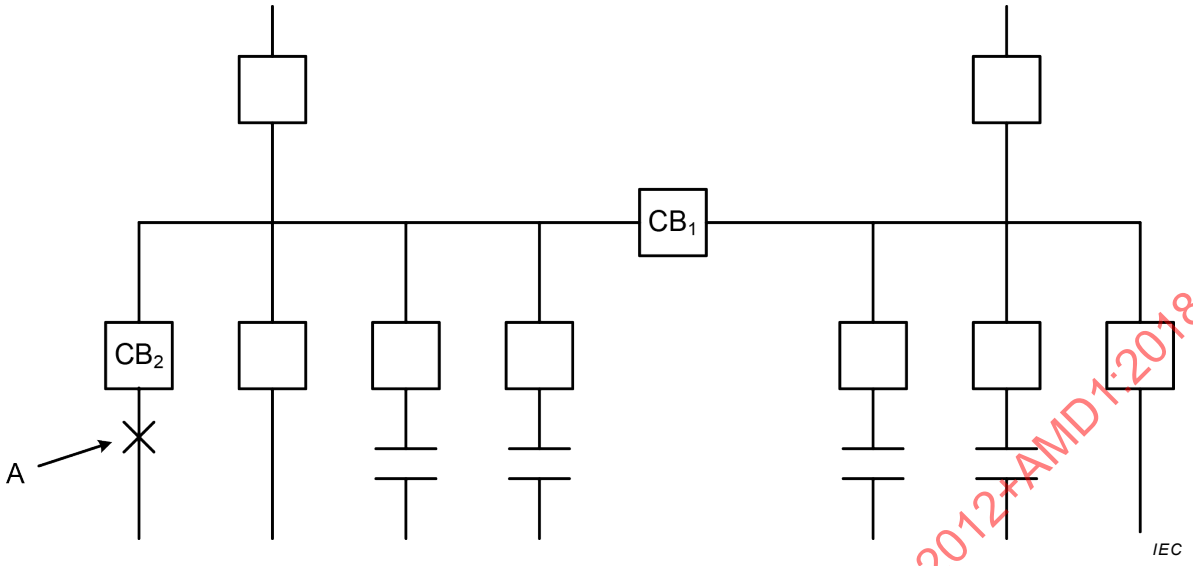

Key

CB_1, CB_2 Circuit-breakers

Figure 126 – Station illustrating large transient inrush currents through circuit-breakers from parallel capacitor banks

The total discharge current (peak) of all banks behind the circuit-breaker is equal to the algebraic sum of the individual banks of capacitors. Neglecting resistance, the discharge current of an individual capacitor bank is equal to:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{C}{L}} \tag{33}$$

where

$I_{\text{d peak}}$ is the crest value of discharge current;

U_{r} is the rated voltage;

C is the capacitance per phase of individual bank;

L is the inductance per phase between capacitor bank and fault location.

The inductance L is primarily made up of bus conductors and any additional inductance added to the bank for limiting the inrush currents.

If there are n capacitor banks of approximately equal capacitance and separated by an approximately equal inductance to the fault, then the total discharge current is approximately equal to the sum of the crest current of each bank or n times that of one bank. This is demonstrated as follows:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{Cn}{L/n}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} n \sqrt{C/L} \tag{177}$$

In addition to the checking of the crest current, it may be necessary also to check the rate of change of the discharge current with the manufacturer.

The transient discharge current passing through a circuit-breaker should also be examined for its effects upon the current transformers. The discharge currents may substantially exceed the magnitudes and the frequency of the inrush currents described in Table 9 of

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IEC 62271-100:2008. This occurs because the contribution may come from a number of capacitor banks and is not limited by the inrush impedance seen when energizing a bank of capacitors.

9.7.13 Exposure to capacitive switching duties during fault switching

Where parallel banks of capacitors are located on bus sections in a station, caution should be exercised in the fault switching sequence so that the last circuit-breaker to clear is not subjected to a capacitive switching duty beyond its capability. This is especially a concern for a circuit-breaker used as a bus section tie circuit-breaker with capacitors located on both sides of the circuit-breaker as shown in Figure 126, CB_1.

The worst case occurs in a station where the bus section tie circuit-breaker is last to clear the bus for a fault that leaves one or more phases of the capacitor banks fully energised. In this situation, the bus tie circuit-breaker should be properly equipped and rated for the parallel switching of the capacitor banks remaining on the bus section to be de-energised. In the example of Figure 126, this means that the tie circuit-breaker should be capable of switching two banks of capacitors in parallel with two banks of capacitors on the source side. Another solution is to coordinate if possible the clearing times so that the tie circuit-breaker is always first to clear to avoid the capacitor switching duty.

9.7.14 Effect of load

The situation can occur where a circuit-breaker is called upon to switch a combination of a capacitive current and a load current. The circuit-breaker will have the required switching capability if the total current does not exceed the rated continuous current of the circuit-breaker and either

a) the power factor is at least 0,8 leading, or

b) the capacitive current does not exceed the rated capacitive switching current of the circuit-breaker.

Where the above conditions are exceeded, the capability and performance of the circuit-breaker is not defined by the standards and the manufacturer should be consulted. When the power factor is below 0,8 leading, the voltage may be sufficiently out-of-phase with the current to cause unacceptable restriking. The situation will be more severe if there is also a bank of capacitors located on the source side of the circuit-breaker.

9.7.15 Effect of reclosing

Up to twice normal inrush currents are possible when reclosing is applied to a circuit-breaker switching capacitive loads. When capacitor bank current is interrupted at or near a normal current zero, the voltage remaining on the bank may be near peak value. Reclosing a circuit-breaker against such a charged capacitor bank may produce high inrush current.

When a capacitor bank is connected to the load side of a feeder circuit-breaker equipped with automatic reclosing, high inrush currents can be avoided by isolating the capacitor bank from other loads after the circuit-breaker is tripped and before reclosing. The switching device used for regular capacitor bank switching can be employed for isolation. This technique is particularly recommended where other capacitor banks are connected to the same station bus.

A second technique to avoid high inrush currents during reclosing is to increase reclosing time delay. Normally, the discharge resistors inside each capacitor unit, or other deliberately introduced discharge devices will reduce residual voltage.

Discharge curves are available from the capacitor supplier and should be consulted where reclosing time is delayed.

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9.7.16 Resistor thermal limitations

For capacitor bank circuit-breakers equipped with pre-insertion resistors, the thermal capability of the resistors should be considered in determining the time interval between capacitive current switching operations. The resistance value is related to the size of the capacitor bank and the pre-insertion resistors should normally have a thermal capability as defined by the rated operating sequence.

If capacitive current switching field tests are planned which exceed the number of operations as defined by the thermal capacity of the pre-insertion resistors, or which utilize a specially designed circuit-breaker, the manufacturer should be consulted regarding the frequency of operations.

9.7.17 Application considerations for different circuit-breaker types

9.7.17.1 General

The switching of capacitive current poses different stresses on the different types of circuit-breakers. Restrikes on opening and prestrikes on closing may or may not be a problem. The considerations given below are general and are based on experiences gained by laboratory tests, field tests and field experience.

9.7.17.2 Oil circuit-breakers

9.7.17.2.1 Restrikes

Depending on the design (contact speed, electrode shape, etc.), an oil circuit-breaker generally has long arcing times when interrupting. The restrike probability increases with increased current, because gas bubbles reduce the effective amount of oil between the contacts causing a reduction of the dielectric strength of the contact gap. These circuit-breakers deserve special consideration when used or relocated to a system where the line charging current exceeds the rating.

Some oil circuit-breakers are pressurized to reduce the size of the bubbles and therewith increasing the dielectric strength of the contact gap. Some oil circuit-breakers may be fitted with opening resistors, to reduce the effects of a restrike.

An oil circuit-breaker will normally not interrupt the high-frequency current associated with the restrike and the high arc impedance introduces an additional damping of the restrike current. This will reduce the risk for multiple restrikes.

Older contraction type oil circuit-breakers are known to produce multiple restrikes that may result in voltage escalation and subsequent development of an evolving fault.

9.7.17.2.2 Prestrikes

Oil circuit-breakers are especially sensitive to high-frequency prestrikes when energizing capacitor banks. The prestrikes cause a shock wave in the oil. As oil is not compressible, the shock wave causes mechanical stresses on the internal components of the breaking chamber. As a result of the exposure to these high mechanical stresses, the breaking chamber insulator may shatter and even stationary contacts may crack. Application of an oil circuit-breaker for capacitor bank switching requires a severe reduction of the inrush current frequency or special design of the oil circuit-breaker (e.g. using pre-insertion resistors).

Bulk oil circuit-breakers have been applied using a limitation of 20 kAkHz for over 30 years with no documented problems.

For minimum oil circuit-breakers, a value of 1 kAkHz is suggested.

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9.7.17.3 Vacuum circuit-breakers

9.7.17.3.1 Restrikes

The voltage withstand of the contact gap of a vacuum circuit-breaker rises very fast and the restrike probability is low. When a restrike occurs, the contact gap is small and the vacuum circuit-breaker is usually capable of interrupting the high-frequency restrike current, which may result in voltage escalation.

9.7.17.3.2 NSDDs

NSDDs (see 9.2.1.3) are normally associated with vacuum circuit-breakers and are generally not a concern.

9.7.17.3.3 Prestrikes

The duration of the prestrike in a vacuum circuit-breaker is short. Shock waves are not a problem for this type of circuit-breaker.

The high-frequency discharge together with contact bouncing may lead to micro contact melting, especially when the arc is burning in the anode-spot mode (this occurs with currents higher than 10 kA). The breaking of welded points during a subsequent breaking operation with a very low current can damage the contact surface and this may reduce the dielectric withstand of the contact gap. However, a subsequent breaking operation with higher current may increase the dielectric withstand to its original condition. A subsequent no-load operation may flatten the micro spot resulting in an increased dielectric strength.

9.7.17.4 SF_6 circuit-breakers

9.7.17.4.1 Restrikes

The interrupting capacity of SF_6 circuit-breakers is limited by the recovery voltage, which means that the frequency and earthing conditions (i.e. whether the circuit is effectively or non-effectively earthed) are important factors in the determination of the capability of the circuit-breaker.

The capacity of clearing the high-frequency restrike current is low for puffer circuit-breakers and even lower for self-blast (or arc assisted) circuit-breakers. This also means that the risk for voltage escalation is low. However, a restrike may cause tracking and/or puncture of the insulating material between the contacts (e.g. nozzle, sleeve, etc.).

9.7.17.4.2 Prestrikes

The duration of the prestrike is depending on the voltage per breaking unit and the closing speed. In general this duration is short. Regarding the limit of inrush current peak and frequency there is referred to 9.7.10.3.4.

9.7.17.5 Air-blast circuit-breakers

9.7.17.5.1 Restrikes

In general, the restrike probability of an air-blast circuit-breaker is higher than that of an SF_6 circuit-breaker. The flashover characteristic of air has a wider scatter than that of SF_6. Air-blast circuit-breakers can interrupt the high-frequency discharge current, which means that they have a higher probability of multiple restrikes, which may lead to voltage escalation.

9.7.17.5.2 Prestrikes

The considerations given in 9.7.17.4.2 also applies to air-blast circuit-breakers.

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9.8 Considerations of capacitive currents and recovery voltages under fault conditions

9.8.1 Voltage and current factors

Some requirements, general ratings and tests for capacitive current switching are based on switching operations in the absence of faults. The presence of a fault can increase the value of both the capacitive switching current and recovery voltage. This is recognized by IEC 62271-100 by the specification of two voltage factors when breaking in the presence of faults. These voltage factors are given in Annex S of IEC 62271-100:2008/AMD2:2017 and are 1,4 for effectively earthed systems and 1,7 for non-effectively earthed systems. Tests for these conditions are not mandatory. An example of such a fault is a circuit-breaker switching an overhead line that interrupts fault current in one phase and capacitive current in the other two phases.

The fact that the capacitive switching current increases in the presence of earth faults is recognized in Annex S of IEC 62271-100:2008/AMD2:2017, where the line and cable charging currents are multiplied by 1,25 for effectively earthed neutral systems and 1,7 for non-effectively earthed systems. The number of tests is reduced to reflect the fact that such operations do not occur frequently. The test procedure given in Annex S of IEC 62271-100:2008/AMD2:2017 is based on a class C1 test procedure (i.e. no pre-conditioning of the circuit-breaker) and is common for both class C1 and class C2 circuit-breakers.

For capacitor banks, the situation is different. No tests are required for switching of solidly earthed neutral single capacitor banks in solidly earthed neutral systems. Switching of non-effectively earthed neutral capacitor banks in solidly earthed neutral systems is not considered a normal system condition and no requirements or tests have been specified. Switching back-to-back is not considered a normal system condition and no requirements and tests have been specified.

9.8.2 Reasons for these specific tests being non-mandatory in the standard

In service, circuit-breakers have been successful in interrupting capacitive circuits under faulted conditions for a number of reasons. Principal reasons for successful operation include:

a) the probability of a fault occurring at minimum operating conditions of the circuit-breaker and its operating mechanism is extremely small;

b) the voltage factor used for single-phase tests is in excess of the service condition giving the tested circuit-breaker added margin;

c) laboratory tests are performed using a minimal voltage jump, resulting in short arcing times. This condition is more severe than the actual network condition where the voltage jump is generally higher.

9.8.3 Contribution of a capacitor bank to a fault

Consider the network situation given in Figure 126. A single line simplification is given in Figure 127. A fault has occurred on the line that is interrupted by the circuit-breaker (CB). The capacitance of the capacitor bank will modify the TRV across the circuit-breaker to a 1-cosine waveshape having a moderate rate-of-rise with a higher amplitude factor as compared to the case without the presence of the capacitor bank.

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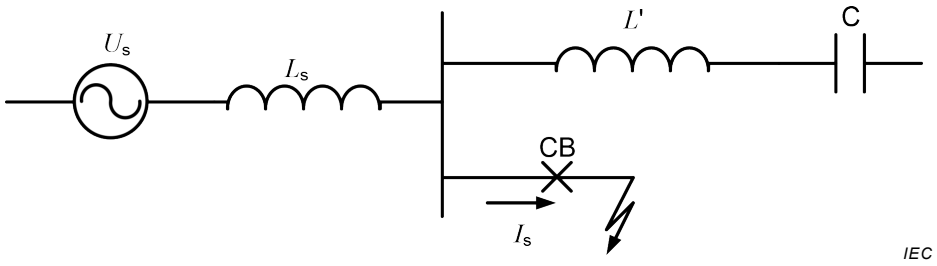

Key

U_s	Source voltage	CB	Circuit-breaker
L_s	Short-circuit inductance	I_s	Short-circuit current
L'	Busbar inductance		

Figure 127 – Fault in the vicinity of a capacitor bank

When the ITRV is negligible, the circuit-breaker will attempt to interrupt at the first available current zero following contact separation, resulting in a relatively small contact gap. As the recovery voltage increases across the gap, a re-ignition might occur and the capacitor bank will discharge into the fault through the circuit-breaker. The amplitude of the discharge current depends on the voltage across the circuit-breaker contacts at the time of re-ignition and the frequency of the discharge current is determined by the inductance between the capacitor bank and the fault location.

The high-frequency discharge current is superimposed on the fault current, which creates additional current zeros. Depending on the type of circuit-breaker (oil, air-blast, vacuum or SF_6), the high-frequency current may be interrupted causing high overvoltages. For further information refer to [128] and [129].

A similar situation may occur, when circuit-breaker CB closes into a fault. The capacitor bank discharges into the fault and depending on the magnitude of the inductance between the capacitor bank and the fault location, the discharge current can reach peak values and frequencies that exceed those given in Table 9 of IEC 62271-100:2008 (see also 9.7.12.2).

For these specific outrush cases the manufacturer should be consulted. For further treatment of this subject, see IEEE 1036 [130].

9.8.4 Switching overhead lines under faulted conditions

The voltages and currents that occur when switching a faulted transmission line are affected by the circuit parameters and the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage for switching an unfaulted transmission line as $2 \times 1{,}2 \times U_r \sqrt{(2/3)} = 2{,}4$ p.u. When switching a faulted line this value may be exceeded, as may be the rated capacitive switching current value as listed in Table 9 of IEC 62271-100:2008 (see also [131]).

When switching a no-load overhead line with a phase-to earth fault, the highest voltage occurs on the unfaulted phase, which interrupts prior to the faulted phase (see Figure 128). The highest current occurs on the last phase to interrupt when the faulted phase is the first to interrupt. The current for this case is not a sine wave but is distorted, as shown in Figure 129. Under these conditions, the voltages and currents may exceed those on which the design tests are based.

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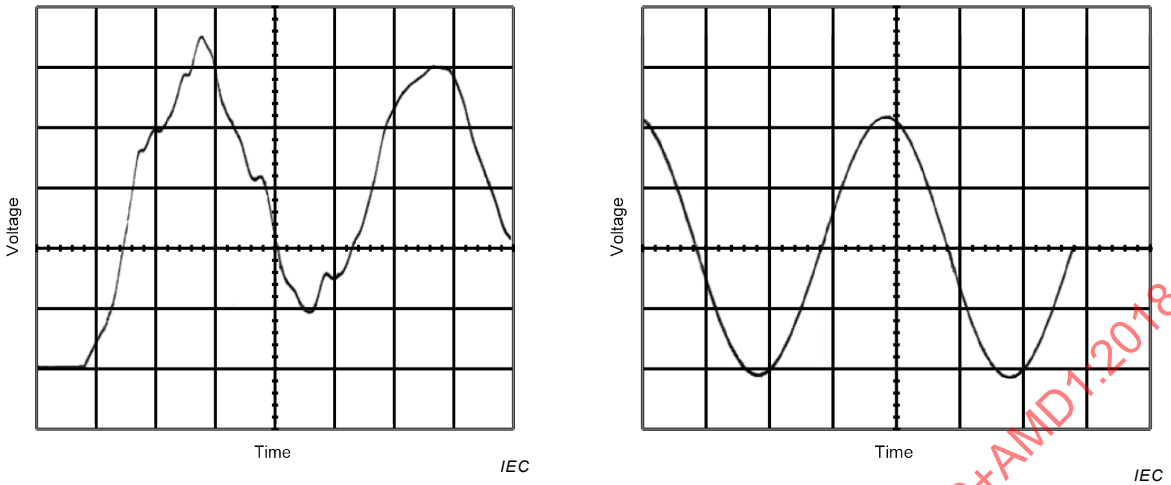
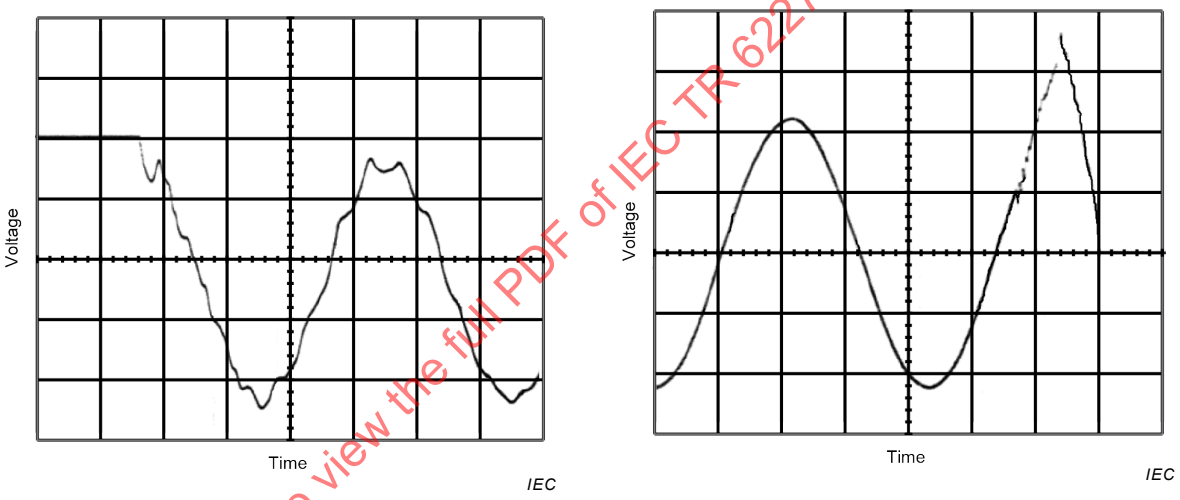


Maximum recovery voltage 2,74 × U_{max} (phase-to-earth) Maximum current 1,09 × rated current

Figure 128 – Recovery voltage and current for first-phase-to-clear when the faulted phase is the second phase-to-clear



Maximum recovery voltage 2,18 × U_{max} (phase-to-earth) Maximum current 1,77 × rated current

Figure 129 – Recovery voltage and current for last-phase-to-clear when the faulted phase is the first-phase-to-clear

For the phase-to-phase fault condition, the recovery voltage and capacitive current are less severe than for the two phase-to-earth fault condition, see also [130].

9.8.5 Switching capacitor banks under faulted conditions

9.8.5.1 General

The voltages and currents that can occur when switching a faulted capacitor bank depend upon the earthing conditions, whether the fault is to the bank neutral or to earth, and on the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage in switching an unfaulted shunt capacitor bank as 2,8 p.u. When switching a faulted bank, this value may be exceeded, as may the rated capacitive switching current value. In the following subclauses, a comparison is given between the recovery voltages and currents of a reference condition and two faulted conditions: a fault to neutral in the capacitor bank and a fault to earth in one phase.

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NOTE The factor 2,8 for the maximum recovery voltage specified in IEC 62271-100 is valid when switching a non-effectively earthed capacitor bank where the second and third phases clear 90° after the first. This is true for modern circuit-breakers. For older circuit-breakers, where the second and third phases do not clear 90° after the first, this factor is 3,0.

9.8.5.2 Reference condition

9.8.5.2.1 General

The reference condition is illustrated in Figure 130. The neutral of the source and the capacitor bank may be solidly earthed and/or non-effectively earthed. The size of the capacitor bank is such that the current is equal to the preferred single capacitor bank current.

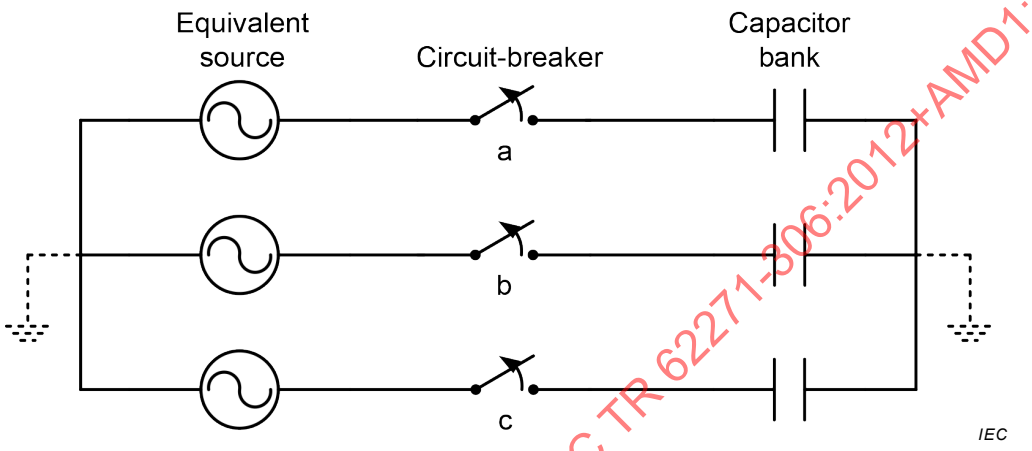

Figure 130 – Basic circuit for shunt capacitor bank switching

9.8.5.2.2 Recovery voltage

The highest recovery voltage (2,5 p.u.) is obtained in the first-pole-to-clear when either the neutral of the capacitor bank, the neutral of the source or both are non-effectively earthed and poles 2 and 3 clear 90° after the first.

The voltage across the last poles to interrupt when at least one of the neutrals (source or bank) is non-effectively earthed can reach $2 \times \sqrt{3} = 3{,}46$ p.u. However, the two phases are in series so that neither is stressed to more than 1,73 p.u.

9.8.5.2.3 Capacitor bank current

In all cases, the capacitor bank current does not exceed the preferred single capacitor bank current.

9.8.5.3 Fault to neutral in one phase (one capacitor bank phase short-circuited)

9.8.5.3.1 Recovery voltage

The highest recovery voltage ($2 \times \sqrt{3} = 3{,}46$ p.u.) is obtained when at least one neutral is non-effectively earthed and the first-pole-to-clear clears a healthy phase. This is in agreement with the voltage factor of 1,7 specified in IEC 62271-100. If the first-pole-to-clear interrupts an unfaulted phase, it is subjected to a recovery voltage of 3,46 p.u. until the second and third phases interrupt.

The highest recovery voltage in the remaining phases is 3,46 p.u., but it is shared by two poles in series.

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9.8.5.3.2 Current

The highest capacitive current is obtained in the cases described under 9.8.5.3.1 when the faulted phase is the first-pole-to-clear and is equal to 3 times that of the reference case.

9.8.5.4 Fault to earth in one phase

For systems that are effectively earthed, the highest recovery voltage is obtained when the first-pole-to-clear interrupts a non-faulted phase. In this case, the maximum recovery voltage peak will be 2,8 p.u.

The most severe case is when the source is non-effectively earthed and the bank neutral is solidly earthed. If an unfaulted pole is the first to interrupt, the current may reach √3 times that of the reference condition and the recovery voltage 3,46 p.u. The remaining poles are subjected to the same current, but upon interrupting, share the 3,46 p.u. recovery voltage. When the faulted pole is the first-pole-to-clear, the current may be 3 times the rated current value and the recovery voltage $2 \times 1{,}25 \times \frac{U_r \sqrt{2}}{\sqrt{3}}$. The second pole to interrupt will have a lower current but a higher recovery voltage of $2 \times \sqrt{3} = 3{,}46$ p.u. which will be shared with the third pole. If the faulted pole reignites, one of the unfaulted poles will then interrupt and the conditions will be as previously described when an unfaulted pole was the first to interrupt.

9.8.5.5 Other fault cases

For phase-to-phase earth faults, or phase-to-phase non-effectively earthed faults, with the source solidly earthed and the bank neutral non-effectively earthed, recovery voltages and currents are no more severe than for the standard unfaulted condition.

9.8.6 Switching cables under faulted conditions

The normal frequency capacitive currents and recovery voltages on a faulted cable circuit will be the same as for a solidly earthed capacitor bank under faulted conditions.

9.8.7 Examples of application alternatives

Application options available are:

a) Use a circuit-breaker of a higher rating in those cases of earth faults on non-effectively earthed systems where the recovery voltage and current, or both, exceed the requirements of IEC 62271-100.

b) Reduce the capacitance of the existing capacitor bank size so that the current under faulted conditions does not exceed the rated capacitive switching current of the circuit-breaker.

c) Use a high-speed switch to earth the source or capacitor bank neutral before switching the capacitor bank under faulted conditions.

d) Use a Δ configuration for the capacitor bank instead of a non-effectively earthed Y.

9.9 Explanatory notes regarding capacitive current switching tests

9.9.1 General

Subclause 6.111 of IEC 62271-100:2008 deals with capacitive current switching tests. In the 1st edition of this standard, a new test procedure has been introduced for the two classes of capacitive current switching that deserve some explanation.

9.9.2 Restrike performance

See 9.7.6.

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9.9.3 Test programme

In defining the test programme for these two classes, the following elements have been taken into account:

– the average number of operations per year carried out by circuit-breakers switching capacitive loads;

– the ability to reduce the number of tests by performing an increased number of switching operations at the minimum arcing time, usually the most difficult capacitive switching operation for circuit-breakers, thus keeping a high level of reliability;

– the recommendations of CIGRE working group A3.04. The expected restrike probability is exclusively related to the type tests.

The proposed number of tests may be questioned because of different assumptions for probability calculations. Nevertheless, these values represent a good compromise (which is the role of the standard where conflicting views exist), reflecting the needs of users (in response to market demand) and above all they avoid unrealistic demands. These tests are not reliability tests but type tests to demonstrate a satisfactory capacitive current switching capability of the equipment in service.

9.9.4 Characteristics of supply circuit

The paragraph concerning factor k_c/k_{pp} (from earlier versions of the standard) where k_c is the voltage factor as described in 9.6 and k_{pp} is the first-pole-to-clear factor has been deleted because there is neither use nor need for testing.

The variation of the power frequency voltage has been chosen as 5 % for test-duty 2 (LC2, CC2 and BC2) and 2 % for test-duty 1 (LC1, CC1 and BC1). These values are a compromise, taking limitations of testing laboratories into account. Considering the type test as a whole, because of the different stresses in the individual test-duties, any undue reduction of the electric stress during the tests is avoided. The actual values for the power frequency voltage variation (depending on the short-circuit power of the system and the capacitive load) is in the range of 1 % to 2 %.

9.9.5 Common features for class C1 and class C2 test-duties

The interval after final arc extinction, in which the voltage decay should not exceed 10 %, has been changed from 100 ms to 300 ms based on service conditions.

9.9.6 Specific feature for class C2 test-duties

Performing these capacitive current switching tests for class C2 equipment on a preconditioned circuit-breaker is, on the one hand, a recommendation of CIGRE working group A3.04; on the other hand, it draws closer to the real conditions of service, without prejudice as to whether this preconditioning improves the capacitive current switching performance of the circuit-breaker or not.

Close-open operations may be performed with no-load closing operations. In any case, the complete sequence should be tested in order to test the circuit-breaker during opening in a dynamic condition, i.e. during the motion of the fluid (if any) caused by the previous closing operation.

9.9.7 Class C1 and C2 test duties

The tolerance of the testing current values for test-duty 1 (LC1, CC1 and BC1) was increased from the old range 20 % to 40 % to the new range 10 % to 40 % in order to give more freedom during testing for combined test-duties for different applications.

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The proposed test sequences have been tested in a laboratory (particularly the adjustment of the minimum arcing time by steps of 6°) and are well adapted to the philosophy of the tests.

Performing some tests at rated pressure is a more pragmatic approach to the notion of type testing, knowing that the circuit-breaker does not always stand under the worst functioning conditions.

9.9.8 Single-phase and three-phase line- and cable-charging current tests

In test-duty 2 of single-phase line-charging and cable-charging tests (LC2 and CC2), the tests are split into open operations and close-open operating cycles to follow more or less the actual service conditions. However, for practical reasons, owing to the small number of tests, in three-phase tests in test-duty 2 (LC2 and CC2), close-open operating cycles are performed exclusively.

9.9.9 Three-phase and single-phase line, cable and capacitor bank switching tests

Close-open operating cycles are important for capacitor bank switching because of the effect of inrush current. Close-open operating cycles are not significant for line- or cable-switching applications, therefore for line- and cable-switching tests, only a small number of close-open operations are requested (closing may be performed as a no-load operation).

A rough parity of the number of three-phase and single-phase tests has been maintained.

The mandatory order for capacitor bank switching tests (single- or back-to-back) is due to the necessity to introduce the effect of inrush current at the beginning of the tests.

9.9.10 Three-phase and single-phase capacitor bank switching tests

Because of the large number of operations in actual service compared with the limited number of operations during type testing, a high number (80 or 120 respectively) of close-open operating cycles is carried out in capacitor bank tests to simulate the wear in service even if the close-open operation is not the normal switching sequence.

For capacitor bank switching tests test-duty 1 (BC1) also needs to be performed, even if the actual service switching duty is always at 100 % nominal current, for the following reasons:

– the tests at 10 % to 40 % nominal current cover an increased number of actual currents;
– knowledge of the capacitive current switching performance is improved.

10 Gas tightness

10.1 Specification

From a maintenance or environmental approach, it would be advisable to specify a "leakage-free" or "fully-tight" equipment. Unfortunately it is not realistic for at least two reasons:

– perfect tightness does not exist: every wall allows gas to get through (the flow of SF_6 gas through a cast aluminium wall has been measured);
– tightness is measured by the leakage rate, and the smaller the specified leakage rate, the more difficult to measure it, in particular to cover decades of years.

As a result, specification should be based on the actual need, which depends on the system class and on the use. Since the standard was addressed to any type of high-voltage circuit-breaker, it was necessary to classify the different pressure systems. At the time of the first issue of tightness specification for high-voltage circuit-breakers, the main concern was to link the tightness to the maintenance schedule.

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"Controlled pressure systems" are automatically replenished. This class applies mainly to air-blast circuit-breakers and pneumatic operating mechanisms. For external tightness of compressed air systems, there is no ecological question and the specification for tightness is only linked to the compressor plant performance. Controlled SF_6 gas pressure systems are not recommended for SF_6 switchgear and controlgear.

"Closed pressure systems" are those which are replenished only periodically, for instance during maintenance. Tightness can be specified from an ecological approach. By specifying the annual gas leakage rate in %/year, easy calculation of the amount of gas escaped per year is possible. Subclause 5.15.2 of IEC 62271-1:2007 specifies tightness for SF_6 with values of 1 % and 0,5 %/year. The original value of 3 %/year specified in Annex EE of the 4th edition of IEC 60056 published in 1987 is no longer specified, because service records show that 1 %/year can usually be met.

"Sealed pressure systems" are designed not to need replenishment during their whole expected service life. The tightness of gas insulated switchgear and controlgear should be demonstrated accordingly, to show that the minimum functional density will not be attained before the expected end of life.

10.2 Testing

10.2.1 General

To check the tightness characteristics for closed and sealed pressure systems for gas, the method generally used during type tests is to measure the leakage rate of the complete assembled circuit-breaker using a cumulative test method as mentioned in 6.8 of IEC 62271-1:2007. In case a measurement of the complete assembled circuit-breaker is not possible, the leakage measurement may be performed on parts, components or subassemblies. In such cases, the leakage rate of the total gas system is to be determined by summation of the component leakage rates as described in Figure 131.

Table 46 provides an overview of the different leakage detection methods and their sensitivity.

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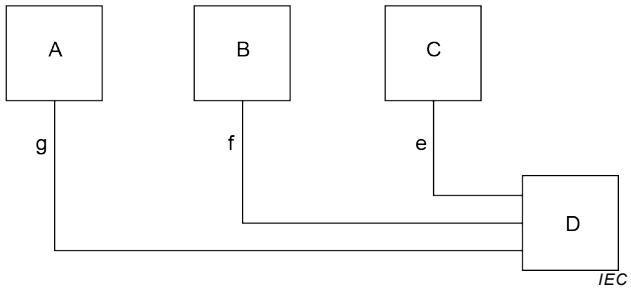

Example:

Gas-insulated metal-enclosed switchgear, single-phase encapsulated circuit-breaker compartments of the three phases connected to the same gas-system.

Leakage rate of the system:

Compartment A	9×10^{-6} Pa × m^3/s
Compartment B	9×10^{-6} Pa × m^3/s
Compartment C	9×10^{-6} Pa × m^3/s
Control box D (including valves, gauges, monitoring devices)	$2{,}3 \times 10^{-6}$ Pa × m^3/s
Piping e	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Piping f	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Piping g	$0{,}2 \times 10^{-6}$ Pa × m^3/s
Complete system	$29{,}9 \times 10^{-6}$ Pa × m^3/s

Filling pressure	p_{re}: 700 kPa (relative)
Alarm pressure	p_{ae}: 640 kPa (relative)
Total internal volume	270 dm^3

$$F_{rel} = \frac{29{,}9 \times 10^{-6} \times 60 \times 60 \times 24 \times 365}{700 \times 10^{3} \times 270 \times 10^{-3}} = 0{,}5\ \%\ \text{per year}$$

$$t_r = \frac{\ln(p_{re} / p_{ae})}{\ln(1 + F_{rel}/100)} = \frac{\ln(700/640)}{\ln(1 + 0{,}005)} = 18\ \text{years}$$

NOTE F_{rel} is the leakage rate and t_r is the time between replenishment.

Figure 131 – Example of a tightness coordination chart, TC, for closed pressure systems

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Table 46 – Sensitivity and applicability of different leak-detection methods for tightness tests

Measurement methodology	Sensitivity of leakage rate (best case)	Test result	Comments	Suitable for leakage rate determination		Suitable for major leaks detection
				High-voltage equipment	Medium-voltage equipment	
Vacuum/pressure increase test	100 P/h (approximately 10 kg/year of SF_6)	Qualitative	Normally used to verity equipment integrity before SF_6 filling	No	No	Yes if the cumulative test method is used
Infrared camera using BAGI (Backscatter/ Absorption Gas Imaging)	1 kg/year of SF_6 at a distance range of 35 m	Qualitative	Suitable for remotely determining the approximate location of major leaks	No	No	Yes
Bubble test with soap or special fluids	1 kg/year of SF_6	Qualitative	Simple and useful for determining the exact location of major leaks. Can also be used for other gases	No	No	Yes and for major leak localisation
Density monitoring (pressure drop)	600 g/year of SF_6 for an observation time of 1 year	Quantitative	Suitable for long term trend analysis of leakage detection or for equipment integrity test. Can also be used for other gases	No	No	Yes if the observation time is long enough
Infrared absorption spectroscopy	60 mg/year of SF_6 or 3 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type, routine and commissioning test. Not influenced by other common gases and water	Yes if the cumulative test method is used. Can be also used for minor leak localisation	Hardly suitable	Yes if the cumulative test method is used. Can also be used for major leak localisation
Negative ion capture detector (using corona discharge)	20 mg/year of SF_6 or 1 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type test, routine test, commissioning test and maintenance. Reading may be influenced by other gases and moisture content.	Yes if the cumulative test method is used Can be also used for minor leak localisation	Yes if the cumulative test method is used Hardly suitable for minor leak localisation	Yes if the cumulative test method is used. Can also be used for major leak localisation

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Measurement methodology	Sensitivity of leakage rate (best case)	Test result	Comments	Suitable for leakage rate determination		Suitable for major leaks detection
				High-voltage equipment	Medium-voltage equipment	
Electron capture leak detector (using radioactive emitter)	2 mg/year of SF_6 or 0,1 ppm_v	Quantitative if the cumulative test method is used or qualitative for sniffing test	May be used for type test, routine test, commissioning test and maintenance. Reading may be influenced by other gases and moisture content.	Yes if the cumulative test method is used Can be also used for minor leaks localisation	Yes if the cumulative test method is used Hardly suitable for minor leak localisation	Yes if the cumulative test method is used. Can also be used for major leak localisation
Helium mass spectrometer	2 mg/year of SF_6 if checked by a calibration source	Quantitative	Type test and routine test. Can only be used with the cumulative test method	Yes Can also be used on equipment components	Yes	Yes. Cannot be used for leak localisation.
Photo-acoustic infrared spectroscopy	0,2 mg/year of SF_6 or 0,01 ppm_v	Quantitative	Type test and routine test. Can only be used with the cumulative test method	Yes	Yes	Yes. Cannot be used for leak localisation

See CIGRE Technical Brochure 430 [144] for more detailed information.

NOTE 1 "minor leak" qualitatively indicates a leak having a leakage rate "L" in the order of the permissible leakage rate L_p ($L \approx L_p$).

NOTE 2 "major leak" qualitatively describes leaks having at least one order of magnitude higher than the permissible leakage rate L_p ($L >> L_p$).

NOTE 3 The "cumulative test method" can also be called "integral test".

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During routine tests, a cumulative test method is preferred but such a test may be impractical in industrial environments. For routine tests, as mentioned in 7.5 of IEC 62271-1:2007, a leak detection using a sniffing device may be used instead of using a cumulative test method. IEC 62271-1 specifies a minimum sensitivity of sniffing device of 10^{-8} Pa m^3/s.

This required minimum sensitivity corresponds to a single leak of less than 0,04 %/year for a typical 245 kV SF_6 circuit-breaker having an internal volume of 200 l filled at an absolute pressure of 0,5 MPa and if the moving speed of the sniffer detector around sealing joints is relatively slow, for instance, not exceeding 1 cm/s. Obviously, if the filling pressure, volume or moving speed of the leak detector are different, then the leakage rate sensitivity changes. Each case should be evaluated individually.

If a leak is detected when using a sniffing device, then the leakage rate cannot be quantified since this device is only giving an alert if a leak is detected. As mentioned in 7.5 of IEC 62271-1:2007, in the case of a detection of a leak with the sniffing device, the leakage rate should be then quantified by repeating the tightness test by using a cumulative test method. Only the cumulative test method can be used to quantify a leakage rate.

10.2.2 Cumulative test method and calibration procedure for type tests on closed pressure systems

10.2.2.1 Description of the cumulative test method

10.2.2.1.1 General

The cumulative test method is the recommended test method for the determination of gas leaks that can occur in closed pressure systems such as for SF_6 circuit-breakers. This method consists of erecting a relatively gastight enclosure (e.g. plastic tent or similar enclosure, see NOTE 2) around the complete test object or by erecting several smaller relatively gastight enclosures (plastic tents or similar enclosures, see NOTE 2) around each part, component or subassembly. The circuit-breaker should be filled as in service, at its rated filling pressure. The measurement consists of measuring the tracer gas content increase (e.g. SF_6) within the enclosure(s) during a sufficient time period. With today's available measuring equipment, a time period of 1 h is generally sufficient. If an enclosure(s) of small volume are used, then this measuring period can be reduced. For very large enclosures, this time period may need to be increased. As a rule of thumb, the time period should be long enough that the calculated tracer gas content in the enclosure for the maximum permissible leakage rate should be at least 3 times the minimum resolution of the measuring equipment. From the tracer gas content increase within the enclosure(s) during a given time period, then the annual leakage rate can be calculated. This method is considered to be very accurate and has been widely used during type tests on circuit-breakers at ambient, low and high temperatures.

The tightness of the enclosure should be demonstrated for the duration of the measuring time period. This can be done at the same time as the calibration of the enclosure.

The cumulative test method steps can be summarized as follows:

– install a relatively gastight enclosure(s) over the entire test object or over parts, components or subassemblies;

– pressurize the circuit-breaker at its rated filling pressure with its specified gas or gas mixture, pure SF_6 instead of gas mixture, or with a tracer gas such as helium;

– determine the enclosure(s) volume V_m (m^3);

– measure the tracer gas concentration C_0 (p.p.m_v. or cc/m^3) within the enclosure(s) at reference time t_0 (s);

– measure the final gas concentration C_1 (p.p.m_v. or cc/m^3) within the enclosure(s) at time t_1 (s);

– calculate the leak rate using the following equation:

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$$F = V_m \times P_e \times \frac{\Delta C}{\Delta t} \times 10^{-6}$$

where

F is the leakage rate in m^3Pa/s;

V_m is the enclosure gas volume in m^3;

P_e is the atmospheric pressure in Pa;

ΔC is the tracer gas concentration increase (C_1-C_0) in $p.p.m_v$. during the measuring time period;

Δt is the measuring time period in seconds.

NOTE 1 A fan installed inside the enclosure helps to get an homogeneous gas tracer content within the enclosure. This recommendation applies mainly to large enclosure used around a complete circuit-breaker.

NOTE 2 The enclosure does not need to be as tight as a pressure vessel since the pressure within the enclosure is equal to the atmospheric pressure outside the enclosure. Thus, the air inside the enclosure (including traces of the tracer gas) is not forced to escape from the enclosure nor the air outside the enclosure is forced to enter within the enclosure.

10.2.2.1.2 Sensitivity, accuracy and calibration

The accuracy of the cumulative method depends on three main factors: sensitivity of the tracer gas detector, volume of enclosure and duration of the measuring period. For example, a minimum threshold sensitivity and resolution of 0,01 $p.p.m_v$ is recommended when SF_6 is used as the tracer gas. Such gas detectors are commercially available.

NOTE 1 Infrared photo acoustic spectroscopy method is widely used to measure SF_6 concentration.

The uncertainty concerning the enclosure volume can be considerably reduced by using a suitable calibration technique. The recommended calibration procedure consists of injecting a known quantity of tracer gas into the enclosure.

NOTE 2 Experience gained from measurements showed that the estimation error of the enclosure volume is less than 10 %.

The enclosure volume (V_m in m^3) should be determined by calibration. A small tracer gas quantity, $V_{injected}$ (cm^3), is injected into the enclosure volume V_m. The injected gas quantity should be in the same order of magnitude than the gas quantity corresponding to the maximum allowable leakage rate.

The tracer gas concentration C_0 ($p.p.m_v$.) is measured before and after injection by the gas detector. The enclosure volume is then calculated as follows:

$$V_m = V_{injected} / \Delta C_0$$

This procedure should be repeated twice in order to get a better evaluation of the enclosure volume. The average value of the two measurements should be used as the enclosure volume V_m.

10.2.2.1.3 Test set-up and test procedure

For type test, the test object should be pressurized at its nominal filling pressure with its assigned gas mixture (if applicable). Nevertheless, industrial environments and local safety rules may force a deviation from service conditions. For instance, some tests could be performed using pure SF_6 instead of the assigned gas mixture, or other tracer gases such as helium may be used. All deviations from service conditions have to be carefully evaluated to see their impacts on the measurement sensitivity.

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In order to have an effective test set-up, the following is recommended:

– the enclosure volume should be as small as possible in order to obtain a better sensitivity of the tracer gas concentration within the enclosure;

– a fan should be installed inside the enclosure in order to provide an homogeneous gas content within the enclosure;

– the gas detector device should be able to measure accurately 1/3 of the maximum allowable leakage rate.

For low and high ambient temperature tests, the following additional recommendations are given:

– Thermocouples should be installed at different heights along the test object inside the enclosure. The ambient temperature to be reached during test is the temperature measured inside the enclosure.

– Controllable electric heaters should be installed inside the enclosure in order to help to fulfill the temperature increase of 10 K/h specified during the low temperature test sequence. For the high-temperature test, the temperature decrease of 10 K/h within the enclosure can be met by making a temporary opening of the enclosure since the leak rate determination is not required during this test part of the test. Required temperature variations have to be met within the enclosure.

NOTE 1 One way to obtain the desired temperature inside the enclosure is to lower the ambient temperature in the climatic room such that it is slightly lower than the required temperature for low temperature test or slightly higher for high temperature test.

The maximum leakage rate (m^3Pa/s) based on acceptance leakage rate limit of 0,5 % per year (see 5.15.2 of IEC 62271-1:2007) is calculated as follows:

$$F = \frac{0{,}005 \times V_{\text{to}} \times \left(P_{\text{to}} \times \frac{273 + T_{\text{test}}}{273\,\text{K} + 20} - 101{,}3 \times 10^3 \right) \times \gamma}{365 \times 24 \times 60 \times 60}$$

where

F is the leakage rate in m^3Pa/s;

V_{to} is the circuit-breaker gas volume in m^3;

P_{to} is the circuit-breaker absolute filling pressure at T = 20 °C in Pa (see NOTE 2);

T_{test} is the ambient temperature during leakage measurement in °C;

γ is the percentage of tracer gas in the circuit-breaker gas volume.

NOTE 2 It is assumed only gas exceeding the atmospheric pressure can escape from the breaker. Other leakage mechanisms such as atomic migration through solid materials are considered to be negligible. The pressure correction for the test temperature is applied to the absolute gas pressure.

Finally, the leakage rate per year (%/year) can also be directly expressed by the following equation:

$$F_{\text{year}} = \frac{P_{\text{atm}} \times 365 \times 24 \times 60 \times 60 \times V_{\text{m}} \times \Delta C \times 10^{-6}}{V_{\text{to}} \times \left(P_{\text{to}} \times \frac{273 + T_{\text{test}}}{273 + 20} - 101{,}3 \times 10^3 \right) \times \gamma \times t}$$

where

F_{year} is the leakage rate in %/year;

P_{atm} is the atmospheric pressure during measurement (a default value of 101,3 kPa can be used);

ΔC is the tracer gas concentration increase (C_1-C_0) in p.p.m_v. during the measuring time period;

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V_m is the enclosure gas volume in m^3;

V_{to} is the circuit-breaker gas volume in m^3;

P_{to} is the circuit-breaker absolute gas pressure in Pa;

T_{test} is the ambient temperature during leakage measurement in °C;

γ is the percentage of tracer gas in the circuit-breaker gas volume;

t is the measuring time period in s.

10.2.2.1.4 Example: leakage rate measurement of a circuit breaker during low temperature test

The test object is filled with its gas mixture SF_6/N_2 at nominal filling pressure and ambient temperature. A relatively gastight enclosure is installed over the circuit-breaker. A calibration by injection method is performed in order to evaluate the enclosure volume.

Table 47 shows the results of a calibration of the enclosure.

Table 47 – Results of a calibration procedure prior to a low temperature test

Description	Quantity of SF_6 gas injected within the enclosure	Concentration of SF_6 gas measured within the enclosure	Variation of concentration of SF_6 gas within the enclosure	Calculated volume V_m
	(cm^3)	(p.p.m_v)	(p.p.m_v)	(m^3)
Before test	-	0,05	-	
First Injection	10	1,03	0,98	10,20
Second injection	10	2,06	1,03	9,71

Thus, the enclosure volume is considered to be the average value of the volumes determined with both injections e.g. 9,96 m^3.

Then, if a circuit-breaker having an internal volume of 0,375 m^3 filled with a gas mixture consisting of SF_6 and N_2 at an absolute pressure of 1,0 MPa and the SF_6/N_2 mixture is 30 % SF_6 and 70 % N_2, the 0,5 %/year permissible maximum leakage rate at ambient temperature (20 °C) corresponds to a maximum concentration of tracer gas within the enclosure during a measuring period of 1,0 h of:

$$\Delta C = \frac{F_{year} \times V_{to} \times \left(P_{to} \times \frac{273 + T_{test}}{273 + 20} - 101{,}3 \times 10^3 \right) \times \gamma \times t}{P_{atm} \times 365 \times 24 \times 60 \times 60 \times V_m \times 10^{-6}}$$

$$\Delta C = \frac{0{,}005 \times 0{,}375 \times \left(1 \times 10^6 \times \frac{273 + 20}{273 + 20} - 101{,}3 \times 10^3 \right) \times 0{,}3 \times 3600}{101{,}3 \times 10^3 \times 365 \times 24 \times 60 \times 60 \times 9{,}96 \times 10^{-6}} = 0{,}057 \text{ p.p.m}_v.$$

Accordingly, if the same enclosure is used for the low-temperature test, the maximum allowable gas concentration increase for a measuring time period of 1 h at an ambient temperature of −25 °C will be:

$$3 \times F_{year} = 3 \times 0{,}057 \times \left(1 \times 10^6 \times \frac{273 - 25}{273 + 20} - 101{,}3 \times 10^3 \right) = 0{,}127 \text{ p.p.m}_v.$$

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and accordingly at −50 °C

$$6 \times F_{year} = 6 \times 0{,}057 \times \left(1 \times 10^6 \times \frac{273 - 50}{273 + 20} - 101{,}3 \times 10^3 \right) = 0{,}226 \text{ p.p.m}_v .$$

It should be noted that the relative leakage rate of N_2 cannot be measured using this method. It may be higher than the value obtained by relating the leakage rate of N_2 to that of SF_6, i.e. $\Delta C(N_2) \neq \Delta C(SF_6) \times 0{,}7 / 0{,}3$.

10.2.2.2 Time between replenishment

With a given leakage rate F in %/year, the time between replenishments t_r is obtained from the following equation. t_r is the number of periods on which the leakage rate is defined (in this case 1 year):

$$t_r = \frac{\ln(p_{re} / p_{ae})}{\ln(1 + F/100)}$$

where

t_r is the time between replenishments;

p_{re} is the relative filling pressure in Pa;

p_{ae} is the relative alarm pressure in Pa;

F is the measured leakage rate in %/year.

10.3 Cumulative test method and calibration procedure for type tests on closed pressure systems

10.3.1 Description of the cumulative test method

The cumulative test method is the recommended test method for the determination of gas leaks which can occur in closed pressure systems such as for SF_6 circuit-breakers. This method consists of erecting a relatively gastight enclosure (e.g. plastic tent or similar enclosure, see NOTE 2) around the complete test object or by erecting several smaller relatively gastight enclosures (plastic tents or similar enclosures, see NOTE 2) around each part, components or subassemblies. The circuit-breaker should be filled as in service, at its rated filling pressure. The measurement consists of measuring the tracer gas content increase (e.g. SF_6) within the enclosure(s) during a sufficient time period. With the today's available measuring equipment, a time period of 1 h is generally sufficient. If enclosure(s) of small volume are used, then this measuring period can be reduced. For very large enclosures, this time period may need to be increased. As a rule of thumb, the time period should be long enough that the calculated tracer gas content in the enclosure for the maximum permissible leakage rate should be at least 3 times the minimum resolution of the measuring equipment. From the tracer gas content increase within the enclosure(s) during a given time period, then the annual leakage rate can be calculated. This method is considered to be very accurate and has been widely used during type tests on circuit-breakers at ambient, low and high temperatures.

The cumulative test method steps can be summarized as follows:

– install a relatively gastight enclosure(s) over the entire test object or over parts, components or subassemblies;

– pressurize the circuit-breaker at its rated filling pressure with its specified gas or gas mixture, pure SF_6 instead of gas mixture, or with a tracer gas such as helium;

– determine the enclosure(s) volume V_m (m^3);

– measure the tracer gas concentration C_0 (p.p.m_v. or cc/m^3) within the enclosure(s) at time reference time t_0 (s);

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– measure the final gas concentration C_1 (p.p.m$_v$. or cc/m^3) within the enclosure(s) at time t_1 (s);
– calculate the leak rate using the following equation:

$$F = V_m \times P_e \times \frac{\Delta C}{\Delta t} \times 10^{-6}$$

where

F is the leakage rate, in m^{3}Pa/s;

V_m is the enclosure gas volume, in m^3;

P_e is the atmospheric pressure, in Pa;

ΔC is the tracer gas concentration increase (C_1-C_0), in p.p.m$_v$. during the measuring time period;

Δt is the measuring time period, in s.

NOTE 1 A fan installed inside the enclosure helps to get an homogeneous gas tracer content within the enclosure. This applies mainly to large enclosures used around a complete circuit-breaker.

NOTE 2 The enclosure does not need to be as tight as a pressure vessel since the pressure within the enclosure is equal to the atmospheric pressure outside the enclosure. Thus, the air inside the enclosure (including traces of the tracer gas) is not forced to escape from the enclosure nor the air outside the enclosure is forced to enter within the enclosure.

10.3.2 Sensitivity, accuracy and calibration

The accuracy of the cumulative method depends on three main factors: sensitivity of the tracer gas detector, volume of enclosure and duration of the measuring period. For example, a minimum threshold sensitivity and resolution of 0,01 p.p.m$_v$. is recommended when SF_6 is used as the tracer gas. Such gas detectors are commercially available.

NOTE 1 Infrared photo acoustic spectroscopy method is widely used to measure SF_6 concentration.

The uncertainty concerning the enclosure volume can be considerably reduced by using a suitable calibration technique. The recommended calibration procedure consists of injecting a known quantity of tracer gas into the enclosure.

NOTE 2 Experience gained from measurements showed that the estimation error of the enclosure volume is less than 10 %.

The enclosure volume (V_m) should be determined by calibration. A small tracer gas quantity, $V_{injected}$ (cm^3), is injected into the enclosure volume V_m. The injected gas quantity should be in the same order of magnitude than the gas quantity corresponding to the maximum allowable leakage rate.

The tracer gas concentration C_{ppm} (p.p.m$_v$.) has to be measured before and after injection by the gas detector. The enclosure volume is then calculated as follows:

$$V_m(m^3) = V_{injected}(cm^3) / \Delta C_{ppm}$$

This procedure should be repeated twice in order to get a better evaluation of the enclosure volume. The average value of the two measurements should be used as the enclosure volume V_m.

10.3.3 Test set-up and test procedure

For type test, the test object should be pressurized at its nominal filling pressure with its assigned gas mixture (if applicable). Nevertheless, industrial environments and safety rules may require a deviation from service conditions. For instance, some tests could be performed

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using pure SF_6 instead of the assigned gas mixture or other tracer gas such as helium may be used. The filling pressure may also be reduced. Nevertheless, for type tests it is not recommended to use a lower filling pressure since the applied forces on the circuit-breaker seals are reduced. All deviations from service conditions have to be carefully evaluated to see their impacts on the measurement sensitivity.

In order to have an effective test set-up, the following is recommended:

– the enclosure volume shall be as small as possible in order to obtain a better sensitivity of the tracer gas concentration within the enclosure;
– a fan should be installed inside the enclosure in order to provide an homogeneous gas content within the enclosure;
– the gas detector device should be able to measure accurately half of the maximum allowable leakage rate.

For low and high ambient temperature tests, the following additional recommendations are given:

– thermocouples should be installed at different heights along the test object inside the enclosure. The ambient temperature to be reached during test is the temperature measured inside the enclosure;
– controllable electric heaters should be installed inside the enclosure in order to help to fulfil the temperature increase of 10°C/h specified during the low temperature test sequence. For the high temperature test, the temperature decrease of 10°C/h within the enclosure can be met by making a temporary opening of the enclosure since the leak rate determination is not required during this test part of the test. Required temperature variations have to be met within the enclosure.

NOTE It may be necessary to use an ambient temperature in the climatic room slightly lower than the required temperature for low temperature test or slightly higher for high temperature test in order to get the required test temperature inside the enclosure.

The maximum leakage rate (m^3Pa/s) based on acceptance leakage rate limit of 0,5 % per year (see 5.15.2 of IEC 62271-1:2007) is calculated as follow:

$$F = \frac{0{,}5\,\% \times V_{to} \times P_{to} \times \left(\left(273\,\mathrm{K} + T_{test}\right) \Big/ \left(273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}\right) \right) \times \gamma}{365\ \text{days} \times 24\ \text{hours} \times 60\ \text{minutes} \times 60\ \text{seconds}}$$

where

F is the leakage rate, in m^3Pa/s;
V_{to} is the circuit-breaker gas volume, in m^3;
P_{to} is the rated filling pressure at T = 20 °C, in Pa absolute;
T_{test} is the ambient temperature during leakage measurement, in °C;
γ is the percentage of tracer gas in the circuit-breaker gas volume.

Finally, the leakage rate per year (%/year) can also be directly expressed by the following equation:

$$F(\%) = \frac{P_{atm} \times 365\ \text{days} \times 24\ \text{hours} \times \Delta C \times V_m}{V_{to} \times P_{to} \times \left(\left(273\,\mathrm{K} + T_{test}\right) \Big/ \left(273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}\right) \right) \times \gamma \times t}$$

where

$F(\%)$ is the leakage rate, in %/year;

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P_{atm} is the atmospheric pressure during measurement (a default value of 101,3 kPa can be used);

ΔC is the tracer gas concentration increase (C_1-C_0), in p.p.m_v. during the measuring time period;

V_m is the enclosure gas volume, in m^3;

T_{test} is the ambient temperature during leakage measurement, in °C;

γ is the percentage of tracer gas in the circuit-breaker gas volume;

t is the measuring time period.

10.3.4 Example: leakage rate measurement of a circuit-breaker during low temperature test

The test object is filled with its gas mixture SF_6/N_2 at nominal filling pressure and ambient temperature. A relatively gastight enclosure is installed over the circuit-breaker. A calibration by injection method is performed in order to evaluate the enclosure volume.

Table 16 shows the results of a calibration of the enclosure.

Table 16 – Results of the calibration of the enclosure

Description	Quantity of SF_6 gas injected within the enclosure	Concentration of SF_6 gas measured within the enclosure	Variation of concentration of SF_6 gas within the enclosure	Calculated volume V_m
	(cm^3)	(p.p.m_v)	(p.p.m_v)	(m^3)
Before test	-	0,05	-	
First injection	10	1,03	0,98	10,20
Second injection	10	2,06	1,03	9,71

Thus, the enclosure volume is considered to be the average value of the volumes determined with both injections e.g. 9,96 m^3.

Then, if a circuit-breaker having an internal volume of 0,375 m^3 filled with a gas mixture consisting of SF_6 and N_2 at a pressure of 1,0 MPa(abs) and the SF_6/N_2 mixture is 30 % SF_6 and 70 % N_2, the 0,5 %/year permissible maximum leakage rate at ambient temperature (20 °C) corresponds to a maximum concentration of tracer gas within the enclosure during a measuring period of 1 h is:

$$\Delta C = \frac{F(\%) \times V_{to} \times P_{to} \times \left((273\,\mathrm{K} + T_{test}) / (273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}) \right) \times \gamma \times t}{P_{atm} \times 365\ \mathrm{days} \times 24\ \mathrm{h} \times V_m}$$

$$\Delta C = \frac{0{,}5\,\% \times 0{,}375\,\mathrm{m}^3 \times 1\,\mathrm{MPa\ abs} \times \left((273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}) / (273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}) \right) \times 30\,\% \times 1\,\mathrm{h}}{0{,}1013\,\mathrm{MPa} \times 365\ \mathrm{days} \times 24\ \mathrm{h} \times 9{,}96\,\mathrm{m}^3} = 0{,}063\ \mathrm{p.p.m_v}.$$

Accordingly, if the same enclosure is used for low temperature test, the maximum allowable gas concentration increase for a measuring time period of 1 h at an ambient temperature of -25 °C will be:

$$3 \times F(\%) = 3 \times 0{,}063\ \mathrm{p.p.m_v} \times \left((273\,\mathrm{K} - 25\,^{\circ}\mathrm{C}) / (273\,\mathrm{K} + 20\,^{\circ}\mathrm{C}) \right) = 0{,}159\ \ \mathrm{p.p.m_v}$$

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and accordingly at -50 °C

$$6 \times F(\%) = 6 \times 0{,}063 \text{ p.p.m}_{\text{v.}} \times \left((273\,\text{K} - 50\,°\text{C}) \Big/ (273\,\text{K} + 20\,°\text{C}) \right) = 0{,}287 \text{ p.p.m}_{\text{v.}}$$

11 Miscellaneous provisions for breaking tests

11.1 Energy for operation to be used during demonstration of the rated operating sequence during short-circuit making and breaking tests

For circuit-breakers equipped with operating mechanisms having the possibility to store more energy than consumed by a single operation (for example hydraulic and pneumatic operating mechanisms), it is needed to specify the minimum levels of energy at which the breaking capacity still is guaranteed. Consequently, each test operating sequence shall be carried out at the relevant minimum energy level. In particular, minimum energy levels are specified for O, CO and O-CO operating sequences, which will ensure that the circuit-breaker will interrupt at the last O operation.

For the auto-reclose operating sequence O-*t*-CO-*t*'-CO the following conditions shall be fulfilled:

– the capability of the circuit-breaker for each short-circuit type-test duty must be demonstrated during performance of the rated operating sequence O-*t*-CO-*t*'-CO;

– demonstration is by three valid breaking operations during the sequence O-*t*-CO-*t*'-CO;

– the minimum and maximum arc duration shall be demonstrated during the tests;

– the starting energy for the O-*t*-CO part of the operating sequence cannot be less than the energy that takes account of the energy consumption of the O-*t*-C operating sequence to enable the final O operation to be performed at an energy down to (in practice during testing, at) the opening lock-out condition;

NOTE This O-*t*-CO start energy is often termed the auto-reclose lock-out setting.

– the circuit-breaker shall be able to perform the required three valid shots at the minimum functional pressure (i.e. minimum operating energy) for the specified operating sequence as described in 6.102.3.1 of IEC 62271-100:2008;

– where appropriate, the gas pressure for interruption shall also be at its lock-out setting.

The combination of events necessary to produce such boundary condition requirements are credible in practice, i.e. lowest gas, lowest operating pressure, minimum and/or maximum arc duration operation, and full short-circuit current rating and as such they should be tested.

Each operating sequence shall be initiated at the lowest applicable energy: the O-CO and CO test sequence should be performed setting the operating energy at the declared O-CO and CO lockout energy, respectively.

If single-phase tests in substitution for three-phase conditions are performed under direct or synthetic conditions, the rated operating sequence may be split in sub sequences.

For example, for synthetic testing the O-CO will be split in a single Os (breaking operation using synthetic circuit) for the 1st O and in a subsequent Od-COs, where Od is a breaking operation using a direct circuit (i.e. at reduced voltage).

The single O operation is here reproducing the 1st O of an O-CO sequence and shall be carried out at the O-CO lockout energy.

Even if a single O operation performed at minimum operation energy is not explicitly foreseen in the symmetrical test cases, the last O in the O-CO and CO sequences are performed at an

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operating energy equal to the O lock-out condition, since the operation energy has been consumed by previous operations (O-C and C, respectively).

The breaking capacity for single O operations carried out at O lockout condition is verified in the T100a test duty, since that test duty consists of single O operations (minimum, maximum and intermediate arcing time).

11.2 Alternative operating mechanisms

11.2.1 General

During the lifetime of a circuit-breaker or due to new developments of operating mechanisms a type tested circuit-breaker may be operated with an alternative operating mechanism that is different from the one type tested. To limit the quantity of tests for this new combination of operating mechanism and circuit-breaker, a statement is included in 6.102.7 of IEC 62271-100:2008 that repetition of type tests is not necessary for short-circuit, out-of-phase and capacitive current switching tests.

This statement applies if the type tested combination of operating mechanism and circuit-breaker and the alternative operating mechanism with the same circuit-breaker if the following conditions are fulfilled.

a) the mechanical characteristics under no-load conditions of the circuit-breaker with the alternative operating mechanism shall be within the limits defined in 6.101.1.1 of IEC 62271-100:2008;

b) a T100s test shall be done with the circuit-breaker and both operating mechanisms. Also here the mechanical characteristics shall be compared according to 6.101.1.1 of IEC 62271-100:2008;

c) a mechanical endurance test shall be performed in accordance with the specified class of the circuit-breaker;

Additionally, the circuit-breaker with alternative operating mechanisms shall pass a T100a test if the operating times are such that the circuit-breaker will fall into a different category of minimum clearing time (see 11.2.43 and subclause 3.7.159 of IEC 62271-100:2008);

If all requirements are met, the alternative operating mechanism combined with the type tested circuit-breaker is deemed to have the same characteristics and all type tests performed on the original combination are also valid for this new configuration.

11.2.2 Comparison of the mechanical characteristics

The mechanical characteristics of both operating mechanisms shall be recorded under the same no-load conditions with the same type of circuit-breaker. The sensor used during the alternative drive tests should be of the same type as for the original operating mechanism. The position of the sensor should be at the same position as during the original test to allow a direct comparison of the travel curves. If it is not possible to use the same position or type of sensor during the alternative drive test, because the design of the alternative drive does not allow this, the manufacturer should provide a transfer function to calculate the corresponding travel characteristic for comparison. The evaluation of the transfer function should be explained in detail for easy check of validity. The position of the type and sensor for the record of the mechanical characteristics should be stated in the test report. In the ideal case both closing and opening travel curves of the alternative operating mechanism should fall into the ±5 % tolerance band of the type tested operating mechanism. The tolerance band is drawn from the beginning of the mechanical characteristics to the instant of contact touch for the closing operation and from the instant of contact separation to the end of the contact travel for the opening operation. The mechanical characteristics of the alternative operating mechanism is placed into the envelope of reference curve. The envelope can be moved in the vertical direction until one of the envelope curves covers the curve of the alternative operating mechanism. This gives the following maximum tolerances over the mechanical characteristics:

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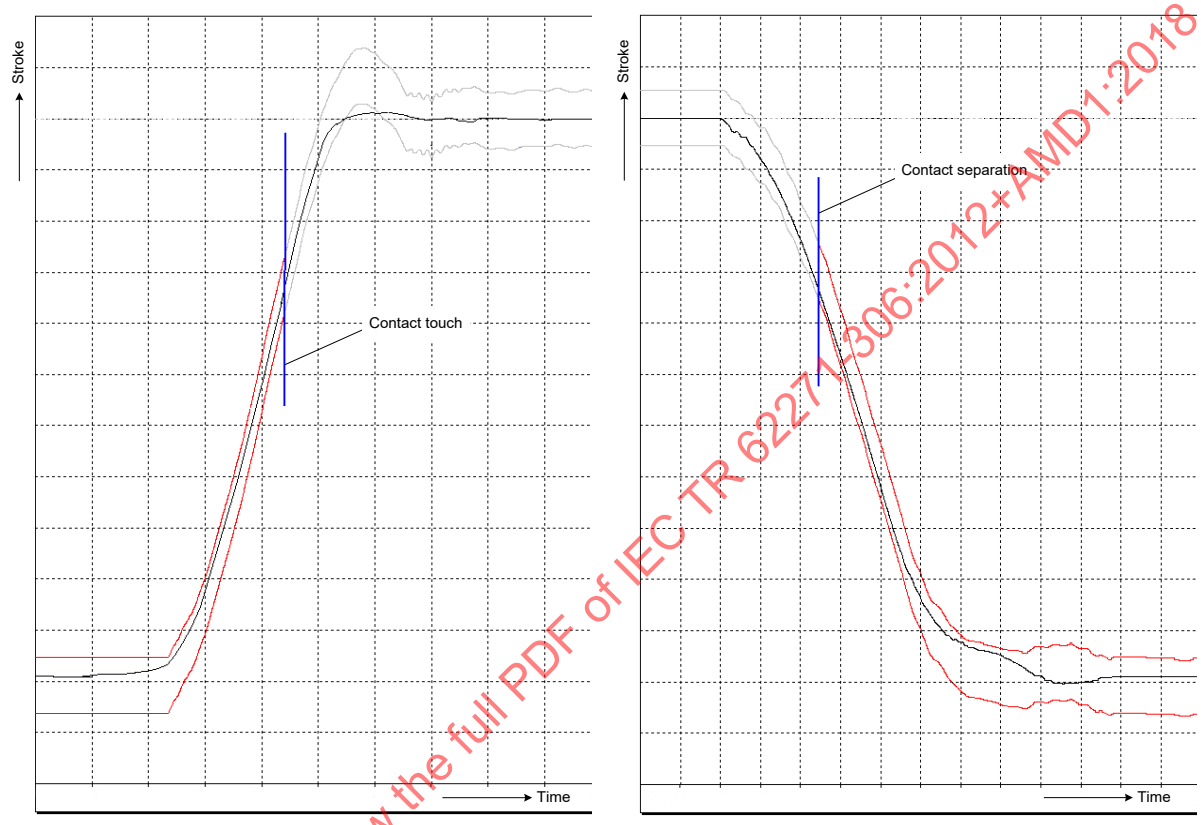
– $^{+10}_{-0}$ %;

– 0 %;

– $^{+0}_{-10}$ %.

The displacement of the envelope can be used only once for the complete procedure in each test in order to obtain a maximum total deviation from the reference characteristic of 10 %. An example is shown in Figure 64.



Closing operation **Opening operation**

Key

Red traces Envelope of the reference mechanical characteristics

Black trace Mechanical characteristics of the alternative operating mechanism

Figure 64 – Comparison of reference and alternative mechanical characteristics

Example 1:

As can be seen in Figure 64, the alternative operating mechanism (solid black line) has a slightly different travel curve. But the comparison fulfils the requirements of 6.101.1.1 of IEC 62271-100:2008. Even in the case that the curve during closing is leaving the reference travel boundaries is acceptable as the travel during closing shall be within the boundaries only until contact touch has taken place. This is before the end position of the circuit-breaker.

For the given example the requirement of the no-load characteristic is fulfilled.

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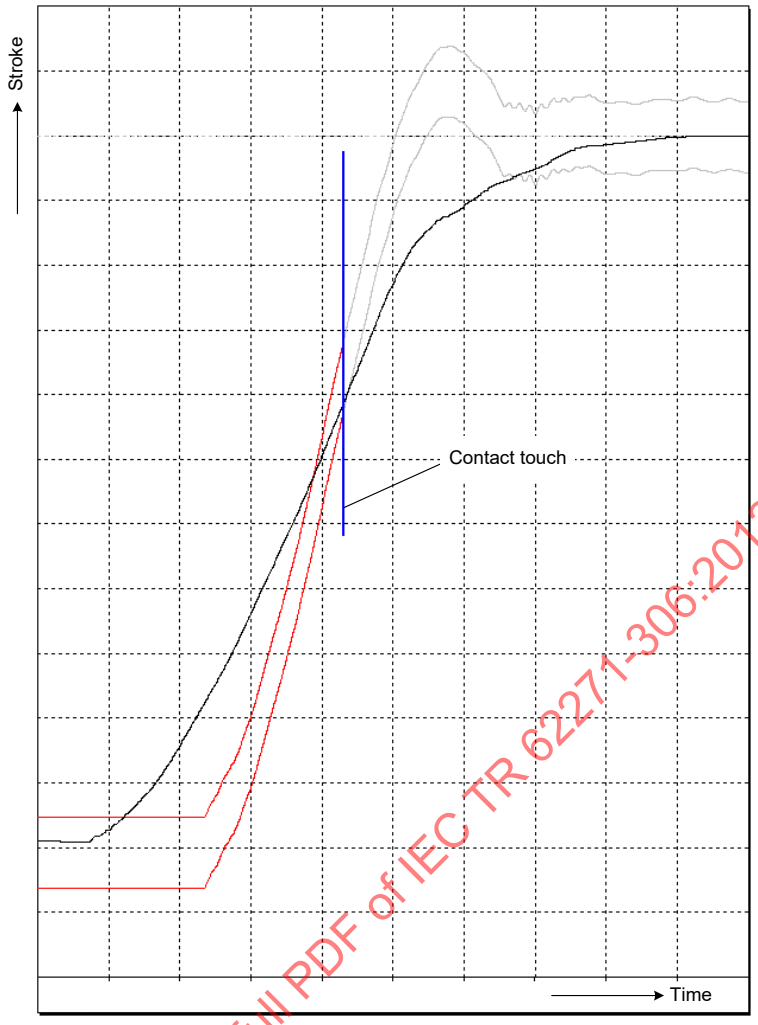

Key

Red traces	Envelope of the reference mechanical characteristics
Black trace	Mechanical characteristics of the alternative operating mechanism

Figure 65 – Closing operation outside the envelope

Example 2:

In Figure 65 the closing operation of another alternative operating mechanisms is shown. In this case the closing speed of the alternative operating mechanism is different. According to the requirements of 6.101.1.1 of IEC 62271-100:2008 the mechanical characteristics for closing do not fulfil the requirements.

Therefore the alternative operating mechanism should be tested for all relevant short-circuit, out-of-phase and capacitive current switching duties.

11.2.3 Comparison of T100s test results

As mentioned in IEC 62271-100, the number of tests shall be limited when qualifying an alternative operating mechanism. One test-duty to be performed is T100s. This test was chosen as it should demonstrate the ability of the circuit-breaker to close against a short-circuit and to clear a 100 % short-circuit current. As the original circuit-breaker is deemed to be fully type tested, results of the T100s tests are available. Therefore only the new combination of the type tested circuit-breaker and the alternative operating mechanism has to

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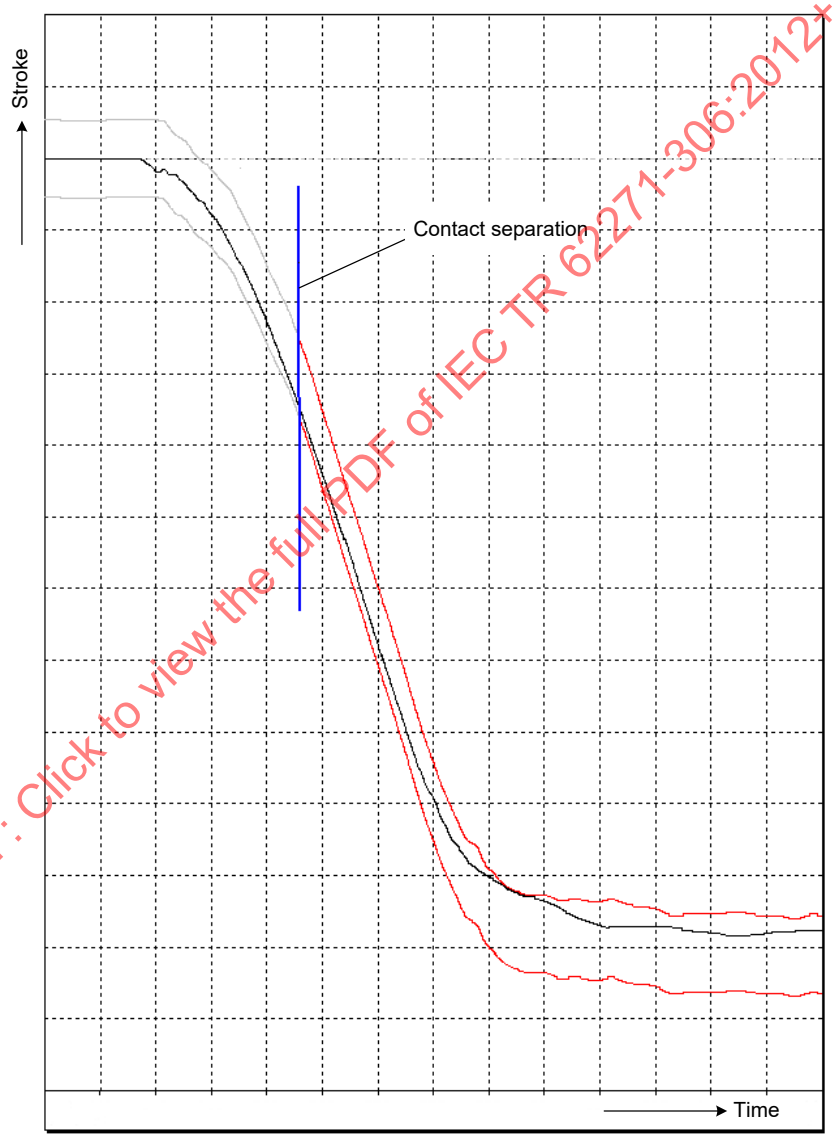
be subjected to a T100s test. The test shall be done under the same conditions as during the original type test.

The new combination shall pass the test according to the procedure of IEC 62271-100. Additionally, the mechanical characteristic during opening under the conditions of longest arcing time shall be compared with the travel curve of the original type test. The travel curve shall fulfil the requirements according to 6.101.1.1 of IEC 62271-100:2008.

In Figure 66 an example of the comparison of travel curves is given. The reference curve (red) was taken during a T100s test with the original operating mechanism, longest arcing time 18 ms. The alternative operating mechanism had a longest arcing of time 19 ms (black curve). The requirement to stay in the ±5 % tolerance band (or the shifted envelope curves) after contact separation is fulfilled. Therefore the alternative operating mechanism fulfils the requirement B of 6.102.7 of IEC 62271-100:2008.



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Key

Red traces	Envelope of the reference mechanical characteristics
Black trace	Mechanical characteristics of the alternative operating mechanism

Figure 66 – Mechanical characteristics during a T100s test

11.2.4 Additional test T100a

11.2.4.1 General

In some cases the opening time of the operating mechanisms can vary and the alternative operating mechanism may fall into a different category of minimum clearing time (see 3.7.157 of IEC 62271-100:2008 and Tables 15 to 22 of IEC 62271-100:2008). According to IEC 62271-100, in this case a test duty T100a shall be performed on the circuit-breaker with alternative operating mechanism.

As the aim of the test procedure of 6.102.7 of IEC 62271-100:2008 is to reduce the number of tests during qualification of an alternative operating mechanism two cases are investigated.

11.2.4.2 Case 1

Data of the original test:

– Opening time 25 ms
– Shortest arcing time 12 ms
– Test frequency 50 Hz → Relay time 10 ms
– Network time constant 45 ms → Table 15 of IEC 62271-100:2008

The circuit-breaker was tested according to row 3 of Table 15 of IEC 62271-100:2008 as the minimum clearing time $t_{clear\ min}$ is

$t_{clear\ min}$ = 25 ms + 12 ms + 10 ms = 47 ms

43,5 ms < $t_{clear\ min}$ ≤ 64 ms → row 3 of Table 15 of IEC 62271-100

Data of the alternative operating mechanism:

– Opening time 19 ms
– Shortest arcing time 12,5 ms

The travel curve of the alternative operating mechanism will be within the boundaries if a comparison is made according to 6.101.1.1 of IEC 62271-100:2008. The difference of opening time is only a result of a longer reaction time on the trip command of the drive used for the original tests.

$t_{clear\ min}$ = 19 ms+ 12,5 ms + 10 ms = 41,5 ms

$t_{clear\ min}$ < 43,5 ms → not row 3 of Table 15 of IEC 62271-100:2008

22,5 ms < $t_{clear\ min}$ ≤ 43,5 ms → row 2 of Table 15 of IEC 62271-100:2008

As the combination of circuit-breaker with alternative operating mechanism falls into a higher severity class for the T100a test, this test has to be performed with the alternative operating mechanism.

11.2.4.3 Case 2

Data of the original test:

– Opening time 17 ms
– Shortest arcing time 12 ms
– Test frequency 50 Hz → Relay time 10 ms

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– Network time constant 45 ms → Table 15 of IEC 62271-100:2008

The circuit-breaker was tested according to row 2 of Table 15 of IEC 62271-100:2008 as the minimum clearing time is

$t_{clear\ min}$ = 17 ms+ 12 ms + 10 ms = 39 ms

22,5 ms < $t_{clear\ min}$ ≤ 43,5 ms → row 2 of Table 15 of IEC 62271-100:2008

Data of the alternative operating mechanism:

– Opening time 23 ms
– Shortest arcing time 12,5 ms

The travel curve of the alternative operating mechanism will be within the boundaries if a comparison is made according to 6.101.1.1 of IEC 62271-100:2008. The difference of opening time is only a result of a longer reaction time of trip command.

$t_{clear\ min}$ = 23 ms + 12,5 ms + 10 ms = 45,5 ms

43,5 ms < $t_{clear\ min}$ ≤ 64 ms → row 3 of Table 15 of IEC 62271-100:2008

As the combination of circuit-breaker with the alternative operating mechanism falls into a less severe class for the T100a test, this test does not need to be performed with the alternative operating mechanism. The stress for the circuit-breaker under the conditions of an asymmetric short-circuit is less for the circuit-breaker with the alternative operating mechanism as the d.c. component will be smaller during the arcing time. The original test with the higher d.c.-component covers the smaller dc-component.

11.2.5 Conclusions

An alternative operating mechanism is qualified when the requirements of 6.102.7 of IEC 62271-100:2008 are fulfilled.

Test duty T100a should only be performed when the minimum clearing time of the alternative operating mechanism is shorter, such that the circuit-breaker should be tested with a higher d.c. component.

12 Rated and test frequency

12.1 General

Two different frequencies are used in electric power systems. These frequencies are 50 Hz and 60 Hz.

All circuit-breakers have to operate properly for each test duty and their rated frequency.

The rated frequency has an influence on the following tests:

– temperature rise;
– short-time withstand current;
– terminal fault tests;
– short-line fault test;
– capacitive current switching.

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The different test circuits used during testing also have an influence on the switching performance. These circuits are:

– direct test circuits;
– synthetic test circuit with voltage injection;
– synthetic test circuits with current injection.

12.2 Basic considerations

12.2.1 Temperature rise tests

The maximum temperature rise is dependent on the test frequency and the type of apparatus (GIS or AIS equipment) to be tested.

12.2.2 Short-time withstand current and peak withstand current tests

The short-time withstand current test is characterised by the duration of the short-circuit.

The tolerance of the frequency is ±10 %, but for convenience of testing a wider tolerance is allowed. IEC 62271-1 contains a cautionary note that care should be taken when interpreting test results when 50 Hz test are used to cover 60 Hz and vice versa.

The highest dynamic stress on the contacts and connections occurs during the peak withstand current test. The peak of the current is determined by the time constant of the network (see Annex A) and the rated frequency. IEC 62271-1 specifies three values for the peak factor (k = I_{peak}/i_{sym}). They are:

– 2,5 for a rated frequency of 50 Hz and a time constant of 45 ms;
– 2,6 for a rated frequency of 60 Hz and a time constant of 45 ms;
– 2,7 for rated voltages higher than 800 kV, where the standard time constant is 120 ms, independent of the frequency.

The special cases time constants are covered by a preferred peak factor of 2,7.

12.2.3 Short-circuit making current

The peak of the making current is determined by the time constant of the network and the rated frequency. IEC 62271-100 states the following values for the peak factor (k = I_{peak}/i_{sym}):

– 2,5 for a rated frequency of 50 Hz and a time constant of 45 ms;
– 2,6 for a rated frequency of 60 Hz and a time constant of 45 ms;
– 2,7 for rated voltages higher than 800 kV, where the standard time constant is 120 ms, independent of the frequency;
– 2,7 for all special cases time constants, independent of the frequency.

12.2.4 Terminal faults

A higher frequency leads to a shorter arcing window, because the time between two current zeros is correspondingly lower. For example, when the minimum arcing time of a circuit-breaker is 12 ms, the maximum arcing time that has to be demonstrated for single-phase testing at 50 Hz is 21 ms (12 – 1 + 10 ms). At 60 Hz the maximum arcing time is 19,5 ms (12 – 0,8 + 8,3 ms).

For test-duty T100a, a separate test may be necessary to prove that the operating mechanism has sufficient energy in case of 50 Hz application when the test has been performed using a 60 Hz current source, even if longer arcing times derived from 50 Hz requirements have been tested. The same is applicable for metal enclosed and dead tank circuit-breakers due to

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higher exhaust energy at longer arcing times, which can influence the phase-to-phase or phase-to-earth insulation.

The ITRV stress for different rated frequencies in live-tank circuit-breaker application is not taken into consideration when:

– the short-line fault test is carried out with a line-side time-delay t_{dL} equal to zero without significant differences in arcing time between short-line fault and terminal fault tests;
– the arcing window covers the corresponding frequency.

In the case that the terminal fault test is tested in a synthetic test circuit with voltage injection and the short-line fault test is not carried out with a line-side time delay less than 100 ns, the terminal fault test has to be performed with ITRV, where applicable.

12.2.5 Short-line fault

For short-line fault tests both the rate-of-decay of the short-circuit current before current zero and the arcing window are important factors. A higher rated frequency means a higher rate-of-rise of the line side TRV. Since the rate-of-rise of the line side TRV influences mainly the thermal interrupting behaviour of a circuit-breaker, it is important that the di/dt in the test report equal to or higher than required for the specified frequency.

For example a 90 % short-line fault test performed at 50 Hz with a line impedance of 450 Ω for a rated short-circuit current of 40 kA results in a line-side rate-of-rise of the TRV of 7,2 kV/μs, whereas the same test performed at 60 Hz would have a 20 % higher rate-of-rise of the line side TRV.

Therefore tests performed at 50 Hz are only valid for 60 Hz provided that the tests are performed with a synthetic test circuit where the di/dt is adjusted to 60 Hz.

If the test is performed at 60 Hz, it is only valid for a rated frequency of 50 Hz provided that the maximum arcing time for 50 Hz is covered. However, this is only possible in synthetic test circuit because any arcing time can be chosen.

12.2.6 Capacitive current switching

When the interrupting performance of a circuit-breaker for different rated frequencies is compared in capacitive switching tests, the only important factor is the recovery voltage as function of time. It is characterised by the voltage peak and the time to peak. Since the withstand capability of a circuit-breaker is a function of time, the higher frequency results in a higher stress on the circuit-breaker at arcing times close to zero. For example, the time to peak for 50 Hz is 10 ms, whereas it is only 8,3 ms in 60 Hz applications.

When interrupting with arcing times longer than the minimum arcing time, the contact gap is wider and therefore the voltage withstand of the circuit-breaker is higher. Maximum arcing time is therefore not an important factor when comparing tests performed at different frequencies.

To obtain the correct voltage stress between circuit-breaker contacts, synthetic capacitive circuits can be used.

12.3 Applicability of type tests at different frequencies

12.3.1 Temperature rise tests

Applicability of the tests for the different frequencies is given in Table 17.

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Table 17 – Temperature rise tests

Test frequency (Hz)	Test results acceptable at other frequency?
50	Yes, see NOTE
60	Yes
NOTE Tests performed at 50 Hz on circuit-breakers having no ferrous components adjacent to the current-carrying parts cover the performance at 60 Hz, provided that the temperature-rise values recorded during the tests at 50 Hz do not exceed 95 % of the maximum permissible values.	

12.3.2 Short-time withstand current and peak withstand current tests

Applicability of the tests for the different frequencies is given in Table 18 and Table 19.

Table 18 – Short-time withstand current tests

Test frequency (Hz)	Test results acceptable at other frequency?
50	Yes
60	Yes

Table 19 – Peak withstand current tests

Test frequency (Hz)	Test results acceptable at other frequency?
50	Yes, if 60 Hz peak factor is used
60	Yes

12.3.3 Short-circuit making current test

Applicability of the tests for the different frequencies is given in Table 20.

Table 20 – Short-circuit making current tests

Test frequency (Hz)	Test results acceptable at other frequency?
50	Yes, if 60 Hz peak factor is used
60	Yes

12.3.4 Terminal faults (direct and synthetic tests)

It is widely accepted that, for presently available technologies, the applicability of the tests for different frequencies is as presented in Table 21 and Table 22. However, in order to ensure the best possible clarity and accuracy for (type) testing, and to avoid any doubt about the applicability of results, IEC 62271-100 requires that tests be made at the rated frequency.

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Table 21 – Terminal faults: symmetrical test duties

Test frequency		Test method		Test results acceptable at other frequency?
50 Hz	60 Hz	Direct	Synthetic	
X		X		No, di/dt for 60 Hz not covered, see NOTE
X			X	Yes, provided di/dt for 60 Hz covered
	X	X		Yes, if arcing window for 50 Hz is covered
	X		X	Yes, provided arcing window for 50 Hz is covered
NOTE It is recognized that for vacuum circuit-breakers di/dt is not a relevant criterion for comparison and tests at 50 Hz are acceptable for 60 Hz ratings, but not vice versa.				

Table 22 – Terminal faults: asymmetrical test duties

Test frequency		Test results acceptable at other frequency?
50 Hz	60 Hz	
X	X	Yes, if the asymmetry requirements and arcing times of IEC 62271-100 are met

12.3.5 Short-line fault (direct and synthetic tests)

It is widely accepted that, for presently available technologies, the applicability of the tests for different frequencies is as presented in Table 23. However, in order to ensure the best possible clarity and accuracy for (type) testing, and to avoid any doubt about the applicability of results, IEC 62271-100 requires that tests be made at the rated frequency.

Table 23 – Short-line faults

Test frequency		Test method		Test results acceptable at other frequency?
50 Hz	60 Hz	Direct	Synthetic	
X		X		No, di/dt for 60 Hz not covered, see NOTE
X			X	Yes, if di/dt for 60 Hz covered
	X	X		Yes, if arcing window for 50 Hz is covered
	X		X	Yes, if arcing window for 50 Hz is covered
NOTE It is recognized that for vacuum circuit-breakers di/dt is not a relevant criterion for comparison and tests at 50 Hz are acceptable for 60 Hz ratings, but not vice versa.				

12.3.6 Capacitive current switching

Applicability of the tests for the different frequencies is given in Table 24.

Table 24 – Capacitive current switching

Test frequency (Hz)	Test results acceptable at other frequency?
50	No
60	Yes

Tests performed at 50 Hz are only applicable to 60 Hz if the recovery voltage at any point from zero to the first peak equals to or exceeds the required 60 Hz recovery voltage waveshape. This means that a higher test voltage needs to be used. To fully cover a 60 Hz

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test with a 50 Hz voltage, the test voltage needs to be increased with a factor of 1,44 compared to the 50 Hz test voltage.

13 Symmetrical and asymmetrical currents

13.1 General

This clause treats symmetrical and asymmetrical short-circuit currents and their arcing times.

Test requirements for symmetrical terminal fault conditions that are covered by short-circuit test duties T100s, T60, T30, and T10 are covered in 13.3. The asymmetrical duty T100a is covered in 13.4 and the various short-line fault and out-of-phase duties are considered elsewhere in this document.

The purpose of this clause is to provide a background framework for some of these requirements where it may not be clear from the latest revision of the standard, or from readily available text books, how they were derived. Aspects covered in this clause are those relating to the short-circuit current, particularly to the arcing time and the voltages, both power frequency and transient recovery voltage (TRV), associated with terminal faults.

13.2 Arcing time

The arcing time of a pole of a circuit-breaker is defined as the interval of time between the instant of the first initiation of an arc in a pole and the instant of arc extinction in that pole.

There are several possible methods to determine the arcing time.

a) Using the opening time of the circuit-breaker

   When a tripping coil current signal is available, the arcing time is determined by subtracting the opening time from the break time of the pole considered.

b) Using a travel recorder

   The arcing time is the duration between the contact separation point identified on the travel curve, and the instant of interruption. The instant of contact separation is determined during the no load measurements before the test.

c) Using amplified arc voltage

   The arcing time is the duration between the contact separation, determined on the amplified arc voltage, and the instant of current interruption.

For gas circuit-breakers method b) is the preferred method. This method is considered more accurate as it eliminates the possible error in method a) due to mechanical scatter of the operating mechanism. For circuit-breakers having butt contacts, method c) is recommended.

13.3 Symmetrical currents

13.3.1 Demonstration of arcing time

Throughout IEC 62271-100 and related documents the terms arcing time and interrupting window are used, especially in relation to the interruption of short-circuit currents. To understand the requirements of the various subclauses of IEC 62271-100:2008, such as 6.102.10, it is necessary to understand the meaning of these terms and that of the terms minimum and maximum arcing time in particular.

The arcing time of a three-pole circuit-breaker is defined as the interval of time between the instant of first initiation of an arc (typically at contact separation) and the instant of final arc extinction in all three phases. Arcing time is measured in ms, or in electrical degrees (e.g. 10,0 ms at 50 Hz and 8,3 ms at 60 Hz are 180°). The shortest arcing time at which the circuit-breaker is able to interrupt is the minimum arcing time.

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Depending on the point of contact separation and the particular current, the arcing time of a circuit-breaker will vary between this minimum value and a maximum value. The difference between these values is called the interrupting window (or more rarely the arcing window). Although different designs of circuit-breaker will be capable of interrupting with different duration of their interrupting windows there is a basic requirement which is applicable to all modern designs of circuit-breaker. For these circuit-breakers the minimum arcing time is short or relatively short, and in addition they have limited capability for prolonged arcing as their quenching period is also short.

The aim of each test-duty (e.g. T100s or T60) is to demonstrate the breaking capacity with any arcing time within this interrupting window. This requirement is fulfilled by demonstration of interruption at minimum, maximum and medium arcing time. The minimum and maximum arcing times cannot be demonstrated in a single valid test. In the case of fault interruptions involving three-phases, the minimum arcing time is obtained in one of the valid tests of a test-duty with the first-pole-to-clear and the maximum arcing time is obtained in another valid test with the last pole(s) to clear.

For single-phase faults the maximum arcing time is the period to the end of the interrupting window of the faulted phase, consisting of the minimum arcing time plus one loop of fault current minus 18°. This 18° is related to a deliberately specified step, of equal duration for 50 Hz and 60 Hz, giving a point of contact separation a short time later than that giving the minimum arcing time. At this setting the arcing time is too short for satisfactory clearance as a minimum, by definition, and an additional loop i.e.180° will follow until the next current zero. Clearance at this later current zero results in the maximum arcing time and the end of the interrupting window. The specified step of 18° is the smallest practical value for such a step generally achievable at testing stations being 1 ms at 50 Hz and 0,8 ms at 60 Hz.

13.3.2 Demonstration of the arcing time for three-phase tests

In accordance with IEC 62271-100, each test-duty consists of demonstration of interruption within the interrupting window. This requirement is fulfilled by demonstration of interruption at minimum, maximum and medium arcing time, i.e. by three valid tests of each of the specified short-circuit test duties.

When three-phase symmetrical current tests are to be demonstrated using direct test techniques, the possible arcing times are automatically obtained by changing the setting of contact separation by a duration of 40° between each of the three required opening operations of the operating sequence (refer to 6.102.10.1.1 of IEC 62271-100:2008). In this way, taking into account that current passes through zero on one of the phases every 60°, the minimum arcing time is determined with a accuracy of less than 20°.

For synthetic testing the procedure is defined in IEC 62271-101.

13.3.3 Interrupting window and k_p requirements for testing

Separate procedures exist for tests performed in substitution for three-phase conditions by using a single pole of the circuit-breaker.

The procedure as defined is for circuit-breakers to be installed in systems with non-effectively earthed neutral and separately for those with effectively earthed neutrals. The relevant subclauses in IEC 62271-100:2008 are 6.102.10.2.1 and 6.102.10.2.2.

In accordance with IEC 62271-100, the required interrupting window shall be demonstrated for each condition in the case of interruptions with symmetrical currents, as for test duties T10, T30, T60, and T100s. (Note, this also applies to short-line fault and the out-of-phase test-duties OP1 and OP2). Whether the testing is for three-phase test requirements, or single-phase tests in substitution for the three-phase condition, it is important that the interrupting window and associated TRV are demonstrated for the relevant system condition. In the case of a single-phase test, the three tests of the duty are demonstrated on that single pole, as it is

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the representative sample of the circuit-breaker, as allowed in 6.102.2 of IEC 62271-100:2008.

The interrupting windows required by IEC 62271-100:2008 for circuit-breakers applied in a non-effectively earthed system are shown graphically in Figure 132. If contact parting is at the minimum arcing time ($t_{arc\ min}$) on one pole, then that pole clears at 0° in Figure 132 and is followed by the other two poles 90° later. The minimum three-phase arcing time is $t_{arc\ min}$ + 90°. If contact parting is now delayed by 18°, the first-pole-to-clear on one of the other two phases will interrupt the current at ($t_{arc\ min}$ – 18°) + 60° = $t_{arc\ min}$ + 42°. As before, the other two poles will clear 90° later giving a maximum three-phase arcing time of $t_{arc\ min}$ + 132°.

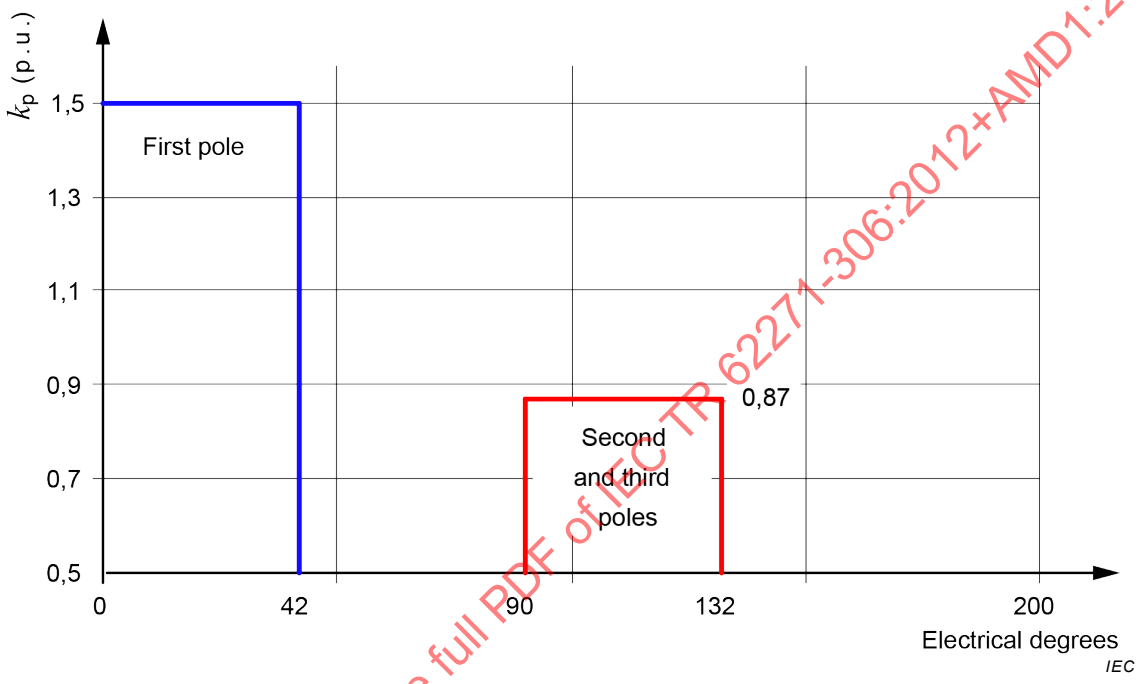

Figure 132 – Interrupting windows and k_p value for three-phase fault in a non-effectively earthed system

A practical example of this case is shown in Figure 133. In the upper trace, the blue phase clears first at the minimum arcing time of $t_{arc\ min}$ and the currents in the red and green each phase shift by 30° to become equal and opposite and are interrupted 90° later. In the lower trace, contact parting is delayed by 18° and the first suitable zero crossing for current interruption occurs on the red phase at ($t_{arc\ min}$ + 42° / 360° × T) ms, where T is the duration of one cycle of current (20 ms for 50 Hz and 16,7 ms for 60 Hz). The blue and green phases then clear at ($t_{arc\ min}$ (42° + 90°) / 360° × T)) ms.

The required interrupting windows for circuit-breakers applied in effectively earthed systems at 800 kV and below are shown in Figure 134 and at voltages above 800 kV are shown in Figure 135.

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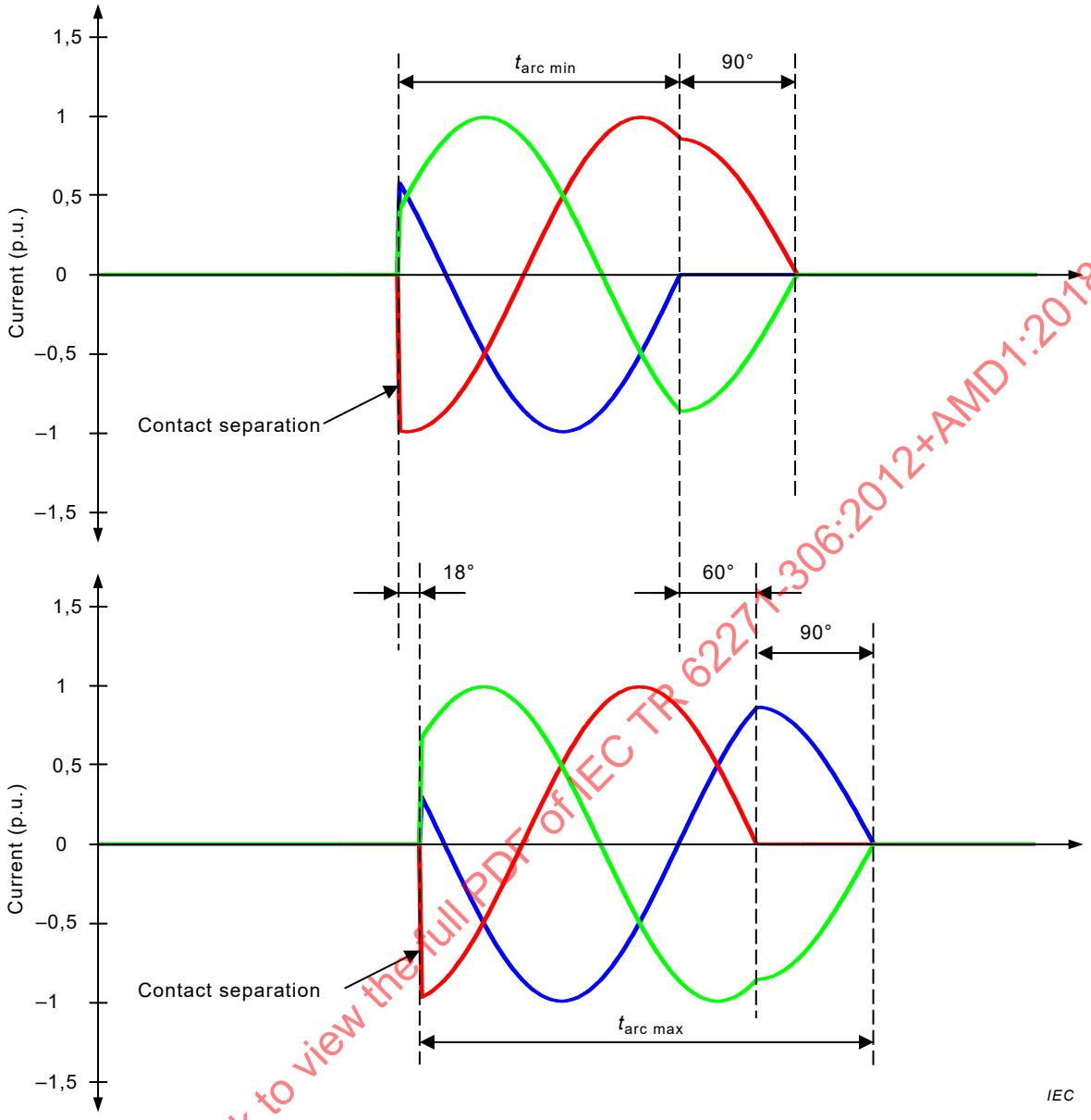

Figure 133 – Three-phase unearthed fault current interruption

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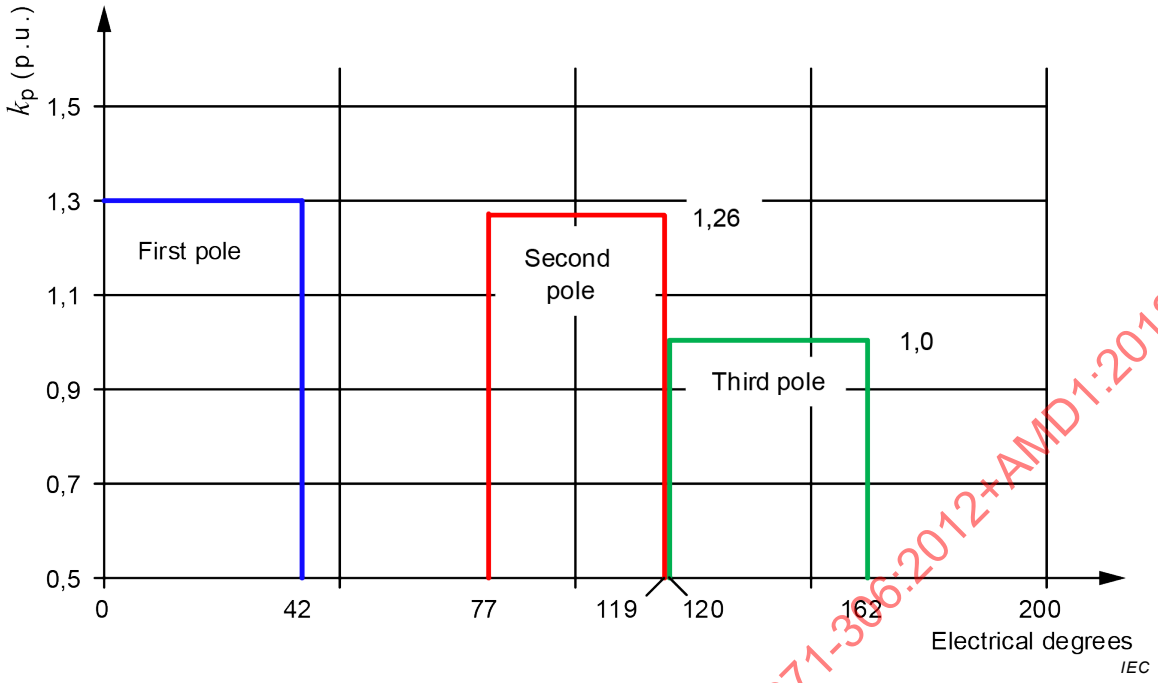

Figure 134 – Interrupting windows and k_p values for three-phase fault to earth in an effectively earthed system at 800 kV and below

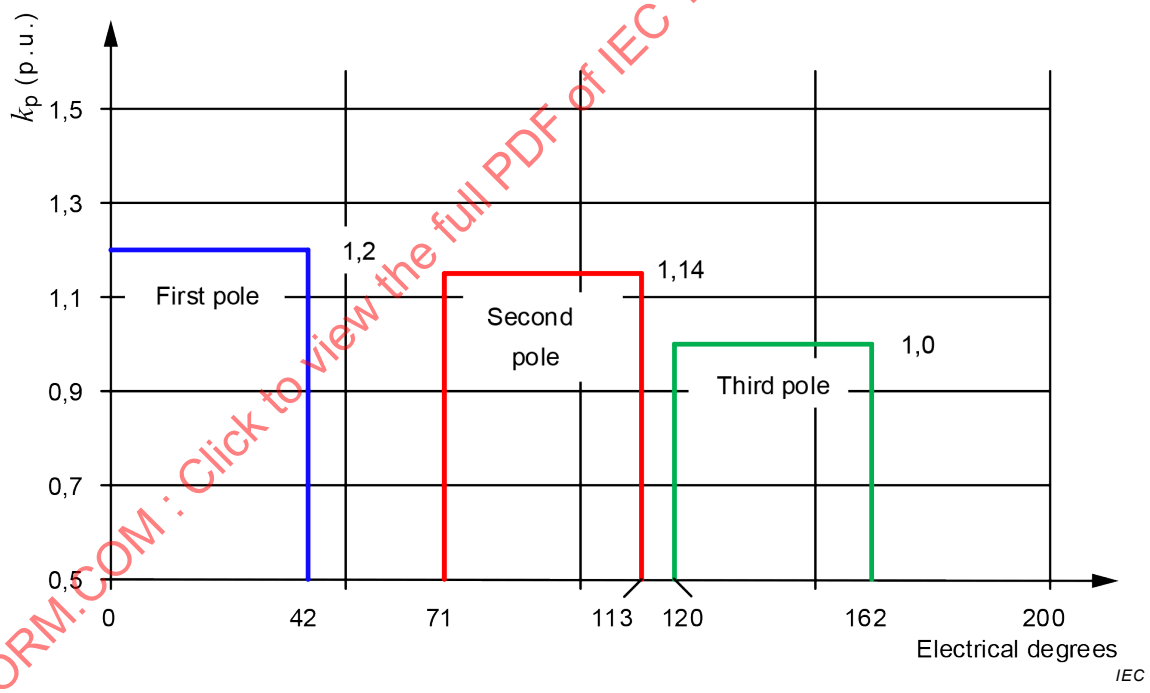

Figure 135 – Interrupting windows and k_p values for three-phase fault to earth in an effectively earthed system above 800 kV

Referring to Figure 134 and Figure 135, if contact parting is at the minimum arcing time on one pole, then that pole clears at 0° in either figure. The transition from a three-phase to a two-phase fault causes a phase shifting of the currents in the other phases and the second pole will clear at 77°. A further transition and phase shift results in the third pole clearing 43° later. The minimum three-phase arcing time is $t_{arc\ min}$ + ((77° + 43°) / 360°) × T = $t_{arc\ min}$ + 120° / 360° × T. If contact parting is delayed by 18°, the first-pole-to-clear will interrupt the current at ($t_{arc\ min}$ – 18° / 360° × T) + 60° / 360° × T, the second pole 77° / 360° × T later and

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the third pole 43° / 360° × T later still. The maximum three-phase arcing time is given by $t_{arc\ max}$ = ($t_{arc\ min}$ – 18° / 360° × T) + 60° / 360° × T + 77° / 360° × T + 43° / 360° × T = $t_{arc\ min}$ + 162° / 360° × T. Figure 136 shows a simulation of a three-phase fault current interruption. The first-pole-to-clear interrupts the current at $t_{arc\ min}$ followed by the second and third poles at 77° and 43°, respectively. The phase shifting of the current at first and second pole clearing is obvious.

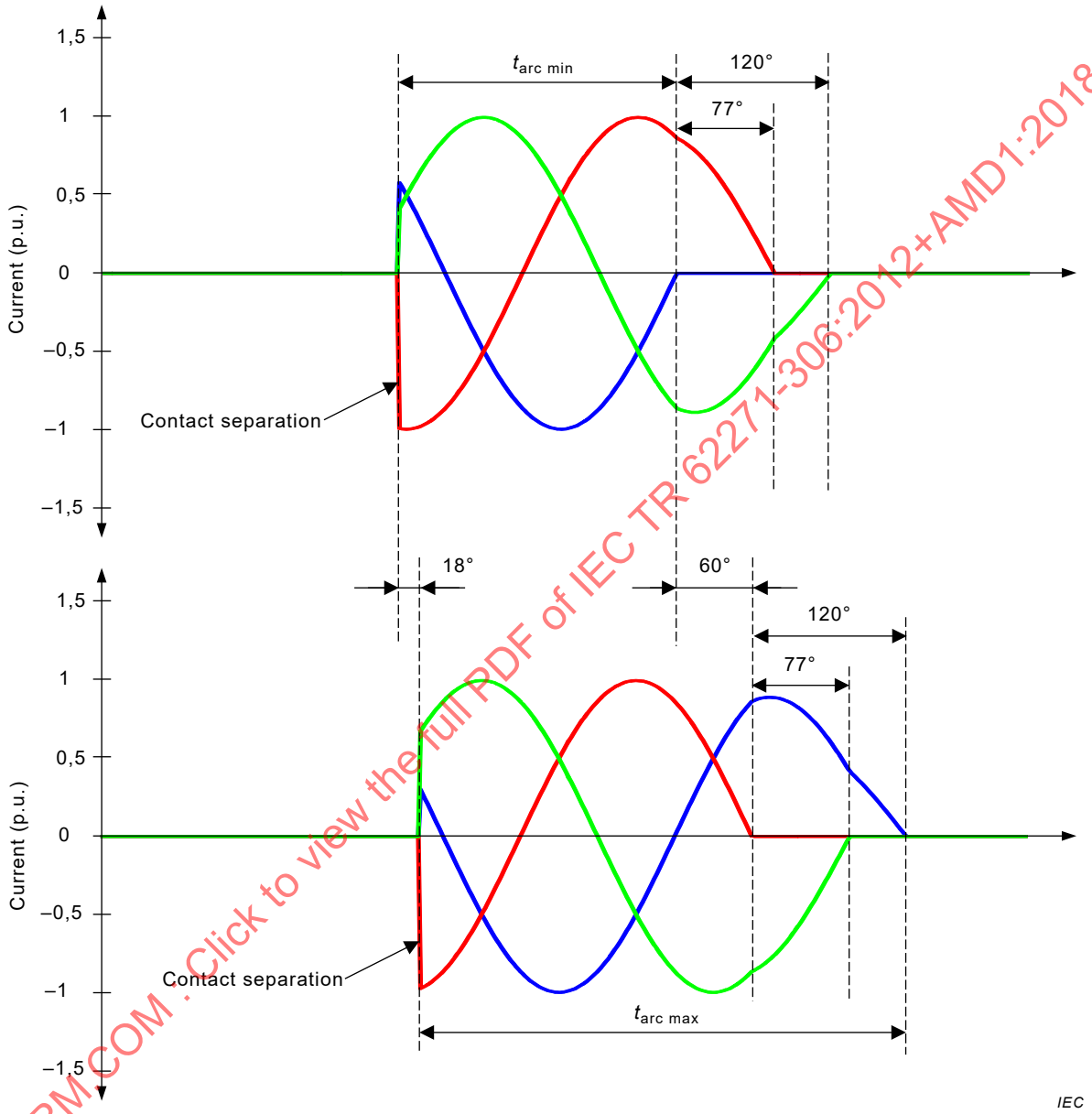

Figure 136 – Simulation of three-phase to earth fault current interruption at 50 Hz

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13.3.4 Single-phase testing to cover three-phase testing requirements

As discussed in 13.3.3, Figure 132, Figure 134 and Figure 135 show the interrupting windows and associated k_p values for individual pole clearing of three-phase faults. From Figure 132, it is acceptable to perform a single-phase test with k_{pp} = 1,5 and arcing times in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 132°. Likewise from Figure 134 and Figure 135, it is acceptable to perform a single-phase test with either k_{pp} = 1,2 or 1,3 as applicable and arcing times in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 162°. These tests are acceptable because the test requirements for each pole are equalled or exceeded and this has the advantage that only three valid interruptions are required.

IEC 62271-100 recognizes that the testing described above is more onerous and allows that the tests be split into individual tests for each pole and earthing arrangement case (see 6.102.10.2.5 of IEC 62271-100:2008). For the non-effectively earthed case (Figure 132), two test series are: the first at k_{pp} = 1,5 and arcing time in the range $t_{arc\ min}$ to $t_{arc\ min}$ + 42° and the second at k_p = 0,87 and arcing times in the range $t_{arc\ min}$ + 90° to $t_{arc\ min}$ + 132°. For the effectively earthed cases (Figure 134 and Figure 135), three test series are correspondingly required to address all three-pole clearing requirements.

13.3.5 Combination tests for k_{pp} = 1,3 and 1,5

For a requirement with a first-pole-to-clear factor of 1,3, it is possible to adapt the test procedure during tests for a factor of 1,5. In accordance with IEC 62271-100, two alternatives exist:

– For three-phase tests, if a complete series of test-duties demonstrating the circuit-breaker performance for k_{pp} = 1,5 is already performed, test-duties T100s and T100a shall be repeated with a test-circuit simulating the earthing condition of an effectively earthed neutral system. The repetition of test-duties T100s and T100a with a three-phase circuit for an effectively earthed neutral system can, as an alternative, be replaced by additional single-phase tests.

– For single-phase tests both conditions (k_{pp} = 1,5 and k_{pp} = 1,3) may be combined in one test series. The transient and power frequency voltages to be used shall be those applicable to a non-effectively earthed neutral system and the arcing times shall be those applicable to an effectively earthed neutral system.

  For test-duty T100a, the arcing times shall be those applicable to a non-effectively earthed neutral system.

13.3.6 Suitability of a particular short-circuit current rated circuit-breaker for use at an application with a lower short-circuit requirement

In accordance with 8.101 of IEC 62271-100:2008, circuit-breakers that have satisfactorily completed type tests for a combination of rated values (i.e. voltage, normal current, making and/or breaking current) are suitable for any application with lower service values (with the exception of frequency), without further testing.

The reason for this is related to the combination of the transient-recovery-voltage (TRV) requirements and the current values for the basic short-circuit test duties. This can be demonstrated by using the following example where a circuit-breaker tested for a rated voltage U_r of 420 kV, 50 kA rating is considered for an application requirement of 420 kV, 30 kA.

At 420 kV, the T100, T60, T30 and T10 duty TRV values are detailed in Table 26 of IEC 62271-100:2008 and reproduced in an abbreviated form below for convenience.

The circuit-breaker being considered satisfies the TRV peak and rate-of-rise etc. of the duties shown in the upper part of Table 48. Those for the application are shown in a similar form in the lower part of the table and are compared as illustrated by the arrows.

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Table 48 – Example of comparison of rated values against application (U_r = 420 kV)

Duty for circuit-breaker (current)	**T100** (50 kA)	**T60** (30 kA)	**T30** (15 kA)	**T10** (5 kA)
TRV peak value	624	669	669	787
Rate of rise	2,0	3,0	5,0	7,0
		↓	↓	↓ ↓ ↓
Duty of application (current)	-	T100 (30 kA)	T60 (18 kA)	T30 (9 kA)	T10 (3 kA)
TRV peak value	-	624	669	669	787
Rate of rise	-	2,0	3,0	5,0	7,0

As can be seen from Table 48, the evidence from the upper part of the table provides significant overlapping evidence for the application shown in the lower part. This is the reason why 8.101 of IEC 62271-100:2008 is acceptable in this case.

Users should exercise due diligence in all cases and most particularly where the difference between the rating and the requirement is so great that the requirements of the application become far removed from the evidence provided by type testing. In such cases, discussions may be required with the supplier. Additional test evidence may be required.

13.4 Asymmetrical currents

13.4.1 Test procedure for test-duty T100a

13.4.1.1 General

A new test procedure was introduced for test-duty T100a in IEC 62271-100:2008/AMD:2017 in order to obtain a better correspondence between the test conditions during three-phase tests and single-phase tests made in substitution for three-phase tests (same amplitude of the major loop, arcing times, etc.). The new test procedure is based on the fact that the relevant major loop of current with full asymmetry to consider before current interruption for the two main test conditions depends on the capability of the circuit-breaker to interrupt after a minor loop of current with intermediate asymmetry. The two main test conditions are as follows:

– interruption of the first-pole-to-clear after a major loop of current with required asymmetry and longest arcing time;

– interruption of a last-pole-to-clear after a major extended loop of current with required asymmetry and longest arcing time in case the of k_{pp} = 1,5 or interruption of the second pole to clear after a major extended loop of current with the required asymmetry and longest arcing time in the case of k_{pp} = 1,3.

This consideration is explained in 13.4.1.2 using the case with k_{pp} = 1,5. In IEC 62271-100:2008, it is not considered necessary to prove interruption of the third-pole-to-clear in case of k_{pp} = 1,3 because the peak of the TRV, di/dt at current zero and the energy in the arc are lower than that of the second-pole-to-clear. The performance of the third-pole-to-clear is verified during test-duty T100s.

A definition has been introduced in IEC 62271-100:2008 to define the minimum clearing time of a circuit-breaker: it is the sum of the minimum opening time, minimum relay time (0,5 cycle) and the shortest arcing time of a minor loop interruption in the phase with intermediate asymmetry that starts with a minor loop at short-circuit current initiation. It will be illustrated by the examples in 13.4.1.2.

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13.4.1.2 Basis for test-duty T100a

To illustrate the different cases of three-phase fault interruption presented hereafter the following parameters are chosen:

– rated frequency is 50 Hz, the relay time is 10 ms, k_{pp} = 1,5;

– opening time = 11,5 ms and the shortest arcing time (blue phase) is 5 ms;

– the minimum clearing time is then 10 + 11,5 + 5 = 26,5 ms.

Figure 137 illustrates a first case of three-phase fault interruption in which a first pole (blue phase) clears after minor loop of current with intermediate asymmetry. This is possible as the minimum clearing time is lower than the duration of 27 ms between initiation of the short-circuit current and passage through zero of current in the blue phase.

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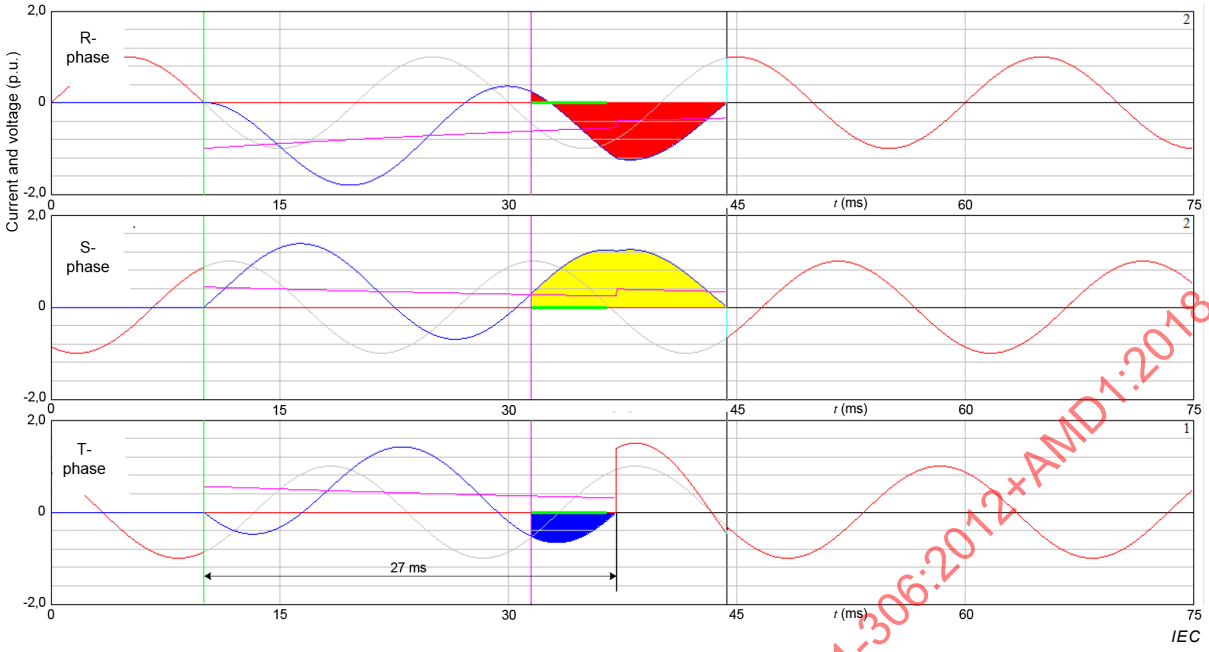

Figure 137a – Case 1 with k_{pp} = 1,5

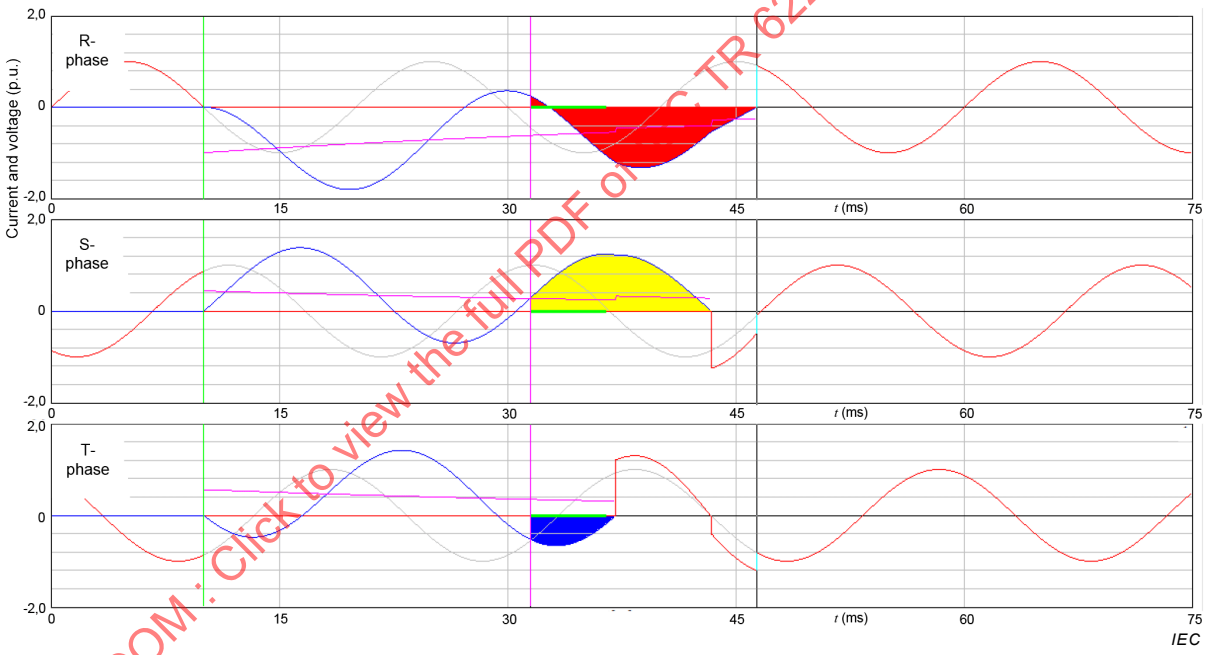

Figure 137b – Case 1 with k_{pp} = 1,3

Figure 137 – Case 1 with interruption by a first pole (blue phase) after minor loop of current with intermediate asymmetry

Figure 138 illustrates case 2 obtained when contact separation is delayed by 18° (1 ms at 50 Hz), a first pole interrupts after a major loop of current with intermediate asymmetry (yellow phase). For the case with k_{pp} = 1,5 a last pole clears a major extended loop with required asymmetry and the longest possible arcing time. For the case with k_{pp} = 1,3 the second pole clears a major loop with required asymmetry and the longest possible arcing time. This is one of the two breaking conditions for which interruption shall be proved.

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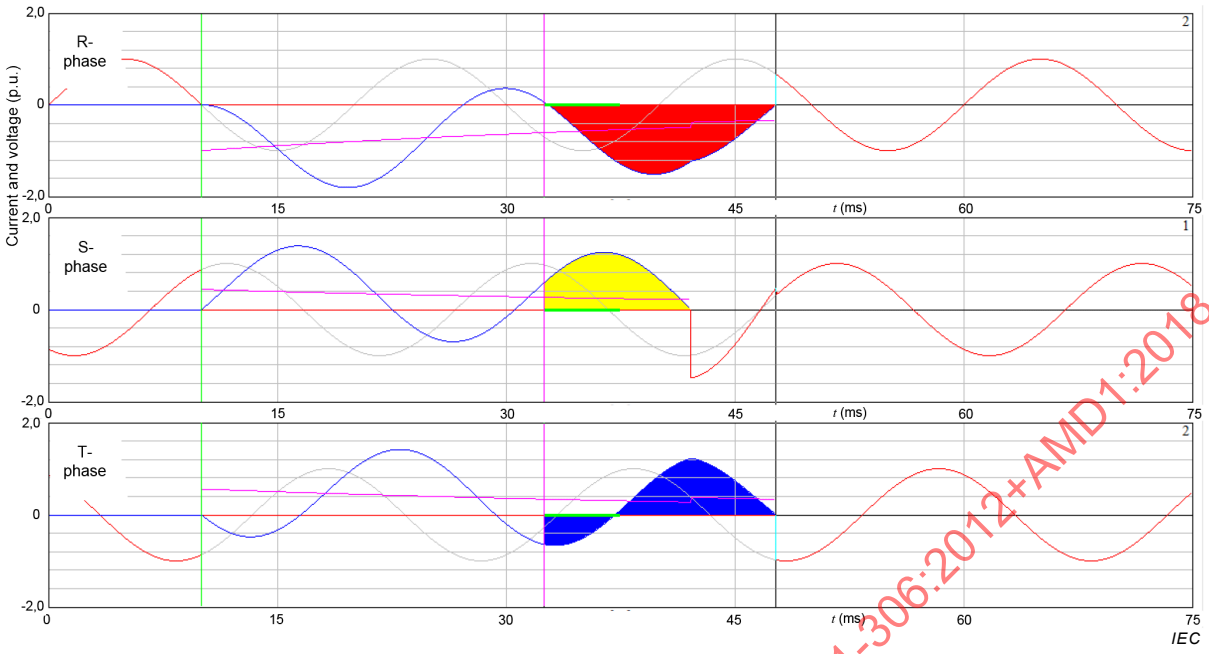

Figure 138a – Case 2 with k_{pp} = 1,5

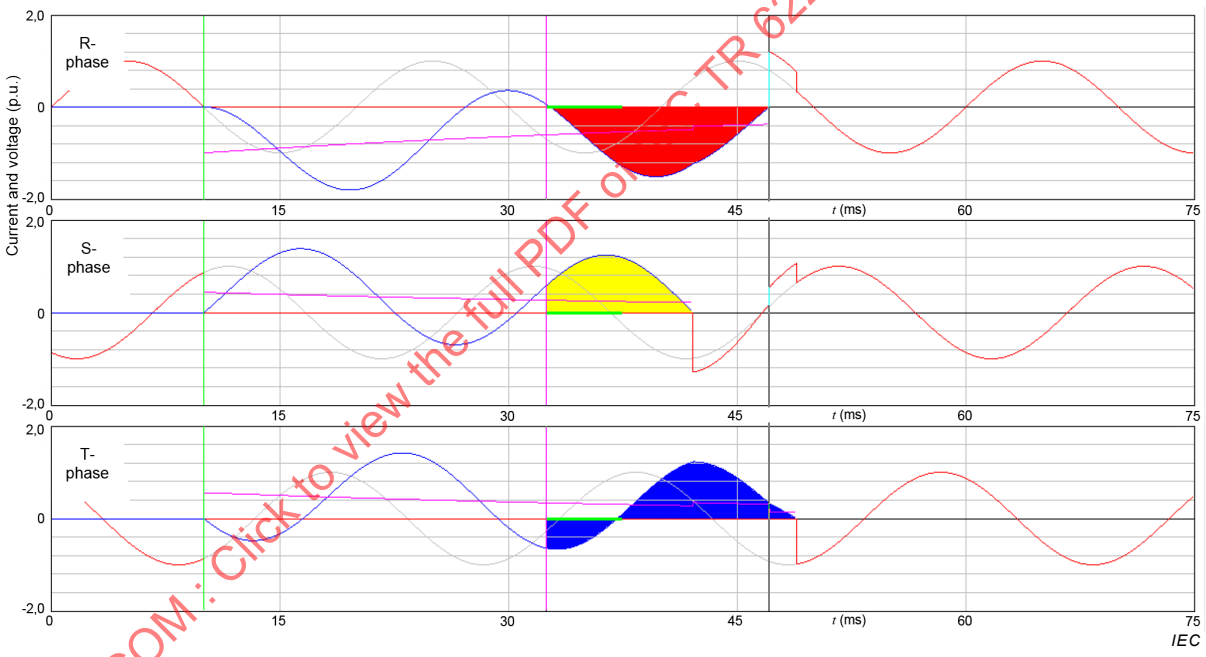

Figure 138b – Case 2 with k_{pp} = 1,3

Figure 138 – Case 2 with interruption of a last pole-to-clear after a major extended loop of current with required asymmetry and longest arcing time

Figure 139 illustrates case 3 obtained when contact separation is delayed by 72°, this test condition is less severe, as last pole that clears in the red phase with a major extended loop has a shorter arcing time.

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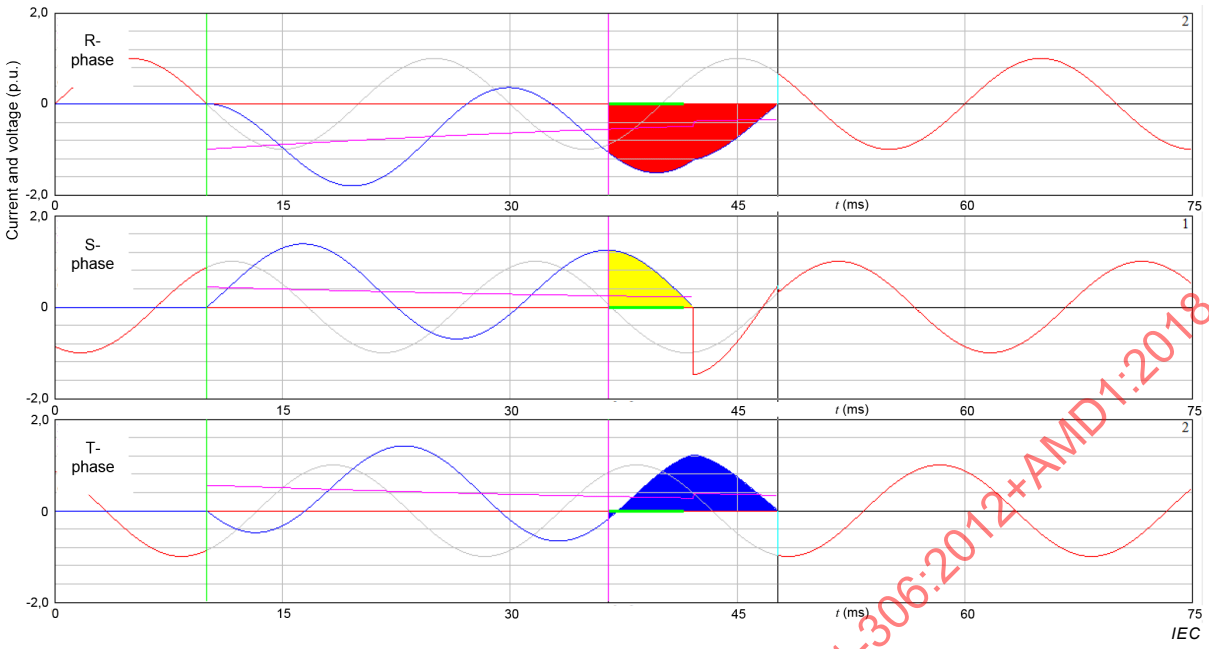

Figure 139 – Case 3 with interruption of a last pole-to-clear after a major extended loop of current with required asymmetry but not the longest arcing time

Figure 140 illustrates case 4 obtained when contact separation is further delayed by 18°. It shows that the first pole clears in the red phase after a major loop with required asymmetry and the longest arcing time for a first-pole-to-clear. It is the second breaking condition for which interruption shall be proved. It should be noted that the major loop with maximum asymmetry to consider for the first-pole-to-clear is the same as seen in case 2 (for a last-pole-to-clear). It is function of the minimum clearing time.

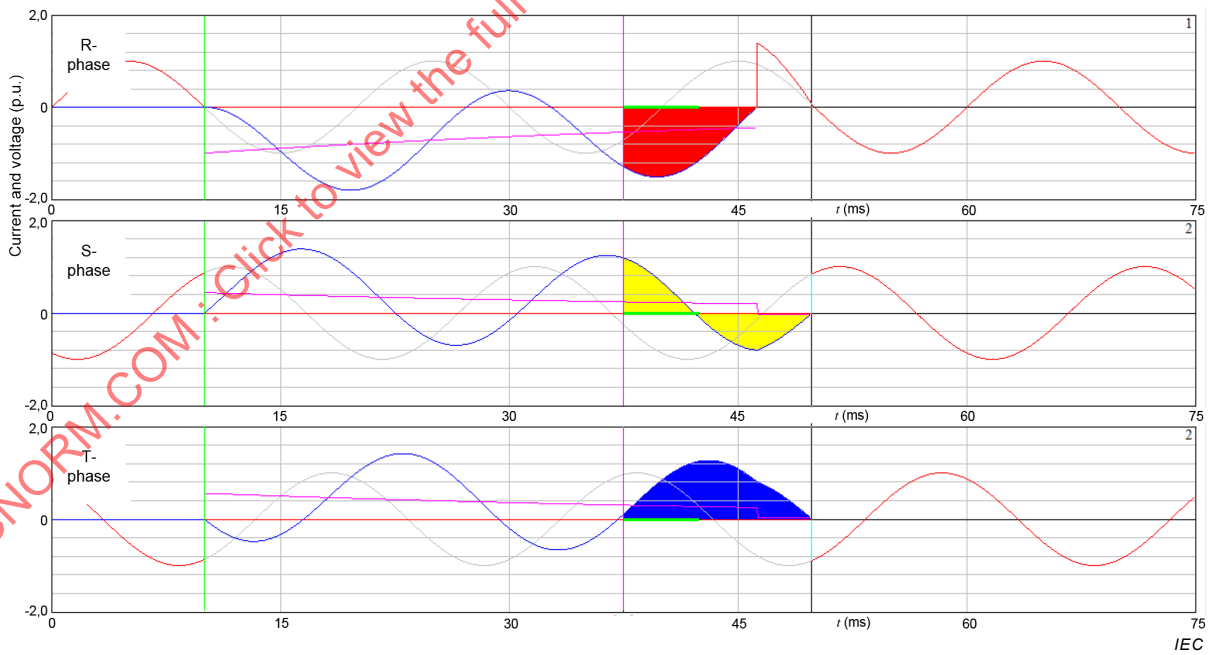

Figure 140 – Case 4 with interruption by the first pole in the red phase after a major loop of current with required asymmetry and the longest arcing time (for a first-pole-to-clear)

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The case considered in this example corresponds to the first line of Table 41 in IEC 62271-100:2008/AMD2:2017, i.e. with a minimum clearing time in the interval higher than 10 ms and equal to or lower than 27 ms. The other intervals of minimum clearing time given in Table 41 are the intervals between each possible instant of interruption after a minor loop in the blue phase.

13.4.2 Advice for the choice of the appropriate time constant

A DC time constant of 45 ms is adequate for the majority of actual cases except for rated voltages higher than 800 kV for which the standard DC time constant is 120 ms. Special case time constants, related to the rated voltage of the circuit-breaker, should cover such cases where the standard time constant 45 ms is not sufficient. This may apply, for example, to systems with very high rated voltage (for example 800 kV systems with higher X/R ratio for lines), to some medium voltage systems with radial structure or to any systems with particular system structure or line characteristics. Special case time constants have been defined, taking into account the results of the survey by CIGRE WG13.04 [139] .

When specifying a special case time constant, the following considerations should be taken into account:

a) The time constants referred to in IEC 62271-100:2008 are only valid for three-phase fault currents. The single-phase to ground short-circuit time constant is lower than that for three-phase fault currents.

b) For maximum asymmetrical current, the initiation of the short-circuit current has to take place at system voltage zero in at least one phase.

c) The time constant is related to the maximum rated short-circuit current of the circuit-breaker. If, for example, higher time constants than 45 ms are expected but with a short-circuit current lower than rated, such a case may be covered by the asymmetrical rated short-circuit current test using a 45-ms time constant.

d) The time constant of a complete system is a time-dependent parameter considered to be an equivalent constant derived from the decay of the short-circuit currents in the various branches of that system and is not a real, single time constant.

e) Various methods for the calculation of the DC time constant are in use, the results of which may differ considerably. Caution should be taken in choosing the right method.

f) When choosing a special case time constant, it has to be kept in mind, that the circuit-breaker is stressed by the asymmetrical current after contact separation. The time instant of contact separation corresponds to the opening time of the circuit-breaker and the reaction time of the protection relay. In this document, this relay time is one half-cycle of power frequency. If the protection time is longer this should be taken into account.

13.4.3 DC component during T100a testing

With the introduction of the special case time constants in IEC 62271-100:2001, the decisive parameters with their respective tolerances that should be followed during interruption of asymmetrical faults need to be defined in order to:

– be able to perform asymmetrical tests with a test circuit having a DC time constant different from the rated DC time constant of the rated short-circuit breaking current, because laboratories are not able to tune the DC time constant of the test circuit. For direct tests, when the DC time constant of the test circuit is higher than the rated DC time constant of the rated short-circuit breaking current, the resulting di/dt and TRV peaks are lower than those that can be seen in service conditions. The reverse situation is also true, mainly with the special case DC time constants (60 ms, 75 ms and 120 ms) introduced in IEC 62271-100:2001;

– be able to use the results obtained from one specific test to cover more than one DC time constant ratings. This concept of asymmetry equivalence may also help the user in establishing equivalence between system needs and the rating requirements.

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A lot of calculations made confirm that the former concept of DC component at contact separation (for example IEC 60056 and the first edition of IEC 62271-100:2001) leads to stresses during the tests (including minor and major loop interruptions) being different from those expected under service conditions. That is why IEC 62271-308 was published in 2002. IEC 62271-308 was incorporated in the first amendment to IEC 62271-100:2001.

The only way to obtain that equivalence is to introduce the concept of DC component at current zero. This concept is also applied in IEC 62271-101.

The maximum prospective DC component at current zero required during tests is determined by using the DC component given for the next complete current loop following the minimum interrupting time.

The parameters concerned by general equivalence criteria are:

a) the amplitude of the last current loop (both major loop or major extended loop);
b) duration of the last current loop (both major loop or major extended loop) before interruption;
c) arcing time;
d) di/dt at current zero;
e) TRV peak voltages, waveshape.

The three first points are linked to the arc energy.

To reach the equivalence according to this concept has led to a modification of some tolerances. For example, the tolerance (0 %, +10 %) on the symmetrical value of the test current has been changed in IEC 62271-100:2008/AMD2:2017 to +10 % and −10 % in order to be able to adjust the last current loop amplitude and duration to the required values. For some cases, it may be necessary to decrease or increase these values from the rated symmetrical short-circuit current.

With this procedure, depending on the actual test parameters, a specific test may cover several ratings if the applicable asymmetry criteria for each rating with their associated tolerances are met.

Annex A gives some guidance on how to use the asymmetry criteria.

13.5 Double earth fault

13.5.1 Basis for specification

This test requirement is limited to applications in non-effectively earthed systems.

In accordance with 6.108 of IEC 62271-100:2008, circuit-breakers applied in non-effectively earthed neutral systems shall be capable of clearing the short-circuit currents that may occur in the case of double earth faults i.e. earth faults on two different phases, one of which occurs on one side of the circuit-breaker and the other one on the other side.

Such a situation can occur if, after a single phase-to-earth fault, the two other phases stay energized long enough to allow another fault to earth to develop on another phase. This situation is unlikely to happen if the healthy phases are opened in a relatively short time after the occurrence of the initial fault. However, it may be provoked by the voltage elevation on healthy phases that is produced by the first fault to earth.

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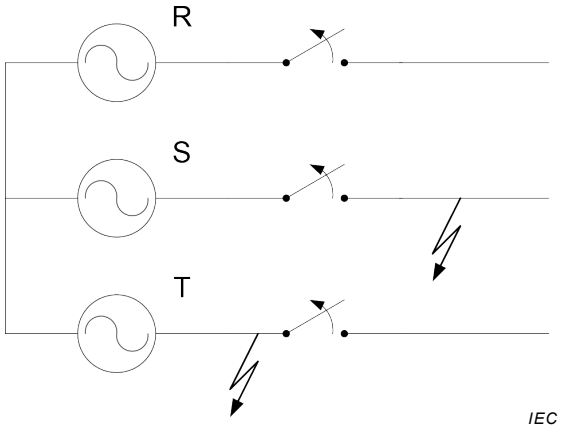

Figure 141 – Representation of a system with a double earth fault

Figure 141 illustrates the case where a fault is present in phase S. Due to the voltage increase on the healthy phases a fault develops on the other side of the circuit-breaker in phase T. The total fault current needs to be interrupted by pole S.

From Figure 141, it can be seen that one pole of the circuit-breaker is required to interrupt a short-circuit under phase-to-phase voltage. As the recovery voltage is higher than in other terminal fault test duties, this breaking condition could be more severe than a terminal fault T100 condition, but, as explained in 13.5.4, the short-circuit current is only 87 % of the rated short-circuit current.

This condition is not covered by test duty T100 and, since it has a low probability of occurrence, IEC 62271-100 requires only one breaking test to be performed. When this standard was established, it was considered that it is only necessary to test with the most severe condition of arcing time, i.e. with a long arcing time corresponding to a high energy content of the arc and with a moving contact position close to the fully open position.

13.5.2 Short-circuit current

The calculation of the short-circuit current is detailed in 13.5.4.

A symmetrical current is specified in testing, as in test duty T100s, because a symmetrical condition leads to the highest TRV peak possible when compared to the value specified for test duty T100.

13.5.3 TRV

The RRRV is the same as for terminal fault test duty T100s. The voltage factor for the double earth fault is $\sqrt{3}$, since the full phase-to-phase voltage is applied to one pole, whereas it is 1,5 for terminal fault. The di/dt is obtained by multiplying the di/dt value of T100s by $\frac{\sqrt{3}}{2}$. It follows that the rate of rise of recovery voltage is equal to the values of T100s multiplied by $\frac{\sqrt{3}}{1,5} \times \frac{\sqrt{3}}{2} = 1$

Specified TRVs with two parameters and four-parameters are determined from the RRRV and a pole-to-clear factor of $\sqrt{3}$. They are given in Table 28 of IEC 62271-100:2008.

In the case of a two-parameter TRV, t_3 is derived from u_c and the RRRV.

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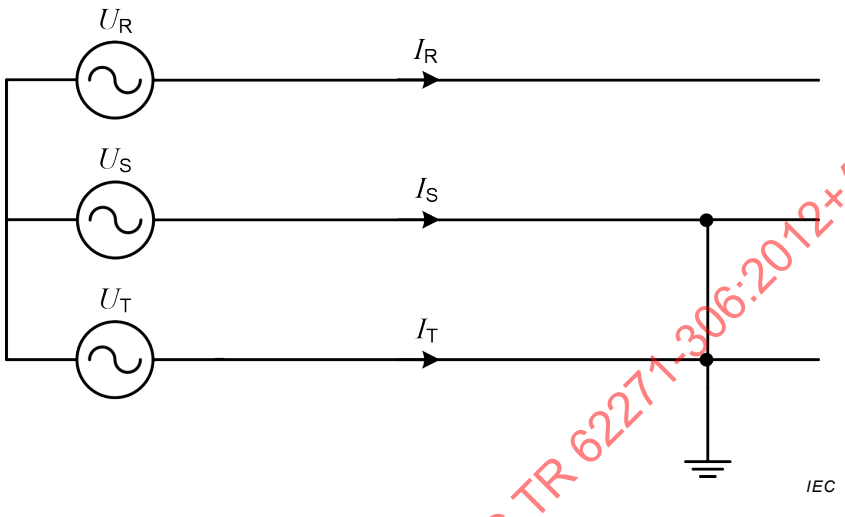
In the case of a four-parameter TRV, u_1 and u_c are calculated on the basis of a pole-to-clear factor of $\sqrt{3}$, t_1 is derived from u_1 and the RRRV and $t_2 = 4 \times t_1$.

13.5.4 Determination of the short-circuit current in the case of a double-earth fault

Figure 142 shows a schematic representation of the fault case illustrated in Figure 141.

Phase supply voltage is U.



Key

U_R, U_S, U_T	Voltages in R, S and T-phase, respectively
I_R, I_S, I_T	Currents in R, S and T-phase, respectively

Figure 142 – Representation of circuit with double-earth fault

The circuit in Figure 142 is analysed using symmetrical components. The indices used are 0 for zero sequence component, 1 for the positive sequence component and 2 for the negative sequence component.

$I_R = 0 \rightarrow \quad I_0 + I_1 + I_2 = 0$

$U_S = 0 \rightarrow \quad U_0 + a^2 U_1 + a U_2 = 0$

$U_T = 0 \rightarrow \quad U_0 + a U_1 + a^2 U_2 = 0$

with

$a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

$$U_1 = U - X_1 I_1 \tag{178}$$

$$U_2 = -X_2 I_2 \tag{179}$$

$$U_0 = -X_0 I_0 \tag{180}$$

this gives:

$-X_0 I_0 + a^2 (U - X_1 I_1) - a X_2 I_2 = 0$

$-X_0 I_0 + a (U - X_1 I_1) - a^2 X_2 I_2 = 0$

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$I_1 + I_2 + I_0 = 0$

or,

$$a^2 X_1 I_1 + a X_2 I_2 + X_0 I_0 = a^2 U \quad (181)$$

$$a X_1 I_1 + a^2 X_2 I_2 + X_0 I_0 = a U \quad (182)$$

$$I_1 + I_2 + I_0 = 0 \quad (183)$$

Multiplying Equation (182) with "a" and subtracting Equation (181) leads to:

$$(1 - a) X_2 I_2 + (a - 1) X_0 I_0 = 0 \Rightarrow X_2 I_2 = X_0 I_0 \quad (184)$$

Multiplying Equation (181) with "a" and subtracting Equation (180) leads to:

$$X_1 I_1 (1\text{-}a) + (a\text{-}1) X_0 I_0 = (1\text{-}a) U \rightarrow X_1 I_1 - X_0 I_0 = U \quad (185)$$

A system of 3 equations with 3 unknown is obtained:

$$I_1 + I_2 + I_0 = 0 \quad (186)$$

$$X_2 I_2 = X_0 I_0 \quad (187)$$

$$X_1 I_1 - X_0 I_0 = U \quad (188)$$

Resolution of Equations (186), (187) and (188):

$$I_1 + \frac{X_0 I_0}{X_2} + I_0 = 0$$

$$I_0 \times \frac{X_2 + X_0}{X_2} = -I_1 \quad I_0 = -\frac{I_1 X_2}{X_2 + X_0}$$

$$X_1 I_1 + \frac{X_0 X_2}{X_2 + X_0} \times I_1 = U \text{ , or } I_1 \left(X_1 + \frac{X_0 X_2}{X_2 + X_0} \right) = U \Rightarrow I_1 = \frac{U}{X_1 + \frac{X_0 X_2}{X_2 + X_0}} \quad (189)$$

and

$$I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad (190)$$

$$I_2 = -I_1 - I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad (191)$$

The current in phase S is given by:

$I_S = I_0 + a^2 I_1 + a I_2$ with $a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

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From Equations (190) and (191), and with the standard hypothesis $X_2 = X_1$:

$$I_S = -\frac{X_1 I_1}{X_1 + X_0} + a^2 I_1 - a\frac{X_0 I_1}{X_1 + X_0}$$

$$\frac{I_S}{I_1} = \frac{-X_1 + a^2 X_1 + a^2 X_0 - aX_0}{X_1 + X_0} = \frac{-X_1\left(3/2 + j\frac{\sqrt{3}}{2}\right) - jX_0\sqrt{3}}{X_1 + X_0}$$

Using the equation for I_1 given in Equation (188), the current for the double earth fault (I_{def}) is then:

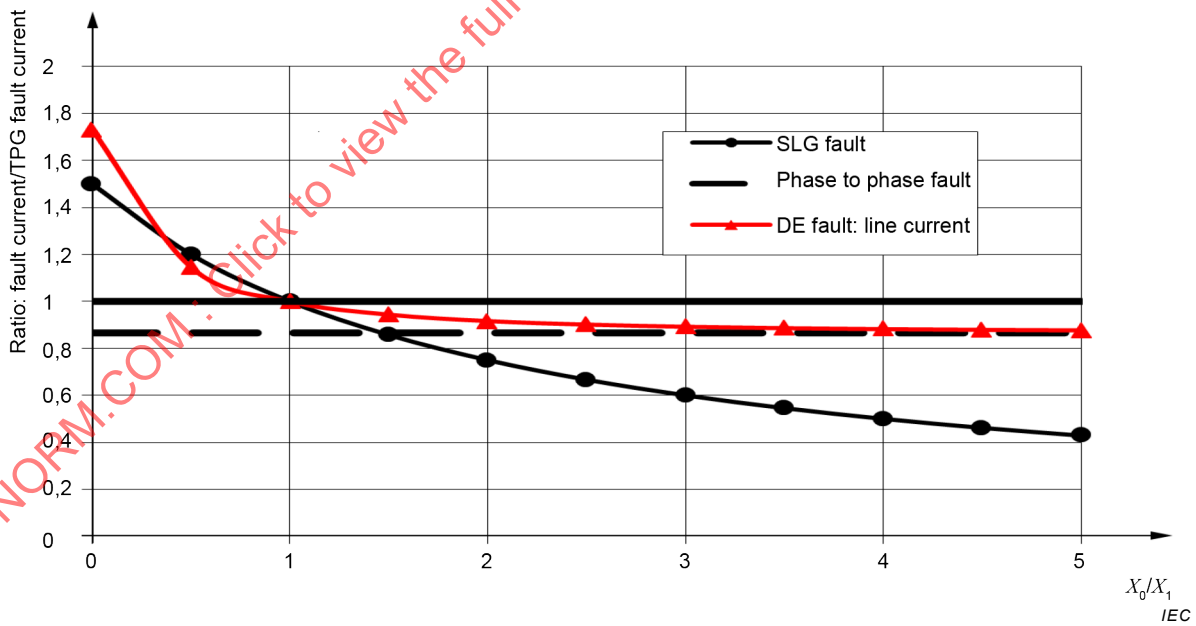
$$I_{def} = I_S = \frac{-U\sqrt{3}}{X_1 + 2X_0}\left(\frac{\sqrt{3}}{2} + \frac{j}{2} + j\frac{X_0}{X_1}\right)$$

For non-effectively earthed networks $X_0 >> X_1$, which gives:

$$I_{def} = -\frac{U\sqrt{3}}{X_1 + 2X_0} \times j\frac{X_0}{X_1} = -j\frac{U\sqrt{3}}{2X_1}$$

The three-phase short-circuit is given by $I_{sc} = U/X_1 \rightarrow I_{def} = -j\frac{\sqrt{3}}{2} I_{sc}$, or $|I_{def}| = 0{,}87|I_{sc}|$.

Fault currents relative to the three-phase short-circuit current are shown in Figure 143 for this case and for other fault cases.



Key

SLG fault	Single-line to earth fault	TPG fault	Three-phase to earth fault
DE fault	Double earth fault	Solid line	Three-phase to earth current

Figure 143 – Fault currents relative to the three-phase short-circuit current

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13.6 Break time

The break time of a circuit-breaker is the maximum interval between the instant of initialization of the opening operation (i.e. energizing of the trip circuit) and the instant of interruption of the current in all three phases during terminal fault test-duties T30, T60 and T100s under the following conditions:

– rated auxiliary supply voltage and frequency;

– rated pressures for operation, insulation and interruption;

– an ambient air temperature of (20 ± 5) °C.

The break time is defined based on the minimum arcing time because the longest recorded arcing time during the tests can be longer than under the actual field condition.

Terminal fault tests are carried out at the minimum auxiliary supply voltage and/or pressures for operation and/or interruption. For convenience of testing, the auxiliary supply voltage may be the rated or maximum value as long as it does not affect the making or breaking capability. (The operating times of some circuit-breakers may vary with the auxiliary supply voltage). In order to verify the break time during these test-duties, the maximum break time should be amended to take account of the lower auxiliary supply voltage and pressures as follows:

$$t_{\text{bmax}} = t_{\text{or}} + t_{\text{am}} + t_{\text{w}} - \frac{18^{\text{o}}}{360^{\text{o}}} \times T$$

where

t_{bmax} is the maximum determined break time;

t_{or} is the opening time under rated conditions (recorded during no-load operation at rated supply voltage and frequency of closing and opening devices and of auxiliary circuits, at rated pressure for operation and at a ambient temperature of 20 °C ± 5 °C)

t_{am} is the longest of the recorded minimum arcing times during test-duties T30, T60 and T100s;

$\frac{18^{\text{o}}}{360^{\text{o}}} \times T$ takes the uncertainty in the determination of the minimum arcing time into account;

T is one period of power frequency (20 ms for 50 Hz, 16,7 ms for 60 Hz) and t_{w} is the necessary interrupting window expressed in ms:

– for single-phase tests in substitution for three-phase conditions
  - non-effectively earthed neutral systems: $t_{\text{we}} = 150 - \text{d}\alpha$
  - effectively earthed neutral systems: $t_{\text{we}} = 180 - \text{d}\alpha$

– for three-phase tests

  $t_{\text{we}} = 60 - \text{d}\alpha$

  t_{we} is expressed in electrical degrees

$$t_{\text{w}} = \frac{t_{\text{we}}}{360^{\text{o}}} \times T$$

$\text{d}\alpha$ is the tripping impulse step in the search for the minimum arcing time, it is equal to 18 electrical degrees.

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If the maximum break time determined according to this procedure exceeds the break time, the test-duty that has given the longest break time may be repeated with auxiliary supply voltage and pressure for operation and interruption at their rated values.

NOTE The break time during a make-break operation may be longer than that of a single break operation for some circuit-breaker designs. Such longer break times may impact system protection strategy and stability if the delay is longer than the relay time. Users should advise the manufacturer of the maximum allowable break time during make-break operations.

14 Synthetic making and breaking tests

14.1 General

With the increasing voltage and current ratings of circuit-breakers, the total available short-circuit power of a high power laboratory has to be increased accordingly. The investments required to increase the short-circuit power are very high. In order to still be able to perform the correct type tests on circuit-breakers with the available short-circuit power, synthetic tests are performed.

Requirements for synthetic testing and examples of synthetic circuits are given in IEC 62271-101.

Generally a synthetic test circuit consists of separate current and voltage circuits (see Figure 144). During the high-current interval, the short-circuit current will be fed from a current circuit (source providing the necessary current at a reduced voltage). This reduced voltage should have an amplitude of sufficient magnitude to prevent the arc voltage from distorting the short-circuit current in such a way that the circuit-breaker is not stressed in the same way as under system conditions. For tests that need less power (e.g. capacitive current switching tests), some synthetic test circuits using a single source can also be used.

When the current is interrupted by the circuit-breaker under test (TB in Figure 144), the voltage circuit will give the correct voltage stresses across the contact gap. An auxiliary circuit-breaker (AB in Figure 144) is used to separate the voltage circuit from the current circuit, thus avoiding that the high-voltage from the voltage circuit stresses the current circuit.

The principle used for the making operation is similar. The voltage circuit first provides the correct voltage stress during the closing operation and as soon as the pre-arcing occurs, the current circuit will then provide the correct short-circuit current.

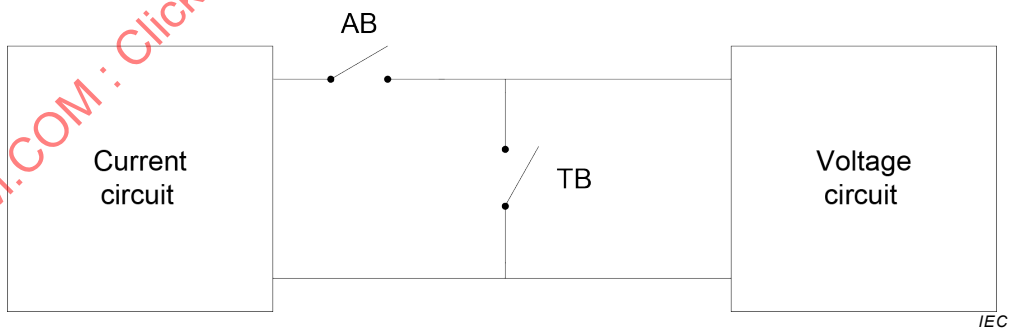

Figure 144 – Principle of synthetic testing

In order for a synthetic test to be valid, the following requirements should be met:

– the arc energy in the contact gap should be equal to that of a direct test;
– the di/dt at current zero should be in accordance with the current and frequency specified;
– the recovery voltage should appear immediately after current zero i.e. without delay;
– the prospective TRV should be at least equal to the required TRV;

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– the voltage source should have a sufficient power to avoid excess damping of the transient process by the post arc current.

Synthetic testing allows in general testing at one particular arcing time per operation. In order to cover the full extinguishing window, it may be necessary to use re-ignition circuits.

14.2 Current injection methods

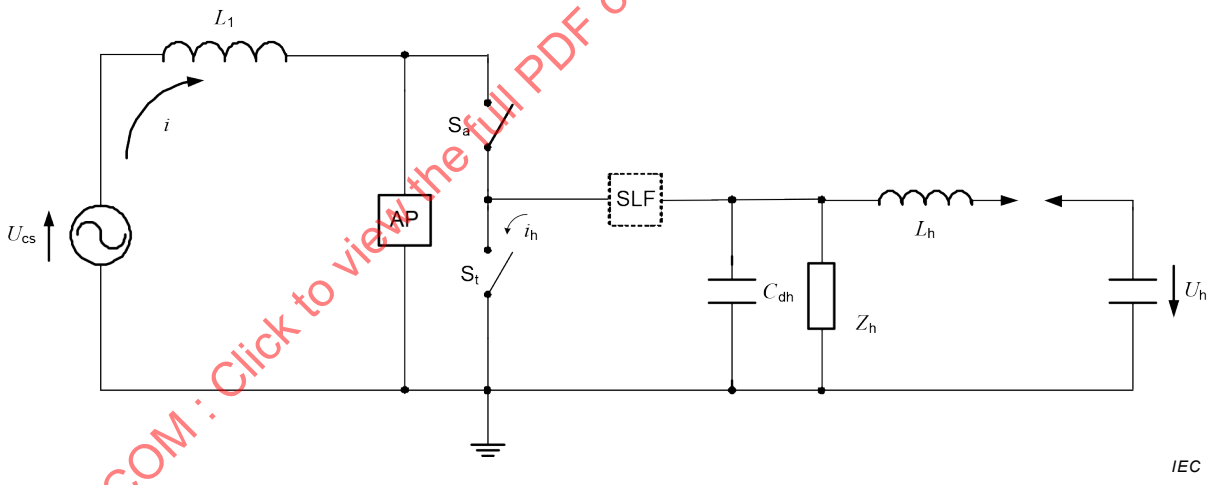
14.2.1 General

In a synthetic test circuit using current injection, the superposition of the currents takes place shortly before the zero of the power-frequency short-circuit current. A current of smaller amplitude but higher frequency, derived from the voltage circuit, is superimposed either in the test circuit-breaker or in the auxiliary circuit-breaker. The instant of switching in this injected current is selected by means of a current-dependent control circuit. This instant should be such that the character of the resulting current wave in the test circuit-breaker corresponds to that of the specified breaking current prior to the current zero during the interval of significant change of arc voltage.

In this way, the circuit-breaker under test is automatically connected into the voltage circuit after the interruption of the current in the auxiliary circuit-breaker, so there will be no delay between the current stress and the application of the voltage stress.

14.2.2 Current injection circuit with the voltage circuit in parallel with the test circuit-breaker (parallel circuit)

Figure 145 shows the simplified circuit diagram of a current injection circuit with the voltage circuit connected in parallel with the test circuit-breaker.



Key

U_{cs}	voltage of current circuit	C_{dh}	capacitance for time delay of voltage circuit
L_1	inductance of current circuit	L_h	inductance of voltage circuit
AP	arc prolonging circuit	U_h	charging voltage of voltage circuit
S_a	auxiliary circuit-breaker	i	current of the current circuit
S_t	test circuit-breaker	i_h	injected current
Z_h	equivalent surge impedance of voltage circuit	SLF	short-line-fault circuit (for the corresponding tests)

Figure 145 – Typical current injection circuit with voltage circuit in parallel with the test circuit-breaker

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