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TECHNICAL REPORT

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Semiconductor devices – Standardization roadmap of fault test method for automotive vehicles

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CONTENTS

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SEMICONDUCTOR DEVICES – STANDARDIZATION ROADMAP OF FAULT TEST METHOD FOR AUTOMOTIVE VEHICLES

FOREWORD

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The text of this Technical Report is based on the following documents:

Draft	Report on voting
47/2677/DTR	47/2714/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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- withdrawn,
- replaced by a revised edition, or
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SEMICONDUCTOR DEVICES – STANDARDIZATION ROADMAP OF FAULT TEST METHOD FOR AUTOMOTIVE VEHICLES

1 Scope

This Technical Report describes standardization roadmap of fault test methods for integrated circuits used in automotive vehicles. Since automotive vehicles are exposed in harsh environment such as very low or high temperature, vibration, high frequency signals, etc. Therefore, they are tested for possible faults which can be caused by harsh environment. There are several fault test methods and related issues to be standardized.

Semiconductor devices used in automotive vehicles are exposed in harsh environment of very high or very low temperature, vibration, high frequency signals, etc. Therefore, they are tested for possible faults which can be caused by harsh environment Evaluation results following this fault test methods will provide robustness of the semiconductor device.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60050-192*, International Electrotechnical Vocabulary (IEV) – Part 192: Dependability*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60050-192 apply, as well as the following.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
automatic test pattern generation
ATPG
method/technology used to find an input (or test) sequence that, when applied to a digital circuit, enables automatic test equipment to distinguish between the correct circuit behavior and the faulty circuit behavior caused by defects

Note 1 to entry: The generated patterns are used to test semiconductor devices after manufacture, or to assist with determining the cause of failure. The effectiveness of ATPG is measured by the number of modeled defects, or fault models, detectable and by the number of generated patterns. These metrics generally indicate test quality (higher with more fault detections) and test application time (higher with more patterns).

3.2
error
discrepancy between an observed or measured value or condition, and the true, specified or theoretically correct value or condition

[IEC 60050-192:2015, 192-03-02, modified – The words "a computed, observed or measured" have been replaced by "an observed or measured" and the notes to entry have been removed.]

3.3
failure
loss of ability to perform as required

[IEC 60050-192:2015, 192-03-01, modified – The specific use <of an item> as well as the three existing notes have been removed.]

3.4
fault
inability to perform as required, due to an internal state

[IEC 60050-192:2015, 192-04-01, modified – The specific use <of an item> has been deleted, as well as the four existing notes.]

3.5
fault coverage
proportion of faults that can be detected, under given conditions

[IEC 60050-192:2015, 192-07-24]

3.6
fault detection
event by which the presence of a fault becomes apparent

[IEC 60050-192:2015, 192-06-18, modified – The note has been removed.]

3.7
fault model
definition of a possible fault type which gives incorrect values at any speed or at-speed, and sensitized by performing only one operation or multiple operations sequentially

3.8
fault simulation
simulation of DUT in the presence of faults to evaluate the quality of a test set, usually in terms of fault coverage

3.9
permanent fault
fault that will remain unless it is removed by some intervention

Note 1 to entry: The "intervention" may be modification or maintenance.

[IEC 60050-192:2015, 192-04-04, modified – The specific use <of an item> and the second preferred term "persistent fault" have been removed.]

3.10
scan test
functional test in which test data are first entered via a scan chain, the appropriate functions are then performed, and finally the test results are extracted via the scan chain

3.11
scan chain
group of scan cells that can be connected when required as a shift register for entry of test input data or extraction of test results data

3.12
scan cell
1-bit storage unit that would normally function as part of the DUT, that can be set instead to hold input data prior to a test or hold data resulting from a test

Note 1 to entry: Scan cells are placed at strategic points in the DUT that break up its overall function into smaller segments that can be tested independently for success or failure. Thereby a complex arrangement of logic can be tested more easily than it can as a whole.

Note 2 to entry: A scan cell need not be a functioning part of the DUT.

3.13
test coverage
proportion of tests that can be performed by a set of tests relative to the number of tests that are needed to verify all the intended functions or only a subset of them

3.14
transient fault
fault that disappears without intervention

[IEC 60050-192:2015, 192-04-05, modified – The specific use <of an item>, the deprecated term "volatile fault" as well as the notes have been removed.]

4 Background

4.1 Motivation

Semiconductor devices in automotive vehicles are exposed to harsh environments such as vibration, dust, high and low temperature, and high-frequency signals as shown in Figure 1.

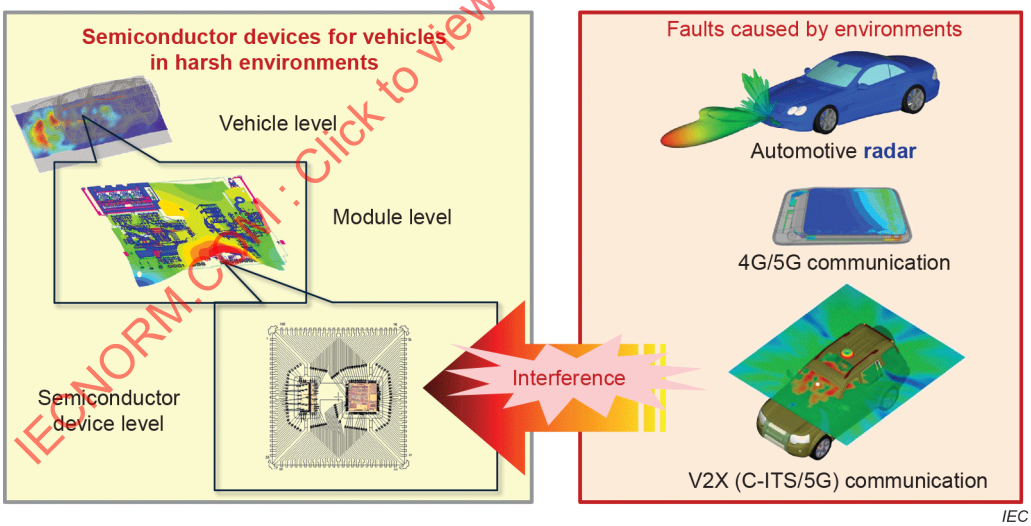

Figure 1 – Conceptual diagram of environment for semiconductor devices used in automotive vehicles

High-frequency signals include automotive RADAR from other vehicles, RF signals from mobile phones and stations, and V2X communications.

According to regulations on automotive RADAR, frequency bands are 24 GHz and 77 GHz to approximately 81 GHz as shown in Figure 2. And frequency band from 77 GHz to 81 GHz is promising since it provides wide bandwidth of 4 GHz.

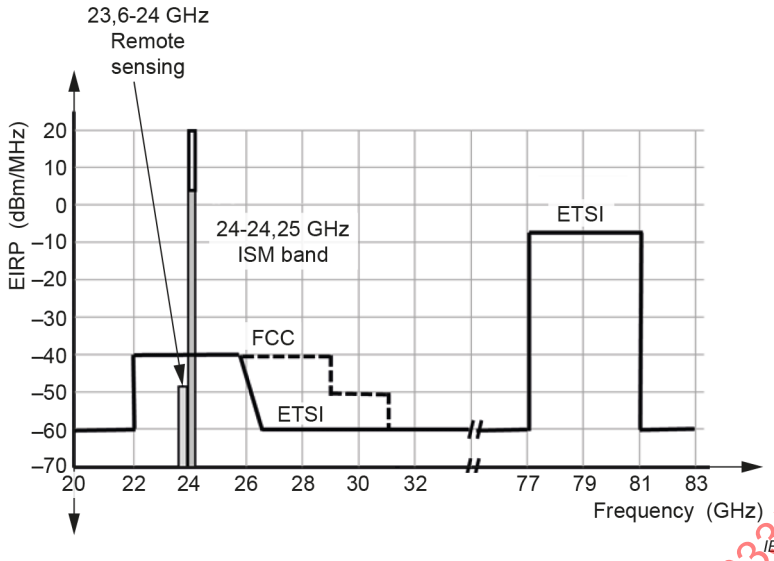

Figure 2 – Regulations on automotive RADAR

Frequency ranges of wireless communications are, 26 GHz to 28 GHz, 38 GHz to 42 GHz, and up to 100 GHz after 2020 as show in Figure 3.

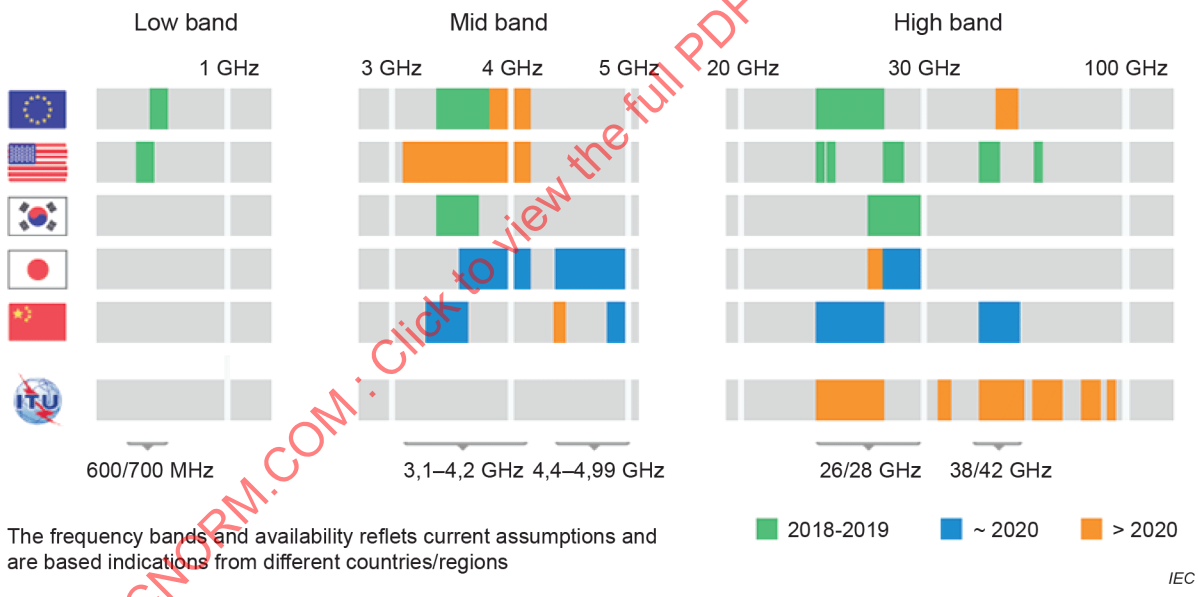

Figure 3 – Frequency bands for wireless communications

Frequency ranges of V2X communications used in Intelligent Transport Systems are 5,9 GHz (ECC) and 3,4 GHz to 3,8 GHz as show in Table 1.

Table 1 – Standards of frequency band used for V2X

Parameter	ETSI	IEEE	ARIB	TTA
Operating frequency range	5,855 MHz to 5,925 MHz	5,850 MHz to 5,925 MHz	755,5 MHz to 764,5 MHz	5,855 MHz to 5,925 MHz
RF channel bandwidth	10 MHz	10 MHz or 20 MHz	Less than 9 MHz	Less than 10 MHz
RF Transmit Power/EIRP	Max 33 dBm EIRP			23 dBm
RF transmit power density			10 dBm/MHz	

4.2 Technologies on fault test methods

4.2.1 Joint test action group (JTAG)

JTAG is an integrated method for testing interconnects on printed circuit boards (PCBs) that are implemented at the integrated circuit (IC) level introduced as an industry standard in 1990. It has continuously grown in adoption, popularity, and usefulness even today, new revisions and supplements to the IEEE 1149.1 standard are being developed and implemented.

4.2.2 Design for test (DFT)

Design for testing or design for testability (DFT) consists of IC design techniques that add testability features to a hardware product design. The added features make it easier to develop and apply manufacturing tests to the designed hardware. The purpose of manufacturing tests is to validate that the product hardware contains no manufacturing defects that could adversely affect the product's correct functioning.

Tests applied at several steps in the hardware manufacturing flow and, for certain products, should be used for hardware maintenance in the customer's environment. The tests are generally driven by test programs that execute using automatic test equipment (ATE) or, in the case of system maintenance, inside the assembled system itself. In addition to finding and indicating the presence of defects (i.e., the test fails), tests should be able to log diagnostic information about the nature of the encountered test fails. The diagnostic information can be used to locate the source of the failure.

In other words, the response of vectors (patterns) from a good circuit is compared with the response of vectors (using the same patterns) from a DUT (device under test). If the response is the same or matches, the circuit is good. Otherwise, the circuit is not manufactured as it was intended.

DFT plays an important role in the development of test programs and as an interface for test application and diagnostics. Automatic test pattern generation, or ATPG, is much easier if appropriate DFT rules and suggestions have been implemented.

4.2.3 Design for manufacturability (DFM)

Design for manufacturability (also sometimes known as design for manufacturing or DFM) is the general engineering practice of designing products in such a way that they are easy to manufacture. The concept exists in almost all engineering disciplines, but the implementation differs widely depending on the manufacturing technology. DFM describes the process of designing or engineering a product in order to facilitate the manufacturing process in order to reduce its manufacturing costs. DFM will allow potential problems to be fixed in the design phase which is the least expensive place to address them. Other factors may affect the manufacturability such as the type of raw material, the form of the raw material, dimensional tolerances, and secondary processing such as finishing.

Depending on various types of manufacturing processes, there are set guidelines for DFM practices. These DFM guidelines help to precisely define various tolerances, rules and common manufacturing checks related to DFM.

While DFM is applicable to the design process, a similar concept called DFSS (Design for Six Sigma) is also practiced in many organizations.

4.2.4 Scan test

4.2.4.1 General

As semiconductor devices become more complex, it took increasing amounts of time and effort to manually create and validate tests, it was too hard to determine the test coverage, and the tests took too long to run. The technique is referred to as a functional test. So, the industry moved to a design for test (DFT) approach where the design was modified to make it easier to test. The approach that ended up dominating IC test is called structural, or "scan" test because it involves scanning test patterns into internal circuits within the device under test (DUT). Scan cells should be added to the design to ensure that each segment starts and ends with one as shown in Figure 4.

The modified scan cells allow the overall design to be viewed as many small segments of combinational logic that can be more easily tested. For a design with a million flops, introducing scan cells is like adding a million control and observation points. Segmenting the logic in this manner is what makes it feasible to automatically generate test patterns that can exercise the logic between the flops. The test software doesn't need to understand the function of the logic, it just tries to exercise the logic segments observed by a scan cell. Since scan test modifies flip-flops that are already in the design to enable them to also act as scan cells, the impact of the test circuitry is relatively small, typically adding about only 1 % to 5 % to the total gate count.

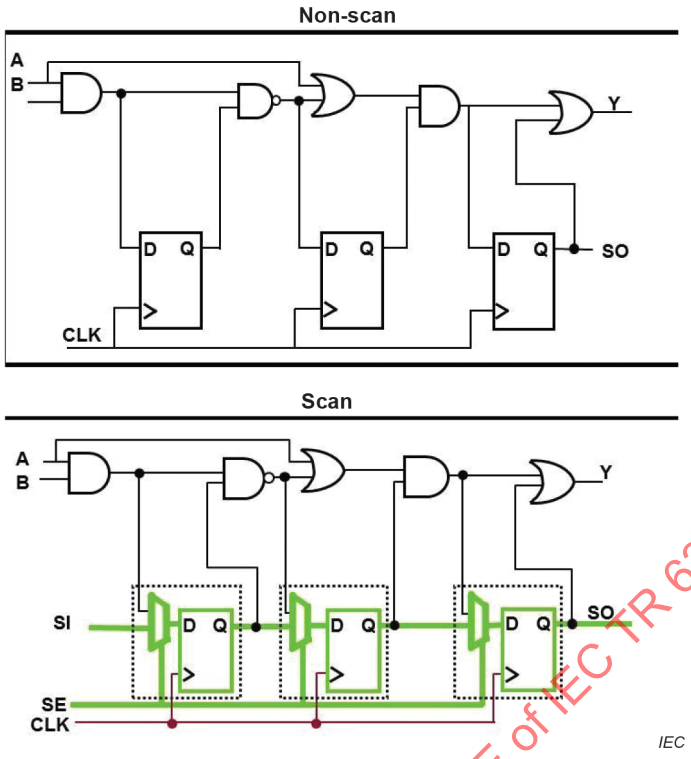

Figure 4 – Non-scan and scan cells

The scan cells are linked together into "scan chains" that operate like big shift registers when the circuit is put into test mode. The scan chains are used by external automatic test equipment (ATE) to deliver test pattern data from its memory into the device. After the test pattern is loaded, the design is placed back into functional mode and the test response is captured in one or more clock cycles. The design is again put in test mode and the captured test response is shifted out, while the next test pattern is simultaneously shifted into the scan cells. The ATE then compares the captured test response with the expected response data stored in its memory. Any mismatches are likely defects and are logged for further evaluation.

Many designs do not connect up every register into a scan chain. This is called partial scan.

To enable automatic test pattern generation (ATPG) software to create the test patterns, fault models are defined that predict the expected behaviours (response) from the IC when defects are present. The ATPG tool then uses the fault models to determine the patterns required to detect those faults at all points in the circuit (or almost all-coverage of 95 % or more is typical). There are a number of different fault models that are commonly used.

4.2.4.2 Stuck-at test

The most basic and common is the "stuck-at" fault model, which checks each node location in the design for either stuck-at-1 or stuck-at-0 logic behaviour. For example, if a NAND gate in the design had an input pin shorted to ground (logic value 0) by a defect, the stuck-at-0 test for that node would catch it. The stuck-at model can also detect other defect types like bridges between two nets or nodes. The stuck-at model is classified as a static model because it is a slow speed test and is not dependent on gate timing (rise and fall times and propagation delay).

4.2.4.3 At-speed test

A second common type of fault model is called the "transition" or "at-speed" fault model, and is a dynamic fault model, i.e., it detects problems with timing. It is similar to the stuck-at model in that there are two faults for every node location in the design, classified as slow-to-rise and slow-to-fall faults. The transition fault model uses a test pattern that creates a transition stimulus to change the logic value from either 0-to-1 or from 1-to-0. The time allowed for the transition is specified, so if the transition doesn't happen, or happens outside the allotted time, a timing defect is presumed.

4.2.4.4 Path delay test

The "path delay" model is also dynamic and performs at-speed tests on targeted timing critical paths. While stuck-at and transition fault models usually address all the nodes in the design, the path delay model only tests the exact paths specified by the engineer, who runs a static timing analysis to determine which are the most critical paths. These paths are specified to the ATPG tool for creating the path delay test patterns. The theory is that if the most critical timing paths can pass the tests, then all the other paths with longer slack times should have no timing problems. In a way, path delay testing is a form of process check (e.g., showing timing errors if a process variable strays too far), in addition to a test for manufacturing defects on individual devices.

4.2.4.5 IDDQ test

The IDDQ test relies on measuring the supply current (Idd) in the quiescent state (when the circuit is not switching, and inputs are held at static values). Test patterns are used to place the DUT in a variety of selected states. By performing current measurements at each of these static states, the presence of defects that draw excess current can be detected. The value of Iddq testing is that many types of faults can be detected with very few patterns. The drawback is the additional test time to perform the current measurements.

4.2.4.6 Measuring fault coverage

Some of the methods can distinguish between transient and permanent faults. Most of the methods handle faults occurring within logic resources. None of the methods handles faults occurring within I/O blocks. Faults occurring within interconnect resources are important. Since the interconnect resources can compose up to 80 % of the DUT area, the probability of a fault occurring within interconnect is higher than that of an occurrence within logic area.

5 Standardization roadmap of fault test methods for automotive vehicles

Based on the techniques described in Clause 4, the following roadmap as shown in Table 2 is proposed to be standardized by TC 47.