TECHNICAL SPECIFICATION

IEC TS 60071-5

First edition
2002-06

Insulation co-ordination –

Part 5: Procedures for high-voltage direct current (HVDC) converter stations

Coordination de l'isolement -

Partie 5:

Procédures pour les stations de conversion CCHT

Reference number
IEC/TS 60071-5:2002(E)

Publication numbering

As from 1 January 1997 all IEC publications are issued with a designation in the 60000 series. For example, IEC 34-1 is now referred to as IEC 60034-1.

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International Electrotechnical Commission
Международная Электротехническая Комиссия

PRICE CODE W

For price, see current catalogue

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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FOREWORD

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 60071-5, which is a technical specification, has been prepared by IEC technical committee 28: Insulation co-ordination.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
28/139/CDV	28/144A/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

This technical specification is published in English only.

Annexes A, B and C are for information only.

The committee has decided that the contents of this publication will remain unchanged until 2008. At this date, the publication will be

- transformed into an International standard
- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INSULATION CO-ORDINATION –

Part 5: Procedures for high-voltage direct current (HVDC) converter stations

1 General

1.1 Scope

This part of IEC 60071 provides guidance on the procedures for insulation co-ordination of high-voltage direct current (HVDC) converter stations, without prescribing standardized insulation levels.

The guide applies only for HVDC applications in high-voltage a.c. power systems and not for industrial conversion equipment. Principles and guidance given are for insulation co-ordination purposes only. The requirements for human safety are not covered by this application guide.

1.2 Additional background

The use of power electronic thyristor valves in a series and/or parallel arrangement, along with the unique control and protection strategies employed in the conversion process, has ramifications requiring particular consideration of overvoltage protection of equipment in converter stations compared with substations in a.c. systems. This guide outlines the procedures for evaluating the overvoltage stresses on the converter station equipment subjected to combined d.c., a.c. power frequency, harmonic and impulse voltages. The criteria for determining the protective levels of series- and/or parallel combinations of surge arresters used to ensure optimal protection is also presented.

The basic principles and design objectives of insulation co-ordination of converter stations, in so far as they differ from normal a.c. system practice, are described.

Concerning surge arrester protection, this guide deals only with metal-oxide surge arresters, without gaps, which are used in modern HVDC converter stations. The basic arrester characteristics, requirements for these arresters and the process of evaluating the maximum overvoltages to which they may be exposed in service, are presented. Typical arrester protection schemes and stresses of arresters are presented, along with methods to be applied for determining these stresses.

This guide includes insulation co-ordination of equipment connected between the converter a.c. bus (including the a.c. harmonic filters, the converter transformer, the circuit breakers) and the d.c. line side of the smoothing reactor. The line and cable terminations in so far as they influence the insulation co-ordination of converter station equipment are also covered.

Although the main focus of the guide is on conventional HVDC systems where the commutation voltage bus is at the a.c. filter bus, outlines of insulation co-ordination for the capacitor commutated converter (CCC) as well as the controlled series compensated converter (CSCC) and some other special converter configurations are covered in the annexes.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60060-1:1989, *High-voltage test techniques – Part 1: General definitions and test requirements*

IEC 60071-1:1993, *Insulation co-ordination – Part 1: Definitions, principles and rules*

IEC 60071-2:1996, *Insulation co-ordination – Part 2: Application guide*

IEC 60099-4:1991, *Surge arresters – Part 4: Metal-oxide surge arresters without gaps for a.c. systems*

IEC 60633:1998, *Terminology for high-voltage direct current (HVDC) transmission*

IEC 60700-1:1998,*Thyristor valves for high-voltage direct current (HVDC) power transmission – Part 1: Electrical testing*

IEC 60815:1986, *Guide for the selection of insulators in respect of polluted conditions*

3 Definitions

For the purposes of this part of IEC 60071, the following terms and definitions apply.

Many of the following definitions refer to actual insulation co-ordination concepts, or to actual arrester parameters. For more information on these, please refer to IEC 60071-1 or to IEC 60099-4, respectively.

3.1
d.c. system voltage
highest mean or average operating voltage to earth, excluding harmonics and commutation overshoots (IEC 123 pollution test of HVDC insulator)

3.2
peak value of continuous operating voltage (PCOV)
highest continuously occurring crest value of the voltage at the equipment on the d.c. side of the converter station including commutation overshoots and commutation notches (see figure 6)

3.3
crest value of continuous operating voltage (CCOV)
highest continuously occurring crest value of the voltage at the equipment on the d.c. side of the converter station excluding commutation overshoots (see figure 6)

3.4
overvoltage
voltage between one phase conductor and earth or between phase conductors having a peak value exceeding the corresponding peak of the highest voltage of the system on the a.c. side and the PCOV on the d.c. side of the HVDC converter station

3.4.1
temporary overvoltage (TOV)
power frequency overvoltage of relatively long duration (IEC 60071-1)

NOTE The overvoltage may be undamped or weakly damped. In some cases its frequency may be several times smaller or higher than power frequency.

3.4.2
slow-front overvoltage
transient overvoltage, usually unidirectional, with time to peak 20 µs < Tp < 5 000 µs, and tail duration T2 < 50 ms (IEC 60071-1)

NOTE For the purpose of insulation co-ordination, slow-front overvoltages are classified according to their shape, regardless of their origin. Although considerable deviations from the standard shapes occur on actual systems, in this standard it is considered sufficient in most cases to describe such overvoltages by their classification and peak value.

3.4.3
fast-front overvoltage
overvoltage at a given location on a system, due to a lightning discharge or other cause, the shape of which can be regarded, for insulation co-ordination purposes, as similar to that of the standard impulse (IEC 60060-1) used for lightning impulse tests.

Transient overvoltage, usually unidirectional, with time to peak 0,1 µs < T1 < 20 µs, and tail duration T2 < 300 µs (IEC 60071-1).

NOTE For the purpose of insulation co-ordination, slow-front and fast-front overvoltages are classified according to their shape, regardless of their origin. Although considerable deviations from the standard shapes occur on actual systems, in this standard it is considered sufficient in most cases to describe such overvoltages by their classification and peak value.

3.4.4
very fast-front overvoltage
transient overvoltage, usually unidirectional, with time to peak T_f < 0,1 µs, total duration < 3 ms, and with superimposed oscillations at frequency 30 kHz < f < 100 MHz (IEC 60071-1)

3.4.5
steep-front overvoltage
transient overvoltage classified as a kind of fast-front overvoltage with time to peak 3 ns < T1 < 1,2 µs). A steep-front impulse voltage for test purposes is defined in figure 1 of IEC 60700-1

NOTE The front time is decided by means of system studies.

3.4.6
combined overvoltage (temporary, slow-front, fast-front, very fast-front)
overvoltage consisting of two voltage components simultaneously applied between each of the two phase terminals of a phase-to-phase (or longitudinal) insulation and earth. It is classified by the component of higher peak value

3.5
representative overvoltages
overvoltages assumed to produce the same dielectric effect on the insulation as overvoltages of a given class occurring in service due to various origins (IEC 60071-1)

NOTE In this specification it is generally assumed that the representative overvoltages are characterized by their assumed or obtained maximum values.

3.5.1
representative slow-front overvoltage (RSLO)
voltage value between terminals of an equipment having the shape of a standard switching impulse

3.5.2
representative fast-front overvoltage (RFAO)
voltage value between terminals of an equipment having the shape of a standard lightning impulse

3.5.3
representative steep-front overvoltage (RSTO)
voltage value with a standard shape having a time to crest less than that of a standard lightning impulse, but not less than that of a very-fast-front overvoltage as defined by IEC 60071-1

NOTE A steep-front impulse voltage for test purposes is defined in figure 1 of IEC 60700-1. The front time is decided by means of system studies.

3.6
continuous operating voltage of an arrester (U_c)
permissible r.m.s. value of power frequency voltage that may be applied continuously between the terminals of the arrester in accordance with IEC 60099-4.

3.7
continuous operating voltage of an arrester including harmonics (U_{ch})
r.m.s. value of the combination of power frequency voltage and harmonics that may be applied continuously between the terminals of the arrester

3.8
equivalent continuous operating voltage of an arrester (ECOV)
r.m.s. value of the sinusoidal power frequency voltage at a metal-oxide surge arrester stressed by operating voltage of any wave-shape that generates the same power losses in the metal-oxide materials as the actual operating voltage

3.9
residual voltage of an arrester
peak value of voltage that appears between the terminals of an arrester during the passage of a discharge current (IEC 60099-4)

3.10
co-ordination currents of an arrester
for a given system under study and for each class of overvoltage, the current through the arrester for which the representative overvoltage is determined. Standard shapes of co-ordination currents for steep-front, lightning and switching current impulses are given in IEC 60099-4

NOTE The co-ordination currents are determined by system studies.

3.11
directly protected equipment
equipment connected in parallel to a surge arrester for which the separation distance can be neglected and any representative overvoltage be considered equal to the corresponding protective level

3.12
protective levels of an arrester
for each voltage class, residual voltage that appears between the terminals of an arrester during the passage of a discharge current corresponding to the co-ordination current

For HVDC converter equipment the following specific definitions 3.12.1 to 3.12.3 apply.

3.12.1
switching impulse protective level (SIPL)
residual voltage of a surge arrester subjected to a discharge current corresponding to the co-ordination switching impulse current

3.12.2
lightning impulse protective level (LIPL)
residual voltage of a surge arrester subjected to a discharge current corresponding to the co-ordination lightning impulse current

3.12.3
steep-front impulse protective level (STIPL)
residual voltage of a surge arrester subjected to a discharge current corresponding to the co-ordination steep-front impulse current

3.13
co-ordination withstand voltage
for each class of voltage, value of the withstand voltage of the insulation configuration, in actual service conditions, that meets the performance criterion (IEC 60071-1)

3.14
required withstand voltage
test voltage that the insulation withstands in a standard withstand test to ensure that the insulation will meet the co-ordination withstand voltage in actual service

(IEC 60071-1 modified)

3.15
specified withstand voltage
test voltage suitably selected equal or above the required withstand voltage (see 3.14)

NOTE 1 For a.c. equipment, values of specified withstand voltages are standardized as per IEC 60071-1. For HVDC equipment, there is no standardized values for the specified withstand voltages which are rounded up to convenient practical values.

NOTE 2 The standard impulse shapes used for withstand tests on equipment as well as the test procedures are defined in IEC 60060-1 and IEC 60071-1. For some d.c. equipment (e.g. the thyristor valves), the standard impulse shapes may be modified in order to more realistically reflect expected conditions.

3.15.1
specified switching impulse withstand voltage (SSIWV)
withstand voltage of insulation with the shape of the standard switching impulse

3.15.2
specified lightning impulse withstand voltage (SLIWV)
withstand voltage of insulation with the shape of the standard lightning impulse

3.15.3
specified steep-front impulse withstand voltage (SSFIWV)
withstand voltage of insulation with the shape specified in IEC 60700-1

3.16
thyristor valve protective firing (PF)
method of protecting the thyristors from excessive voltage in the forward direction by firing them at a pre-determined voltage

4 Symbols and abbreviations

The list covers only the most frequently used symbols and abbreviations some of which are illustrated graphically in the single-line diagram of figure 1 and table 1. For a more complete list of symbols which has been adopted for HVDC converter stations, and also for insulation co-ordination, refer to the standards listed in the normative references and to the bibliography.

4.1 Subscripts

0 (zero)	at no load (IEC 60633)
d	direct current or voltage (IEC 60633)
i	ideal (IEC 60633)
max	maximum (IEC 60633)
n	pertaining to harmonic component of order n (IEC 60633)

4.2 Letter symbols

K_a	atmospheric correction factor (IEC 60071-1)
K_c	co-ordination factor (IEC 60071-1)
K_s	safety factor (IEC 60071-1)
U_{ch}	continuous operating voltage of an arrester including harmonics
U_{dio}	ideal no-load direct voltage (IEC 60633)
U_{dim}	maximum value of U_{dio} taking into account a.c. voltage measuring tolerances, and transformer tap-changer offset by one step
U_s	highest voltage of an a.c. system (IEC 60071-1 and 60071-2)
U_{v0}	no-load phase-to-phase voltage on the valve side of converter transformer, r.m.s. value excluding harmonics
α	delay angle (IEC 60633); "firing angle" also used in this standard
β	advance angle (IEC 60633)
γ	extinction angle (IEC 60633)
μ	overlap angle (IEC 60633)

4.3 Abbreviations

CCC	capacitor commutated converter
CSCC	controlled series compensated converter
CCOV	crest value of continuous operating voltage
ECOV	equivalent continuous operating voltage
LIPL	lightning impulse protective level
PCOV	peak continuous operating voltage
PF	protective firing
RFAO	representative fast-front overvoltage (the maximum voltage stress value)
RSLO	representative slow-front overvoltage (the maximum voltage stress value)
RSTO	representative steep-front overvoltage (the maximum voltage stress value)
RLIWV	required lightning impulse withstand voltage
RSIWV	required switching impulse withstand voltage
RSFIWV	required steep-front impulse withstand voltage
SIPL	switching impulse protective level

STIPL	steep-front impulse protective level
SLIWV	specified lightning impulse withstand voltage
SSIWV	specified switching impulse withstand voltage
SSFIWV	specified steep-front impulse withstand voltage
TOV	temporary overvoltage

4.4 Typical HVDC converter station schemes and associated graphical symbols

Figures 1, 2 and 3 show the single line diagrams of typical HVDC converter stations equipped with two 12-pulse converter bridges in series. The main differences between the schemes consist in the presence, or not, of commutated capacitors (figure 2) or controlled series capacitors (figure 3) on the a.c. side of the HVDC converter station.

NOTE Figures 1, 2 and 3 show all the possible arresters covered in this standard. However, some of them may be eliminated because of specific designs.

Table 1 presents the specific graphical symbols associated with figures 1, 2 and 3 and which are defined for the purpose of this report. Arrester designations and details on their design and specific roles are presented in clause 9.

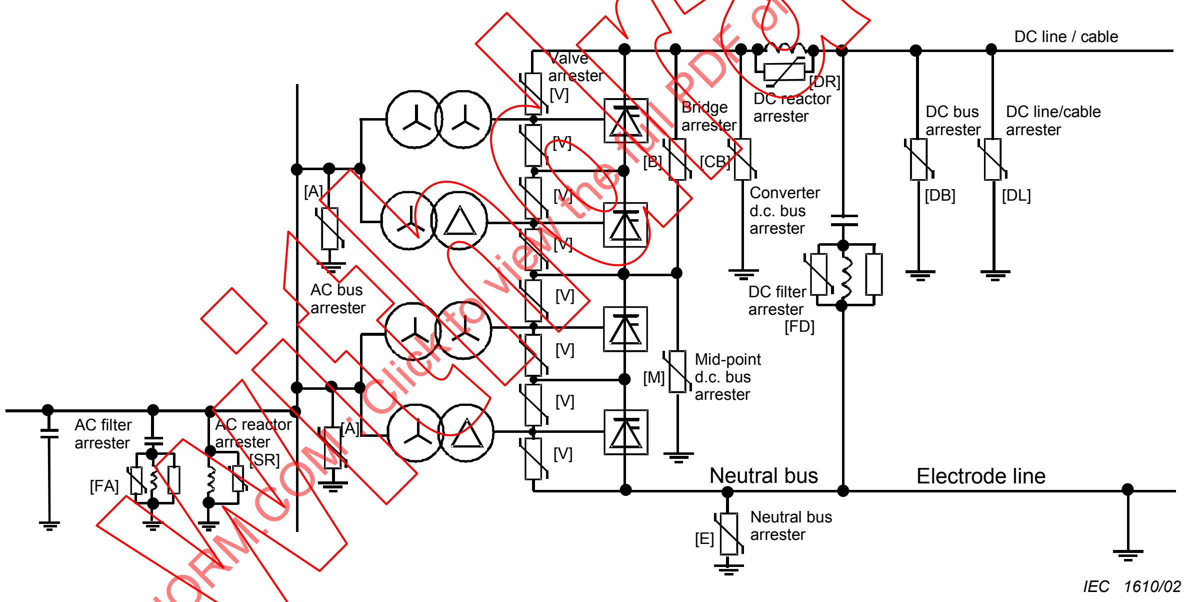


Figure 1 – Single line diagram of typical converter pole with two 12-pulse converters in series

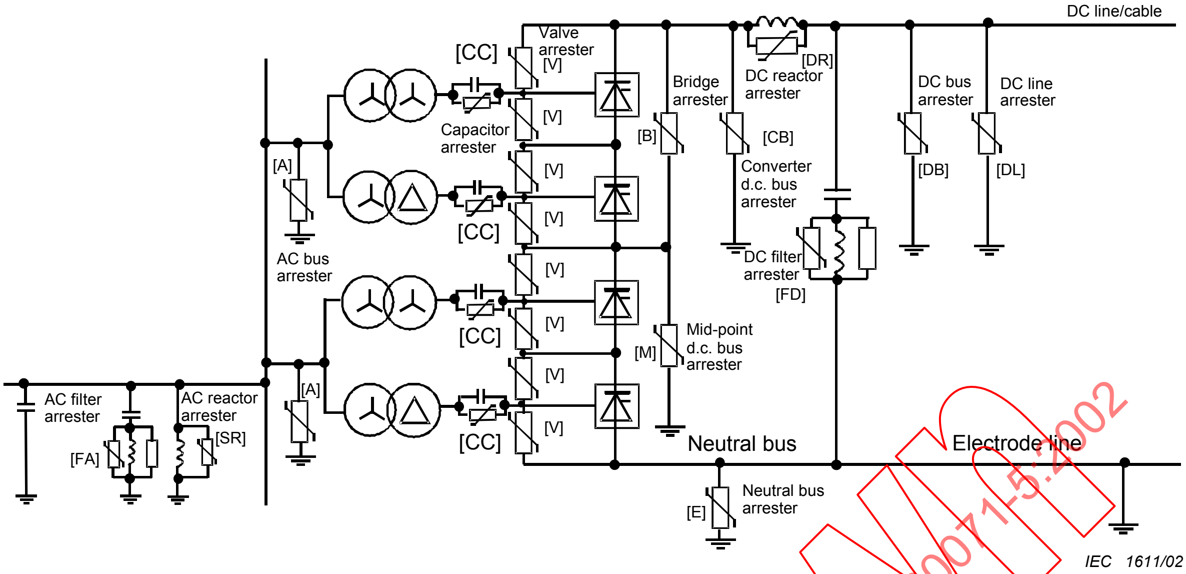


Figure 2 – Single line diagram of typical capacitor commutated converter (CCC) pole with two 12-pulse converters in series

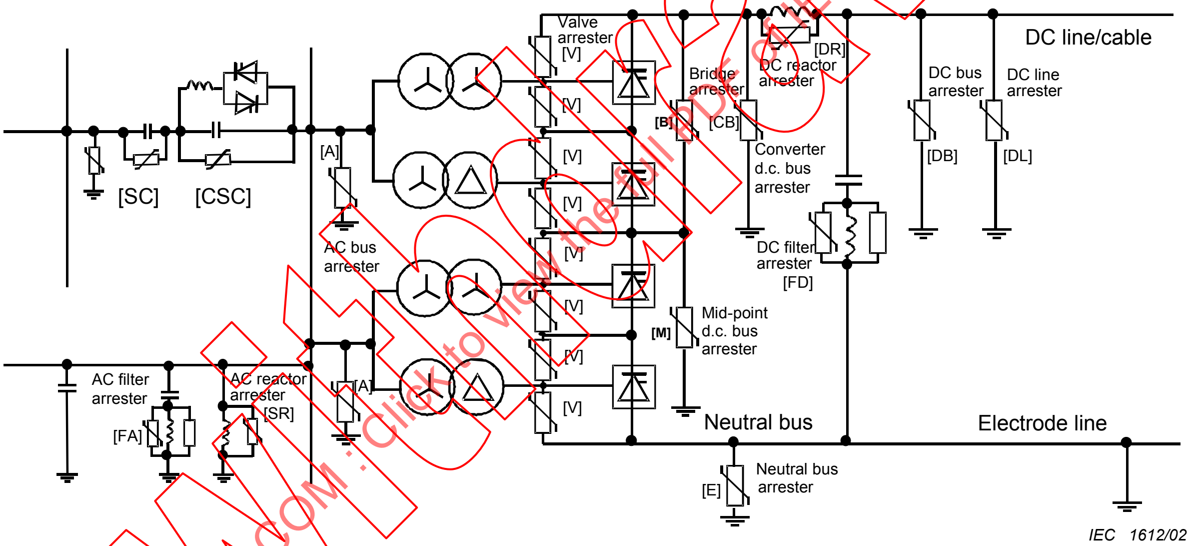
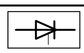
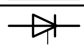
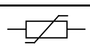
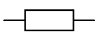
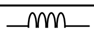
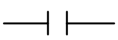
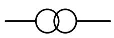
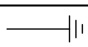


Figure 3 – Single line diagram of typical controlled series compensated converter (CSCC) pole with two 12-pulse converters in series

Table 1 – Symbol description

Symbol	Description
	Valve (commutation group)
	Valve (one arm)
	Arrester
	Resistor
	Reactor
	Capacitor
	Transformer with two windings
	Earth (ground)

5 Principles of insulation co-ordination

The primary objectives of insulation co-ordination are

– to establish the maximum steady state, temporary and transient overvoltage levels to which the various components of a system may be subjected in practice,

– to select the insulation strength and characteristics of equipment, including those for protective devices, used in order to ensure a safe, economic and reliable installation in the event of the above overvoltages.

5.1 Essential differences between a.c. and d.c. systems

In terms of the above objectives, insulation co-ordination applied to an HVDC converter station is basically the same in principle as that of an a.c. substation. However, essential differences exist which warrant particular consideration when dealing with HVDC converter station insulation co-ordination. For example, there is a need to consider the following:

- the requirements of series-connected valve groups involving surge arresters connected across individual valves and between terminals away from earth potential which involves the use of different insulation levels for different parts of the HVDC converter station;
- the topology of the converter circuits with no direct exposure to the external overvoltage since these circuits are bounded by inductances of converter transformers and smoothing reactors (see also 9.4.3);
- the presence of reactive power sources and harmonic filters on both the a.c. and d.c. sides;
- the presence of converter transformers with two major windings including the valve side winding floating from earth potential when the valves are not conducting, and a d.c. component of current flowing when the valves are conducting;
- the characteristics of the converter valves, including their controls;
- the impact of control and protection in reducing overvoltages;
- voltage polarity effects of d.c. stress which, by attracting greater contaminants to the d.c. insulation because of constant polarity, lead to greater creepage and clearance requirements and to worse pollution and flashover performance compared with a.c. insulation under the same environment;
- long overhead transmission lines and cables without intervening switching stations;
- interaction between the a.c. and d.c. systems, particularly where the a.c. system is relatively weak;
- composite continuous operating voltages which include in some cases direct voltage, fundamental frequency voltage, harmonic voltages and high frequency components;
- the various operating modes of the converter such as monopolar, bipolar, parallel or multi-terminal.

5.2 Insulation co-ordination procedure

Table 2 is a flow chart showing the comparison between the insulation co-ordination procedure for a.c. systems (refer to figure 1 of IEC 60071-1) and for HVDC converter stations.

The general method of investigation is basically the same for an a.c. scheme as it is for an HVDC converter station. This requires:

- an evaluation of characteristics of the system and the HVDC converter station;
- an assessment of the nature of the insulation in each equipment;
- the determination of different representative overvoltages;
- consideration of the type of overvoltage protection adopted and of current/energy stresses imposed to surge arresters and determinant on their design.

However, characteristics of insulation and voltage distribution are different for a.c. and d.c. systems.

Table 2 – Comparison of the selection of withstand voltages for three-phase a.c. equipment with that for HVDC converter station equipment

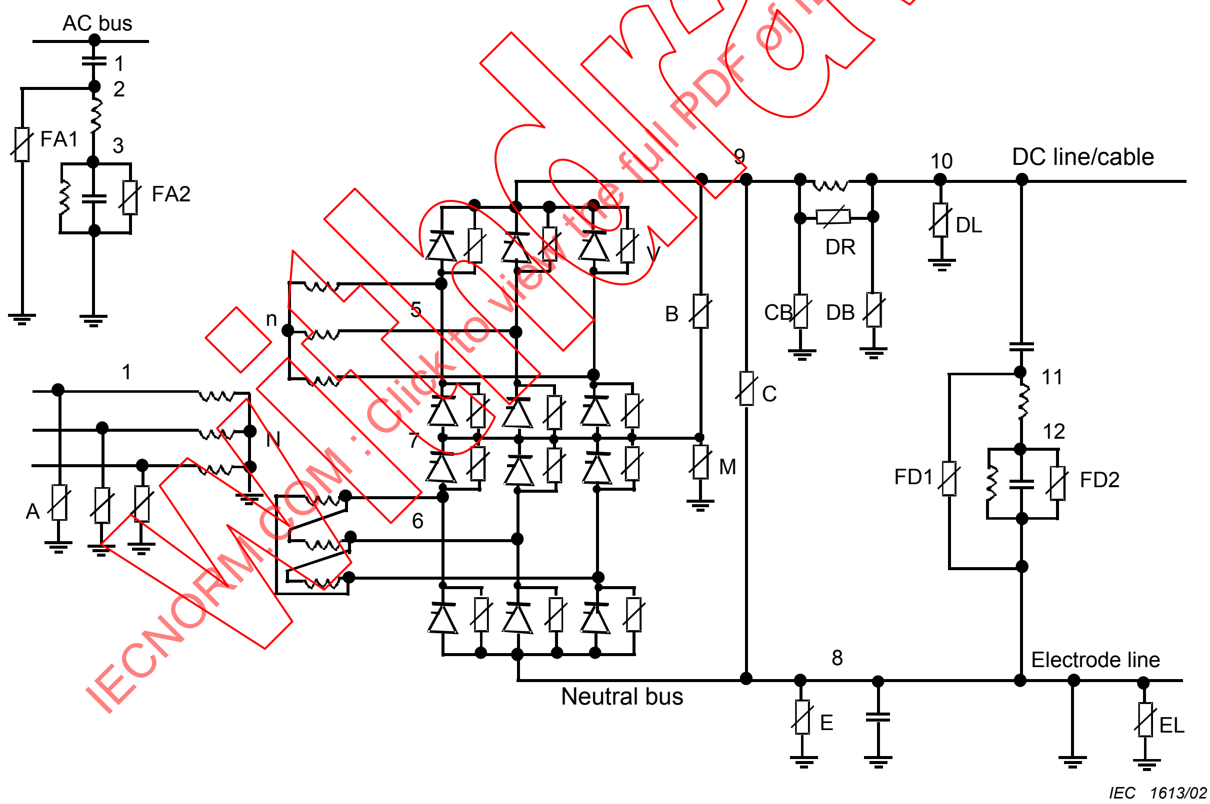
Flow chart for the determination of rated or standard insulation levels for three-phase a.c. equipment according to IEC 60071-1	Deviations from IEC 60071-1 in the selection of withstand voltages for HVDC converter station equipment
System analysis	System analysis. Same approach as for a.c.
Representative voltages and overvoltages	Representative voltages and overvoltages. Same approach as for a.c.
Selection of the insulation meeting the performance criterion	Selection of the insulation meeting the performance criterion. Same approach as for a.c.
Co-ordination withstand voltages	In general, co-ordination withstand voltages are determined in the same way as for a.c. For HVDC converter equipment requiring a very close protection with surge arresters (directly protected equipment), co-ordination withstand voltages are deduced from a process involving the determination of the co-ordination currents
Application of factors to account for the differences between type test conditions and actual service conditions	Application of factors to account for the differences between test conditions and actual service conditions. Same approach as for a.c.
Required withstand voltages	Required withstand voltages. Same approach as for a.c.
Selection of standard withstand voltages	Selection of standard withstand voltages for a.c. side equipment only. The present step is skipped for equipment on d.c. side because there are no standardized withstand voltage levels for such equipment
Rated or standard insulation level: set of standard withstand voltages	Set of standard withstand voltages is applicable only for equipment on the a.c. side. For equipment on the d.c. side, specified insulation levels are rounded up to convenient practical values

6 Voltages and overvoltages in service

6.1 Arrangements of arresters

Since the late 1970s, overvoltage protection of HVDC converter stations has been based exclusively on metal-oxide surge arresters. This is largely due to their superior protection characteristics compared with the gapped SiC arresters (earlier technology) and their reliable performance when connected in series or parallel with other arresters. The actual arrangement of the arresters depends on the configuration of the HVDC converter station and the type of transmission circuit. The basic criteria used however is that each voltage level and the equipment connected to it is adequately protected at a cost commensurate with the desired reliability and equipment withstand capability.

A typical arrester arrangement between the a.c. side of the converter bridges and the d.c. transmission circuit is shown in figure 4 for a two terminal bipolar HVDC scheme with one 12-pulse converter per pole. It should be noted however, that some of the arresters may be deleted, depending upon the overvoltage withstand capability of the equipment connected at that point, and upon the overvoltage protection afforded by a combination of other arresters at the same point. For example, the d.c. bus can be protected by a series combination of the bridge (B) and mid-point d.c. bus (M) arresters, instead of the converter unit d.c. bus arrester (CB).



NOTE This figure shows all the possible arresters covered in this standard. However, some of them may be eliminated because of specific designs.

Figure 4 – HVDC converter station diagram with 12-pulse converter bridges

Similar protective arrangements may be used for stations with two 12-pulse converters per pole or for back-to-back stations. In the latter case, only the valve arresters (V) are normally needed on the valve side since the operating voltage is much lower than for a line or cable transmission scheme. However, mid-point bus (M) or bridge (B) arresters are sometimes included.

For HVDC converter stations connected directly to d.c. cables, the d.c. line/cable arrester (DB and DL) may be deleted since the pole may not be exposed to fast-front overvoltages.

On the a.c. side of the HVDC converter station, phase-to-earth arresters (A) are normally provided to protect the converter a.c. bus and the a.c. filter bus.

Arresters are also normally connected across both a.c. and d.c. harmonic filter reactors or from the high-voltage terminals of the filter reactors to earth, as shown in figure 4.

In systems involving a combination of d.c. cables and/or overhead lines, arresters may be needed at the cable terminations to protect them from overvoltages originating from the overhead line.

More detailed discussion of the need for and the requirements of the arresters is included in clause 9.

The basic principles when selecting the arrester arrangement are that:

- Overvoltages generated on the a.c. side should, as far practicable, be limited by arresters on the a.c. side. The main protection is given by the a.c. bus arresters (A).
- Overvoltages generated on the d.c. or earth electrode line should, in a similar way, be limited by d.c. line/cable arresters (DB and DL), converter bus arresters (CB), and neutral bus arresters (E).
- For overvoltages within the HVDC converter station, critical components should be directly protected by arresters connected close to the components, such as valve arresters (V) protecting the thyristor valves and a.c. bus arresters (A) protecting the line side windings of the transformers. Protection of the valve side of the transformers will usually be achieved by arresters connected in series, e.g. a combination of bridge arrester (B), mid-point arrester (M) and a valve arrester (V). However, where the HVDC converter station transformers may be disconnected from the bridges, provision should be made to protect the transformer valve windings.

6.2 Continuous operating voltages at various locations in the converter station

Figure 5 shows typical waveforms of continuous operating voltages excluding commutation overshoots at various locations in the HVDC converter station either to earth (G) or to another point for the typical configuration of figure 4.

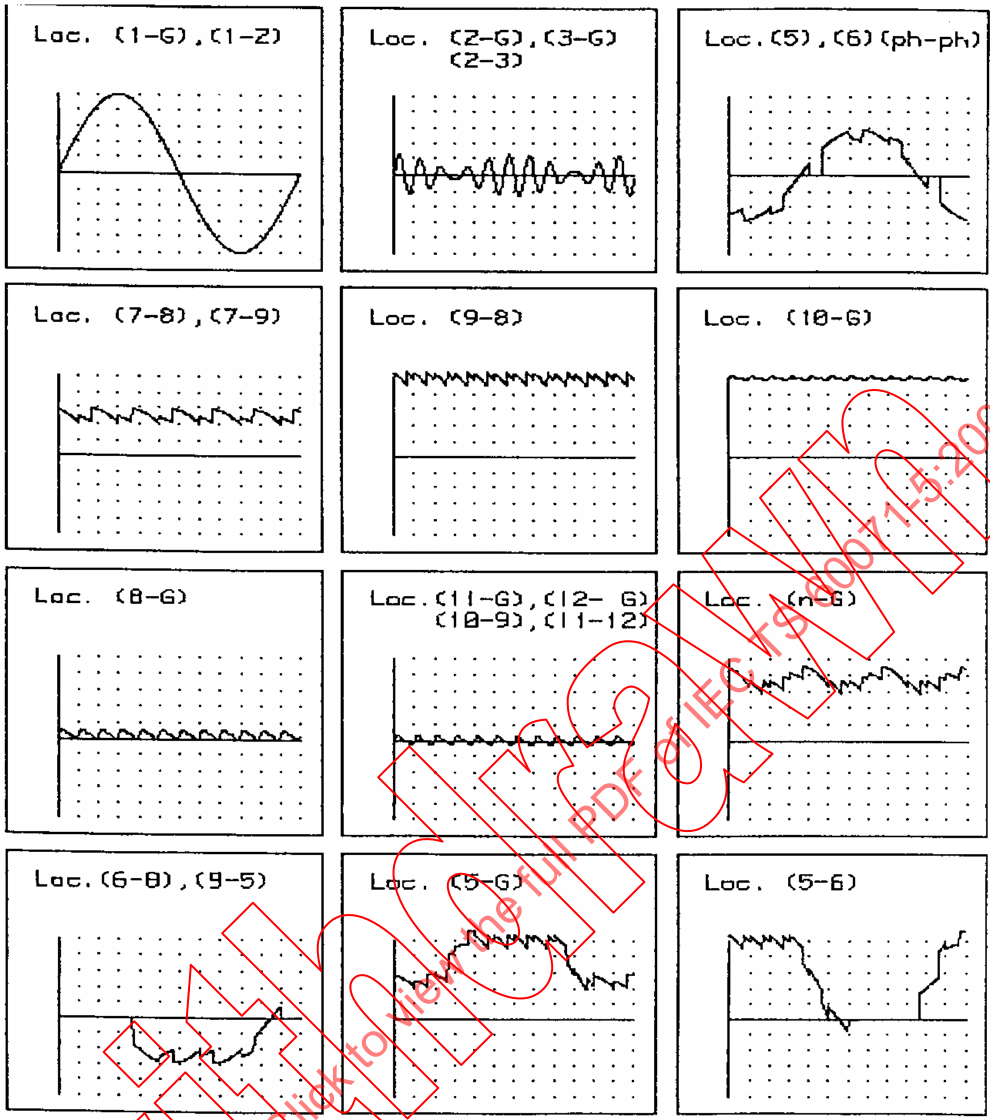


Figure 5 – Continuous operating voltages at various locations (location identification according to figure 4)

6.3 Peak (PCOV) and crest value (CCOV) of continuous operating voltage applied to valves and arresters

The continuous operating voltage for HVDC arresters differs from that for normal a.c. arresters in that it consists of not simply the fundamental frequency voltage but rather of components of direct voltage, fundamental frequency voltage and harmonic voltages, and high frequency transients.

The switching action of the valves produces high frequency turn-on and turn-off commutation transient voltages which are superimposed on the commutation voltage. The overshoot at turn-off increases the transformer valve-side winding voltage and in particular the off-state voltage across the valves and associated valve arresters. The amplitude of the overshoot is determined by:

- the inherent characteristics of the thyristors (particularly the recovery charge);
- the distribution of the recovered charge in a series-connected string of thyristors in a valve;
- the damping resistors and capacitors at individual thyristor levels;
- the various capacitances and inductances within the valve and commutation circuit;
- the firing and overlap angles,
- the valve commutation voltage at the instant of turn-off.

Special attention shall to be paid to the commutation overshoots with respect to energy absorption in the valve arresters and other arresters on the d.c. side.

The continuous operating voltage waveform for the valve and valve arrester (V) is shown in figure 6. The CCOV (defined in clause 3) is proportional to the $U_{dim,}$ and is given by:

$$\text{CCOV} = \frac{\pi}{3} \times U_{\text{dim}} = \sqrt{2} \times U_{\text{v0}}$$

Refer to 4.2 for the definition of U_{dim} and U_{v0} .

Operation with large delay angles α increases the commutation overshoots and special care shall be taken that these do not overstress the arresters.

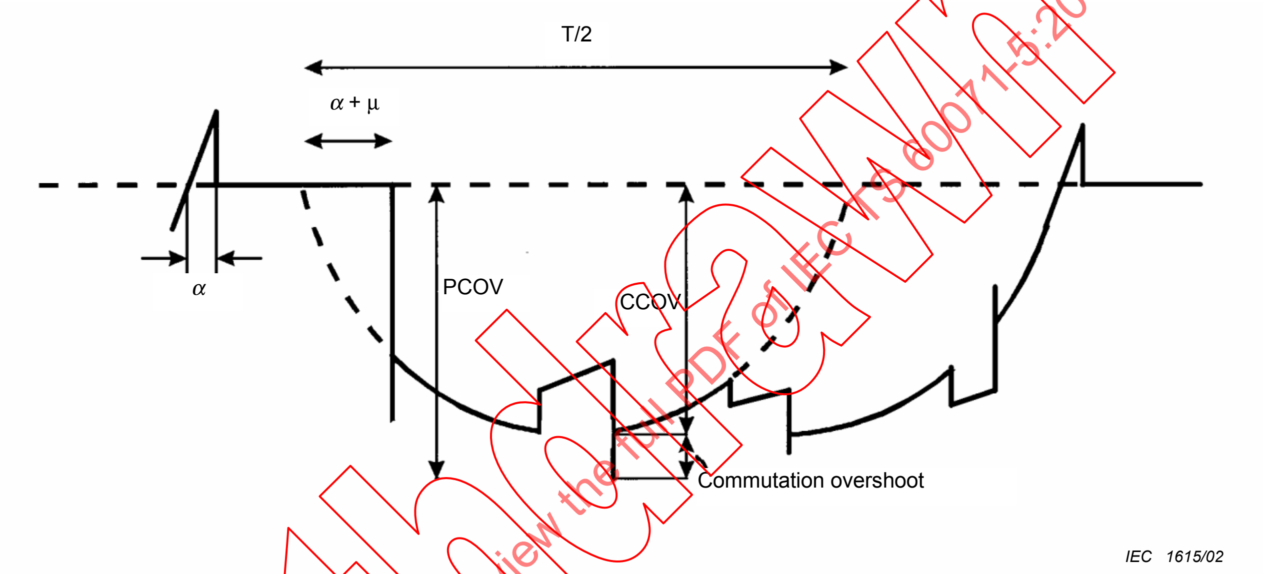


Figure 6 – Operating voltage of a valve arrester (V), rectifier operation

6.4 Sources and types of overvoltages

Overvoltages on the a.c. side may originate from switching, faults, load rejection or lightning. The dynamic characteristics of the a.c. network, its impedance and also its effective damping at dominant transient oscillation frequencies, and the proper modeling of the converter transformers, of static and synchronous compensators and the filter components, are important in evaluating the overvoltages. If the length of busbars in the a.c. switchyard are significant, they shall be taken into account in the overvoltage evaluation (e.g. distance effects) and in the location of arresters.

Overvoltages on the d.c. side may originate from either the a.c. system or the d.c. line and/or cable, or from in-station flashovers or other fault events.

In assessing the overvoltages, the configuration of the a.c. and d.c. systems shall be taken into account as well as the dynamic performance of the valves and controls, and credible worst case combinations, as discussed in 6.8. Impacts on arrester requirements are discussed in clause 9.

6.4.1 Slow-front and temporary overvoltages on the a.c. side

Slow-front and temporary overvoltages occurring on the a.c. side are important to the study of arrester applications. Together with the highest a.c. operating voltages (U_s) they determine the overvoltage protection and insulation levels of the a.c. side of the HVDC converter station. They also influence valve insulation co-ordination.

Slow-front overvoltages on the a.c. bus of an HVDC station, can be caused by switching of transformers, reactors, static var compensators, a.c. filters and capacitor banks connected to the converter a.c. bus, and by fault initiation and fault clearing as well as by closing and reclosing of lines. Slow-front overvoltages occur with high amplitude only for the first half cycle of the transient with significantly reducing amplitudes for subsequent cycles. Slow-front overvoltages which originate at locations in the a.c. network remote from the HVDC converter station usually have magnitudes which are relatively low in comparison with those caused by events occurring close to the converter a.c. bus.

During the operating life of the equipment, switching of equipment connected to the converter a.c. bus may occur many times. The overvoltages caused by these routine switching operations are generally less severe than the slow-front overvoltages caused by faults. However, switching-off of a circuit breaker can, in rare cases, produce restrike phenomenon and this gives rise to overvoltage.

The selection of a.c. arresters for HVDC stations should consider the presence of existing arresters connected in parallel in the a.c. network and avoid the existing arresters being overloaded during slow-front and temporary overvoltages.

6.4.1.1 Overvoltages due to switching operations

Because of the frequency of these operations, it is generally desirable that the surge arresters used to protect equipment do not absorb appreciable energy during these events. Hence, in some cases, the slow-front overvoltages arising from such routine operations are minimized by the use of circuit breakers incorporating closing and/or opening resistors, or by synchronizing the closing and/or opening of the circuit breaker poles, or equipping the breaker with arresters across the poles. The HVDC control system can also be used to effectively damp certain overvoltages such as temporary overvoltages.

Energization of transformers causes inrush current, due to saturation effects, containing harmonics dominated by second order harmonic and other low order harmonics. If one or more of these harmonic currents meet resonant conditions, in a network with low damping, high harmonic voltages are produced in the network leading to overvoltages. In an HVDC station, resonant conditions are often more severe because of the presence of a.c. filters and capacitor banks. These capacitances lower the resonance frequency and second or third harmonic resonances may be present. These overvoltages can last for several seconds, such as temporary overvoltages.

6.4.1.2 Overvoltages due to faults

When an asymmetric fault occurs in the a.c. network, transient and temporary overvoltages occur on the healthy phases, influenced by the zero sequence network. In solidly earthed systems that are typical for networks connected to HVDC stations, the transient overvoltages (phase-to-earth) normally range between 1,4 p.u. and 1,7 p.u. and the temporary overvoltage from 1,2 p.u. to 1.4 p.u.

At fault clearance following a single-phase or three-phase fault close to the busbar of the HVDC station, the saturation of the transformer depends both on the fault instant and on the fault clearing instant. It is therefore necessary to vary the fault conditions when this phenomenon is studied. This fault case is discussed further in clause 9.

The highest temporary overvoltages usually occur in conjunction with sudden three-phase faults and complete load rejection if the converters are blocked as a consequence of the fault without simultaneous disconnection of filters. The filters and capacitor banks together with the a.c. system can result in low resonance frequencies. The temporary overvoltages due to faults can be more severe both from the overvoltage point of view and with regard to possible arrester energy stresses. The presence of filters tuned or damped at frequencies between the second and the fifth harmonic can often be effective in reducing the distortion of the voltage and thereby the stresses on the arresters but at a very high cost. AC active filters may be used for this purpose.

6.4.2 Slow-front and temporary overvoltages on the d.c. side

Except for the a.c. side overvoltages transmitted through the converter transformers, the d.c. side insulation co-ordination for slow-front overvoltages and temporary overvoltages is mainly determined by fault and generated slow-front overvoltages on the d.c. side.

Events to be considered include d.c. line-to-earth faults, d.c. side switching operations, events resulting in an open earth electrode line, generation of superimposed a.c. voltages due to faults in the converter control (e.g. complete loss of control pulses) misfiring, commutation failures, earth faults and short-circuits within the converter unit. These contingencies are discussed in more detail in clause 9.

Energization of the d.c. line with the remote inverter terminal open (rectifier at peak d.c. output voltage) should also be considered if measures have not been taken to avoid such an event.

In HVDC converter stations with series connected converter bridge units, events such as by-pass operation on one converter while the second converter bridge unit is in operation shall be considered, particularly during inverter operation. Special attention shall be paid to insulation co-ordination of parallel connected converter bridge units. Some information on these and other special converter configurations is given in annex C.

6.4.3 Fast-front, very fast-front and steep-front overvoltages

The different sections of HVDC converter stations should be examined in different ways for fast-front and steep-front overvoltages. The sections include:

- a.c. switchyard section from the a.c. line entrance up to the line side terminals of the converter transformers;
- d.c. switchyard section from the line entrance up to the line side terminal of the smoothing reactor;
- converter bridge section between the valve side terminal of the converter transformers and the valve side terminal of the smoothing reactor.

The converter bridge section is separated from the other two sections by series reactances, i.e. at the one end, the inductance of the smoothing reactor and at the other end, the leakage reactance of the converter transformers. Traveling waves such as those caused by lightning strokes on the a.c. side of the transformer or on the d.c. line beyond the smoothing reactor, are attenuated (but may also be capacitively transferred as discussed in 9.4.3) due to the combination of series reactance and shunt capacitance to earth to a shape similar to slow-front overvoltages. Consequently they should be considered as part of the slow-front overvoltage co-ordination.

The a.c. and d.c. switchyard sections have low impedance compared with overhead lines. The differences from most conventional a.c. switchyards are the presence of a.c. filters, d.c. filters and possibly large shunt capacitor banks, all of which may have an attenuating effect on the incoming overvoltages.

Steep-front overvoltages caused by earth faults in the HVDC converter station, including locations inside the valve hall, are important for insulation co-ordination, especially for the valves. These overvoltages typically have a front time of the order 0,5 µs to 1,0 µs and durations up to 10 µs. The values and waveshapes to be specified should be determined by digital simulation studies; both peak magnitude and peak rate of change of voltage can be important.

In the a.c. switchyard section, very fast-front overvoltages with front times of 5 ns to 150 ns may also be initiated by operation of disconnectors or circuit breakers in gas-insulated switchgear (GIS). Some further information on the effect of GIS is given in clause C.6.

6.5 Overvoltage limiting characteristics of arresters

Metal-oxide surge arresters without gaps are used for the protection of equipment in most modern day HVDC converter stations and are increasingly being used to replace other types of arresters on systems already in service. These arresters provide superior overvoltage protection for equipment compared with gapped SiC arresters due to their low dynamic impedance and high energy absorption capability. The ability of the metal-oxide arrester blocks to share arrester discharge energy when connected in parallel if they are selected to have closely matched characteristics allows any desired discharge energy capability to be realized. Metal-oxide blocks may be connected in several parallel paths within one arrester unit and several arrester units may be connected in parallel to achieve the desired energy capability. Also, parallel connection of metal-oxide blocks may be used to reduce the residual voltage of the arrester, if required.

For metal-oxide arresters, the variation of voltage U with current I can be represented by the equation:

$$I = k \times U^{\alpha}$$

k is a constant and α is a non-linearity coefficient of the element material. Within the operating range of the arrester the value of this coefficient is high for zinc oxide, typically in the range 30 to 50, as compared to silicon carbide elements used in gapped arresters which exhibit a coefficient of typically 3.

The protective characteristics of an arrester are defined by the residual arrester voltages for maximum steep-front, lightning and switching current impulses that can occur in service. Typical current waveshapes used to define the arrester protective levels are 8/20 µs for the LIPL and 30/60 µs for the SIPL (IEC 60099-4). The STIPL is usually defined for a current impulse of 1 µs front time. The resulting voltage waveforms across the arrester differ because of the high non-linearity coefficient of the arrester block material. The amplitude of the current for which the protective level is specified, which is referred to as the co-ordination current, is usually selected differently for different types of current waveshapes and locations of the arresters. These co-ordination currents are determined from detailed studies carried out during the final stages of the design (see 6.7 below).

The arresters used on the a.c. side are usually specified as for arresters in a normal a.c. system by their rated voltage and maximum continuous operating voltage. The rated voltage is the maximum permissible r.m.s. value of power frequency voltage between the terminals at which the arrester is designed to operate correctly, as established in the operating duty tests. The maximum continuous operating voltage is used as a reference parameter for the specification of operating characteristics.

For the arresters on the d.c. side of a HVDC converter station, the rated voltage is not defined and continuous operating voltage is defined differently because the voltage waveshape which continuously appears across the arresters consists, in many cases, of superimposed direct, fundamental and harmonic components and, in some cases, also commutation overshoots.

The arresters are specified in terms of peak continuous operating voltage (PCOV), crest value of continuous operating voltage (CCOV), and equivalent continuous operating voltage (ECOV), as defined in clause 3. This means that the tests specified for these arresters shall be adjusted for the particular applications, different from standard tests usually applicable for a.c. arresters. The required energy capability of the arresters shall consider the applicable waveshapes as well as the amplitudes, duration and the number of respective discharges.

For filter arresters, the higher losses due to harmonics shall be taken into account.

6.6 Valve protection strategy

The main purpose of the valve arrester (V) is to protect the thyristor valves from excessive overvoltages. This arrester and/or the protective firing of thyristors in the forward direction constitute the overvoltage protection of the valve. Since the cost of the valves and also its power losses are roughly directly proportional to the insulation level across the valves, it is essential to keep this insulation level and therefore the arrester protective level as low as possible.

There are two different strategies used to co-ordinate the protective firing level with the protective level of the valve arrester. In the first strategy, the thyristor firing threshold is set in such a manner that the overvoltage protection of the valve in both the reverse and the forward direction is afforded by the valve arrester. In this case, the protective firing level for the valve is set higher than the protective level of the valve arresters. For this strategy, protective firing action is used to protect the individual thyristor levels in the event of severe non linear stress distribution of fast transient or steep-front voltages within the valve. In the second strategy, while the valve arrester limits overvoltages in the reverse direction, protective firing threshold for the valve is set lower typically 90-95 % of the valve arrester protective level, thus providing the main overvoltage protection in the forward direction. However, the second strategy can be used only when the reverse withstand voltage of the thyristor is higher than the forward withstand voltage of the thyristor. This approach would normally lead to fewer thyristor levels in a valve than with the first strategy, resulting in reduced costs and improved converter efficiency. The protective firing threshold should be set sufficiently high to ensure that activation of protective firing is avoided during the highest temporary overvoltages (taking into account commutation transients and voltage imbalance) or during events which occur frequently (e.g. switching operations). This is to minimize undue interruption of power transmission and facilitate speedy recovery following faults which occur with the converter remaining in operation.

6.7 Methods and tools for overvoltage and surge arrester characteristic studies

This subclause discusses the overall methods and tools required to fix the overvoltage characteristics that may affect an HVDC converter station and to derive the required arrester characteristics. The objective of these studies, as further detailed in clause 7, are as follows:

- determine stresses and protective levels of arresters in an HVDC converter station;
- form the basis for insulation co-ordination of HVDC converter stations;
- derive the specification of all the arresters involved.

6.7.1 General considerations, study approach and study tools

In order to carry out the studies, the following information is required, as further detailed in 6.8:

- configuration of the HVDC station, as well as a.c. and d.c. system data;
- data of equipment connected on both a.c. and d.c. side (e.g. transformers, lines, etc.);
- arrester characteristics;
- converter control and valve protection strategies, including response and/or delay in valve protecting firing circuit;
- operating conditions;

- valve protective strategies (response of valve protective firing).

The overvoltage study approach may consist of the following steps:

Step 1: Define preliminary arrester configuration and determine preliminary arrester parameters such as U_c, U_{ch}, PCOV and/or CCOV for each arrester.

Step 2: Study the cases producing the highest current and energy stresses. At this stage, the minimum number of arrester columns and their ratings are defined, considering the arrester stresses and contingencies.

Step 3: Check for fast-front and steep-front overvoltages to ensure that with the arrester arrangement defined in steps 1 and 2, the whole HVDC station is adequately protected. Additional arresters may be required due to distance effects.

Step 4: Establish the arrester duties (co-ordination current/voltage/energy) based on study results, (see clause 9), and determine the arrester specification (see 7.1 and 9.1).

Step 5: Establish the maximum overvoltages and withstand voltages at various locations (see 7.3).

For arrester duties, general principles consist to consider minimum V-I protection characteristic for energy consumption and to consider maximum V-I protection characteristic for protection level.

Although there are many tools available for the calculation of overvoltages and arrester stresses, it is important to consider the validity of each tool for the proper representation of power system components to obtain the required characteristics of the models for the study undertaken. To obtain meaningful results the components need to be properly modeled with regard to the frequency range of interest and other characteristics of the network components. (For guidance on model representations, see Bibliography). Typically digital computer programs employing numerical transient analysis methods are used for these calculations. TNA with HVDC Simulator is also a possible study tool.

New study tools using real time digital simulation techniques are available. These tools under the present conditions may not be suitable to study the high-frequency overvoltages due to time step limitations.

6.7.2 Events to be studied

Subclauses 6.2 to 6.4 describe the continuous, temporary, slow-front, fast-front and steep-front stresses that arresters can experience in HVDC converter station. These events and stresses are summarized in tables 3 and 4 (source: tables 4.1 and 4.2 of [4][1]).

Table 3 relates to various contingencies and the affected arresters. Table 4 gives further information concerning the type of stresses the different arresters experience, and whether the current or energy stresses can be of significance for particular contingencies and arresters. This information can be used to decide on the relevant system model for detailed studies.

[1] Figures in square brackets refer to the bibliography.

Table 3 – Events stressing the different arresters

NOTE Some events may not need to be considered due to a too low probability occurrence.

Event	Arresters (refer to figure 4 for arrester designation)								
	FA1 FA2	**A**	**V B**	**M**	**CB C**	**E**	**DR**	**DB DL**	**FD1 FD2**
Earth fault d.c. pole						x	x	x	x
Lightning from d.c. line						x	x	x	x
Slow-front overvoltages from d.c. line						x		x	x
Lightning from earth electrode line						x			
Earth fault a.c.-phase on valve side			x	x		x	x		
Current extinction three-pulse commutation group			x						
Current extinction six-pulse bridge			x	x					
Loss of return path, monopolar operation or commutation failure						x			
Earth faults and switching operation, a.c. side	x	x	x	x	x	x	x		x
Lightning from a.c. system	x	x							
Station shielding failure (if applicable)			x	x	x				

Table 4 – Types of stresses on arresters for different events

Contingency	Fast-front and steep-front stresses		Slow-front and temporary overvoltage stresses	
	Current	**Energy**	**Current**	**Energy**
Earth fault, d.c. pole	E, FD1, FD2	E, FD1, FD2	DB, DL, DR, E	E
Lightning from d.c. line	DB, DL, FD1 FD2, DR, E			
Slow-front overvoltages from d.c. line			DB, DL, E, FD1, FD2	
Lightning from earth electrode line	E			
Earth fault on bridge a.c. phase	V, B		DR, V, B, E, M	V, B, E, M
Current extinction, three-pulse group			V, B	V, B
Current extinction, six-pulse group			M, V, B	M, V, B
Loss of return path, monopolar operation and/or commutation failure			E	E
Earth faults and switching operations on a.c. side	FA1, FA2	FA1, FA2	V, M, CB, A, FA1, FA2 E, FD1, FD2, DR, C, B	V, B, A, E FD1, FD2
Lightning from a.c. system	A, FA1, FA2			
Station shielding failure (if applicable)	V, M, CB, C, B			

Converter contingencies such as commutation failures or inverter blocking without by-pass pairs are not critical for determining protective levels and energy requirements of the HVDC converter station arresters. However, inverter blocking with current interruption is important for determining arrester energy requirements. Some cases of commutation failures may be critical (e.g. giving rise to resonances, or in a situation involving the combination of the low neutral arrester protective level (E) and high impedance of a d.c. current return path).

6.8 Necessary system details

6.8.1 Modeling and system general representation

For insulation co-ordination studies, models of network components valid in the range d.c. to 50 MHz may be required. A representation valid for the complete frequency range is difficult to achieve for all network components. Various parameters have different influences on the correct representation of components within the frequency range of interest at which the model should be representative of the system characteristics.

Models shall be regarded as incomplete. If a design by experience has proved to be satisfactory, this may be used. Transformer modeling has limited accuracy.

Transient phenomena appear during transitions from one steady state condition to another. The primary causes of such disturbances in a system are closing or opening of a breaker or another switching equipment, short circuits, earth faults or lightning strikes. The consequential electromagnetic phenomena are traveling waves on lines, cables or busbar sections and oscillations between inductances and capacitances of the system. The frequencies of oscillations are determined by the surge impedances and travel times of connecting lines.

Table 5 gives an overview on the various origins of such transients and their frequency ranges. These frequency ranges are needed for modeling.

Table 5 – Origin of overvoltages and associated frequency ranges

Group	Frequency range for representation	Representation mainly for	Origin
I	0,1 Hz – 3 kHz	Temporary overvoltages	• Transf. energization (ferroresonance) • Load rejection • Fault clearing or initiation, line energization
II	50 Hz – 20 kHz	Slow-front overvoltages	• Terminal faults • Short line faults • Closing/reclosing
III	10 kHz – 3 MHz	Fast-front overvoltages	• Fast-front overvoltages • Circuit breaker restrikes • Faults in substations
IV	1 MHz – 50 MHz	Steep-front overvoltages	• Disconnector switching • Faults in GIS – substations • Flashover

The overall system configuration is schematically represented in figure 7. From an insulation co-ordination point of view, it is convenient to divide an HVDC converter station, including the connected a.c. and d.c. lines, into different parts with regard to the overvoltages generated. These parts or subsystems comprise:

a) the a.c. network;

b) the a.c. part of the HVDC converter station including the a.c. filters and any other reactive power source, circuit breakers and line side of converter transformer;

c) the converter bridges, the valve side of the converter transformer, the d.c. reactor, the d.c. filter and the neutral bus;

d) the d.c. line/cable and earth electrode line/cable.

These parts or subsystems should be considered in defining the study model, which could be either detailed or suitably simplified without losing the validity of the study results.

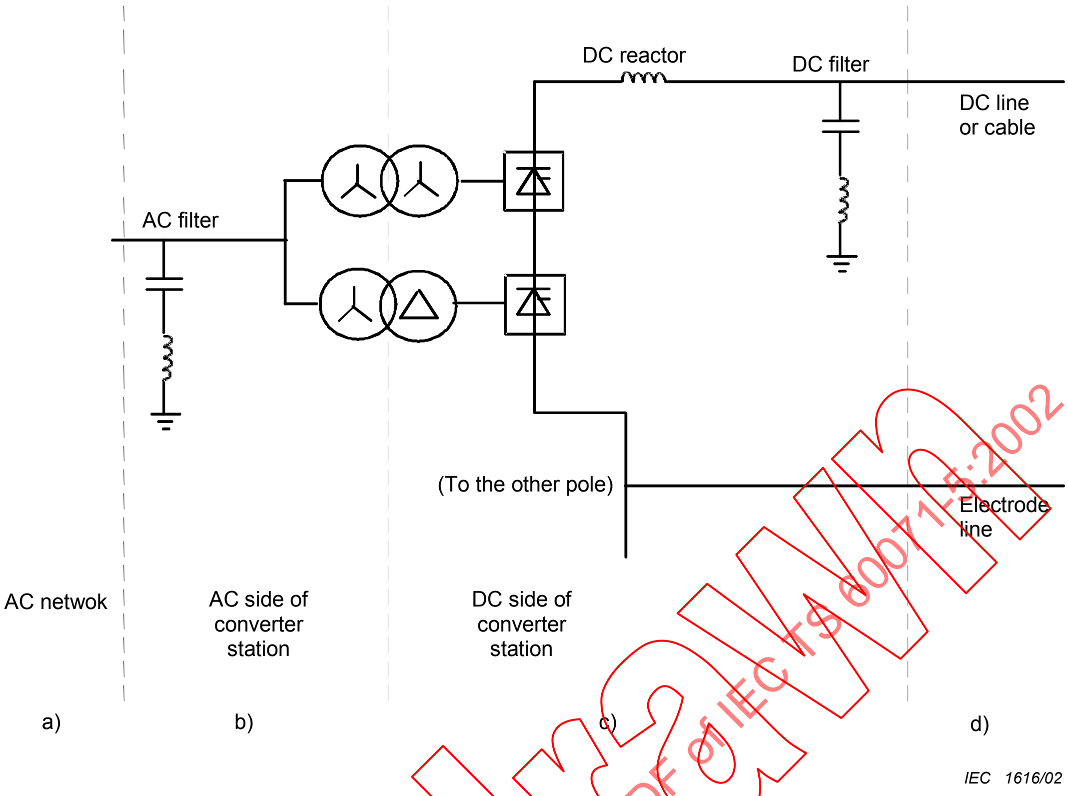


Figure 7 – One pole of an HVDC converter station

6.8.2 AC network and a.c. side of the HVDC converter station

6.8.2.1 Details for slow-front and temporary overvoltages

a) Detailed three-phase modeling or adequate equivalents for the a.c. network near the HVDC converter station. Lines leaving the station and nearby transformers including their saturation characteristics are represented as well as converters electrically close to the plant. Network equivalents should be used for the main part of the a.c. systems and the damping effect of the loads which affect the overall damping at resonance frequencies as seen from the HVDC station is taken into account.

b) Representation of the equipment installed on the a.c. side of the HVDC converter station. This includes any reactive power source and the converter transformers. The saturation of the converter transformer is a key parameter.

c) Representation of a.c. bus and filter arrester characteristics in the frequency range of some hundreds of Hz.

6.8.2.2 Details for fast-front and steep-front overvoltages

a) An adequate high frequency parameter model should be used for a.c. lines, busbars etc.

b) AC filter components shall be represented including stray inductance and capacitance.

c) AC lines of length such that the traveling time exceeds the time frame of the studied event can be represented by their surge impedance.

d) All stray capacitances of equipment made up of windings can be represented by lumped equivalents, both to earth and across the equipment.

e) Arrester characteristics shall be considered for the appropriate frequency range as given in table 5.

f) There shall be an adequate model for the earthing system, the earth connection and flashover arc.

6.8.3 DC overhead line/cable and earth electrode line

6.8.3.1 Details for slow-front and temporary overvoltages

a) DC and earth electrode lines shall be represented from d.c. up to about 20 kHz frequency range according to table 5.

b) Representation of d.c. and neutral bus arresters characteristics in the frequency range of some hundreds of Hz.

6.8.3.2 Details for fast-front and steep-front overvoltages

a) Adequate high-frequency parameters should be used for d.c. and earth electrode lines as well as buses. Also short lines can be represented by their surge impedances as long as the reflection from their far end does not intercept with the studied event. The 50 % flashover voltage levels of the line insulators are decisive for the maximum stresses.

b) DC and neutral bus arresters characteristics should be considered for the appropriate frequency range as given in table 5.

c) There shall be an adequate model for the earth connection and flashover arc.

6.8.4 DC side of HVDC converter station

6.8.4.1 Details for slow-front and temporary overvoltages

a) DC side station equipment (d.c. reactor, valves, d.c. filter and neutral bus arresters and capacitor, etc.) are represented.

b) Representation of d.c. side arresters in the frequency range of some hundreds of Hz.

c) If applicable, control and protection actions shall be considered, particularly for temporary overvoltages.

6.8.4.2 Details for fast-front and steep-front overvoltages

a) DC side equipment (d.c. reactor, d.c. filters, valves etc.), shall be represented including stray inductances and capacitances.

b) All stray capacitances of equipment made up of windings can be represented by lumped equivalents, both to earth and across equipment.

c) Arrester characteristics for the appropriate frequency range shall be indicated.

d) Control and protection actions do not need to be considered since they will not respond to these fast transients.

7 Design objectives of insulation co-ordination

Because of the essential differences between a.c. and d.c. systems leading to some deviations in the process of insulation co-ordination as discussed in 5.1, it is useful in this clause to define clearly the design objectives to be achieved as a result of following the co-ordination procedures of the subsequent clauses. This applies to some extent to the a.c. side of the HVDC converter station but to a greater extent to the d.c. side, particularly because several valve groups are normally connected in series. The valves and other equipment entirely separate from earth are therefore arranged to be protected by means of appropriate surge arresters as illustrated in figure 4.

The first design objective is thus to make a suitable choice of locations of various arresters based on all the available or assembled necessary system details discussed in 6.8 not only for the d.c. converter scheme but also for the a.c. network, the d.c. and earth electrode lines and cables (if any), and the a.c. side of the HVDC converter station. The next important design objective is to plan and conduct studies for determining surge arrester requirements in sufficient detail as illustrated in 7.1. The studies are generally, but not necessarily, based on assessment and evaluation of various transient events affecting the stresses on different arresters using the methods and tools such as those discussed in 6.7.

The main objective is the determination of the requested and specified withstand voltages to achieve the desired reliability.

The following subclauses suggest some illustrative tables suitable both for itemizing the quantities which are to be the design objectives in a clear manner and as a possible means of presenting the design results.

7.1 Arrester requirements

Table 6 suggests for each of the arresters, such as referenced on figure 4, the various requirements which should be the objectives of the insulation co-ordination design. The suggested (or similar) format on groups of arresters and individual items, should facilitate clear identification and presentation of the information.

Table 6 – Table for arrester requirements

Arrester identification – reference [a, b]	Continuous operating voltages [a]				Arrester protective levels at co-ordination currents NOTE Definitions and abbreviations for arrester protective levels are given in clauses 3 and 4, respectively. Subclause 6.5 gives general information on corresponding current impulse waveshapes.						Energy absorption
	U_c, U_{ch}	CCOV	PCOV	ECOV	SIPL		LIPL		STIPL [c]		Duty of arrester
(See figure 4)	kV (r.m.s.)	KV (crest)	KV (peak)	kV (r.m.s.)	kV (peak)	kA (peak)	kV (peak)	kA (peak)	kV (peak)	kA (peak)	kJ
I. AC section											
A			N.A.								
FA1, FA2			N.A.								
II. Converter circuit											
V1	N.A.										
V2	N.A.										
B	N.A.										
M	N.A.										
CB	N.A.										
DB	N.A.		N.A.								
III. DC section											
DL	N.A.		N.A.								
E	N.A.		N.A.								
DR											
FD1, FD2	N.A.		N.A.								
EL	N.A.		N.A.								

[a] Refer to clause 4 for abbreviations and to clause 3 for definitions.
[b] See figure 4 for arrester references in a typical modern HVDC converter station. Arresters may be added, or they may be unnecessary, depending on particular different schemes.
[c] STIPL for valve arresters.
N.A. = not applicable.

7.2 Characteristics of insulation

As in a.c. substations there are two types of insulation used in HVDC converter stations, self-restoring, which applies to air, and non self-restoring which applies to e.g. oil and paper. However, gases that may be used can fall under both types of insulation. In d.c. applications the composite effect of d.c., a.c. and impulse (also polarity reversal) voltages on the characteristics of the insulation shall be considered. The characteristics of the individual insulation is outside the scope of this standard.

7.3 Representative overvoltages

The representative overvoltage as defined in IEC 60071-1 is equal to the maximum overvoltage of each class of overvoltages determined from these examinations. This general concept applies to both a.c. and d.c. systems, but a particular application of this concept for d.c. systems is to consider that representative overvoltages are equal to protection levels of arresters for directly protected equipment.

7.3.1 Influence of arrester arrangement and insulation configuration

7.3.1.1 Insulation directly protected by a single arrester

The maximum overvoltage between points directly protected by their own single arresters (for example valve arrester V across points 5 to 9 in figure 4) is determined from the arrester characteristic together with the co-ordination current through the arrester.

7.3.1.2 Insulation protected by more than one arrester in series

For insulation not directly protected by a single arrester, the protection can be achieved by a number of arresters connected in series as shown in table 7. In this case, the maximum voltages, corresponding to the arrester currents for each single arrester during this event, are added to give a total maximum overvoltage between the points in question.

7.3.1.3 The valve side neutral point of transformers

For slow-front overvoltages and temporary overvoltages, the maximum voltage in the neutral is the same as the phase to earth voltage on the corresponding a.c. phase as determined in table 7.

7.3.1.4 Insulation between phase conductors on the line side and the valve side of the converter transformer

Slow-front overvoltages can occur between the line and valve side phases of the converter transformers, stressing the air clearance between conductors in the switchyard. Usually, this is not a problem for the lower system voltages, but in the case of high a.c. system voltages and a number of series connected valve bridges, the maximum voltage shall be evaluated and air clearances between conductors in the switchyard designed accordingly.

The inter-winding voltages may stress different points inside the converter transformer depending on its construction (two- or three-winding, single- or three-phase transformer).

7.3.1.5 Summary table

Table 7 is an example based on figure 4. In real life such a table should be established in light of the specific design.

Table 7 – Arrester protection of d.c. side of an HVDC converter station

Protected item	Arrester protection identification	Comments
Between terminals of a valve	Valve arrester (V)	
Between terminals of a converter	(1) Converter unit arrester (C) (2) Mid-point d.c. bus arrester (M) and neutral bus arrester (E)	For lower converter Different alternatives are possible
Mid-point d.c. bus	Mid-point d.c. bus arrester (M)	
DC bus, valve side of d.c. reactor	(1) DC bus arrester (CB) (2) Converter unit arrester (C) and mid-point d.c. bus arrester (M)	(1) May give lower protective level. (2) May give lower arrester stresses
Neutral bus	Neutral bus arrester (E)	
DC bus line side of reactor	DC line arrester (DL)	
Between terminals of d.c. reactor	DC reactor arrester (DR)	May be omitted
Valve side a.c. phase to earth		
Lower transformer – lower converter	Valve arrester (V) and neutral bus arrester (E)	
Upper transformer – lower converter	(1) Two valves arrester (2 V) and neutral arrester (E). (2) Mid-point arrester (M)	(1) With deblocked converter. (2) With blocked converter
Lower transformer – upper converter	Mid-point arrester (M) and valve arrester (V)	
Upper transformer – upper converter	(1) Mid-point arrester (M) and two valve arresters (2 V) (2) DC bus arrester (DB)	(1) With deblocked converter. (2) With blocked converter

7.3.2 Representative overvoltages gathering

The representative overvoltages, which may be presented as in table 8, are determined by considering relevant faults and examining the results of the calculation to find out the representative type of overvoltage, i.e. slow-front, fast-front or steep-front. Once the type of overvoltage has been determined, the peak value of the waveform chosen may be adjusted to take into consideration the duration and shape of the overvoltage as per IEC 60071-2, clause 2. This adjustment can be considered to be taken into account when applying factors to the protective levels of arresters as per 7.4.

Table 8 – Table gathering representative overvoltage levels and required withstand voltage levels

Insulation location Between terminal and earth, unless stated as from one terminal to another terminal. Refer to figures 4 and 7, and to table 7 for illustrations and references	Representative overvoltage levels for appropriate type of surge			Required withstand voltage levels (U_{rw} as per IEC 60071-1)		
	SIPL RSLO	LIPL RFAO	STIPL [a] RSTO [a]	Switching	Lightning	Steep front
	kV	kV	kV	kV	kV	kV
I AC switchyard section						
AC busbars and conventional equipment, 1						
Filter capacitors (a) HV side, 1-2 (b) LV or neutral side, 3						
Filter reactors (a) HV side, 2 (b) LV or neutral side, 3 (c) across the reactor, 2-3, 3						
II Converter indoor equipment						
Across a valve, 5-9, 7-5, 6-7, 6-8						
Across lower valve group, 7-8						
Across upper valve group, 9-7						
One phase valve to another phase valve, 5 ph-ph and 6 ph-ph						
Mid-point to earth, 7						
Each converter unit HV side, 9						
Each converter unit LV side, 8						
HVDC bus (indoor), 9						
DC neutral bus, 8						
III DC side equipment						
Across d.c. reactor, 10-9						
Filter capacitors (a) HV side, 10-11 (b) LV or neutral side, 12-8						
Filter reactors (a) HV side, 11 (b) LV or neutral side, 12 (c) across the reactor, 11-12, 12-8						
DC bus (outdoor), 10						
DC line, 10						
Earth electrode line, 8						
IV Other equipment such as transformer, valve, windings (e.g. in oil)						
Star winding (a) phase-to-neutral, 5-n (b) phase to another phase, 5 ph-ph (c) neutral to earth, *n* (d) phase-to-earth, 5						
Delta winding (a) phase-to-earth, 6 (b) phase-to-phase, 6 ph-ph						
Star-winding to delta winding, 5-6						

[a] STIPL and RSTO for valve arresters.

7.4 Determination of the required withstand voltage

As with a.c. systems, equipment is classified into equipment with self-restoring and non-self-restoring insulation according to IEC 60071-1. Self-restoring insulation consists primarily of air gaps and porcelain external insulation while non self-restoring insulation consists primarily of oil and cellulose dielectric materials as used in converters and reactors. Under certain circumstances the thyristor valve is self-restoring. Redundant thyristor levels are provided to maintain the required withstand voltage even in the event of random failures of thyristor levels within the valve between maintenance periods.

Arresters are used to protect equipment insulation as in a.c. applications; however, the arresters are not necessarily directly connected to earth, but are also connected directly across equipment elevated from earth potential. For thyristor valves the arresters are located close to the valve in order to eliminate distance effects.

The essential difference compared with a.c. applications is that in HVDC applications the insulation is stressed by composite a.c., d.c. and impulse voltages. Composite voltages require consideration of both resistive and capacitive voltage distribution and may result in high-voltage stresses. These high-voltage stresses are, however, taken into account in the design and testing of the equipment.

The withstand voltages for switching, lightning and steep-front are determined by multiplying the corresponding maximum overvoltages with a relevant adequate factor. Based upon the withstand voltages, the test voltages for each equipment are determined according to respective equipment standards. In a.c. practice, standard voltage levels are used for equipment withstand voltages. However, in the case of d.c. applications, there are no standardized withstand voltage levels.

The insulation co-ordination procedure recommended in IEC 60071-1 implies the application of a co-ordination factor (K_c) to the representative overvoltages (U_{rp}) to obtain the co-ordination withstand voltages (U_{cw}), which means: $U_{cw} = K_c \times U_{rp}$ (refer to 4.3 of IEC 60071-1) For equipment on the d.c. side, the deterministic method (refer to 3.3 of IEC 60071-2) is actually used so that for such equipment this is the deterministic co-ordination factor K_{cd} (refer to 3.3.2.1 of IEC 60071-2) which is used instead of K_c. The co-ordination factor K_{cd} applied to the representative overvoltages includes:

- allowance for limitations in modeling and in data for calculating the overvoltages, and for the co-ordination currents taking into account the strong non-linearity of the arrester characteristics;
- allowance for shape and duration of overvoltages.

Referring to figure 1 of IEC 60071-1, the required withstand voltages U_{rw} are obtained through a further step of insulation co-ordination procedure which consists in applying to the co-ordination withstand voltage the atmospheric correction factor K_a for external insulation, and a safety factor K_s whose value depends on the type of insulation, internal or external. The safety factor K_s includes:

- allowance for ageing of insulation;
- allowance for changes in arrester characteristics;
- allowance for dispersion in the product quality.

For HVDC converter stations, the deterministic method is applied and, for altitudes up to 1 000 m, experience has shown that the required withstand voltages of equipment can be obtained by applying a factor to the corresponding protective level of the arrester. Such a factor includes all the preceding ones discussed at the beginning of this clause. Table 9 provides a set of indicative values for this factor which may be used as design objectives if not specified by the user or the relevant apparatus committees. In table 9, all equipment is considered to be directly protected by an arrester. If this is not the case, e.g. for some of the equipment on the a.c. side, distance effect for fast and very-fast transients shall be taken into account and indicative ratios should be raised in consequence (refer to IEC 60071-1 and IEC 60071-2: co-ordination factor and co-ordination withstand voltages).

Table 9 – Indicative values of ratios of required impulse withstand voltage to impulse protective level

Type of equipment	Indicative values of ratios of required impulse withstand voltage/Impulse protective level [a, c]		
	RSIWV/SIPL	RLIWV/LIPL	RSFIWV/STIPL [b]
AC switchyard – busbars, outdoor insulators, and other conventional equipment	1,20	1,25	1,25
AC filter components	1,15	1,25	1,25
Transformers (in oil) Line side Valve side	 1,20 1,15	 1,25 1,20	 1,25 1,25
Converter valves	1,15	1,15	1,20
DC valve hall equipment	1,15	1,15	1,25
DC switchyard equipment (outdoor) (including d.c. filters etc and d.c. reactor)	1,15	1,20	1,25

[a] Indicated values are stated for general design objectives only. Appropriate final ratios (higher or lower) can be selected according to the chosen performance criteria.

[b] STIPL for valve arresters.

[c] Indicative ratios are on the basis that any equipment is directly protected with surge arrester.

7.5 Determination of the specified withstand voltage

The specified withstand voltages are values equal to or higher than required withstand voltages. For a.c. equipment, the specified withstand voltages correspond to standard values as stated in IEC 60071-1. For HVDC equipment, there are no standardized withstand voltage values and the specified withstand voltages are rounded up to convenient practical values.

7.6 Creepage distances

For insulation locations, where applicable, the design objective is to determine and assign the minimum creepage distances using the considerations described in clause 8, generally based on the continuous operating voltages (a.c. or d.c.).

7.7 Clearances in air

For all insulation locations in air (outdoor and indoor), it is necessary to determine the minimum clearance distance in air using the considerations described in clause 8, generally based on the required switching impulse withstand voltage.

8 Creepage distances and clearances in air

The creepage distance on the insulators is one of the factors that dictates the performance of external insulations at continuous operating voltages (a.c. or d.c.). Contamination on the insulators reduces their ability to support the operating voltages, particularly during wet conditions. When wet weather conditions concentrate the pollution on some parts of the surface of the insulators, the non uniform distribution of pollution and increase in leakage current creates dry zones resulting in uneven voltage stresses and this can initiate the process of flashover. Rain, snow, dew or fog are some of the weather conditions that can initiate this process. The withstand capability of contaminated insulators is also affected by other factors such as the shed profile, the orientation angle and the diameter of the insulators. In the case of bushings, d.c. current measuring devices, d.c. voltage dividers and other similar equipment the internal construction of the core impacts on both the internal and external voltage distribution.

All these factors should be considered in determining the type and shape of the insulators suitable for the applications.

There have been cases of bushing flashover on various operating d.c. schemes where contamination deposits have been lightly wetted by dew, fog or rain. In addition, flashovers have occurred due to unequal wetting of external insulators, such as horizontally mounted bushings, although this phenomenon is independent of the creepage distance.

The base voltage used together with the specific creepage distance is as follows:

- for the insulation on the a.c. side of the converter (a.c. equipment): the highest value of operating voltage expressed as the r.m.s. voltage phase-to-phase (IEC 60815);
- for the insulation on the d.c. side of the converter (d.c. equipment): the d.c. system voltage as defined in 3.1 for the insulation to earth, or a corresponding average value of the voltage across the insulation for insulations between two energized parts.

8.1 Creepage distance for outdoor insulation under d.c. voltage

The trend in the industry for several years has been to use larger specific creepage distances in HVDC applications. For example, creepage distances as high as 60 mm/kV have been used in HVDC systems. However, such an increase in the specific creepage distance did not eliminate the external flashovers. It should be emphasized that for d.c. system voltages of 500 kV, an increase in the outdoor specific creepage distance did not eliminate the external flashovers due to pollution or unequal wetting.

NOTE Because of the different base voltages used in the determination of the creepage distance (refer to the end of clause 7), for approximately the same stress applied to phase-to-earth insulation, a specific creepage distance of 60 mm/kV in a d.c. system corresponds to about 35 mm/kV in an a.c. system.

Several mitigation techniques have been used on existing HVDC systems to solve both problems. The application of grease or room temperature vulcanized rubber (RTV) on the surface of the insulators has been successful in avoiding flashovers. The frequency of reapplying the grease coating will depend on the pollution conditions at the site. Frequencies of 18 months to 3 years between re-applications has been quoted in the industry. The application of booster sheds has also been successful in avoiding flashovers.

Recently, the use of composite housings for bushings and other devices has been successful in solving the flashovers in HVDC stations, even those with smaller specific creepage distances.

8.2 Creepage distance for indoor insulation under d.c. voltage

For an indoor clean environment, a minimum specific creepage distance of about 14 mm/kV (based on the appropriate d.c. voltage) has been widely used and has not experienced any flashover. The creepage path, in any case, may not be an especially suitable parameter to define the converter valve internal insulation and the arcing distance may be more appropriate.

8.3 Creepage distance of a.c. insulators (external)

For standardization purposes, four qualitative levels of pollution are described in IEC 60071-2, table 1, and IEC 60815 specifies corresponding pollution test severities and minimum specific creepage distances for overhead line insulators in a.c. systems. Insulators shall withstand the pollution level at the highest voltage system operation. The co-ordination withstand voltages are taken equal to the maximum voltage of the system (U_s) and the minimum recommended creepage distances are defined in terms of mm per kV (phase-phase). Typically the range is between 16 mm to 31 mm/kV.

8.4 Clearances in air

Details concerning required clearances in air to assure a specified impulse voltage insulation for a.c. applications are presented in IEC 60071-2, while annex A of this standard gives the correlations between impulse withstand voltages and minimum air clearances. In HVDC applications the presence of composite a.c., d.c. and impulse voltages shall be considered [7].

Depending upon then d.c. voltage level, the switching criterion, rather than lightning, is considered to be the governing factor in determination of air-gap requirements. Typically for a given gap spacing, the positive lightning impulse breakdown voltage will be at least 30 % higher than the positive switching impulse breakdown voltage.

For both d.c. and impulse voltages the positive polarity has lower withstand voltage than the negative polarity. The result of tests with switching impulse alone, of magnitude equal to the total voltage, can generally be used for composite slow-front and d.c. voltages. With appropriate corrections for earth electrode shape, this will give conservative values for conditions of positive slow-front voltage superimposed on positive polarity d.c. voltage for HVDC converter station clearances which are selected relative to surge arrester protective levels. This applies particularly to practical gaps behaving in similar fashion to rod-plane gaps.

9 Arrester requirements

9.1 Arrester specification

The residual voltage of an arrester is the peak voltage that appears between the terminals of an arrester during passage of a discharge current. The arrester currents for which the maximum residual voltages are specified are called the co-ordination currents as illustrated in table 6.

The values of co-ordination currents are determined by system studies, usually carried out by the supplier. The process involves taking into account the energy duty in arresters, the number of columns of arrester in parallel and the peak current in each arrester which depends on the number of arresters in parallel. The final choice for peak current in the arresters is the co-ordination current for which the corresponding residual voltage leads to the representative overvoltage for directly protected equipment. What is looked for is the “best balance” between overall arrester specifications and design and HVDC converter equipment voltage withstand requirements and design, this process resting on the choice of co-ordination currents. For arrester testing purposes and protection levels assessment, standard shapes defined in IEC 60099-4 for switching, lightning and steep current impulse are applied to the co-ordination currents.

For the sections of the HVDC converter station exposed to atmospheric overvoltages, the determination of the arrester co-ordination current for lightning stresses shall consider the design of the station shielding (particularly for outdoor valves). The maximum current at shielding failure may be determined, for example, according to [11] or [14].

Arrester discharge currents during contingencies may be of various durations. In specifying the arrester energy capability, consideration shall be given to both the amplitude and duration of the discharges, including repetitive stresses due to the relevant operating sequence. Repetitive current impulses occurring over several cycles of fundamental frequency are considered as one single discharge, having an equivalent energy content and duration as the accumulated values of the actual energy impulses, and taking into account current amplitudes and durations of the combined impulses. From a stability point of view, repetitive current impulses shall be considered over a longer period of time. When determining the equivalent energy, it shall also be taken into account that the energy withstand capability of metal-oxide arresters is reduced with shorter pulse duration [4].

In specifying the arrester capability, the calculated arrester energy value from the studies should consider a reasonable safety factor. This safety factor is in the range of 0 % to 20 %, depending on allowances for tolerances in the input data, the model used, and the probability of the decisive fault sequence giving higher stresses than the cases which have been studied. The life time of an arrester depends on three factors:

a) peak current of the surge;
b) pulse width;
c) pulse cycle.

9.2 AC bus arrester (A)

The a.c. side of an HVDC converter station is protected by arresters at the converter transformers and at other locations depending on the station configuration (see for example figure 4). These arresters are designed according to the criteria for a.c. applications and they limit the overvoltages on both the line side and the valve side of the converter transformers, taking into account the slow-front overvoltages transferred from the line side to the valve side of the transformers. The arresters are designed for the worst case of fault clearing followed by the recovery, including transformer saturation overvoltages and overvoltages due to load rejection, as well as possible restrike of circuit breakers during their opening.

9.3 AC filter arrester (FA)

The continuous operating voltage of the a.c. filter arrester consists of a power frequency voltage with superimposed harmonic voltages corresponding to the resonance frequencies of the filter branch. The ratings of these arresters are normally determined by the transient events. Since the harmonic voltages result in relatively higher power losses, this shall be considered at the rating of arresters.

The events to be considered with respect to filter arrester duties are slow-front plus temporary overvoltages on the a.c. bus and discharge of the filter capacitors during earth faults on the filter bus. The former determines the required SIPL and the latter the LIPL and the energy discharge requirement. In certain cases, high energy discharge duties may also result from conditions of low order harmonic resonance, or due to low order non-characteristic harmonics generated by unbalanced operation during a.c. systems faults.

9.4 Valve arrester (V)

9.4.1 Continuous operating voltage

The valve arrester continuous operating voltage consists of sine wave sections with commutation overshoots and notches as shown in figure 6. Disregarding the commutation overshoots, the crest value of the continuous operating voltage (CCOV) is proportional to U_{dim} and, as per 6.3, it is given by:

$$\text{CCOV} = \frac{\pi}{3} \times U_{\text{dim}} = \sqrt{2} \times U_{\text{v0}}$$

The peak continuous operating voltage (PCOV), which includes the commutation overshoot shall be considered when the reference voltage of the arrester is determined. The commutation overshoot is dependent on the firing angle α and accordingly special attention shall be given to operation with large firing angles.

9.4.2 Temporary and slow-front overvoltages

The maximum temporary overvoltages are transferred from the a.c. side, normally, during fault clearances combined with load rejections close to the HVDC converter station. However, it shall be noted that only contingencies without blocking or with partial blocking of the converters need be considered, since the valve arresters are relieved from stress when the valve is blocked and the by-pass pair is extinguished.

The events producing significant valve arrester currents of switching character are as follows:

a) earth fault between the converter transformer and the valve in the commutating group at highest potential;

b) clearing of an a.c. fault close to the HVDC converter station;

c) current extinction in only one commutating group (if applicable).

A phase to earth fault on the valve side of the converter transformer of the bridge at the highest d.c. potential will give significant stresses on the valve arresters in the upper commutation group. The discharges through the arresters are composed in principle of two current peaks. Firstly, the stray and the damping capacitances of the converter are discharged giving steep-front surge stresses on the valve connected to the faulty phase (see 9.4.3). Secondly, the d.c. pole and line/cable capacitances are discharged through the d.c. reactor and the transformer leakage reactance giving a slow-front overvoltage type, approximately 1 ms to crest. This latter discharge might expose one of the arresters connected to the other phases with the highest current and energy. The parameters such as the d.c. voltage at the fault instant, d.c. reactor inductance, transformer leakage inductance and line/cable parameters determine which of the three upper arresters will be the most stressed and the magnitude of these stresses. For d.c. schemes having parallel connected converters, this phase to earth fault case implies additional stresses since the unfaulted converter will continue to feed current into the earth fault for some time before the protection trips the converters. Depending on current rating, control system dynamics, inductance of the d.c. reactor, and the protection scheme, this phase to earth fault case may be dimensioning for the energy and current rating of the arresters across the upper three valves.

In the above phase to earth fault case, the calculated stresses are highly dependent on the value of the d.c. bus voltage. It is recommended using the maximum d.c. voltage that can last for a number of seconds. It should be noted that this case may lead to an arrester with very high energy discharge capability. The final decision should consider the probability for the occurrence of voltages higher than the maximum operating voltage in combination with an earth fault.

At fault clearing in the a.c. network, excessive overvoltages on the a.c. side arise only if the converters are blocked. If the converters continue to operate after the fault, this will damp out the overvoltages and the total discharge energy will be much smaller. Often the case that gives the maximum arrester energy is when the converter is permanently blocked with by-pass pairs. The blocking might imply that the converter transformer breakers are opened a few cycles later. If this is the case, the arresters are not exposed to any operating voltage after the fault is cleared. A realistic tap changer position for a relevant load flow shall be used when the transferred overvoltages from the line side are calculated. Unfavourable system conditions can result in ferroresonance between the a.c. filter/shunt capacitor and the converter transformer together with the a.c. network impedance. The fault inception and the instant of fault clearance instants should be varied in order to cover the variations in transformer saturation.

A current extinction in all three valves of one commutating group, while the valves in the commutating groups in series still conduct current, might be decisive for the arrester energy rating. The current is then forced to commutate to one of the arresters connected in parallel with the non-conducting valves. The energy dissipated in this arrester can be substantial if the current is not quickly reduced to zero.

Possible contingencies which may result in current extinction in the valves in only one commutating group include:

- firing failure in a valve, e.g. due to a failure in the valve control unit;
- blocking of all the valves in a converter without a deblocking of the by-pass pairs. This contingency may give a converter current close to zero, during some transient conditions such that the current is only extinguished in one of the commutating groups connected in series. This case is often most stringent during inverter operation.

If current extinction is considered inconceivable then this event is excluded. Whether the current extinction is conceivable or not depends very much on the degree of redundancy and type of control/protection system.

9.4.3 Fast-front and steep-front overvoltages

The valves and the valve arresters within the converter area are separated from the a.c. switchyard and the d.c. switchyard by large series reactances, i.e. the converter transformers and the smoothing reactors. Traveling waves, caused by lightning strokes on the a.c. side of the transformers or on the d.c. line outside of the smoothing reactor, are attenuated by the combination of series reactances and earth capacitances to a smaller magnitude or a shape similar to slow-front overvoltages. However, in the case of large transformer ratios (e.g. back-to-back stations) the capacitive coupling is more predominant and may need consideration. The valve and valve arresters can in general only be subject to fast-front and steep-fronted overvoltages at back-flashovers and earth faults within the converter area. Direct lightning strokes shall be considered only if the lightning passes the shielding system. Direct strokes and back-flashovers can often be excluded in high-voltage HVDC converter stations with adequate shielding and earthing systems.

The most critical case for steep-front overvoltages is normally an earth fault on the valve side of the converter transformer of the bridge with the highest d.c. potential. The circuit is modeled in detail with its stray capacitances and bus inductances represented for the estimation of this case.

A contingency to be recognized in the design of the thyristor valve is when the valve is stressed by a forward overvoltage and the valve is fired during the overvoltage resulting in the immediate commutation of the arrester current from the arrester to the valve. It should be stressed that the arrester current to be considered for this commutation is not necessarily the specified co-ordination current for the valve arrester, which normally refers to an overvoltage in the reversed direction. For an overvoltage in the forward direction, it is adequate to assume a co-ordination current of switching character corresponding to the protective firing level across the valve. However, the tolerances in the arrester characteristics and redundant thyristors may be considered when the arrester current is estimated. If the protective firing level is chosen above SIPL of the valve arrester, an arrester current corresponding the overvoltage level for selection of protective firing level as described in 9.4.4 can be used to define a realistic current for this case.

9.4.4 Valve protective firing (PF)

Protective firing may limit the forward overvoltage across the valve by triggering the thyristors. The level of the protective firing shall be co-ordinated with the overvoltages during different operating conditions. When the level of the protective firing is greater than the protective level of the valve arresters, this should be specified.

Possible adverse effects of the protective firing on the transmission performance need only be considered during external faults when the pole remains in operation and then, in particular, during inverter operation.

Protective firing in rectifier operation during transients in the a.c. network does not give rise to any significant disturbance of the link. On the other hand, if a valve is fired earlier due to a protective firing during inverter operation, the result could be a commutation failure and the recovery time for the transmission after a fault clearing may be increased. In order not to affect the recovery of the link, the protective firing should not be activated during the highest overvoltage that may occur without permanent blocking of the converter acting as inverter.

9.5 Bridge arrester (B)

A bridge arrester may be connected between the d.c. terminals of a six-pulse bridge.

The maximum operating voltage will be the same as for the above-mentioned valve arrester (9.4). The following events may produce arrester currents of switching character:

a) clearing of an a.c. fault close to the HVDC converter station;

b) current extinction in the corresponding six-pulse bridge (if applicable, see 9.4.2).

The switching overvoltages transferred from the a.c. side normally results in low arrester currents since the bridge arrester is then connected in parallel with a valve arrester.

9.6 Converter unit arrester (C)

A converter unit arrester may be connected between the d.c. terminals of a 12-pulse bridge, arrester (C) in figure 4.

The maximum operating voltage is composed of the maximum direct voltage from one converter unit plus the 12-pulse ripple. The voltage CCOV, excluding commutation overshoots, can normally be estimated as:

$$\text{CCOV} = 2 \times U_{\text{dim}} \times \frac{\pi}{3} \times \cos^2(15°)$$

The theoretical maximum operating voltage for small values of the firing and overlap angle is given by the following expression:

$$\text{CCOV} = 2 \times \cos(15°) \times \frac{\pi}{3} \times U_{\text{dim}}$$

The commutation overshoots should be considered in the same way as for the valve arrester when the arrester is specified.

The converter unit arresters are normally not exposed to high discharge currents of switching character. For series connected converters, the closure of a by-pass switch during operation will stress this arrester. The arrester may limit overvoltages due to lightning stresses propagating into the valve area, although these stresses are not decisive for the arrester.

9.7 Mid-point d.c. bus arrester (M)

A mid-point d.c. bus arrester is sometimes used to reduce the insulation on the valve side of converter transformers. The mid-point arrester may be connected across a six-pulse or a 12-pulse bridge in the case of series connected converters (arrester (M) in figure 1).

The operating voltage is similar to that for the bridge arrester or the converter unit arrester with the addition of the voltage drop in the earth electrode line.

An event producing significant arrester stresses of switching character, when applicable (see 9.4.2 above), is current extinction in the lower six-pulse bridge. Also, operation of bypass switches will give rise to stresses, in the case of series connected converter units. Lightning stresses may result from shielding failures.

9.8 Converter unit d.c. bus arrester (CB)

A converter unit d.c. bus arrester may be connected between the bus and earth, arrester (CB) in figure 4.

The operating voltage is similar to that for the converter unit arrester with the addition of the voltage drop in the earth electrode line.

Due to the high protective level, the arrester will normally not be exposed to high discharge currents from slow-front overvoltages. Lightning stresses of moderate amplitude may result from shielding failures.

9.9 DC bus and d.c. line/cable arrester (DB and DL)

The maximum operating voltage is almost a pure d.c. voltage with a magnitude dependent on the converter and tap-changer control and possible measurement errors.

These arresters are mainly subjected to lightning stresses. Critical slow-front overvoltages can often be avoided by suitable selection of the parameters in the main circuit, thus avoiding critical resonances. A pole to earth fault in one pole of a bipolar overhead d.c. line will produce an induced overvoltage on the healthy pole. The magnitude of these overvoltages is dependent on the location of the fault, the line length and the termination impedance of the line. Normally, these types of overvoltages are not critical for the insulation of the terminals.

When the HVDC line comprises overhead line sections as well as cable sections, consideration should be given to the application of surge arresters at the cable-overhead line junction to prevent excessive overvoltages on the cable due to reflection of traveling waves. At HVDC links with very long cables, the energy rating of the cable arresters is decided by the discharge of the cable from the highest voltage it may attain during a contingency. This normally results in comparably low discharge currents. Contingencies to be considered are valve misfire and complete loss of firing pulses in one of the stations. The lightning stresses on the arresters are in this case reduced by the low surge-impedance of the cable.

9.10 Neutral bus arrester (E)

The operating voltage of the neutral bus arrester is normally low. At balanced bipolar operation it will be practically zero. During monopolar operation it will consist mainly of a small d.c. voltage corresponding to the voltage drop in the earth electrode line or the metallic return conductor.

These arresters are provided to protect equipment from fast-front overvoltages entering the neutral bus and to discharge large energies during the following contingencies:

a) earth fault on the d.c. bus;

b) earth fault between the valves and the converter transformer;

c) loss of return path during monopolar operation.

An earth fault on the d.c. bus will cause the d.c. filter to discharge through the neutral bus arrester, giving a very high but short current peak. The most essential assumption is the pre-fault voltage of the filter which normally is chosen as the maximum operating d.c. voltage. The fast discharge of the d.c. filter is followed by a slower fault current from the converter. The rate of rise is mainly limited by the d.c. reactor. The fault current will be shared between the earth electrode line and the neutral bus arrester. In the case of metallic return operation, the impedance in parallel with the arrester is the entire d.c. line impedance.

At an earth fault on a phase between the valve and the converter transformer, the a.c. driving voltage will be shared between the converter transformer impedance and the earth electrode line impedance. The decisive case can be found for the terminal which has the longest earth electrode line and, in the case of metallic return operation, in the unearthed terminal. The worst case occurs when the station is operating as rectifier, because of the polarity of the driving voltage.

Metallic return operation usually gives such high requirements on the neutral bus arrester, that it becomes advantageous to select a higher arrester rating in the unearthed station than in the station that is earthed during metallic return operation. This is also applicable for long electrode lines (normally for distances above 50 km).

Neutral bus capacitors have been included in recent schemes, mainly due to harmonic filtering requirements and due to suppression of overvoltages on the neutral bus, although they will influence the neutral bus arrester stresses and shall be included in the study model. The stresses on the neutral bus arrester will also depend on the converter control and protective actions taken during the fault. When the energy rating results in an excessive design a sacrificial arrester may be used. In particular, this is the preferred design when the replacement of the arrester does not significantly influence the outage time. In bipolar systems sacrificial arresters shall be located so that bipolar outages are avoided.

9.11 DC reactor arrester (DR)

The operating voltage of the d.c. reactor arrester consists only of a small 12-pulse ripple voltage from the converter. The arrester will be subjected to lightning overvoltages of opposite polarity to the converter d.c. bus operating voltage (which may be termed subtractive lightning impulses). The possibility of lightning stresses being coupled through the arrester to the thyristor bridge shall be considered.

In many schemes the d.c. reactor arrester can be dispensed with when the reactor insulation level meets the voltage requirement from the d.c. line arrester combined with the maximum operating voltage of opposite polarity.

9.12 DC filter arrester (FD)

The normal operating voltage of the d.c. filter reactor arrester is low and usually consists of one or more harmonic voltages corresponding to the resonance frequency of the filter branch in question. Since the harmonic voltages result in relatively higher power losses this shall be considered at the rating of arresters.

Arrester duties are mainly determined by filter capacitor discharge transients resulting from earth faults on the d.c. pole.

9.13 Earth electrode station arrester

The equipment at the earth electrode station, for example distribution switches, cables and measuring equipment, requires protection from overvoltages entering via the earth electrode line. An arrester is normally placed at the line entrance. The continuous operating voltage is insignificant. The arrester is dimensioned for lightning stresses entering via the overhead line. The stresses on the arrester at the earth electrode station during unsymmetrical faults and commutation failures may need to be considered for short earth electrode lines.

Annex A
(informative)

Example of insulation co-ordination for conventional HVDC converters

List of contents

A.1 Introductory remarks

This annex gives a description and method of calculation for the insulation co-ordination of a conventional HVDC converter station with a d.c. cable with ground return. This example is intended to be informative and tutorial and is very schematic. It mainly summarizes steps leading to chosen arrester ratings and specified insulation levels, based on procedures explained in the main text.

The results presented in this annex are based on the study approach and described procedures in 6.7.1 as well as in clause 9. Because there are no standard withstand levels for HVDC, calculated values for SSIWV, SLIWV and SSFIWV are rounded up to convenient practical values.

A.2 Arrester protective scheme

Figure A.1 shows the arrester protective schemes for the HVDC converter station. All arresters are of the metal-oxide type without gap.

A.3 Determination of arrester stresses, protection and insulation levels

The following main data are used for the basic design of the HVDC converter station:

AC side: strong a.c. system

DC side:

DC voltage	KV	500	(rectifier)
DC current	A	1500	
Smoothing reactor	MH	225	
Firing angles	Deg	15/17	(rectifier/inverter)

Converter transformer

Rating (three-phase, six-pulse)	MVA	459
Short circuit impedance	Pu	0,12
Sec. voltage (valve side)	kV r.m.s.	204
Tap-changer range		±5 %
Inductance per phase (valve side)	MH	35

AC bus arrester (A)

The following data are given for the HVDC converters:

Parameters		Bus 1 (A)
Nominal system voltage	kV_{rms}	400
Highest system voltage (U_s)	kV_{rms}	420
Continuous operating voltage, phase-to-earth	kV_{rms}	243
SIPL (at 1,5 kA)	kV	632
LIPL (at 10 kA)	kV	713
Maximum slow-front overvoltage transferred to valve side (between two phases)	kV	549
Number of parallel arrester columns	–	2
Arrester energy capability	MJ	3,2

Valve arrester type (V1) and (V2)

The following values are valid for both converter stations:

CCOV	kV	208 × √2	
Number of parallel columns		8	for arrester (V1)
		2	for arrester (V2)
Energy capability	MJ	16,2	for arrester (V1)
	MJ	2,6	for arrester (V2)

The stresses of the valve arresters are determined by computer studies for the following cases:

A.3.1 Transferred slow-front overvoltages from the a.c. side

The highest stresses are expected if the transferred slow-front overvoltage appears between the phases (e.g. R and S), where only one valve is conducting (figure A.2). The value of the transferred slow-front overvoltage is dependent on the maximum protective level of the a.c. bus arrester (A) on the primary side of the converter transformer.

Figure A.3 show the results for the HVDC converters if only one arrester in the circuit is conducting. This fault case is decisive for the design of all lower valve arresters type (V2).

Results (valid for valve arrester (V2)):

The switching impulse protective level (SIPL) of the valve arrester (V2) is given by

SIPL = 500 kV at 1 027 A (see A.3)

RSIWV = 1,15 × 500 kV = 575 kV => **SSIWV = 575 kV**

A.3.2 Earth fault between valve and HV bushing of converter transformer

This fault case gives the highest stresses for the valve arresters protecting the three-pulse commutating group on the highest potential. The equivalent circuit for this case is shown in figure A.4. The stresses for the upper valve arresters are also dependent on the fault insertion time. To determine the maximum values, the fault insertion time is varied from zero to 360 electrical degrees.

The results of the maximum stresses are shown in figure A.5.

This fault case is decisive for the design of all upper valve arresters (V1) if the slow-front overvoltage (case a) does not result in higher arrester stresses.

Results (valid for valve arrester (V1)):

The switching impulse protective level (SIPL) of the valve arrester (V1) is given by

SIPL	=	499,8 kV	at 4 230 A (see figure A.5)			
RSIWV	=	1,15 × 499,8 kV	=	575 kV	=>	SSIWV = 575 kV

Converter group arrester (C)

The following values are valid for both converter stations:

CCOV:	558 kV
Number of parallel columns:	1
Energy capability:	2,5 MJ

The stresses of the group arresters are determined by computer studies transferred slow-front overvoltages from the a.c. side. The magnitude of the transferred slow-front overvoltage voltage is twice the value given for the valve arresters. It is assumed that during normal operation, when four thyristor valves are conducting, a slow-front overvoltage will be transferred between the phases.

For the design of the converter group arrester (C) the following values for the co-ordination currents are chosen:

SIPL	=	930 kV	at 0,5 kA			
LIPL	=	1 048 kV	at 2,5 kA			
RSIWV	=	1,15 × 930 kV	=	1 070 kV	=>	SSIWV = 1 175 kV
RLIWV	=	1,20 × 1 048 kV	=	1 258 kV	=>	SLIWV = 1 300 kV

DC bus arrester (DB)

The following values are valid for both converter stations:

CCOV:	515 kV
Number of parallel columns:	1
Energy capability:	2,2 MJ

For the design of the d.c. bus arrester (DB) the following values for the co-ordination currents are chosen:

SIPL	=	866 kV	at 1 kA			
LIPL	=	977 kV	at 5 kA			
RSIWV	=	1,15 × 866 kV	=	996 kV		SSIWV = 1 050 kV
RLIWV	=	1,2 × 977 kV	=	1 173 kV	=>	SLIWV = 1 300 kV

DC line/cable arrester (DL)

The following values are valid for both ends of the d.c. line/cable arrester (DL):

CCOV:	515 kV
Number of parallel columns:	8
Energy capability:	17,0 MJ

For the design of the d.c. line/cable arresters (DL) the following values for the co-ordination currents are chosen:

SIPL	=	807 kV	at 1 kA			
LIPL	=	872 kV	at 5 kA			
RSIWV	=	1,15 × 807 kV	=	928 kV	=>	SSIWV = 950 kV
RLIWV	=	1,20 × 872 kV	=	1 046 kV	=>	SLIWV = 1 050 kV

Neutral bus arrester (E)

The following values are valid for both converter stations comprising all neutral bus arresters:

CCOV:	30 kV
Number of parallel columns:	12
Energy capability:	2,4 MJ

For the design of all neutral bus arresters (E) the following values for the co-ordination currents are chosen:

SIPL	=	78 kV	at 2 kA			
LIPL	=	88 kV	at 10 kA			
RSIWV	=	1,15 × 78 kV	=	90 kV	=>	SSIWV = 125 kV
RLIWV	=	1,20 × 88 kV	=	106 kV	=>	SLIWV = 125 kV

AC filter arrester (FA)

The operating voltage for the arresters consists of fundamental and harmonic voltages.

The rating of the arresters is determined by the stresses during earth faults followed by recovery overvoltages on the a.c. bus.

AC filter arrester (FA1)

U_{ch}:	60 kV
Number of parallel columns:	2
Energy capability:	1,0 MJ

For the design of the arrester (FA1) the following values for the co-ordination currents are chosen:

SIPL	=	158 kV	at 2 kA			
LIPL	=	192 kV	at 40 kA			
RSIWV	=	1,15 × 158 kV	=	182 kV	=>	SSIWV = 200 kV
RLIWV	=	1,20 × 192 kV	=	230 kV	=>	SLIWV = 250 kV

AC filter arrester (FA2)

U_{ch}:	30 kV
Number of parallel columns:	2
Energy capability:	0,5 MJ

For the design of the arrester (FA2) the following values for the co-ordination currents are chosen:

SIPL	=	104 kV	at 2 kA			
LIPL	=	120 kV	at 10 kA			
RSIWV	=	1,15 × 104 kV	=	120 kV	=>	SSIWV = 150 kV
RLIWV	=	1,20 × 120 kV	=	144 kV	=>	SLIWV = 150 kV

D.C. filter arrester (FD)

The operating voltage for the arresters consists mainly of harmonic voltages.

The rating of the arresters is determined by the stresses during transferred slow-front overvoltage with a subsequent earth fault on the d.c. bus.

D.C. filter arrester (FD1)

U_{ch}:	5 kV
Number of parallel columns:	2
Energy capability:	0,8 MJ

For the design of the arrester (FD1) the following values for the co-ordination currents are chosen:

SIPL	=	136 kV	at 2 kA			
LIPL	=	184 kV	at 40 kA			
RSIWV	=	1,15 × 136 kV	=	156 kV	=>	SSIWV = 200 kV
RLIWV	=	1,20 × 184 kV	=	221 kV	=>	SLIWV = 250 kV

D.C. filter arrester (FD2)

U_{ch}:	5 kV
Number of parallel columns:	2
Energy capability:	0,5 MJ

For the design of the arrester (FD2) the following values for the co-ordination currents are chosen:

SIPL	=	104 kV	at 2 kA			
LIPL	=	120 kV	at 10 kA			
RSIWV	=	1,15 × 104 kV	=	120 kV	=>	SSIWV = 150 kV
RLIWV	=	1,20 × 120 kV	=	144 kV	=>	SLIWV = 150 kV

A.4 Determination of withstand voltages for converter transformers (valve side)

A.4.1 Phase-to-phase

Since the converter transformer valve windings are not directly protected by a single arrester, the following two cases are considered:

- when the valves are conducting, the phase-to-phase insulation of the converter transformer valve side is protected by one valve arrester (V);
- when the valves are blocked, two valve arresters (V) are connected in series, phase-to-phase. During this event, the full transferred slow-front overvoltage will determine the maximum slow-front overvoltage.

SIPL	=	550 kV	
RSIWL	=	1,15 × SIPL	SSIWV = 650 kV
The selected specified lightning withstand voltage is:			SLIWV = 750 kV

If the two phases are in separate transformer units (single-phase, three-winding transformers), and under the assumption that the voltages are not equally shared, the specified insulation levels for the star-winding have been selected to be:

SSIWV = 550 kV
SLIWV = 650 kV

A.4.2 Upper transformer phase-to-earth (star)

The phase-to-earth insulation of the transformer and converters are determined by additive slow-front overvoltages between the transformer phases during the conducting status. These slow-front overvoltages originating from the a.c. side are limited by the arrester (A) on the primary side of the converter transformer. This additive method is not possible in the non-conducting status of the thyristor valves. Therefore only the 'conducting' status needs to be considered.

SIPL = 1 000 kV (2*SIPL of arrester (V2) at 1 025 A, assuming no current in the neutral arrester)

RSIWV = 1,15 × SIPL => SSIWV = 1 175 kV

The selected specified lightning withstand voltage is: SLIWV = 1 300 kV

A.4.3 Lower transformer phase-to-earth (delta)

The insulation levels are the same as phase-to-phase, assuming no current in the neutral arrester.

The selected specified lightning withstand voltage is:

SSIWV = 650 kV
SLIWV = 750 kV

A.5 Determination of withstand voltages for air-insulated smoothing reactors

A.5.1 Terminal-to-terminal at slow-front overvoltages

The worst case for the stresses between the terminals of smoothing reactors is given by the slow-front overvoltages on the d.c. side, which is limited by the arrester (DL). Assuming opposite polarity to the d.c. voltage, the total voltage will be:

SIPL of arrester (DL):	866 kV	
Maximum d.c. voltage:	500 kV	
Sum of both voltages:	1 366 kV	
Smoothing reactors:	225 mH	
Transformer inductances (four phases):	140 mH	(4 × 35 mH)
Total inductance:	365 mH	
Voltage between terminals:	1 366 kV × (225 mH/365 mH) = 842 kV	

SIPL = 842 kV

RSIWV = 1,15 × 842 kV = 968 kV => SSIWV = 1 175 kV

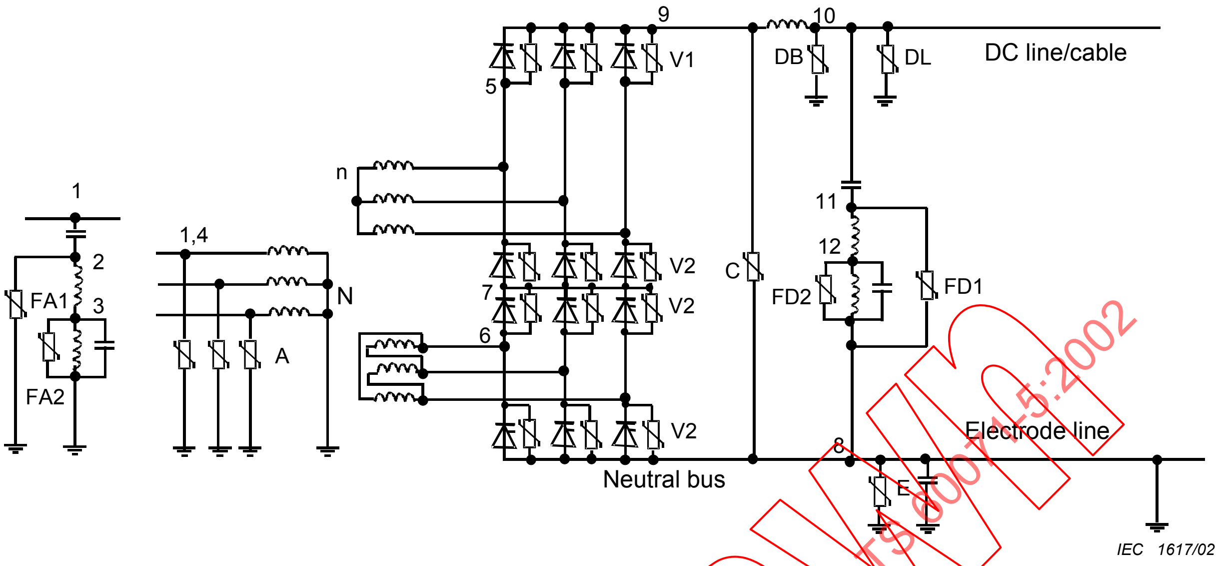
The maximum fast-front overvoltages between terminals are determined by the relative ratio of the capacitance across the reactor to the capacitance to earth on the valve side of the reactor. The specified lightning withstand voltage is: SLIWV = 1 300 kV

A.5.2 Terminal-to-earth

The insulation levels are the same as for the arresters (C) or (DL).

SSIWV = 1175 kV
SLIWV = 1 300 kV

A.6 Tables and computer results



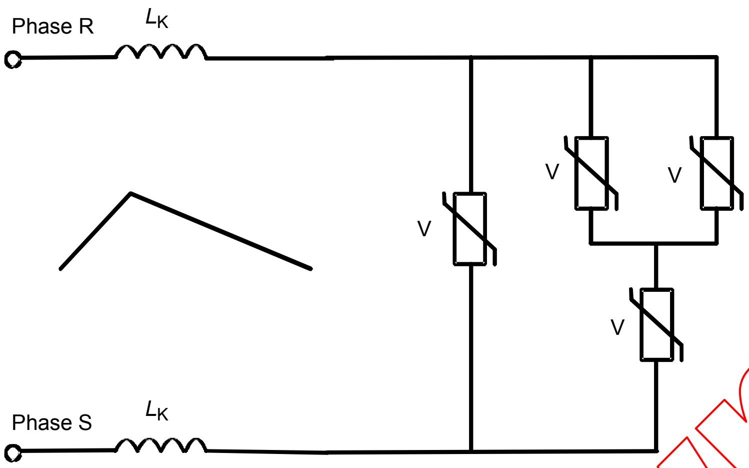
Arrester type		A	V1	V2	C	DB	DL	E	FD1	FD2	FA1	FA2
U_{ch} or CCOV	kV	243 r.m.s.	294 peak	294 peak	558 d.c.	515 d.c.	515 d.c.	30 d.c.	5 d.c.	5 d.c.	60 r.m.s.	30 r.m.s.
Lightning:												
- protection level	KV	713	-	-	1 048	977	872	88	184	120	192	120
- at current	KA	10	-	-	2,5	5	5	10	40	10	40	10
Switching:												
- protection level	KV	632	499,8	500	930	866	807	78	136	104	158	104
- at current	KA	1,5	4,23	1,025	0,5	1,0	1,0	6,0	2,0	2,0	2,0	2,0
No. of columns	-	2	8	2	1	1	8	2	2	2	2	2
Energy capability	MJ	9,2	10,4	2,6	2,5	2,2	17,0	0,4	0,8	0,5	1,0	0,5

Protection location	1	2	3	4	5	6	7	8	9	10	11	12
U_{ch} (kV)	243	60	30	243	558	294	294	30	558	515	15	15
LIPL = RFAO (kV)	713	192	120	713	-	-	-	88	1 048	977	184	120
SIPL = RSLO (kV)	632	158	104	632	1 000	550	550	78	930	866	136	104
SLIWV (kV)	1 425	250	150	1 425	1 300	750	750	125	1 300	1 300	250	150
SSIWV (kV)	1 050	200	150	1 050	1 175	650	650	125	1 175	1 175	200	150

Protection location	1 – 2	2 – 3		5 and 6 ph-ph	5-6	8-9	9-10	10-11	11-12	Valves V1 and V2
LIPL = RFAO (kV)	825	192		-	-	1048	-	977	184	-
SIPL = RSLO (kV)	747	158		550	1 000	930	842	866	136	550
SLIWV (kV)	1 300	250		750	1 300	1 300	1 300	1 300	250	-
SSIWV (kV)	1 050	200		650	1 175	1 175	1 175	1 175	200	575

NOTE Specified withstand voltages on the a.c. side are in line with recommended standard withstand values in IEC 60071-1 for 420 kV a.c. standard voltage class.

Figure A.1 – AC and DC arresters (400 kV a.c. side for conventional HVDC converters)



NOTE The stray capacitances are not shown, but they are design dependent.

Figure A.2 – Simplified circuit configuration for stresses of valve arrester at slow-front overvoltages from a.c. side (conventional HVDC converters) – Illustration of slow-front overvoltage wave (applied voltage)

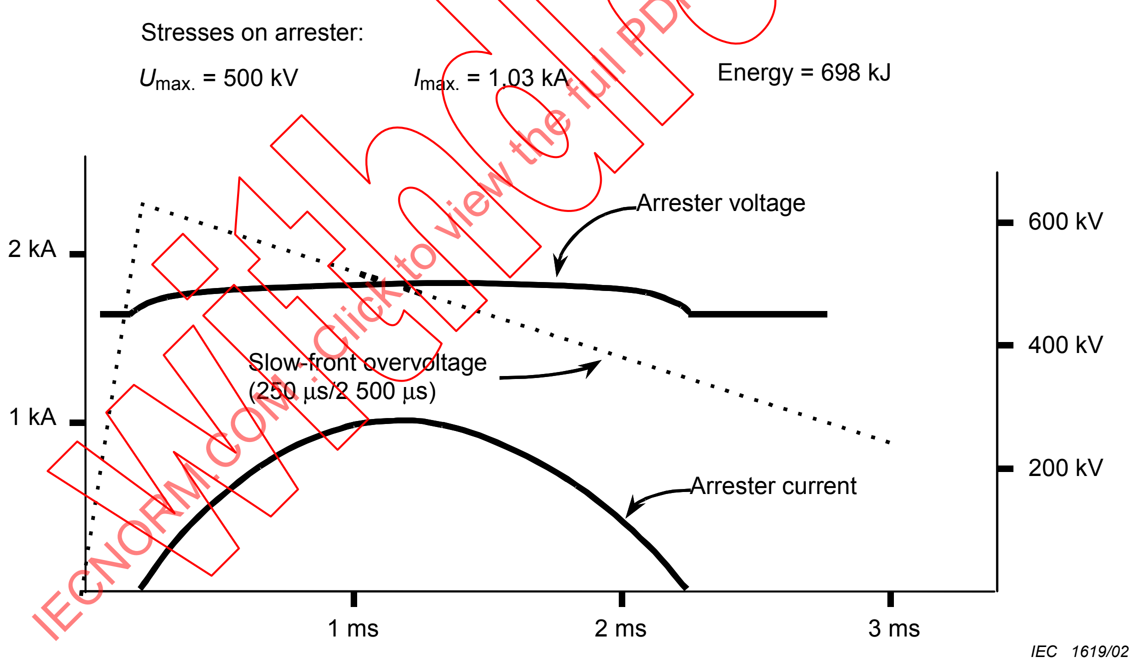
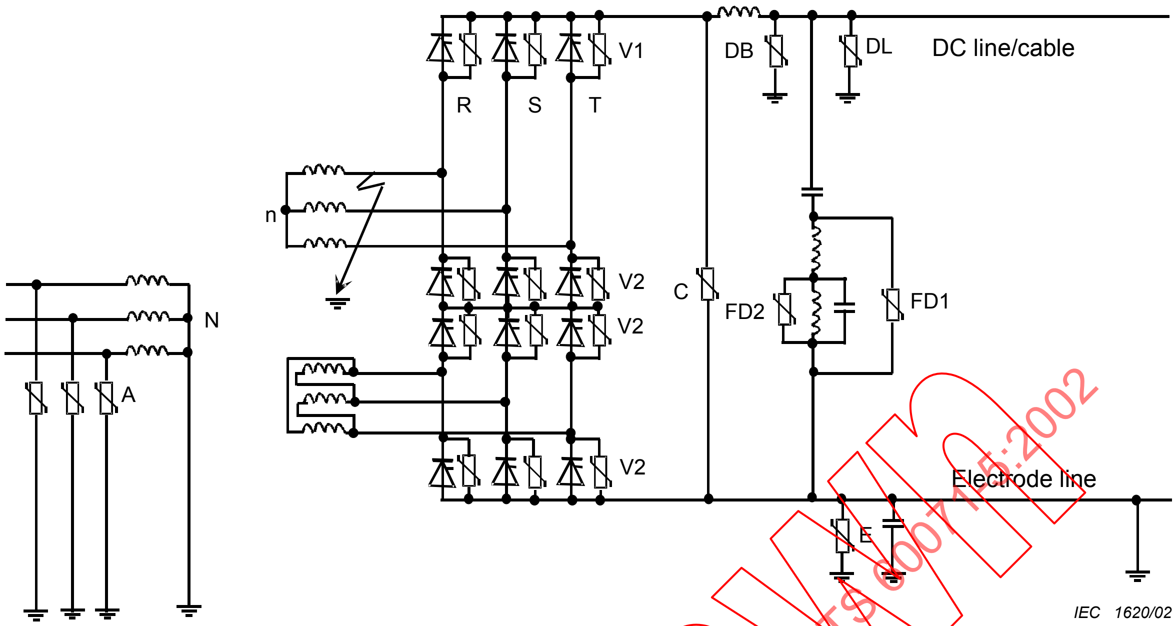


Figure A.3 – Stresses on valve arrester V2 at slow-front overvoltage from a.c. side (conventional HVDC converter)



NOTE The stray capacitances are not shown, and are design dependent.

Figure A.4 – Circuit configuration for stresses on valve arrester at earth fault on transformer HV bushing (conventional HVDC converters)

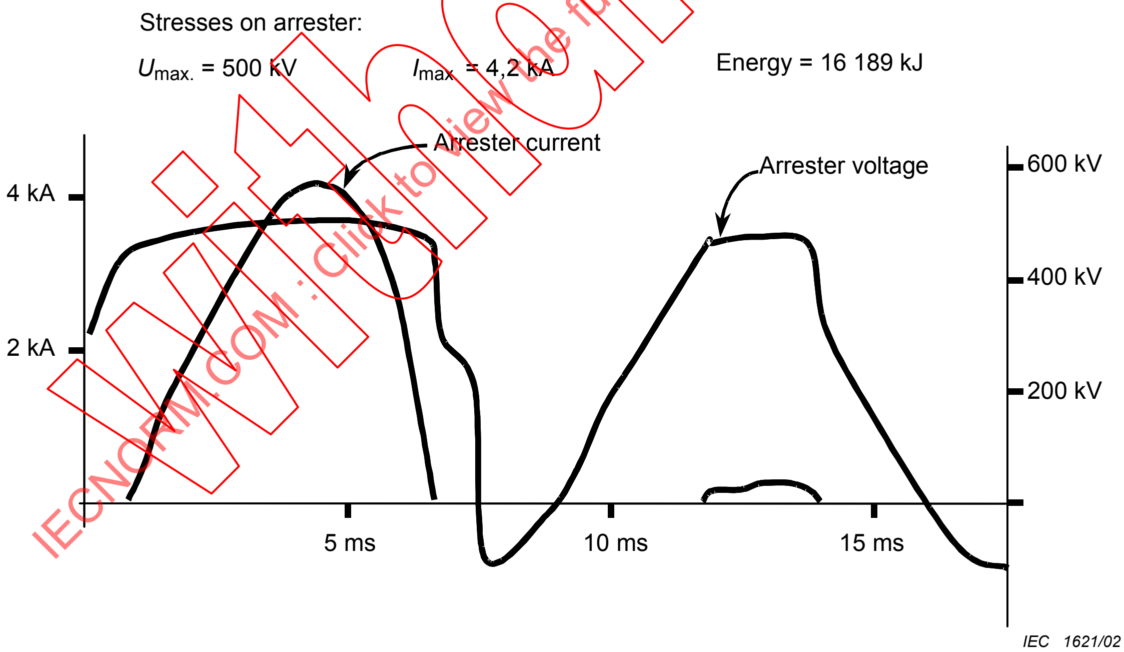


Figure A.5 – Stresses on valve arrester V1 during earth fault on HV bushing of converter transformer (conventional HVDC converter)

Annex B
(informative)

Example of insulation co-ordination for controlled series capacitor converters (CSCC) and capacitor commutated converters (CCC)

List of contents

B.1 Introductory remarks

This annex gives a description and method of calculation for the insulation co-ordination of CSCC and CCC converter stations with a d.c. cable with ground return. This example is intended to be informative and tutorial and is very schematic. It mainly summarizes steps leading to chosen arrester ratings and specified insulation levels, based on procedures explained in the main text.

The results presented are based on the study approach and procedures described in 6.7.1 and clause 9. Because there are no standard withstand levels for HVDC, calculated values for SSIWV, SLIWV and SSFIWV are rounded up to convenient practical values.

B.2 Arrester protective scheme

Figures B.1a and B.1b show the arrester protective schemes for the CSCC and CCC converter station. All arresters are of the metal-oxide type without gap.

B.3 Determination of arrester stresses, protection and insulation levels

The following main data are used for the basic design of the converter station:

AC side: strong a.c. system

DC side:

DC voltage	500	kV	(rectifier)
DC current	1 590	A	
Smoothing reactor	225	mH	
Firing angles	15/17	deg.	(rectifier/inverter)

CCC/CSCC-capacitors		CCC converter	CSCC converter
Capacitance	µF	118	43
U_{ch}	kV r.m.s.	45	136

Converter transformer

Rating (three-phase, six-pulse)	MVA	419	459
Short circuit impedance	pu	0,12	0,12
Secondary voltage (valve side)	kV	186,4	204
tap-changer range	r.m.s.	± 5 %	± 5 %
Inductance per phase (valve side)	mH	32	35

AC bus arresters (A1) and (A4)

The following data are given for the CCC and CSCC converters:

		CCC/CSCC	CSCC
Parameters		Bus 1 (A1)	Bus 4 (A4)
Nominal system voltage	kV_{rms}	400	400
Highest system voltage (U_s)	kV_{rms}	420	420
Continuous operating voltage, phase-to-earth	kV_{rms}	243	256
SIPL (at 1,5 kA)	kV	632	690
LIPL (at 10 kA)	kV	713	790
Maximum slow-front overvoltage transferred to valve side (between two phases)	kV	512/560	N.A.
Number of parallel columns	-	2	2
Arrester energy capability	MJ	3.2	3.4

Valve arrester type (V1) and (V2)

The following values are valid for both converter stations:

		CCC	CSCC	
CCOV	kV	218 × √2	208 × √2	
Number of parallel columns		4	4	for arrester (V1)
		2	2	for arrester (V2)
Energy capability	MJ	5,4	5,2	for arrester (V1)
	MJ	2,7	2,6	for arrester (V2)

The stresses on the valve arresters are determined by computer studies for the following cases:

B.3.1 Transferred slow-front overvoltages from the a.c. side

The highest stresses are expected if the transferred slow-front overvoltage appears between the phases (e.g. R and S), where only one valve is conducting (figures B.2a and B.2b). The value of the transferred slow-front overvoltage overvoltage is dependent on the maximum protective level of the a.c. bus arrester (A) on the primary side of the converter transformer.

Figures B.3a and B.3b show the results for CCC and CSCC converters if only one arrester in the circuit is conducting. This fault case is decisive for the design of all lower valve arresters (V2).

Results valid for valve arrester (V2):

The switching impulse protective level (SIPL) of the valve arrester (V2) is given by:

SIPL		488,1 kV	at 40 A (see figure B.3a for CCC converters)			
		480,8 kV	at 466 A (see figure B.3b for CSCC converters)			
RSIWV	=	1,15 × 488,1 kV	=	561,3 kV	=>	SSIWV = 605 kV
	=	1,15 × 480,8 kV	=	553 kV	=>	
		for both CCC and CSCC converters				

B.3.2 Earth fault between valve and HV bushing of converter transformer

This fault case gives the highest stresses for the valve arresters protecting the three-pulse commutating group on the highest potential. The equivalent circuit for this case is shown in figures B.4a and B.4b. The stresses for the upper valve arresters are also dependent on the fault insertion time. To determine the maximum values, the fault insertion time is varied from zero to 360 electrical degrees.

The results of the maximum stresses are shown in figures B.5a and B.5b for both CCC and CSCC converters.

This fault case is decisive for the design of all upper valve arresters (V1) if the slow-front overvoltage (case a) doesn't result in higher arrester stresses.

Results (valid for valve arrester (V1)):

The switching impulse protective level (SIPL) of the valve arrester (V1) is given by:

SIPL	=	523,6 kV	at 1 776 A (see figure B.5a for CCC converter)			
		498,9 kV	at 2 244 A (see figure B.5b for CSCC converter)			
RSIWV	=	1,15 × 523,6 kV	=	602,1 kV	=>	SSIWV = 605 kV
	=	1,15 × 498,9 kV	=	574 kV	=>	

for both CCC and CSCC converters.

CCC and CSCC capacitor arresters (Ccc/Csc)

		CCC converter	CSCC converter
CCOV	kV	45	136
Number of parallel columns		8	6
Energy capability *	MJ	4,0	4.0
SIPL	kV	149	207
at co-ordination current	kA	7,8	8,8
		(figure B.6a)	(figure B.6b)
LIPL	kV	172	250
at co-ordination current	kA	10	10
RSIWV = 1,15*SIPL	kV	200	250
RLIWV = 1,20*LIPL	kV	250	300

* This is based on the earth fault on the HV bushing of the converter transformer.

Converter group arrester (C)

The following values are valid for both converter stations:

CCOV:	558 kV
Number of parallel columns:	1
Energy capability:	2,5 MJ

The stresses of the group arresters are determined by computer studies transferred slow-front overvoltages from the a.c. side. The magnitude of the transferred slow-front overvoltage is twice the value given for the valve arresters. It is assumed that during normal operation, when four thyristor valves are conducting, a slow-front overvoltage will be transferred between the phases.

For the design of the converter group arrester (C) the following values for the co-ordination currents are chosen:

SIPL	=	930 kV	at 0,5 kA			
LIPL	=	1 048 kV	at 2,5 kA			
RSIWV	=	1,15 × 930 kV	=	1 070 kV	=>	SSIWV = 1 175 kV
RLIWV	=	1,20 × 1048 kV	=	1 258 kV	=>	SLIWV = 1 300 kV

DC bus arrester (DB)

The following values are valid for both converter stations:

CCOV:	515 kV
Number of parallel columns:	1
Energy capability:	2,2 MJ

For the design of the d.c. bus arrester (DB) the following values for the co-ordination currents are chosen:

SIPL	=	866 kV	at 1 kA			
LIPL	=	977 kV	at 5 kA			
RSIWV	=	1,15 × 866 kV	=	996 kV		SSIWV = 1 050 kV
RLIWV	=	1,2 × 977 kV	=	1 173 kV	=>	SLIWV = 1 300 kV

DC line/cable arrester (DL)

The following values are valid for both ends of the d.c. line/cable:

CCOV:	515 kV
Number of parallel columns:	8
Energy capability:	17,0 MJ

For the design of the d.c. line/cable arresters (DL) the following values for the co-ordination currents are chosen:

SIPL	=	807 kV	at 1 kA			
LIPL	=	872 kV	at 5 kA			
RSIWV	=	1,15 × 807 kV	=	928 kV	=>	SSIWV = 950 kV
RLIWV	=	1,20 × 872 kV	=	1046 kV	=>	SLIWV = 1 050 kV

Neutral bus arrester (E)

The following values are valid for both converter stations comprising all neutral bus arresters:

CCOV:	30 kV
Number of parallel columns:	12
Energy capability:	2,4 MJ

For the design of all neutral bus arresters (E) the following values for the co-ordination currents are chosen:

SIPL	=	78 kV	at 2 kA			
LIPL	=	88 kV	at 10 kA			
RSIWV	=	1,15 × 78 kV	=	90 kV	=>	SSIWV = 125 kV
RLIWV	=	1,20 × 88 kV	=	106 kV	=>	SLIWV = 125 kV

AC filter arrester (FA)

The operating voltage for the arresters consists of fundamental and harmonic voltages.

The rating of the arresters is determined by the stresses during earth faults followed by recovery overvoltages on the a.c. bus.

AC filter arrester (FA1)

U_{ch}:	60 kV
Number of parallel columns:	2
Energy capability:	1,0 MJ

For the design of the arrester (FA1) the following values for the co-ordination currents are chosen:

SIPL	=	158 kV	at 2 kA			
LIPL	=	192 kV	at 20 kA			
RSIWV	=	1,15 × 158 kV	=	182 kV	=>	SSIWV = 200 kV
RLIWV	=	1,20 × 192 kV	=	230 kV	=>	SLIWV = 250 kV

AC filter arrester (FA2)

U_{ch}:	30 kV
Number of parallel columns:	2
Energy capability:	0,5 MJ

SIPL	=	104 kV	at 2 kA			
LIPL	=	120 kV	at 10 kA			
RSIWV	=	1,15 × 104 kV	=	120 kV	=>	SSIWV = 150 kV
RLIWV	=	1,20 × 120 kV	=	144 kV	=>	SLIWV = 150 kV

DC filter arrester (FD)

The operating voltage for the arresters consists mainly of harmonic voltages.

The rating of the arresters is determined by the stresses during transferred slow-front overvoltage with a subsequent earth fault on the d.c. bus.

DC filter arrester (FD1)

U_{ch}:	5 kV
Number of parallel columns:	2
Energy capability:	0,8 MJ

For the design of the arrester (FD1) the following values for the co-ordination currents are chosen:

SIPL	=	136 kV	at 2 kA			
LIPL	=	184 kV	at 40 kA			
RSIWV	=	1,15 × 136 kV	=	156 kV	=>	SSIWV = 200 kV
RLIWV	=	1,20 × 184 kV	=	221 kV	=>	SLIWV = 250 kV

DC filter arrester (FD2)

U_{ch}:	5 kV
Number of parallel columns:	2
Energy capability:	0,5 MJ

For the design of the arrester (FD2) the following values for the co-ordination currents are chosen:

SIPL	=	104 kV	at 2 kA				
LIPL	=	120 kV	at 10 kA				
RSIWV	=	1,15 × 104 kV	=	120 kV	=>	SSIWV = 150 kV
RLIWV	=	1,20 × 120 kV	=	144 kV	=>	SLIWV = 150 kV

B.4 Determination of withstand voltages for converter transformers (valve side)

B.4.1 Phase-to-phase

Since the converter transformer valve windings are not directly protected by a single arrester, the following two cases are considered:

- when the valves are conducting, the phase-to-phase insulation of the converter transformer valve side is protected by one valve arrester (V);
- when the valves are blocked, two valve arresters (V) are connected in series, phase-to-phase. During this event, the full transferred slow-front overvoltage will determine the maximum slow-front overvoltage.

SIPL	=	512 kV	(transferred slow-front voltage for CCC)	
		560 kV	(transferred slow-front voltage for CSCC)	
RSIWL	=	1,15 × SIPL		SSIWV = 650 kV
				SLIWV = 750 kV

If the two phases are in separate transformer units (single-phase, three-winding transformers) and under the assumption that the voltages are not equally shared, the specified insulation levels for the star-winding have been selected to be:

SSIWV = 550 kV
SLIWV = 650 kV

B.4.2 Upper transformer phase-to-earth (star)

The phase-to-earth insulation of the transformer and converters are determined by additive slow-front overvoltages between the transformer phases during the conducting status. Thus, slow-front overvoltages originating from the a.c. side are limited by the arrester (A) on the primary side of the converter transformer. This additive method is not possible in the non-conducting status of the thyristor valves. Therefore only the 'conducting' status needs to be considered.

SIPL	=	976 kV	for CCC	(2 × SIPL of arrester (V2), see figure B.3a assuming no current in the neutral arrester)	
		962 kV	for CSCC	(2 × SIPL of arrester (V2), see figure B.3b assuming no current in the neutral arrester)	
RSIWV	=	1,15 × SIPL		=>	SSIWV = 1 175 kV
					SLIWV = 1 300 kV

B.4.3 Lower transformer phase-to-earth (delta)

The specified insulation levels are the same as phase-to-phase, assuming no current in the neutral arrester.

SSIWV = 650 kV
SLIWV = 750 kV

B.5 Determination of withstand voltages for air-insulated smoothing reactors

Terminal-to-terminal at slow-front overvoltages

The worst case for the stresses between the terminals of smoothing reactors is given by the slow-front overvoltages on the d.c. side, which is limited by the arrester (DL). Assuming opposite polarity to the d.c. voltage, the total voltage will be:

SIPL of arrester (DL):	866 kV	
Maximum d.c. voltage:	500 kV	
Sum of both voltages:	1 366 kV	
Smoothing reactors:	225 mH	
Transformer inductances (four phases):	140 mH	(4 × 35 mH)
Total inductance:	365 mH	

One 225 mH smoothing reactor
Voltage between terminals: 1 366 kV × (225 mH/365 mH) = 842 kV

SIPL = 842 kV
RSIWV = 1,15 × 842 kV = 968 kV => **SSIWV = 1 175 kV**

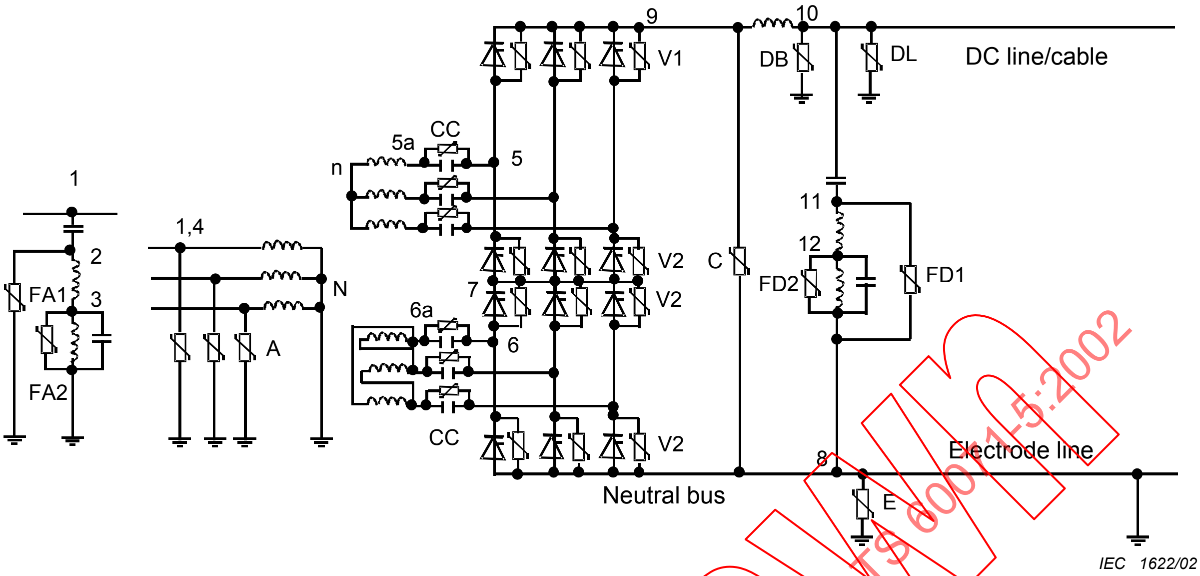
The maximum fast-front overvoltages between terminals are determined by the relative ratio of the capacitance across the reactor to the capacitance to earth on the valve side of the reactor. The specified lightning withstand voltage is: **SLIWV = 1 300 kV**

Terminal-to-earth

The specified insulation levels are the same as for the arresters (C) or (DL)

SSIWV = 1 175 kV
SLIWV = 1 300 kV

B.6 Tables and computer results

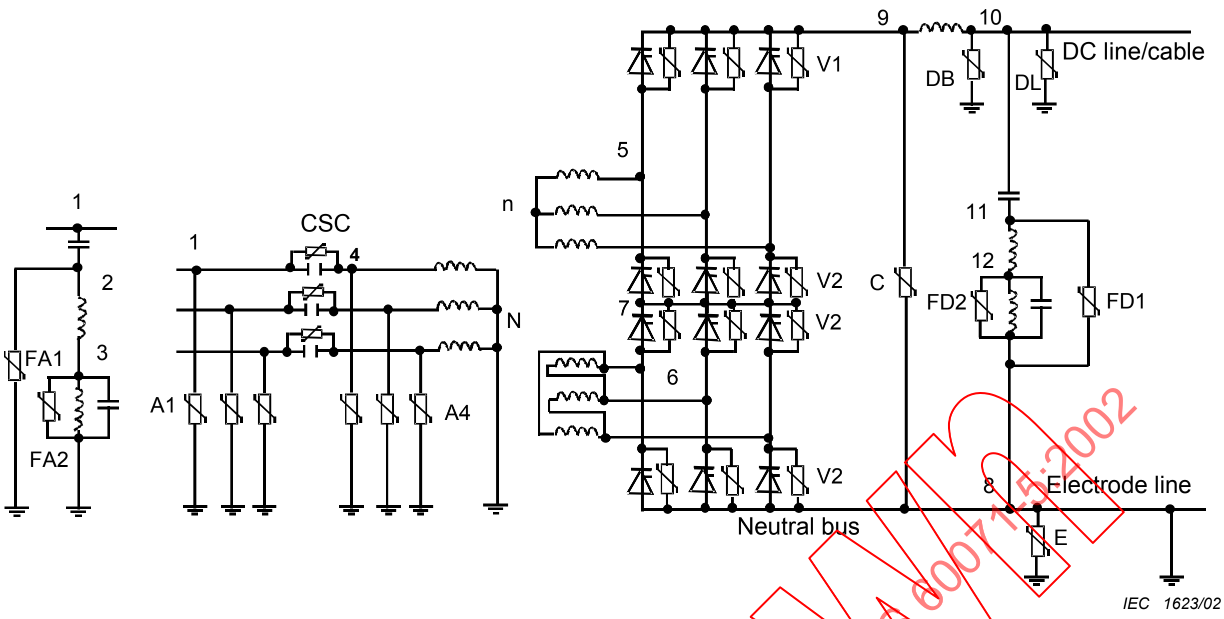


Arrester type		A	V1	V2	C	DB	DL	E	FD1	FD2	FA1	FA2	CC
U_{ch} or CCOV	kV	243 r.m.s.	308 peak	308 peak	558 d.c.	515 d.c.	515 d.c.	30 d.c.	5 d.c.	5 d.c.	60 r.m.s.	30 r.m.s.	60 peak
Lightning - protection level - at current	 kV kA	 713 10	 - -	 - -	 1 048 2,5	 977 5	 872 5	 88 10	 184 40	 120 10	 192 20	 120 10	 172 10
Switching - protection level - at current	 kV kA	 632 1,5	 523 1,8	 488 0,1	 930 0,5	 866 1,0	 807 1,0	 78 2,0	 136 2,0	 104 2,0	 158 2,0	 104 2,0	 149 7,8
Number of columns	-	2	4	2	1	1	8	2	2	2	2	2	8
Energy capability	MJ	9,2	5,2	2,6	2,5	2,2	17,0	0,4	0,8	0,5	1,0	0,5	4,0

Protection location	1	2	3	4	5	6	7	8	9	10	11	12
U_{ch} (kV)	243	60	30	243	558	308	308	30	558	515	15	15
LIPL = RFAO (kV)	713	192	120	713	-	-	-	88	1 048	977	184	120
SIPL = RSLO (kV)	632	158	104	632	976	523	523	78	930	866	136	104
SLIWV (kV)	1 425	250	150	1 425	1 300	750	750	150	1 300	1 300	250	150
SSIWV (kV)	1 050	200	150	1 050	1 175	650	650	150	1 175	1 175	200	150

Protection location	1 – 2	2 – 3	5-5a Ccc	5 and 6 ph-ph	5-6	8-9	9-10	10-11	11-12	Valves V1 and V2
LIPL = FFMO (kV)	825	192	172	-	-	1 048	-	977	184	-
SIPL = RSLO (kV)	747	158	149	523	976	930	842	866	136	523
SLIWV (kV)	1 300	250	250	750	1 300	1 300	1 300	1 300	250	-
SSIWV (kV)	1 050	200	200	650	1 175	1 175	1 175	1 175	200	605

Figure B.1a – AC and DC arresters (400 kV a.c. side for CCC converters)



Arrester type		A	V1	V2	C	DB	DL	E	FD1	FD2	FA1	FA2	CSC	A4
U_{ch} or CCOV	kV	243 r.m.s.	294 peak	294 peak	558 d.c.	515 d.c.	515 d.c.	30 d.c.	5 d.c.	5 d.c.	60 r.m.s.	30 r.m.s.	96 r.m.s.	256 r.m.s.
Lightning - protection level	kV	713	-	-	1 048	977	872	88	184	120	192	120	250	790
- at current	kA	10	-	-	2,5	5	5	10	40	10	20	10	10	10
Switching - protection level	kV	632	499	481	930	866	807	78	136	104	158	104	207	690
- at current	kA	1,5	2,2	0,5	0,5	1,0	1,0	2,0	2,0	2,0	2,0	2,0	8,8	1,5
No. of columns	-	2	4	2	1	1	8	2	2	2	2	2	6	2
Energy apability	MJ	9,2	5,2	2,6	2,5	2,2	17,0	0,4	0,8	0,5	1,0	0,5	4,0	3,4

Protection location	1	2	3	4	5	6	7	8	9	10	11	12
U_{ch} (kV)	243	60	30	256	558	294	294	30	558	515	15	15
LIPL = RFAO (kV)	713	192	120	790	-	-	-	88	1 048	977	184	120
SIPL= RSLO (kV)	632	158	104	690	962	499	499	78	930	866	136	104
SLIWV (kV)	1 425	250	150	1 425	1 300	750	750	150	1 300	1 300	250	150
SSIWV (kV)	1 050	200	150	1 050	1 175	650	650	150	1 175	1 175	200	150

Protection location	1 – 2	2 – 3	1-4 Csc	5 and 6 ph-ph	5-6	8-9	9-10	10-11	11-12	Valves V1 and V2
LIPL = RFAO (kV)	825	192	250	-	-	1 048	-	977	184	-
SIPL= RSLO (kV)	747	158	207	523	962	930	842	866	136	523
SLIWV (kV)	1 300	250	300	750	1 300	1 300	1 300	1 300	250	-
SSIWV (kV)	1 050	200	250	650	1 175	1 175	1 175	1 175	200	605

Figure B.1b – AC and DC arresters (400 kV a.c. side for CSCC converter)