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TECHNICAL SPECIFICATION

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Device embedding assembly technology – Part 2-10: Design specification for cavity substrate

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IEC Secretariat
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

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IEC TS 62878-2-10 has been prepared by IEC technical committee 91: Electronics assembly technology. It is a Technical Specification.

The text of this Technical Specification is based on the following documents:

Draft	Report on voting
91/1909/DTS	91/1928/RVDTS

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Specification is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-10: Design specification for cavity substrate

1 Scope

This document provides a general specification for the design of cavity substrates.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194-2, *Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
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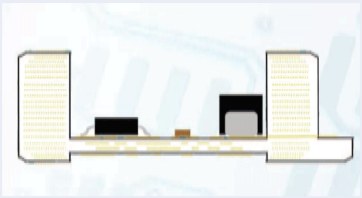
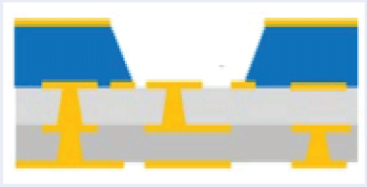
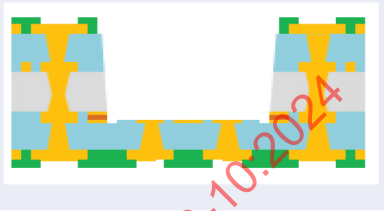
4 Objective

The number of applications of SiP (System in Package) is increasing because of its benefit of fast development and cost-effectiveness compared to SOC (System on Chip). Despite its strength, there is constant demand for reducing the form factor of SiP. WLP (Wafer-Level Package) or PLP (Panel-Level Package) usually provides smaller form factor than the conventional packages with substrates. For these SiP, cavity substrates can be used to achieve a similar package thickness with better cost and proven assembly process. For the reduction of package thickness, a design specification for cavity substrates for small form factor applications is necessary.

5 Cavity formation

There are three types, i.e., milling type, etching type, and laser type for forming cavity substrates as shown in Table 1. Milling type is forming the cavity structure by using milling technology to obtain deep cavities. Etching type is forming the cavity structure by etching the dielectric materials and the cavity structure is isotropic. Laser type is forming the cavity structure by laser cutting and detaching technology. Both, etching type and laser type are used to obtain shallow cavities.

Table 1 – Cavity formation types

Process type		
Milling type	**Etching type**	**Laser type**
		

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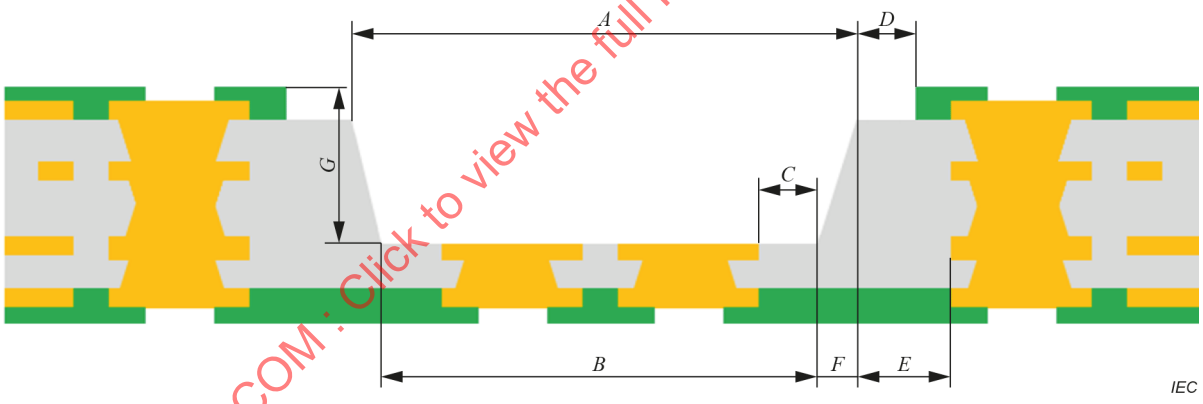
6 Design guideline

Figure 1 shows the general schematic of cavity substrate and Table 2 contains the cavity substrate drawing designators. If looking at design rule of cavity substrate as shown in this schematic, A is the top cavity size, B is the bottom cavity size, C is the cavity wall to layer 2 pattern, D is the cavity opening to SR, E is the cavity opening to layer 3 patterns, F is the cavity taper and G is the cavity depth. Annex A shows the cavity formation examples depending on design guidelines of cavity substrate.



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Key

A top cavity size
B bottom cavity size
C cavity wall to layer 2 pattern
D cavity opening to SR
E cavity opening to layer 3 patterns
F cavity taper
G cavity depth

Figure 1 – Schematic of cavity substate

Table 2 – Cavity substrate drawing designators

Designator	Description
A	top cavity size
B	bottom cavity size
C	cavity wall to L3 Pattern
D	cavity opening to SR
E	cavity opening to L3 Pattern
F	cavity taper
G	cavity depth

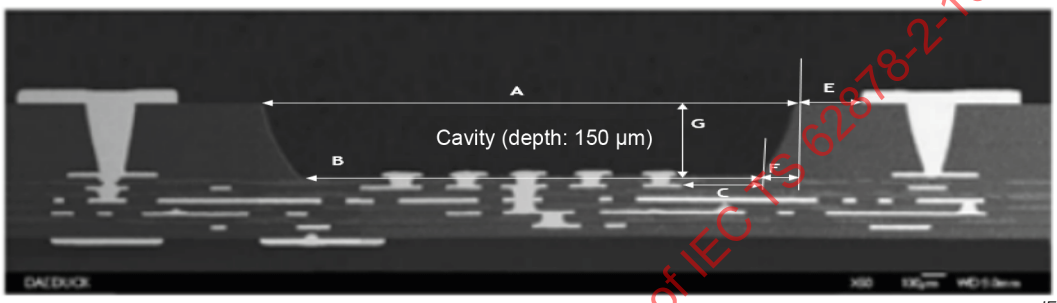
Annex A
(informative)

Cavity formation examples

A.1 General

Design guidelines for most of cavity substrates are similar if looking at the two types illustrated in Figure A.1 and Figure A.2. However, design rules and fabrication methods are different depending on the various cavity structures.

A.2 Etching type example



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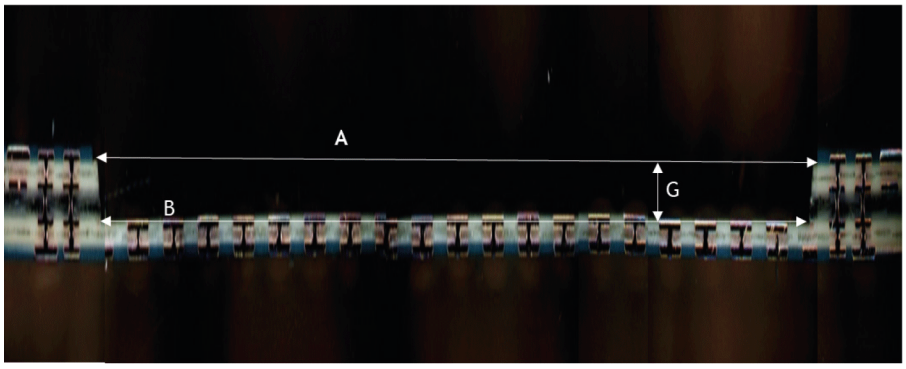
Key

A top cavity size
B bottom cavity size
C cavity wall to layer 2 pattern
E cavity opening to layer 3 patterns
F cavity taper
G cavity depth

Figure A.1 – Etching type

A.3 Laser type example



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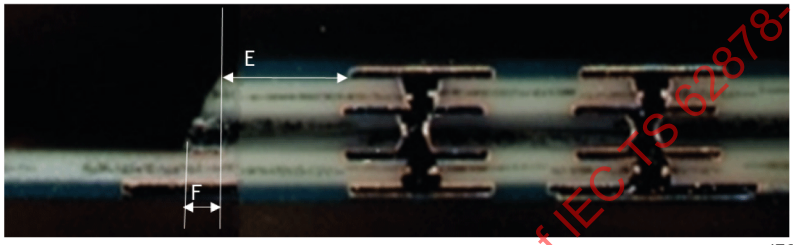
a) The whole cross-section view



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b) The left cross-section view

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c) The right cross-section view

Key

A top cavity size
B bottom cavity size
C cavity wall to layer 2 pattern
E cavity opening to layer 3 patterns
F cavity taper
G cavity depth

Figure A.2 – Laser type