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Cards and security devices for personal identification — Test methods —

Part 6: Contactless proximity objects

Cartes et dispositifs de sécurité pour l'identification personnelle — Méthodes d'essai —

Partie 6: Objets sans contact de proximité

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of document should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives or www.iec.ch/members_experts/refdocs).

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This document was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, SC 17, *Cards and security devices for personal identification*.

This fifth edition cancels and replaces the fourth edition (ISO/IEC 10373-6:2020), which has been technically revised. It also incorporates the Amendment ISO/IEC 10373-6:2020/Amd.2:2020.

The main changes are as follows:

— addition of explicit RFU reception test methods;

— modifications of the PICC transmission test methods;

— simplifications of the impedance matching networks; and

— corrections of the conformance test plan.

A list of all the parts in the ISO/IEC 10373 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html and www.iec.ch/national-committees.

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Cards and security devices for personal identification — Test methods —

Part 6: Contactless proximity objects

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1 Scope

This document defines test methods which are specific to proximity cards and objects, proximity coupling devices and proximity extended devices, defined in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3 and ISO/IEC 14443-4.

NOTE Test methods defined in this document are intended to be performed separately. A given proximity card or object, proximity coupling device or proximity extended device, is not required to pass through all the tests sequentially.

The conformance test plan defined in Annex O specifies the list of tests required for each part of the ISO/IEC 14443 series.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7810, *Identification cards — Physical characteristics*

ISO/IEC 14443-1:2018, *Cards and security devices for personal identification — Contactless proximity objects — Part 1: Physical characteristics*

ISO/IEC 14443-2:2020, *Cards and security devices for personal identification — Contactless proximity objects — Part 2: Radio frequency power and signal interface*

ISO/IEC 14443-3:2018, *Cards and security devices for personal identification — Contactless proximity objects — Part 3: Initialization and anticollision*

ISO/IEC 14443-4:2018, *Cards and security devices for personal identification — Contactless proximity objects — Part 4: Transmission protocol*

3 Terms, definitions, symbols and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3, ISO/IEC 14443-4 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at https://www.electropedia.org/

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3.1.1
base standard
standard to which the *test method* (3.1.8) is used to verify conformance

3.1.2
CascadeLevels
number of cascade levels of the PICC

3.1.3
command set
set describing the PICC commands during initialization and anticollision

Note 1 to entry: See ISO/IEC 14443-3:2018, 6.4 for PICC Type A and ISO/IEC 14443-3:2018, 7.5 for PICC Type B.

3.1.4
loading effect
change in PCD antenna current caused by the presence of PICC(s) in the field due to the mutual coupling modifying the PCD antenna resonance and quality factor

3.1.5
mute
no response within a specified timeout

EXAMPLE Expiration of FWT.

3.1.6
scenario
defined typical protocol and application specific communication to be used with the *test methods* (3.1.8) defined in this document

3.1.7
test initial state
TIS
element from PICC states that is the PICC state before performing a specific PICC command from *command set* (3.1.3)

3.1.8
test method
method for testing characteristics of devices in scope for the purpose of verifying their conformance with International Standards

3.1.9
test target state
TTS
element from PICC states that is the PICC state after performing a specific PICC command from *command set* (3.1.3)

3.2 Symbols and abbreviated terms

For the purposes of this document, the symbols and abbreviated terms given in ISO/IEC 14443-1, ISO/IEC 14443-2, ISO/IEC 14443-3, ISO/IEC 14443-4 and the following apply.

NOTE Elements in bold square brackets **[ ]** are optional.

Answer to ATTRIB(cid)	Answer to ATTRIB with CID = cid
ATTRIB(cid, fsdi)	ATTRIB command with CID = cid and Maximum Frame Size Code value = fsdi

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~CRC	Invalid CRC with respect to the communication signal interface Type A (CRC_A) or Type B (CRC_B), transmitted instead of the specified CRC if present in the command or response definition
DUT	Device under test; within the scope of this document, DUT represents the PICC under test
$I(c)_n$([INF = inf] [,CID = cid] [,NAD = nad])	ISO/IEC 14443-4 I-block with chaining bit c∈{1,0}, block number n∈{1,0} and information field INF. By default no CID and no NAD will be transmitted. If CID = cid∈{0...15} is specified, it will be transmitted as second parameter. If NAD = nad∈{0...'FF'} is specified, it will be transmitted as third parameter (or second parameter if no CID is transmitted).
IUT	Implementation Under Test (ISO/IEC 9646); within the scope of this document, IUT represents the PCD under test
LT	Lower Tester (ISO/IEC 9646), the PICC-emulation part of the PCD-test-apparatus
N/A	Not applicable
PPS(cid, dri, dsi)	PPS request with CID = cid, DRI = dri and DSI = dsi
~PUPI	Unmatched PUPI, transmitted instead of the specified PUPI if present in the command or response definition
$R(ACK\ [,CID = cid])_n$	ISO/IEC 14443-4 R(ACK) block with block number n. The definition of the optional CID symbol is as described in the $I(c)_n$ block above
$R(NAK\ [,CID = cid])_n$	ISO/IEC 14443-4 R(NAK) block with block number n. The definition of the optional CID symbol is as described in the $I(c)_n$ block above
RATS(cid, fsdi)	RATS command with CID = cid and FSDI value = fsdi
READY(I)	READY state in cascade level I, I ∈ {1, 2, 3}; e.g. READY(2) is a PICC cascade level 2
READY*(I)	READY* state in cascade level I, I ∈ {1, 2, 3}; e.g. READY*(2) is a PICC cascade level 2
REQB(N)	REQB command with N as defined in ISO/IEC 14443-3:2018, 7.7
S(WTX)(WTXM [,CID = cid])	ISO/IEC 14443-4 S(WTX) block with parameter WTXM. The definition of the optional CID symbol is as described in the $I(c)_n$ block above
S(DESELECT [,CID = cid])	ISO/IEC 14443-4 S(DESELECT) block. The definition of the optional CID symbol is as described in the $I(c)_n$ block above
SAK(cascade)	the SELECT(I) answer with the cascade bit (bit 3) set to (1)b
SAK(complete)	the SELECT(I) answer with the cascade bit (bit 3) set to (0)b
SELECT(I)	SELECT command of cascade level I, i.e. SELECT(1) = ('93 70' $UIDTX_1$ BCC CRC_A) SELECT(2) = ('95 70' $UIDTX_2$ BCC CRC_A) SELECT(3) = ('97 70' $UIDTX_3$ BCC CRC_A)

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SLOTMARKER(n)	Slot-MARKER command with slot number n, i.e. (16 × (n − 1) + 5 CRC_B)
TB-PDU	Transmission Block Protocol Data Unit, which consists of either I-block, R-block or S-block
TEST_COMMAND_SEQUENCE1	Sequence of commands used for several PICC tests. When transmitted to DUT Type A, the sequence should contain at least one I-block ending with (0)b and at least one I-block ending with (1)b. NOTE Its definition depends on applicative layer and represents a standard transaction of the application supported by the DUT. The applicant may also provide a specified set of commands.
TEST_COMMAND1(1)	Default test command consisting of one unchained I-block NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND1(n), n > 1	Default test command consisting of n chained I-blocks (PCD chaining) NOTE This command depends on the negotiated maximum frame size value of the PICC.
$TEST_COMMAND1(n)_k$	INF field of k'th I-block chain of TEST_COMMAND1(n) NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND2(n), n > 1	Default test command which expects a response consisting of n chained I-blocks NOTE This command depends on the negotiated maximum frame size value of the PCD.
TEST_COMMAND3	Default test command consisting of one I-block which needs more than FWT time for execution
TEST_COMMAND4	Default test command which expects a response of one I-block in conformance with the PICC transmission minimum frame length required for the PICC transmission test
TEST_RESPONSE1(n)	INF field of the response to TEST_COMMAND1(n) NOTE This response is assumed to be always unchained.
TEST_RESPONSE2(n)	Response to TEST_COMMAND2(n) NOTE This response depends on the negotiated maximum frame size value of the PCD.
$TEST_RESPONSE2(n)_k$	INF field of k'th I-block chain of TEST_RESPONSE2(n) NOTE This response depends on the negotiated maximum frame size value of the PCD.
TEST_RESPONSE3	Response I-block to TEST_COMMAND3 NOTE This response is always assumed to be unchained.
TEST_RESPONSE4	Response I-block to TEST_COMMAND4
TM-PDU	Test Management Protocol Data Unit (ISO/IEC 9646-1, PDU)
t_{START}	Start of PICC transmission
$UIDTX_I$	UID 32-bit data at cascade level I ∈ {1, 2, 3} (see Table 1)
$\sim UIDTX_I$	Wrong UID 32-bit data cascade level I ∈ {1, 2, 3} (see Table 1)

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UT	Upper Tester (ISO/IEC 9646), the master part of the PCD-test-apparatus
UT_APDU	Upper Tester Application Protocol Data Unit: a packet of data to be sent by the PCD to the LT through the RF interface
V_{load}	DC voltage measured at connector CON3 of the Reference PICC
WUPB(N)	WUPB command with N as defined in ISO/IEC 14443-3:2018, 7.7
~X	Bit sequence consisting of the inverted bits of bit sequence X or any other bit sequence different from X
X[[a...b]]	Bit subsequence of bit sequence X consisting of the bits between position a and b included. If a > b then the sequence is empty
X[[n]]	Bit at position n of bit sequence X. First bit is at position 1
X[n]	Byte at position n of bit sequence X. First byte is at position 1 (i.e. X[n] = X[[(n − 1) × 8 + 1...n × 8]])

Table 1 shows the mapping from UID to UIDTX.

Table 1 — Mapping from UID to UIDTX

Cascade level	Single UID PICC	Double UID PICC	Triple UID PICC
$UIDTX_1$	UID0 UID1 UID2 UID3	'88' UID0 UID1 UID2	'88' UID0 UID1 UID2
$UIDTX_2$	—	UID3 UID4 UID5 UID6	'88' UID3 UID4 UID5
$UIDTX_3$	—	—	UID6 UID7 UID8 UID9

4 Default items applicable to the test methods

4.1 Test environment

Unless otherwise specified, testing shall take place in an environment of temperature 23 °C ± 3 °C (73 °F ± 5 °F) and of relative humidity 25 % to 75 %.

4.2 Pre-conditioning

No environmental pre-conditioning of PICCs or PCDs is required by the test methods in this document.

4.3 Setup tolerances

The following absolute tolerances shall be used when adjusting the Test PCD assembly modulation waveform:

a) for timings (t_1, t_2, t_3, t_5, t_6, t_r, t_f):
   1) $\pm 1/f_c$ for a PCD to PICC bit rate of $f_c/128$;
   2) $\pm 0{,}5/f_c$ for a PCD to PICC bit rate of $f_c/64$;
   3) $\pm 0{,}3/f_c$ for PCD to PICC bit rates higher than $f_c/64$;

b) for envelope overshoot, Type A, PCD to PICC bit rate of $f_c/128$: ±1 % of $H_{INITIAL}$;

c) for envelope overshoot, Type A, PCD to PICC bit rates higher than $f_c/128$: $\pm 0{,}01 \times (1\text{-}a)$;

d) for envelope overshoot and undershoot, Type B: $\pm 0{,}01 \times (1\text{-}b)$;

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e) for the modulation index m: ±0,5 %;

f) for the pulse shape factor a: ±0,02;

g) for PCD field envelope during 60 % of t_2: ±0,5 % of $H_{INITIAL}$.

Unless otherwise specified, a tolerance of ±5 % shall be applied to the quantity values given to specify the characteristics of the test equipment (e.g. linear dimensions) and the test method procedures (e.g. test equipment adjustments).

4.4 Spurious inductance

Resistors and capacitors should have negligible inductance.

4.5 Measurement uncertainty

The measurement uncertainty for each quantity determined by these test methods shall be stated in the test report.

Basic information is given in ISO/IEC Guide 98-3.

4.6 DUT position

Unless otherwise specified, the PICC and Reference PICC antennas shall be centered on the sense coil a of the Test PCD assembly.

4.7 Test conditions for PCD

Unless otherwise specified, the test conditions defined in Table 2 shall be applied.

Table 2 — Test conditions for PCD

Conditions	Values
Type	Type A and Type B
Test positions	Position 0: See Table 3 Position Z_{max}: See Table 3
Reference PICCs	Reference PICC 1, Reference PICC 2 and Reference PICC 3 In accordance with the support of optional PICC classes as declared by the PCD manufacturer in Table 3: a) Reference PICC 4 if PICC Class 4 is supported; b) Reference PICC 5 if PICC Class 5 is supported; c) Reference PICC 6 if PICC Class 6 is supported.

The information defined in Table 3 shall be provided by the PCD manufacturer.

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Table 3 — PCD manufacturer information

Parameter	Description	Unit
Position 0	Position and orientation of the Reference PICCs on the PCD surface. This position may be PICC classes dependent.	
Position Z_{max}	Position with maximum operating distance on the Z axis[a]. This position may be PICC classes dependent.	
Temperature range	Minimum and maximum temperature values.	°C
Optional PICC classes	List of supported optional PICC classes	
PCD to PICC supported bit rates	List of supported optional PCD to PICC bit rates.	
PICC to PCD supported bit rates	List of supported optional PICC to PCD bit rates.	
Maximum frame size supported	Maximum frame size in reception.	Bytes
PCD to PICC frame with error correction supported	Frame with error correction from PCD to PICC.	
PICC to PCD frame with error correction supported	Frame with error correction from PICC to PCD.	
Internal output buffer size	Maximum size of the command UT_APDU.	Bytes
Internal input buffer size	Maximum size of the response UT_APDU.	Bytes
Type A collision resolution	Collision resolution for Type A supported.	
Polling in order to detect PICCs requiring 5 ms	PCD commits to periodically present an unmodulated RF field of at least 5,1 ms duration prior to both Type A and Type B request commands.	

[a] Z axis shall be perpendicular to the PCD surface through Position 0. If the PCD surface is not flat, Z axis shall correspond to the axis along which PICCs would habitually be held to the PCD and shall be coherent with PCD ergonomics; if not, the test laboratory may choose to redefine it (directionally).

Unless otherwise specified, the values defined in Table 4 shall be used to adjust PCD-test-apparatus parameters.

Table 4 — Values of the PCD-test-apparatus parameters unless otherwise specified

Parameter	Value	Applies to
PCD to PICC and PICC to PCD bit rates	f_c/128	Type A and Type B
Load modulation amplitude	More than 20 mV at H_{min}	Type A and Type B
Reference PICCs resonance frequency	16,5 MHz	Type A and Type B
J1 setting	position 'a'	Type A and Type B
J2 setting	position 'a'	Type A and Type B
Reference PICCs position	Position Z_{max}	Type A and Type B
Start Of Frame (SOF) timing	10 etu "0" followed by 2 etu "1"	Type B
End Of Frame (EOF) timing	10 etu "0"	Type B
Extra Guard Time (EGT) timing	0 etu	Type B
TR0 for ATQB and DESELECT	$200/f_s$	Type B
Frame waiting time	Any value as specified in ISO/IEC 14443-4:2018, 7.3	Type A and Type B
UID	Any of the size and contents as specified in ISO/IEC 14443-3:2018, 6.5.4	Type A
TR1	$140/f_s$	Type B
FSCI	8	Type A
Maximum Frame Size Code in ATQB	8	Type B

4.8 Test conditions for PICC

Unless otherwise specified, the test conditions defined in Table 5 shall be applied:

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Table 5 — Test conditions for PICC

Conditions	Values	
Field strength[a]	For PICC Class 1:	1,5 A/m, 2,5 A/m, 4,5 A/m and 7,5 A/m
	For PICC Class 2 and Class 3:	1,5 A/m, 2,5 A/m, 4,5 A/m and 8,5 A/m
	For PICC Class 4:	2 A/m, 4 A/m, 7 A/m and 12 A/m
	For PICC Class 5:	2,5 A/m, 4,5 A/m, 8 A/m and 14 A/m
	For PICC Class 6:	4,5 A/m, 7 A/m, 11 A/m and 18 A/m
[a] Any additional field strength values between H_{min} and H_{max} may be applied.		

The information defined in Table 6 shall be provided by the PICC manufacturer.

Table 6 — PICC manufacturer information

Parameter	Description	Unit
Location of the external rectangle/ circle of the claimed PICC class[a]	Drawing with dimensions of PICC outside shape and the position of the external rectangle/circle of the claimed PICC class.	
PICC class (optional)[a]	Claimed PICC class.	
Resonance frequency range (optional)	Minimum and maximum resonance frequency.	MHz
Communication signal interface	Supported communication signal interface(s): a) Type A b) Type B c) Type A and Type B	
Temperature range	Minimum and maximum operating temperature.	°C
PCD to PICC supported bit rates	List of supported optional PCD to PICC bit rates.	
PICC to PCD supported bit rates	List of supported optional PICC to PCD bit rates.	
Same bit rate for both directions	Indication if only same bit rate from PCD to PICC and from PICC to PCD is supported.	
Random or fixed UID (Type A) or PUPI (Type B)	Indication whether the UID (Type A) or PUPI (Type B) is random or fixed.	
AFI values (Type B)	List of AFI values (except '00') the PICC matches.	
Maximum frame size supported	Maximum frame size in reception.	Bytes
PCD to PICC frame with error correction supported	Frame with error correction from PCD to PICC.	
PICC to PCD frame with error correction supported	Frame with error correction from PICC to PCD.	
TEST_COMMAND_SEQUENCE1	See 0.2.1	
TEST_COMMAND1	See 0.2.1	
TEST_COMMAND2	See 0.2.1	
TEST_COMMAND3	See 0.2.1	
TEST_COMMAND4	See 0.2.1	
[a] If not provided, test methods for PICC Class 1 shall be used.		

Unless otherwise specified, the values defined in Table 7 shall be used to adjust PICC-test-apparatus parameters.

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Table 7 — Values of the PICC-test-apparatus parameters unless otherwise specified

Parameter	Value	Applies to
Parameters applicable for all PCD to PICC bit rates		
FSDI	8	Type A
Start Of Frame (SOF) timing	10 etu “0” followed by 2 etu “1”	Type B
End Of Frame (EOF) timing	10 etu “0”	Type B
Extra Guard Time (EGT) timing	0 etu	Type B
Maximum Frame Size Code in ATTRIB	8	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/128$		
PCD field envelope during 60 % of t_2	0,5 %	Type A
t_1	$40/f_c$	Type A
t_2	$7/f_c$	Type A
t_3	$12/f_c$	Type A
t_4	$6/f_c$	Type A
Overshoot	0	Type A and Type B
Modulation index m	12 %	Type B
Rise time t_r, fall time t_f	$12/f_c$	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/64$		
a	0,1	Type A
t_1	$18/f_c$	Type A
t_5	$15/f_c$	Type A
t_6	$9/f_c$	Type A
Overshoot	0	Type A and Type B
Modulation index m	12 %	Type B
Rise time t_r, fall time t_f	$10/f_c$	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/32$		
a	0,2	Type A
t_1	$9/f_c$	Type A
t_5	$7/f_c$	Type A
t_6	$8/f_c$	Type A
Overshoot	0	Type A and Type B
Modulation index m	12 %	Type B
Rise time t_r, fall time t_f	$8/f_c$	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/16$		
a	0,4	Type A
t_1	$5/f_c$	Type A
t_5	$4/f_c$	Type A
t_6	$5/f_c$	Type A
Overshoot	0	Type A and Type B
Modulation index m	12 %	Type B
Rise time t_r, fall time t_f	$6/f_c$	Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/8$		
Overshoot	0	Type A and Type B
Modulation index m	8 % for short modulation pulses	Type A and Type B
Rise time t_r, fall time t_f	$5/f_c$	Type A and Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/4$		

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Table 7 *(continued)*

Parameter	Value	Applies to
Overshoot	0	Type A and Type B
Modulation index *m*	8 % for short modulation pulses	Type A and Type B
Rise time t_r, fall time t_f	$4/f_c$	Type A and Type B
Parameters applicable for a PCD to PICC bit rate of $f_c/2$		
Overshoot	0	Type A and Type B
Modulation index *m*	8 % for short modulation pulses	Type A and Type B
Rise time t_r, fall time t_f	$3/f_c$	Type A and Type B
Parameters applicable for a PCD to PICC bit rate of $3f_c/4$ and $3f_c/2$		
PR	56°	Type A and Type B
ISI_d	0	Type A and Type B
ISI_m	1	Type A and Type B
Phase noise	0,03	Type A and Type B
Parameters applicable for a PCD to PICC bit rate of f_c and $2f_c$		
PR	60°	Type A and Type B
ISI_d	0	Type A and Type B
ISI_m	1	Type A and Type B
Phase noise	0,0125	Type A and Type B

5 Apparatus and circuits for test of ISO/IEC 14443-1 and ISO/IEC 14443-2 parameters

5.1 Overview

This clause defines the test apparatus and test circuits for verifying the operation of a PICC or a PCD according to ISO/IEC 14443-1 and ISO/IEC 14443-2. The test apparatus includes the following:

a) measurement instruments (see 5.2);

b) calibration coils (see 5.3);

c) Test PCD assemblies (see 5.4);

d) Reference PICC and Active Reference PICC (see 5.5);

e) PICC transmission test setup (see 5.6);

f) EMD test setup (see 5.7).

These are described in the following subclauses.

5.2 Minimum requirements for measurement instruments — Oscilloscope

The digital sampling oscilloscope shall be capable of sampling at a rate of at least 500 million samples per second with a resolution of at least 8 bits at optimum scaling and shall have an overall minimum bandwidth of 250 MHz. The oscilloscope should have the capability to output the sampled data as a text file to facilitate mathematical and other operations such as windowing on the sampled data using computer programs (see Annex E and Annex F).

NOTE The overall bandwidth is the combination of oscilloscope and probing system bandwidth.

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5.3 Calibration coils

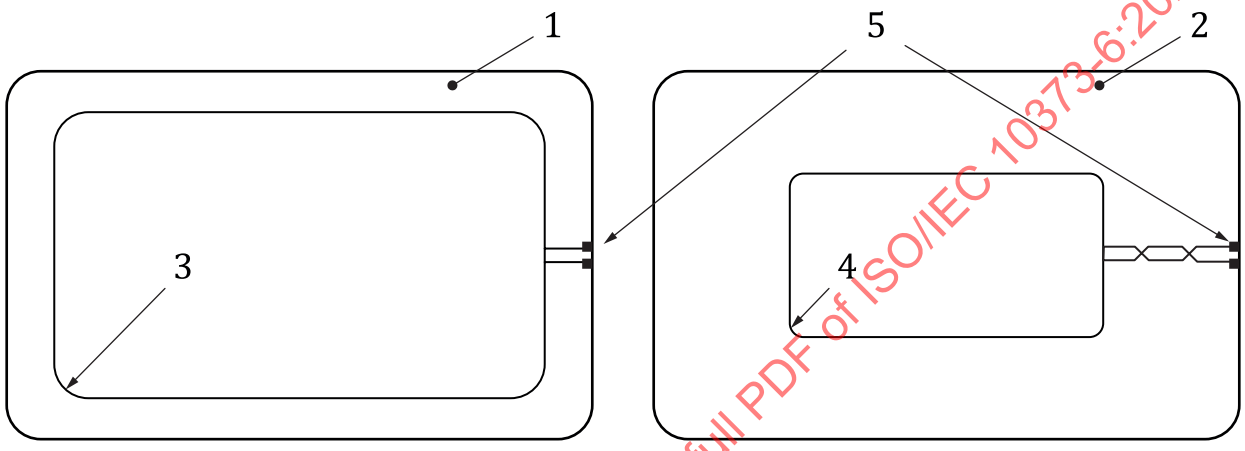
5.3.1 General

This subclause defines the size, thickness and characteristics of the calibration coils 1 and 2.

Calibration coil 1 shall be used only in Test PCD assembly 1 and calibration coil 2 shall be used only in Test PCD assembly 2.

5.3.2 Size of the calibration coil card

The calibration coil card shall consist of an area which has the height and width of an ID-1 type defined in ISO/IEC 7810 containing a single turn coil concentric with the card outline (see Figure 1).



Key

1 calibration coil 1 (ISO/IEC 7810 ID-1 outline)
2 calibration coil 2 (ISO/IEC 7810 ID-1 outline)
3 coil 72 × 42, 1 turn
4 coil 46 × 24, 1 turn
5 connections

NOTE Drawings are not to scale.

Figure 1 — Calibration coils 1 and 2

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5.3.3 Thickness and material of the calibration coil card

The thickness of the calibration coil card shall be less than that of an ID-1 card. It shall be constructed of a suitable insulating material.

5.3.4 Coil characteristics

The coil on the calibration coil card shall have one turn. Relative dimensional tolerance shall be ±2 %.

The outer size of the calibration coil 1 shall be 72 mm × 42 mm with corner radius 5 mm.

NOTE 1 The area over which the field is integrated is approximately 3 000 mm^2.

NOTE 2 At 13,56 MHz the approximate inductance is 250 nH and the approximate resistance is 0,4 Ω.

The open circuit calibration factor for the calibration coil 1 is 0,318 V (rms) per A/m (rms) [equivalent to 900 mV (peak-to-peak) per A/m (rms)].

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The outer size of the calibration coil 2 shall be 46 mm × 24 mm with corner radius 2 mm.

NOTE 3 The area over which the field is integrated is approximately 1 100 mm^2.

NOTE 4 At 13,56 MHz the approximate inductance is 140 nH and the approximate resistance is 0,3 Ω.

The open circuit calibration factor for the calibration coil 2 is 0,118 V (rms) per A/m (rms) [equivalent to 333 mV (peak-to-peak) per A/m (rms)].

The coil shall be made as a printed coil on printed circuit board plated with 35 µm copper. Track width shall be 500 µm with a relative tolerance of ±20 %. The size of the connection pads shall be 1,5 mm × 1,5 mm.

A high impedance oscilloscope probe with an input admittance equivalent to a parallel capacitance C_p < 14 pF and a parallel resistance R_p > 9 kΩ at 13,56 MHz shall be used to measure the (open circuit) voltage induced in the coil.

The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

5.4 Test PCD assemblies

5.4.1 General

Two Test PCD assemblies are defined:

a) Test PCD assembly 1 for PICCs of “Class 1”, “Class 2” and “Class 3” and for PICCs which do not claim conformance with a PICC class;

b) Test PCD assembly 2 for PICCs of “Class 4”, “Class 5” and “Class 6”.

Each Test PCD assembly shall consist of a circular Test PCD antenna directly connected to the suitable impedance matching network and two parallel sense coils, sense coil a and sense coil b, as shown in principle by Figure 2.

The purpose of the impedance matching network is to adapt the signal generator output impedance (Z = 50 Ω) to the antenna impedance. The linear low distortion variable output 50 Ω power driver shall be capable of producing a resulting field strength and Type A and Type B modulations suitable for all applicable tests.

WARNING — The Test PCD assembly definition does not include any measures to avoid overheating of components which may occur during certain tests. Heat dissipation aspects must be considered by the manufacturer.

The sense coils shall be connected such that the signal from one coil is in opposite phase to the other. The 10 Ω potentiometer P1 serves to fine adjust the balance point when the sense coils are not loaded by a PICC or any magnetically coupled circuit. The capacitive load of the probe including its parasitic capacitance shall be less than 14 pF.

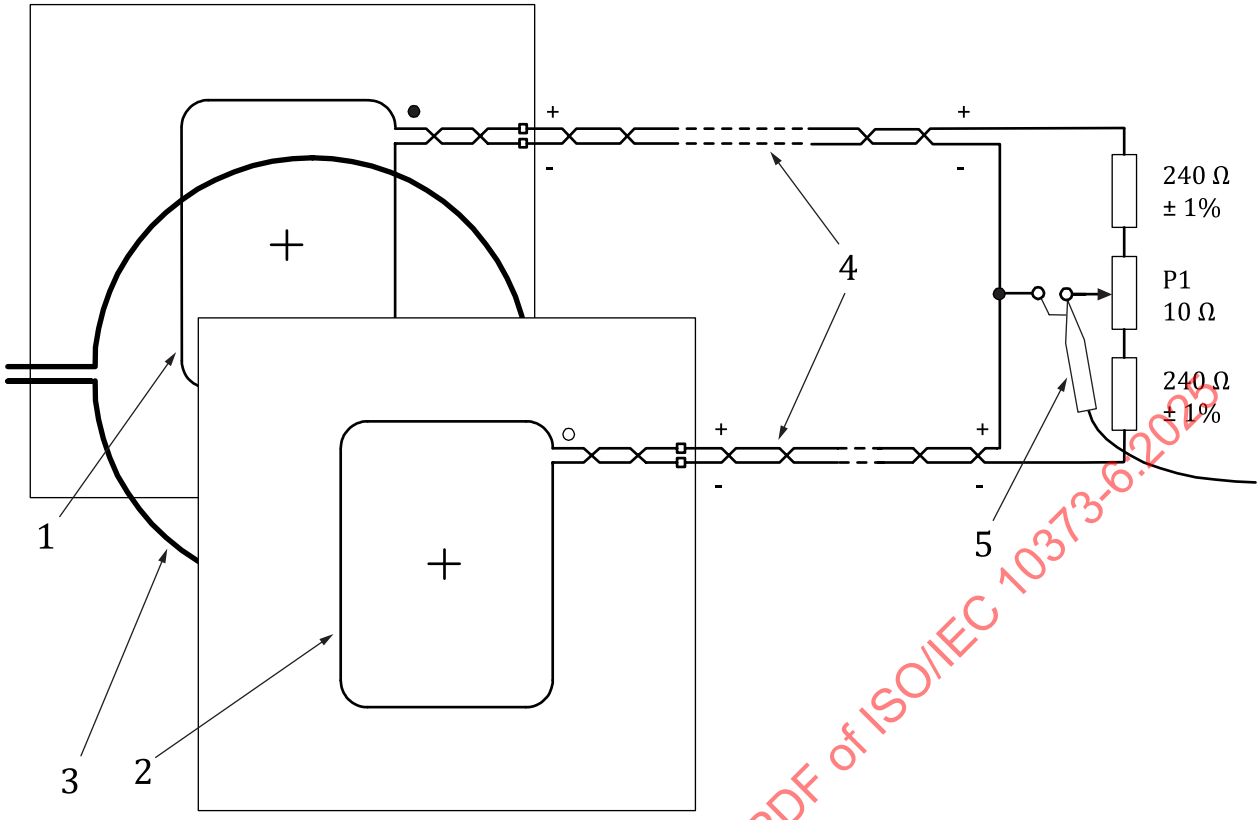
The capacitance of the connections and of the oscilloscope probe should be kept to a minimum for reproducibility.

In order to avoid any unintended misalignment in case of an unsymmetrical set-up the tuning range of the potentiometer P1 is only 10 Ω. If the set-up cannot be compensated by the 10 Ω potentiometer P1, the overall symmetry of the set-up should be checked.

The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

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Key

1 sense coil a
2 sense coil b
3 test PCD antenna
4 identical length twisted pairs or coaxial cables of less than 100 mm
5 probe connected to oscilloscope

Figure 2 — Test PCD assembly (principle)

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5.4.2 Test PCD antennas

The Test PCD antenna 1 for Test PCD assembly 1 shall have a diameter of 150 mm and include the impedance matching network 1.

The Test PCD antenna 2 for Test PCD assembly 2 shall have a diameter of 100 mm and include the impedance matching network 2.

Each Test PCD antenna construction and each impedance network circuitry is defined in Annex A.

The matching of each Test PCD antenna should be accomplished by using an impedance analyser or a network analyser or an LCR meter.

Unless otherwise specified, the impedance matching networks or their components values may be modified as long as not having negative impact on the test parameters and coverage.

5.4.3 Sense coils

In Test PCD assembly 1 the size of the sense coils 1 shall be 100 mm × 70 mm with corner radius 10 mm.

In Test PCD assembly 2 the size of the sense coils 2 shall be 60 mm × 47 mm with corner radius 10 mm.

Each sense coil construction shall conform to the corresponding drawings in Annex C.

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5.4.4 Mechanical construction of the Test PCD assemblies

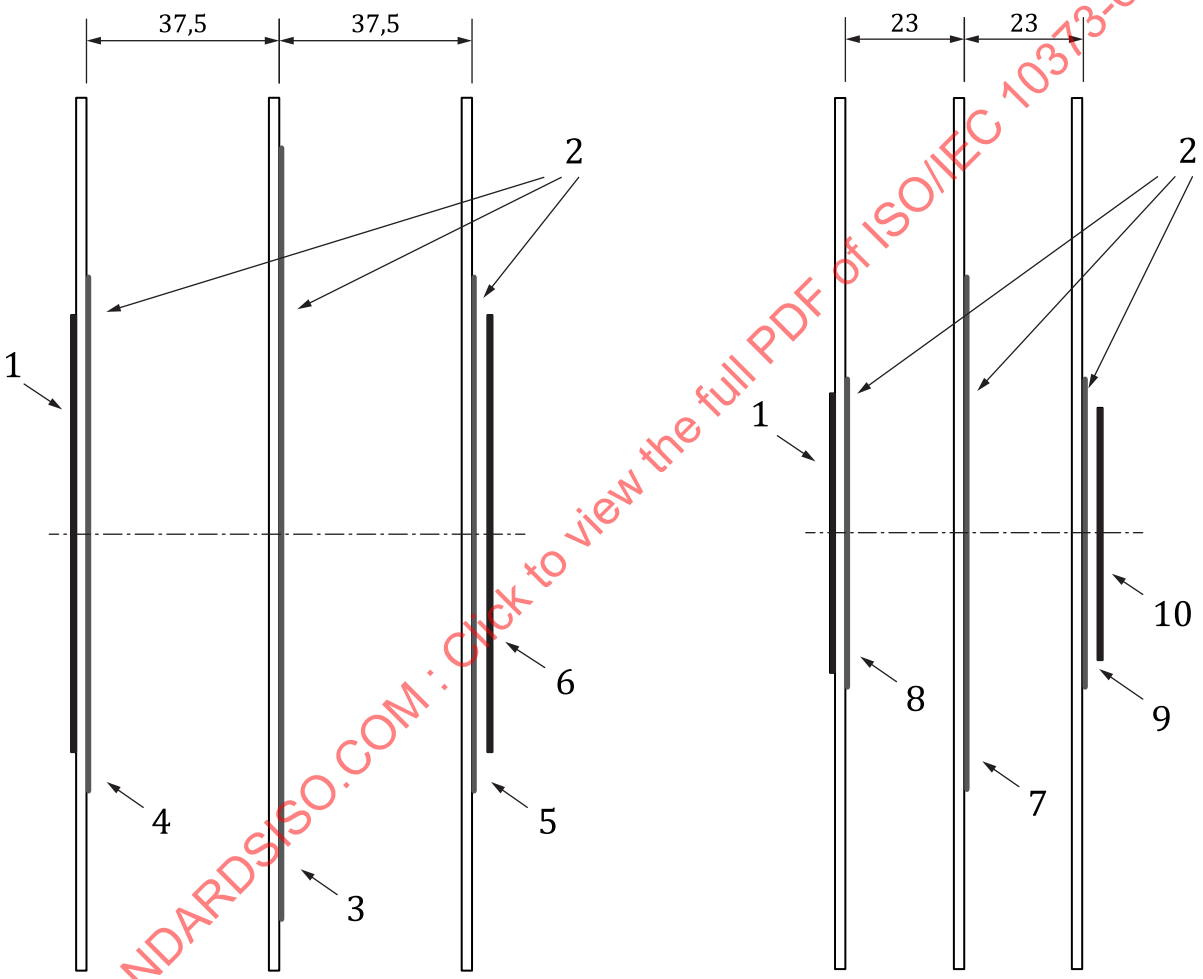
Test PCD assembly 1: The sense coils 1 and the Test PCD antenna 1 shall be assembled in parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 37,5 mm as illustrated in Figure 3 a).

Test PCD assembly 2: The sense coils 2 and the Test PCD antenna 2 shall be assembled in parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 23 mm as illustrated in Figure 3 b).

The dimensional tolerance shall be better than ±0,5 mm. The distance between the coil in the DUT and the calibration coil shall be equal with respect to the coil of the Test PCD antenna.

NOTE These distances are chosen to offer a strong and homogenous magnetic field in the DUT position.

Dimensions in millimetres



a) Test PCD assembly 1 **b) Test PCD assembly 2**

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Key

1 DUT
2 active conductors
3 test PCD antenna 1
4 sense coil 1a
5 sense coil 1b
6 calibration coil 1
7 test PCD antenna 2

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8 sense coil 2a
9 sense coil 2b
10 calibration coil 2

Figure 3 — Test PCD assembly 1 and Test PCD assembly 2

5.5 Reference PICC and Active Reference PICC

5.5.1 General

Two reference equipments are defined for testing PCDs:

a) the Reference PICC;

b) the Active Reference PICC.

5.5.2 Reference PICC

5.5.2.1 General

A Reference PICC is defined to test the ability of a PCD to

a) generate a field strength of at least H_{min} and not exceeding H_{max},

b) transmit a modulated signal to a PICC; and

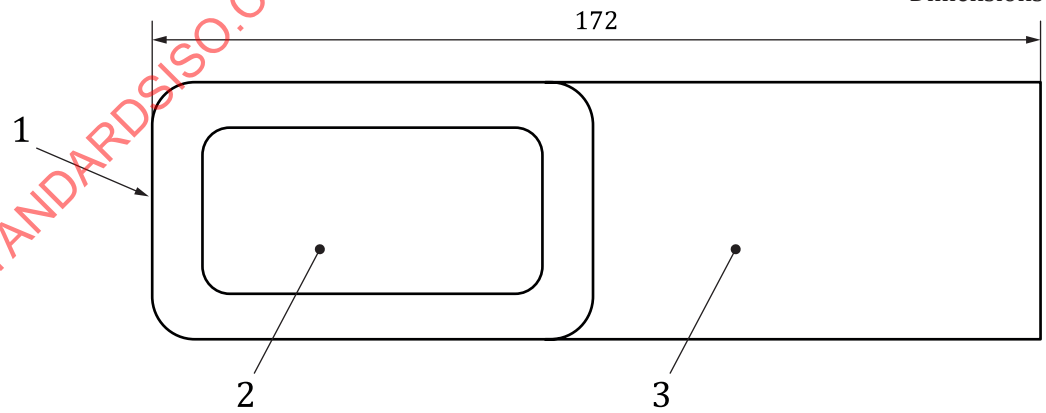
c) be immune against EMD signals from the PICC

in its operating volume.

5.5.2.2 Dimensions of the Reference PICC

The Reference PICC shall consist of an area containing the coils which has the height and width defined in ISO/IEC 7810 for ID-1 type. An area external to this, containing the circuitry which emulates the required PICC functions, shall be appended in such a way as to allow insertion into the test set-ups and so as to cause no interference to the tests. The dimensions shall be as shown in Figure 4.

Dimensions in millimetres



Key

1 outline ISO/IEC 7810 ID-1
2 location of coils
3 location of circuitry

Figure 4 — Reference PICC dimensions

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5.5.2.3 Reference PICC construction

The Reference PICCs coils layouts shall be as defined in D.1. If connectors are used between the coils and the circuitry, those connectors shall have minimal, if any, effect on the RF measurements.

The Reference PICC shall have a circuit diagram as defined in Figure 5 and component values as defined in Table 8.

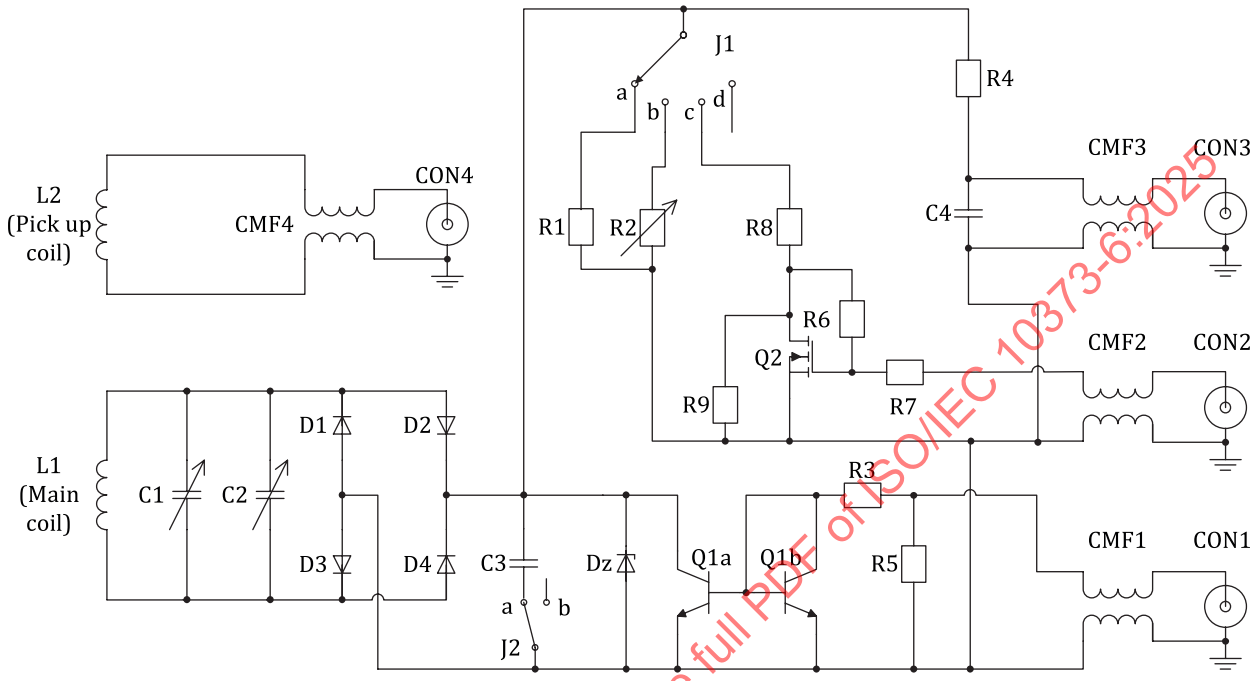


Figure 5 — Reference PICC circuit diagram

NOTE Position "d" of jumper J1 is RFU.

Table 8 — Reference PICC components list

Component	Value	Component	Value
L1	As defined in D.1	C1	7 pF – 50 pF[b]
L2	As defined in D.1	C2	3 pF – 10 pF[b]
R1	1,8 kΩ	C3	27 pF
R2	0 kΩ – 2 kΩ[a]	C4	1 nF
R3	220 Ω	D1, D2, D3, D4	BAR43S or equivalent[c]
R4	51 kΩ	Dz	BZX84, 15 V or equivalent[c]
R5	51 Ω	Q1a, Q1b	BCV61A or equivalent
R6	500 kΩ	Q2	BSS83 or equivalent
R7	110 kΩ	CMF1, CMF2, CMF3, CMF4	ACM3225-102-2P or equivalent
R8	51 Ω	CON1, CON2, CON3, CON4	RF connector
R9	1,5 kΩ		

[a] A multi-turn potentiometer (turns ≥10) should be used.

[b] Q-factor shall be higher than 100 at 13,56 MHz.

[c] Care should be taken on parameters Cj (junction capacitance), Cp (package capacitance), Ls (series inductance) and Rs (series resistance) of equivalent diodes. Note that these values could be unavailable in the datasheet.

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At CON1 the load modulation signal shall be applied. The load modulation can be determined in Test PCD assembly. When not used, the load modulation signal generator shall be disconnected or set to 0 V.

With the voltage at CON2 the Reference PICC load can be adjusted until the required DC voltage shows at CON3.

The Reference PICC DC voltage shall be measured at CON3 using a high impedance voltmeter and the connection wires should be twisted or coaxial.

The PCD waveform parameters are picked up at CON4 using a high impedance oscilloscope probe. The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

Position "a" of J2 shall be used for testing bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$.

Position "b" of J2 shall be used for testing bit rates of $f_c/8$, $f_c/4$ and $f_c/2$.

5.5.2.4 Reference PICC resonance frequency tuning

The Reference PICC resonance frequency shall be calibrated with the following procedure.

a) Set jumper J1 to position "a".

b) Connect the calibration coil directly to a signal generator and the Reference PICC CON3 to a high impedance voltmeter. Connect all the other connectors to the same equipment as used for the tests.

c) Locate the Reference PICC at a distance d = 10 mm above the calibration coil with the axes of the two coils (calibration coil and Reference PICC main coil) being congruent (see Figure 6).

d) Drive the calibration coil with a sine wave set to the desired resonance frequency.

e) Adjust the Reference PICC capacitors C1 and C2 to get maximum DC voltage at CON3.

f) Adjust the signal generator drive level to obtain a DC voltage at CON3 of V_{load} as defined in Table 12.

g) Repeat steps e) and f) until the maximum voltage after step e) is V_{load}.

h) Calibrate the Test PCD assembly to produce the H_{min} operating condition on the calibration coil.

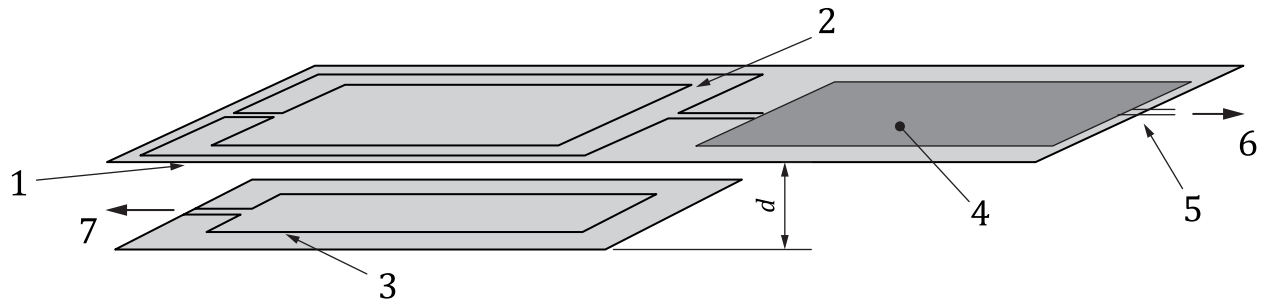
i) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position "b" and adjust R2 to obtain a DC voltage of V_{load} measured at CON3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

j) Repeat steps b) to g) with the obtained value of R2.

Instead of a signal generator, a vector network analyser may be used if sufficient power is provided to produce V_{load} at CON3 while reaching the maximum resistive part of the measured complex impedance of the calibration coil.

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Key

1 main coil (bottom side)
2 pick up coil (top side)
3 calibration coil (top side)
4 reference PICC circuitry
5 CON3
6 to voltmeter
7 to signal generator
d distance (see procedure above)

NOTE Drawing is not to scale.

Figure 6 — Reference PICC frequency tuning set-up (principle)

5.5.3 Active Reference PICC

5.5.3.1 General

An Active Reference PICC is defined to test the ability of a PCD to receive a load modulation signal from the PICC in its operating volume.

5.5.3.2 Dimensions of the Active Reference PICC

See 5.5.2.2.

5.5.3.3 Active Reference PICC construction

The Active Reference PICC's coils layouts shall be as defined in D.2. If connectors are used between the coils and the circuitry, those connectors shall have minimal, if any, effect on the RF measurements.

The Active Reference PICC shall have a circuit diagram as defined in Figure 7 and component values as defined in Table 9. Input and output connectors are described in Table 10.

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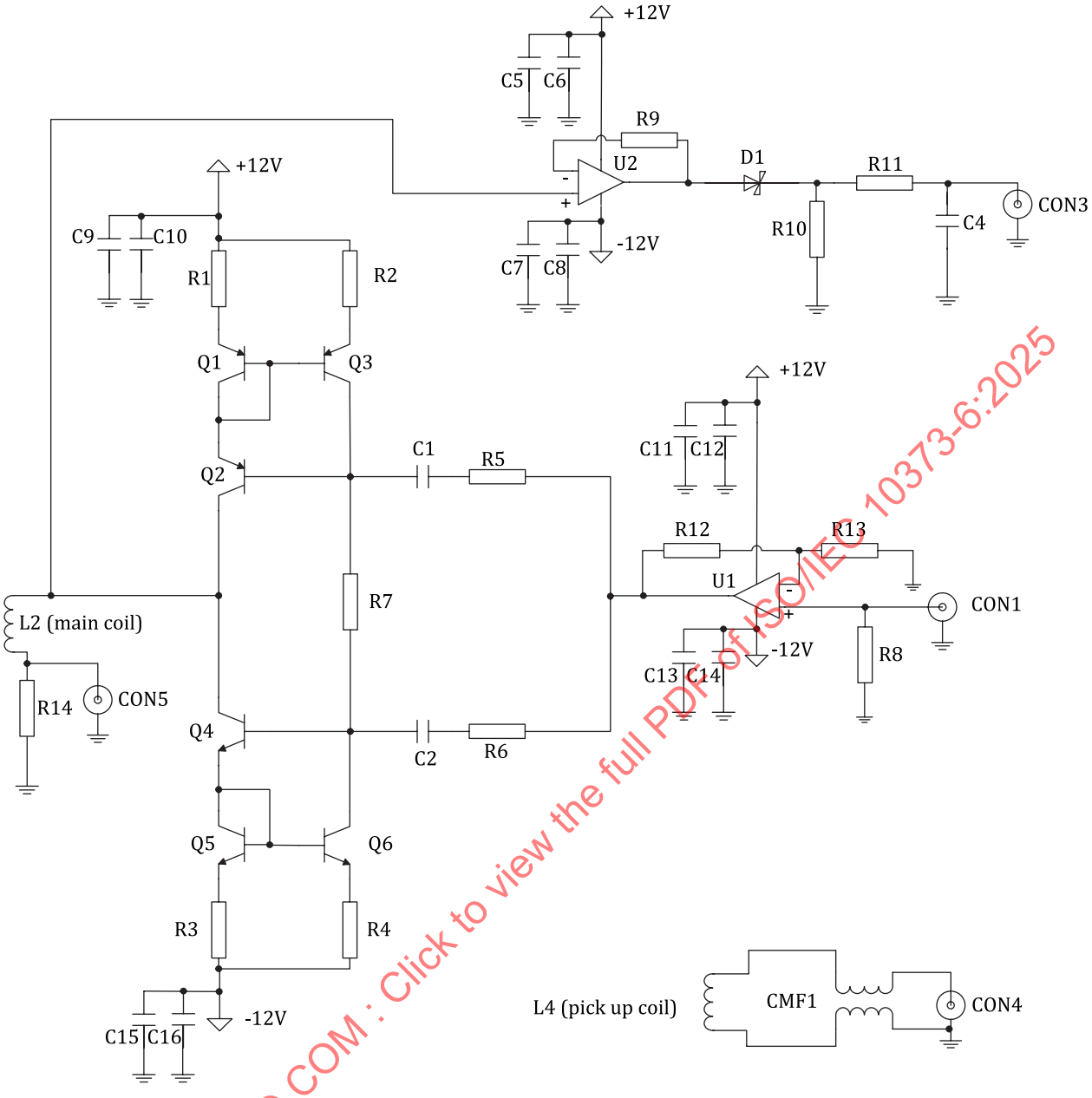


Figure 7 — Active Reference PICC circuit diagram

The resistor R14 should be placed as close as possible to the antenna coil.

Table 9 — Active Reference PICC components list

Component	Value	Power dissipation	Component	Value
R1, R3	10 Ω	235 mW	C1, C2, C4	1 nF
R2, R4, R5, R6	100 Ω	<50 mW	D1	BAT54 or equivalent
R7	1,3 kΩ	250 mW	Q1, Q2, Q3	BD136 or equivalent
R8	50 Ω	250 mW	Q4, Q5, Q6	BD135 or equivalent
R9	1,8 kΩ	<50 mW	U1, U2	THS3091 or equivalent

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Table 9 *(continued)*

Component	Value	Power dissipation	Component	Value
R10, R11	1,5 kΩ	<50 mW	C5, C7, C9, C11, C13, C15	4,7 µF
R12, R13	1,2 kΩ	<50 mW	C6, C8, C10, C12, C14, C16	100 nF
R14	0,5 Ω	<50 mW		

Table 10 — Active Reference PICC Input/Output connector description

Connector	Input/Output	Description
CON1	Input	Generation of the Active Reference PICC transmission and unmodulated state US (loading effect).
CON3	Output	Image of the field received when the Active Reference PICC does not transmit (DC voltage).
CON4	Output	PCD carrier extraction.
CON5	Output	Image of the field transmitted by the Active Reference PICC.

The Active Reference PICC received DC voltage shall be measured at CON3 using a high impedance voltmeter and the connection wires should be twisted or coaxial.

High impedance oscilloscope probes shall be used to pick up the signals at CON4 and CON5.

5.6 PICC transmission test setup

5.6.1 General description

The PICC transmission test setup contains:

a) a signal generator with low phase noise, which is used to generate an RF carrier field and to synthesize PCD test commands sent to the DUT;

b) the Test PCD assembly;

c) a signal amplitude analysing device made of a signal acquiring device (e.g. an oscilloscope) and the PCD phase stability analysis tool defined in Annex M.

The signal amplitude analysing device shall be able to carry out instantaneous phase versus time measurements with fixed frequency, high dynamic range, low measurement uncertainty and high time resolution. See 5.2 for minimum requirements on the amplitude analysing device.

5.6.2 Phase stability precondition test

5.6.2.1 Purpose

In order to guarantee an RF field with high frequency stability, a phase stability test shall be performed and passed successfully by the PICC transmission test setup. The aim of this precondition test is to verify that the test apparatus used for PICC transmission measurements provides a signal frequency with high stability.

The phase stability test is passed if the maximum phase drift is smaller than 6° when measured as described in 5.6.2.2.

NOTE This maximum phase drift value for the phase stability test covers the measurement uncertainty and noise as well as component fabrication tolerances and temperature dependencies.

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5.6.2.2 Test procedure

Perform the following steps to assess the instantaneous phase and compute its maximum phase drift at least at H_{min} and H_{max}.

a) Tune the Reference PICC 1 to 13,56 MHz as described in 5.5.2.4.

b) Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil.

c) Place the Reference PICC 1 into the DUT position on the Test PCD assembly, set jumper J1 to position 'b' and adjust R2 to obtain a voltage of V_{load} at CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a voltage of V_{load} at CON3. In both cases the operating field condition shall be verified by monitoring the voltage in the calibration coil and adjusting if necessary.

d) Record the non-modulated RF carrier signal of the pick up coil for a time period of at least 25 ms.

e) Compute the maximum phase drift from the instantaneous phase using the PCD phase stability analysis tool defined in Annex M. Check if the maximum phase drift of the instantaneous phase is always smaller than the value specified in 5.6.2.1.

5.6.2.3 Test report

The test report shall contain the maximum phase drift of the PICC transmission test setup and shall state whether the requirements have been fulfilled.

5.7 EMD test setup

5.7.1 General description

The EMD test setup contains the following:

a) a signal generator with low phase noise, which is used to synthesize both an EMD test pattern and PCD test commands sent to the DUT;

b) the Test PCD assembly;

c) a signal amplitude analysing device:

   1) either a signal acquiring device (e.g. oscilloscope) and appropriate computation software;

   2) or a spectrum analyser (see additional constraints in 5.7.2).

The signal amplitude analysing device shall be able to carry out power versus time measurements with fixed frequency, fixed bandwidth, high dynamic range, low measurement uncertainty and high time resolution.

The PICC EMD tests may be performed using the RF output signal of a commercial PCD. The PCD EMD test may use a PICC emulator to generate the EMD test pattern.

5.7.2 Computation of power versus time

The beginning of the captured signal shall be windowed by a Bartlett window of exactly two subcarrier cycles. Fourier transformation of these windowed samples produces one power value. By shifting the Bartlett window by steps of $1/f_c$ from the beginning to the end of the captured signal, the desired power versus time result is finally computed.

NOTE The resulting 3 dB bandwidth of the above described window is 531 kHz and its noise equivalent bandwidth amounts to 843 kHz.

The computation of the power versus time shall be performed at $f_c + f_s$ and $f_c - f_s$, using a scaling such that a pure sinusoidal signal results in its peak magnitude. An example of computation is provided in Annex J.

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In case of using a spectrum analyser, the equipment shall have at least an equivalent analysis bandwidth. It shall pass the noise floor precondition test, as defined in 5.7.3, and there shall be some additional margin of $10/f_c$ on $t_{E,\,PICC}$ requirement and no spikes above the EMD limit.

5.7.3 Noise floor precondition test

5.7.3.1 Purpose

In order to ensure a high dynamic range and sufficient sensitivity, a noise floor measurement shall be performed and passed successfully by the EMD test setup. The aim of this precondition test is to verify that the test apparatus used for EMD level measurement satisfies a minimum noise requirement.

The noise floor test is passed if the noise standard deviation is at least three times smaller than the EMD limit $V_{E,\,PICC}$, when measured as described in 5.7.3.2.

The noise standard deviation is determined by calculating the root-mean-square value of the results of the Fourier transformation, as described in 5.7.2.

NOTE This noise floor can be obtained either with a 14-bit digitizer at a sampling rate of 100 million samples per second or with an 8-bit digital oscilloscope at sampling rate of 1 000 million samples per second.

5.7.3.2 Procedure

Perform the following steps to assess the noise floor at least at H_{min} and H_{max}.

a) Tune the Reference PICC 1 to 13,56 MHz.

b) Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil.

c) Place the Reference PICC 1 into the DUT position on the Test PCD assembly, set jumper J1 to position "b" and adjust R2 to obtain a voltage of V_{load} at CON3. Alternatively, jumper J1 may be set to position "c" and the applied voltage on CON2 is adjusted to obtain a voltage of V_{load} at CON3. In both cases the operating field condition shall be verified by monitoring the voltage in the calibration coil and adjusted if necessary.

d) Record the signal of the sense coils for a time period of at least 250 µs.

e) Compute the noise standard deviations at $f_c + f_s$ and $f_c - f_s$ using suitable computer software, as e.g. the one given in Annex J. Check if these noise standard deviations are three times smaller than $V_{E,\,PICC}$.

5.7.3.3 Test report

The test report shall state the noise standard deviations at $f_c + f_s$ and $f_c - f_s$ and shall state whether the requirements have been fulfilled.

6 Test of ISO/IEC 14443-1 parameters

6.1 PCD test for alternating magnetic fields

6.1.1 Purpose

This test determines that the PCD generates a field not higher than the average value specified in ISO/IEC 14443-1 for each PICC class.f

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6.1.2 Procedure

Apply the following procedure with each Reference PICC:

a) Tune the Reference PICC to 19 MHz as described in 5.5.2.4 steps a) to g).

b) Calibrate the Test PCD assembly (see Table 11) to produce the average field value specified in ISO/IEC 14443-1:2018, 4.4 on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly (see Table 11). Switch the jumper J1 to position "b" and adjust R2 to obtain a DC voltage of 3 V measured at CON3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary. The R2 value should be between $R2_{min}$ and $R2_{max}$ as defined in Table 11.

d) Search for the maximum DC voltage at CON3 by moving and rotating the Reference PICC on the PCD surface, starting from Position 0 as defined in Table 3. The DC voltage at CON3 shall not exceed 3 V.

   WARNING — The maximum is usually not obtained in Position 0 as defined in Table 3 but rather in a position where the PICC main coil conductors (traces) maximally overlap the PCD antenna conductors. This position with the maximum DC voltage at CON3 could be out of the PCD operating volume as defined for each PICC class in ISO/IEC 14443-2.

   WARNING — If the PCD field is not continuously emitted, the DC voltage measurement shall be done when the PCD field is present.

e) If exceeded, use the same conversion factor to measure the maximum and average DC voltage and convert in field strength to check the maximum and the average field values specified in ISO/IEC 14443-1:2018, 4.4.

Table 11 — R2 value for alternating magnetic field test

Reference PICC	$R2_{min}$	$R2_{max}$	Test PCD assembly
1	56 Ω	68 Ω	Test PCD assembly 1
2	97 Ω	119 Ω	Test PCD assembly 1
3	100 Ω	122 Ω	Test PCD assembly 1
4	84 Ω	102 Ω	Test PCD assembly 2
5	76 Ω	92 Ω	Test PCD assembly 2
6	88 Ω	108 Ω	Test PCD assembly 2

6.1.3 Test report

The test report shall give the DC voltage measured at CON3 for each Reference PICC. The test result is PASS only if the PCD meets the requirements given by the last two steps of the procedure in 6.1.2 for each Reference PICC, otherwise the test result is FAIL.

6.2 PICC test for alternating magnetic fields

6.2.1 Purpose

The purpose of this test is to check the behaviour of the PICC in relation to alternating magnetic field exposure at 13,56 MHz.

6.2.2 Apparatus

The Test PCD assembly shall be used to produce the alternating magnetic field.

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6.2.3 Procedure

The procedure is as follows.

a) In accordance with the PICC class, adjust the RF power delivered by the signal generator to the Test PCD antenna to a field strength of the average level specified in ISO/IEC 14443-1:2018, 4.4 as measured by the calibration coil.

b) Place the DUT in the DUT position and readjust immediately the RF drive into the Test PCD antenna to the required field strength if necessary.

c) After 5 min, remove the PICC from the DUT position for at least 5 s.

d) In accordance with the PICC class, adjust the RF power delivered by the signal generator to the Test PCD antenna to a field strength of the maximum level specified in ISO/IEC 14443-1:2018, 4.4 as measured by the calibration coil.

e) Place the DUT in the DUT position and readjust immediately the RF drive into the Test PCD antenna to the required field strength if necessary.

f) Apply for 5 min an ASK 100 % modulation to this field with the following duty cycle:

   1) 5 s at 0 A/m (rms);

   2) 25 s at the maximum level specified in ISO/IEC 14443-1:2018, 4.4, in accordance with the PICC class.

g) Wait for 30 s at 0 A/m (rms).

h) Check that the PICC operates as intended. This check should be done at least by successfully executing PICC transmission test defined in 7.2.1.

6.2.4 Test report

The test report shall state whether or not the PICC operates as intended.

6.3 PXD tests

PCD and PICC tests shall be applied as follows:

a) when the PXD is in PCD Mode, tests defined in 6.1 shall be applied;

b) when the PXD is in PICC Mode, tests defined in 6.2 shall be applied.

In automatic mode alternation, the PXD may be forced into the required mode.

7 Test of ISO/IEC 14443-2 parameters

7.1 PCD tests

All the PCD tests described below will be done in the operating volumes as defined by the PCD manufacturer for each supported PICC class.

All PCD tests of ISO/IEC 14443-2 parameters shall be performed using Reference PICCs 1, 2 and 3 and optionally other Reference PICCs corresponding to the optional PICC classes supported by the PCD, with the relevant parameters and Test PCD assembly as defined in Table 12.

NOTE 2 The PCD field strength supporting operation with PICC Class 1, which was defined in former editions of this document, is no longer present.

NOTE 3 The power transfer PCD to PICC test, which was defined in former editions of this document, is no longer present.

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Table 12 — PICC classes parameters

PICC class	Reference PICC	H_{min} test			H_{max} test		Test PCD assembly
		V_{load}	$R2_{min}$	$R2_{max}$	$R2_{min}$	$R2_{max}$	
1	1[a]	4,5 V	647 Ω	791 Ω	76 Ω	94 Ω	Test PCD assembly 1
2	2	4,5 V	1 030 Ω	1 260 Ω	112 Ω	138 Ω	Test PCD assembly 1
3	3	4,5 V	1 080 Ω	1 320 Ω	117 Ω	143 Ω	Test PCD assembly 1
4	4	4,5 V	990 Ω	1 210 Ω	99 Ω	121 Ω	Test PCD assembly 2
5	5	4,5 V	960 Ω	1 170 Ω	103 Ω	127 Ω	Test PCD assembly 2
6	6	4,5 V	700 Ω	900 Ω	117 Ω	143 Ω	Test PCD assembly 2

[a] The PCD should be tested with a V_{load} of 6 V for Reference PICC 1 to ensure interoperability with PICCs conformant with the V_{load} requirement referenced in ISO/IEC 10373-6:2020, where Class 1 defines $R2_{min}$ as 870 Ω and $R2_{max}$ as 1 070 Ω for Test PCD assembly 1.

7.1.1 PCD field strength

7.1.1.1 Purpose

This test measures the field strength produced by a PCD in its operating volume. The maximum and minimum field strength values to be used with each Reference PICC are given in ISO/IEC 14443-2:2020, Table 1.

NOTE 1 The test takes account of PICC loading of the PCD.

7.1.1.2 Procedure

7.1.1.2.1 Procedure for H_{max} test

a) Tune the Reference PICC to 19 MHz as described in 5.5.2.4 steps a) to g).

b) Calibrate the Test PCD assembly to produce the H_{max} operating condition on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position "b" and adjust R2 to obtain a DC voltage of 3 V measured at CON3. Alternatively, jumper J1 may be set to position "c" and the applied voltage on CON2 is adjusted to obtain a DC voltage of 3 V at CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

   The R2 value should be between $R2_{min}$ and $R2_{max}$ as defined in H_{max} test columns in Table 12. Check this range at least once before using the alternative method.

d) Position the Reference PICC within the defined operating volume of the IUT. The DC voltage at CON3 shall not exceed 3 V. If the PCD field is not continuously emitted, the DC voltage measurement shall be done when the PCD field is present.

7.1.1.2.2 Procedure for H_{min} test

a) Tune the Reference PICC to 13,56 MHz as described in 5.5.2.4.

b) Place the Reference PICC into the DUT position on the Test PCD assembly producing the H_{min} operating condition on the calibration coil. Check that the jumper J1 is set to position "b" and that a DC voltage of V_{load} as defined in Table 12 is measured at CON3. Alternatively, the jumper J1 may be set to position "c" and the voltage on CON2 is adjusted to obtain a DC voltage of V_{load} as defined in Table 12 at CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

   WARNING — R2 value should be between $R2_{min}$ and $R2_{max}$ as defined in H_{min} test columns in Table 12. Check this range at least once before using the alternative method.

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c) Position the Reference PICC within the defined operating volume of the IUT. The DC voltage at CON3 shall exceed V_{load} as defined in Table 12. If the PCD field is not continuously emitted, the DC voltage measurement shall be done when the PCD field is present.

d) For Reference PICC 1 repeat:

1) step b) with a DC voltage V_{load} of 6 V measured at CON3 instead of V_{load} as defined in Table 12; and

2) step c), where the DC voltage at CON3 shall exceed 5,3 V [corresponding to H_{min} – 0,2 A/m (rms)], instead of V_{load} as defined in Table 12.

7.1.1.3 Test report

The test report shall confirm the operating volume in which the DC voltage measured at CON3 for R2 or variable load resistor adjusted to H_{min} and H_{max} field strength fulfills the requirements defined in step d) of 7.1.1.2.1 and in step c) and step d) of 7.1.1.2.2.

7.1.2 Modulation index *m* and waveform

7.1.2.1 Purpose

This test is used to determine the index of modulation of the PCD field as well as the rise and fall times and the overshoot values as defined in ISO/IEC 14443-2 for all supported PCD to PICC bit rates.

7.1.2.2 Procedure

a) Position the calibration coil at an arbitrary position in the defined operating volume and display the induced coil voltage on a suitable oscilloscope. Determine the modulation index *m* and waveform characteristics using the analysis tool defined in Annex E.

b) Tune the Reference PICC to 16,5 MHz as described in 5.5.2.4 steps a) to g) and switch the jumper J1 to position "c".

c) Switch the jumper J2 to position "a" or to position "b" according to the tested PCD to PICC bit rate and place the Reference PICC at a particular position in the PCD operating volume.

d) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at CON3 of V_{load} as defined in Table 12. If a DC voltage of V_{load} cannot be reached at the selected position, the maximum achievable voltage should be used for the test.

e) If the unmodulated voltage on CON4, measured with a suitable oscilloscope (requirements see 5.2) is below 1 V (peak-to-peak), use an alternative pick up coil to determine the waveform characteristic. This alternative pick up coil should have a “figure 8” shape with 15 mm radius positioned farthest away from the Reference PICC to minimize coupling and as close as possible to the PCD antenna to maximize induced voltage.

f) Determine the modulation index *m* and waveform characteristic from the voltage at CON4 or at the alternative pick up coil using the analysis tool defined in Annex E.

g) Repeat steps c) to f) for various positions within the operating volume and all supported PCD to PICC bit rates.

NOTE 1 The selected position of the calibration coil within the operating volume is not expected to affect the results.

NOTE 2 The Reference PICC load does not represent the worst case loading effect of a PICC. Higher loading effects can be achieved with resonance frequencies closer to carrier frequency (e.g. 15 MHz or 13,56 MHz).

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7.1.2.3 Test report

The test report shall give the measured modulation index m of the PCD field, the rise and fall times and overshoot values, within the defined operating volume in unloaded and loaded conditions.

7.1.3 Phase stability test

7.1.3.1 Purpose

The purpose of this test is to determine whether the PCD provides f_c with a phase drift within the limit defined in ISO/IEC 14443-2.

7.1.3.2 Test procedure

a) Tune the Reference PICC 1 to 13,56 MHz as described in 5.5.2.4.

b) Place the Reference PICC 1 at an arbitrary position in the PCD operating volume, set jumper J1 to position "b" and adjust R2 to obtain a voltage of V_{load} (see Table 12) at CON3. Alternatively, jumper J1 may be set to position "c" and the applied voltage on CON2 is adjusted to obtain a voltage of V_{load} at CON3.

c) Record the signal of the pick up coil for a time period of at least 25 ms.

d) Compute the maximum phase drift from the instantaneous phase using the PCD phase stability analysis tool defined in Annex M. Check if the maximum phase drift of the instantaneous phase is smaller than the limit specified in ISO/IEC 14443-2:2020, 8.2.5.2.

7.1.3.3 Test report

The test report shall contain the maximum phase drift of the PCD.

The used test conditions shall be mentioned in the test report.

7.1.4 Load modulation reception for PICC to PCD bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$

7.1.4.1 Purpose

This test is used to verify that a PCD correctly detects the load modulation of a PICC which conforms to ISO/IEC 14443-2 for PICC to PCD bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$, if supported.

In order to limit the testing time, only the highest PICC to PCD bit rate corresponding to every supported subcarrier f_s shall be tested.

7.1.4.2 General description

For the load modulation reception test the Active Reference PICC uses the principle of active load modulation to modify the field generated by the PCD.

The active load modulation signal of the Active Reference PICC shall be strictly synchronous to the PCD generated field. The pick up coil voltage on CON4, an alternative pick up coil [see 7.1.4.2, step e)], the main coil current on CON5 or any other mean may be used to synchronize the Active Reference PICC active load modulation signal generating device to the PCD RF field. It is recommended to perform synchronization during time periods when neither the PCD nor the Active Reference PICC modulates the RF field. During the Active Reference PICC response, the Active Reference PICC phase reference shall not vary more than 3° from the $\emptyset_{LM,\ INIT}$ value when it was synchronized; if synchronization is done much before the Active Reference PICC response, care shall be taken to limit the possible phase drift until the start of the Active Reference PICC response.

The active load modulation signal shall be generated such that the load modulation signal envelope observed at the load modulation test circuit of Figure 2 has a sinusoidal shape without phase jumps.

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7.1.4.3 Precondition test

Perform the following steps to verify the synchronous functionality of the Active Reference PICC:

a) Place the Active Reference PICC in the DUT position of the Test PCD assembly.

b) Calibrate the Test PCD assembly to produce any field strength operating condition in the range of [H_{min}, H_{max}] on the calibration coil.

c) Adjust the load of the Active Reference PICC to the equivalent load defined for the Reference PICC (with V_{load} DC voltage at Reference PICC CON3 as defined in Table 12 as setup at H_{min}) having the same antenna class by applying a constant carrier signal to connector CON1, adjusting first its phase in order to achieve destructive interference and then its amplitude. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary. Note the Active Reference PICC CON3 DC voltage corresponding to the field condition.

d) Send a command with the Test PCD assembly.

e) The Active Reference PICC shall respond strictly synchronously, i.e., with a theoretical $\emptyset_{LM,\ INTER}$ of 0° and a constant $\emptyset_{LM,\ INIT}$ between multiple responses. The Active Reference PICC shall respond with a 256 byte frame at a PICC to PCD bit rate of $f_c/128$.

f) Display the whole Active Reference PICC response of both, calibration coil and load modulation test circuit, including at least 200 carrier periods before the first and 20 carrier periods after the last modulation of the Active Reference PICC on the signal acquiring device and store the sampled data of calibration coil and load modulation test circuit in separate files for analysis by the PICC amplitude and phase drift analysis tool defined in Annex N.

g) Repeat steps d) to f) 24 times.

The precondition test is PASS when the Active Reference PICC response $\emptyset_{LM,\ INTER}$ is less than ±3° and its $\emptyset_{LM,\ INIT}$ maximum variation is less than ±3° over 24 responses.

7.1.4.4 Test conditions

7.1.4.4.1 General

This test shall be done at ambient, minimum and maximum temperatures. If minimum and maximum temperatures are not provided in PCD test conditions, load modulation reception test shall be performed only at ambient temperature.

Figure 8 to Figure 13 illustrate the test conditions which are specific for the communication signal interface and PICC to PCD bit rate.

a) The top plot shows the Active Reference PICC carrier signal:

   1) Active Reference PICC carrier transmission, equivalent to state MS1, is shown as a black coloured bar;

   2) inverse Active Reference PICC carrier transmission, equivalent to state MS2, is shown as grey coloured bar; and

   3) no Active Reference PICC carrier transmission, equivalent to state US, is shown in white colour.

b) The bottom plot shows the phase signal also including the interstate phase drift (grey dashed line) over time.

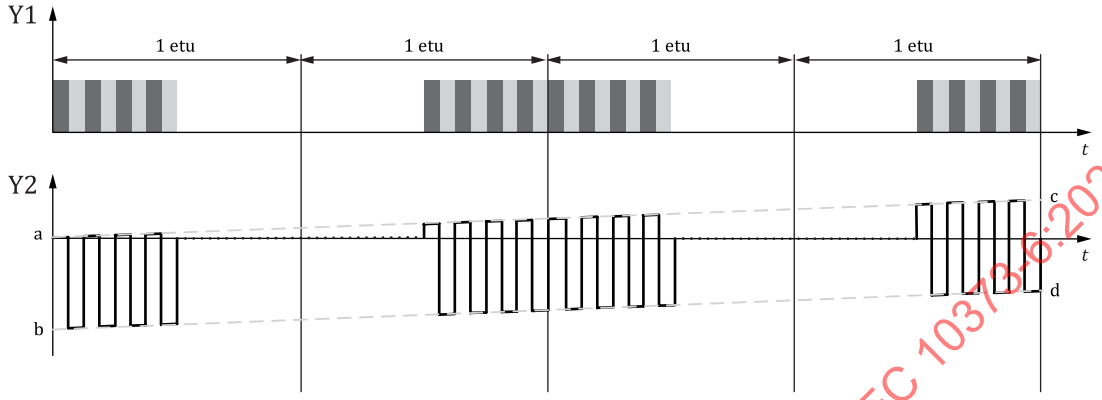
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7.1.4.4.2 Test conditions for Type A for a PICC to PCD bit rate of $f_c/128$

Four phase drift conditions are defined within limits defined in ISO/IEC 14443-2.

a) Phase drift condition A1: Constant interstate phase drift of $Ø_{LM,\ INTER,\ PCD}$ over the complete Active Reference PICC response, active load modulation transmission during state MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2. For an example see Figure 8.



Key

Y_1 amplitude

Y_2 phase (degree)

a $Ø_{LM,\ INIT}$.

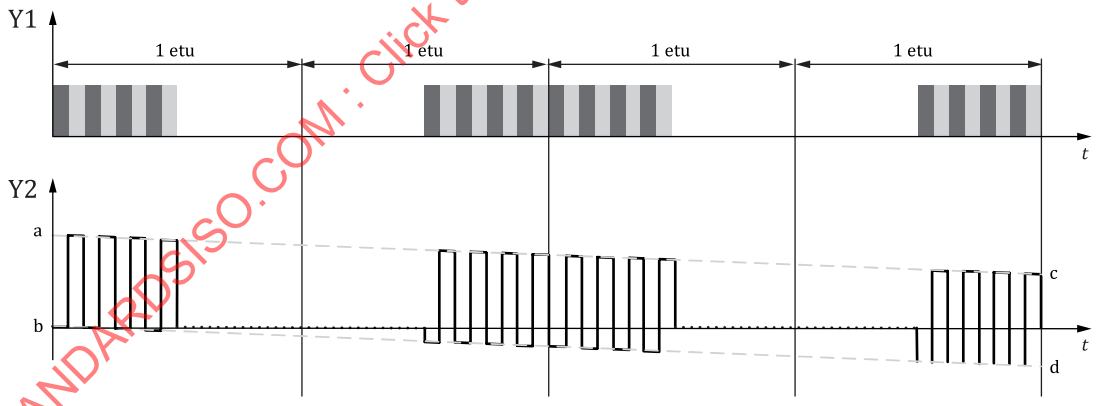
b $Ø_{LM,\ INIT} - 180°$.

c $Ø_{LM,\ INIT} + Ø_{LM,\ INTER,\ PCD}$.

d $Ø_{LM,\ INIT} - 180° + Ø_{LM,\ INTER,\ PCD}$.

Figure 8 — Example of phase drift condition A1 for Type A at a PICC to PCD bit rate of $f_c/128$

b) Phase drift condition A2: Constant phase interstate drift of $-Ø_{LM,\ INTER,\ PCD}$ over the complete Active Reference PICC response, active load modulation transmission during state MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2. For an example see Figure 9.



Key

Y_1 amplitude

Y_2 phase (degree)

a $Ø_{LM,\ INIT} + 180°$.

b $Ø_{LM,\ INIT}$.

c $Ø_{LM,\ INIT} + 180° - Ø_{LM,\ INTER,\ PCD}$.

d $Ø_{LM,\ INIT} - Ø_{LM,\ INTER,\ PCD}$.

Figure 9 — Example of phase drift condition A2 for Type A at PICC to PCD bit rate of $f_c/128$

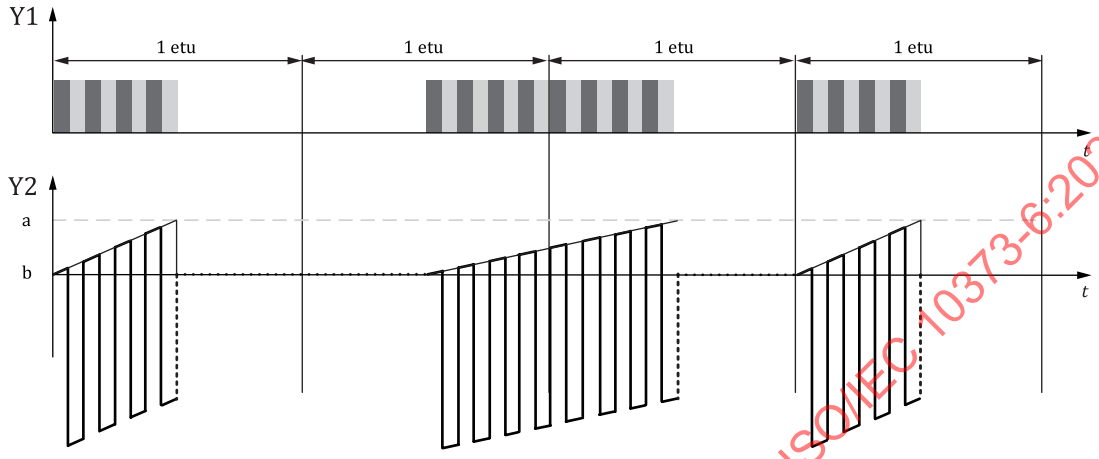
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c) Phase drift condition A3: Constant interstate phase drift of $\emptyset_{LM,\ INTER,\ PCD}$ during sequence D and E defined in ISO/IEC 14443-2:2020, 8.2.6.1. For an example see Figure 10.

1) Active load modulation transmission during MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2.

2) If sequence D directly follows sequence E, the constant interstate phase drift shall be $\emptyset_{LM,\ INTER,\ PCD}$ over both sequences.



Key

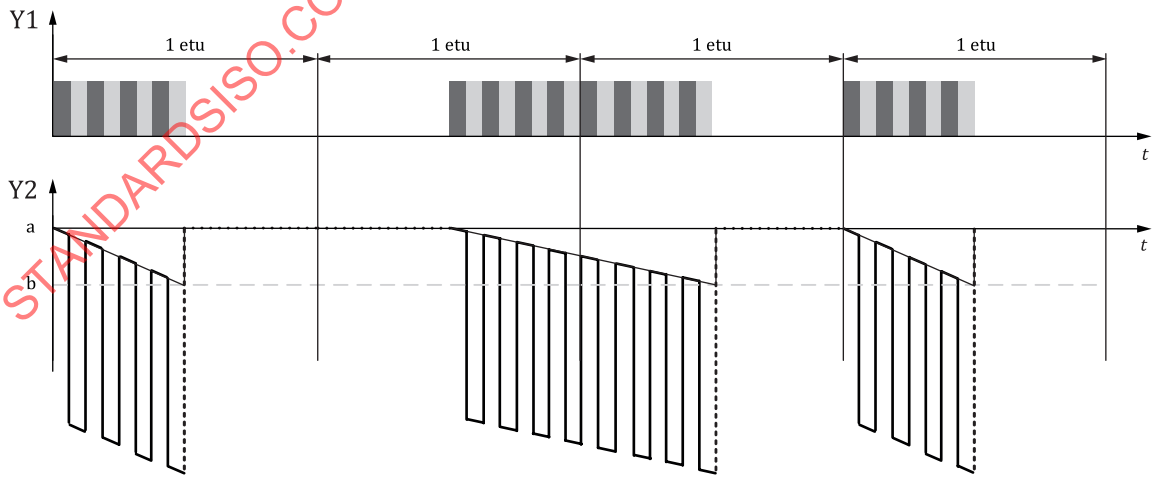
Y_1	amplitude	a	$\emptyset_{LM,\ INIT} + \emptyset_{LM,\ INTER,\ PCD}$.
Y_2	phase (degree)	b	$\emptyset_{LM,\ INIT}$.

Figure 10 — Example of phase drift condition A3 for Type A at PICC to PCD bit rate of $f_c/128$

d) Phase drift condition A4: Constant interstate phase drift of $-\emptyset_{LM,\ INTER,\ PCD}$ during sequence D and E defined in ISO/IEC 14443-2:2020, 8.2.6.1. For an example see Figure 11.

1) Active load modulation transmission during MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2.

2) If sequence D directly follows sequence E, the constant interstate phase drift shall be $-\emptyset_{LM,\ INTER,\ PCD}$ over both sequences.



Key

Y_1	amplitude	a	$\emptyset_{LM,\ INIT}$.
Y_2	phase (degree)	b	$\emptyset_{LM,\ INIT} - \emptyset_{LM,\ INTER,\ PCD}$.

Figure 11 — Example of phase drift condition A4 for Type A at PICC to PCD bit rate of $f_c/128$

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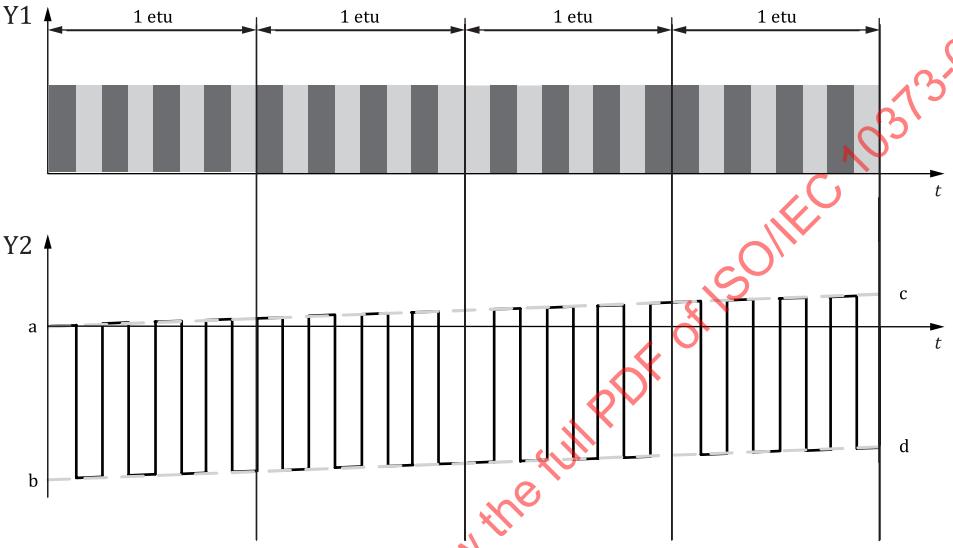
All of these phase drift conditions shall be tested at $V_{LMA,\ min,\ PCD}$ and $V_{LMA,\ max,\ PCD}$ at 24 different $Ø_{LM,\ INIT}$ in steps of 15°.

This results in 192 tests per Active Reference PICC.

7.1.4.4.3 Test conditions for Type B for a PICC to PCD bit rate of $f_c/128$ and for Type A and Type B for optional PICC to PCD bit rates of $f_c/64$, $f_c/32$ and $f_c/16$

Two phase drift conditions are defined within limits defined in ISO/IEC 14443-2.

a) Phase drift condition B1: Constant interstate phase drift of $Ø_{LM,\ INTER,\ PCD}$ over the complete Active Reference PICC response, active load modulation transmission during state MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2. For an example see Figure 12.



Key

Y_1 amplitude

Y_2 phase (degree)

a $Ø_{LM,\ INIT.}$

b $Ø_{LM,\ INIT} - 180°$.

c $Ø_{LM,\ INIT} + Ø_{LM,\ INTER,\ PCD}$.

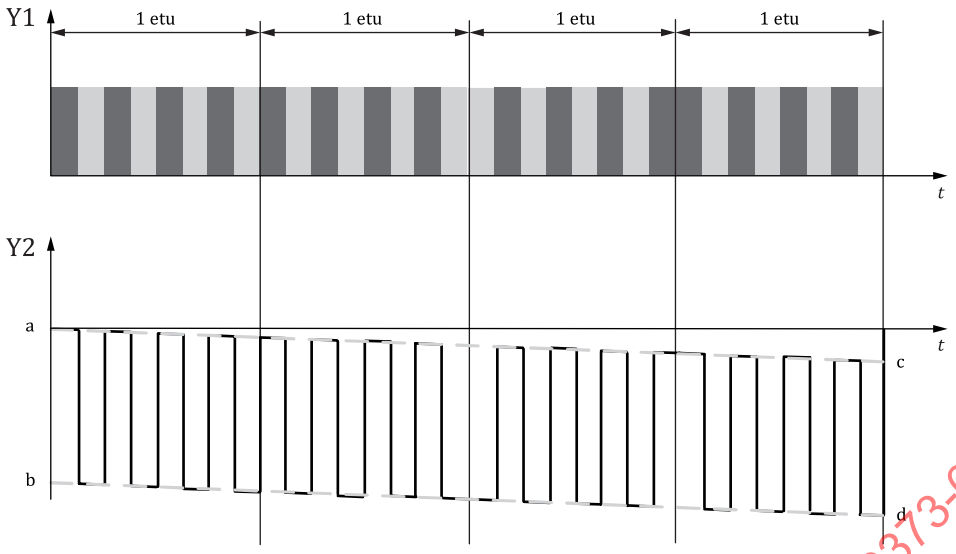
d $Ø_{LM,\ INIT} - 180° + Ø_{LM,\ INTER,\ PCD}$.

Figure 12 — Example of phase drift condition B1 at PICC to PCD a bit rate of $f_c/64$

b) Phase drift condition B2: Constant interstate phase drift of $-Ø_{LM,\ INTER,\ PCD}$ over the complete Active Reference PICC response, active load modulation transmission during state MS1 and active load modulation transmission with the inverse phase of MS1 during state MS2. For an example see Figure 13.

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Key

Y_1 amplitude

Y_2 phase (degree)

a $Ø_{LM, INIT}$.

b $Ø_{LM, INIT} - 180°$.

c $Ø_{LM, INIT} - Ø_{LM, INTER, PCD}$.

d $Ø_{LM, INIT} - 180° - Ø_{LM, INTER, PCD}$.

Figure 13 — Example of phase drift condition B2 at PICC to PCD a bit rate of $f_c/64$

All of these phase drift conditions shall be tested at $V_{LMA, min, PCD}$ and $V_{LMA, max, PCD}$ at 24 different $Ø_{LM, INIT}$ in steps of 15°.

This results in 96 tests per each combination of PICC to PCD bit rate, communication signal interface and Active Reference PICC.

7.1.4.5 Test procedure 1

The PCD shall operate under the conditions defined in 7.1.6.4 after the selection of that PICC to PCD bit rate. The PCD shall correctly react to a received PICC response at the selected PICC to PCD bit rate.

a) Place the Active Reference PICC in the DUT position of the Test PCD assembly.

b) Calibrate the Test PCD assembly to produce H_{min} in accordance with the Active Reference PICC class.

c) Adjust the load of the Active Reference PICC to the equivalent load defined for the Reference PICC (with V_{load} DC voltage at Reference PICC CON3 as defined in Table 12 as setup at H_{min}) having the same antenna class by applying a constant carrier signal to connector CON1, adjusting first its phase in order to achieve destructive interference and then its amplitude. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary. Note the Active Reference PICC CON3 DC voltage corresponding to the field condition.

d) Adjust the Active Reference PICC input signal at CON1 to get $V_{LMA, min, PCD}$ associated with the noted field strength and PICC class as specified in ISO/IEC 14443-2.

NOTE The V_{LMA} is measured as described in 7.2.1.

e) Select an applicable phase drift condition defined in 7.1.6.4.

f) Produce a response at a PICC to PCD bit rate of $f_c/128$ and record the initial phase $Ø_{LM, INIT}$ using the PICC amplitude and phase drift analysis tool of Annex N.

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g) Place the Active Reference PICC in a position in the PCD operating volume with the same field strength condition as setup in step c) by measuring CON3 DC voltage. If this field strength condition cannot be achieved, measure the maximum field strength which can be achieved with a Reference PICC (with V_{load} DC voltage at Reference PICC CON3 as defined in Table 11) having the same antenna class then redo the procedure steps a), b) and d) using this maximum achievable field strength in steps b) and d).

h) The PCD shall correctly detect the Active Reference PICC response.

i) Repeat step h) at least for all mandatory $\emptyset_{LM,\ INIT}$ values defined in 7.1.6.4.

j) Repeat steps h) and i) for all applicable phase drift conditions defined in 7.1.6.4.

k) Repeat steps a) and d) to j) for the highest PICC to PCD bit rate corresponding to every supported subcarrier f_s.

l) Repeat steps a) and d) to k) at least for all mandatory PCD V_{LMA} values defined in 7.1.6.4.

m) Repeat steps a), b) and d) to l) at least for all field strength conditions defined in Table 5.

Any tested position where the load modulation reception test is FAIL, shall be considered out of the operating volume.

7.1.4.6 Test procedure 2

a) Place the Active Reference PICC in the DUT position of the Test PCD assembly.

b) Calibrate the Test PCD assembly to produce H_{min} in accordance with the Active Reference PICC class.

c) Minimize the load of the Active Reference PICC by applying no constant carrier signal to connector CON1. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary. Note the Active Reference PICC CON3 DC voltage corresponding to the field condition.

d) Adjust the Active Reference PICC input signal at CON1 to produce $f_c - f_s$ and $f_c + f_s$ sidebands amplitudes of $V_{LMA,\ min,\ PCD}$ associated with H_{min} and PICC class as specified in ISO/IEC 14443-2.

e) Select phase drift condition A1 or B1 defined in 7.1.6.4, depending on the PICC communication signal interface and the PICC to PCD bit rate.

f) Produce a response and record the initial phase $\emptyset_{LM,\ INIT}$ using the PICC amplitude and phase drift analysis tool of Annex N.

g) Place the Active Reference PICC in a position in the PCD operating volume with the same field strength condition as setup in step c) by measuring CON3 DC voltage.

h) The PCD shall correctly detect the Active Reference PICC response.

i) Repeat step h) at least for all mandatory $\emptyset_{LM,\ INIT}$ values defined in 7.1.6.4.

j) With $f_c + f_s$ sideband amplitude of PCD V_{LMA} as adjusted in step d), repeat steps h) and i) for $f_c - f_s$ sideband amplitude increased by 2,0 dB, 4,0 dB, 6,0 dB, 8,0 dB and 10,0 dB.

k) With $f_c - f_s$ sideband amplitude of PCD V_{LMA} as adjusted in step d), repeat steps h) and i) for $f_c + f_s$ sideband amplitude increased by 2,0 dB, 4,0 dB, 6,0 dB, 8,0 dB and 10,0 dB.

l) Repeat steps h) to k) for the highest supported PICC to PCD bit rate corresponding to every subcarrier f_s.

Any tested position where the load modulation reception test is FAIL, shall be considered out of the operating volume.

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7.1.4.7 Test report

The test report shall confirm the intended operation at the mandatory PICC to PCD bit rate of $f_c/128$ for Test procedure 1 and Test procedure 2. For PCDs supporting one or more of the optional PICC to PCD bit rates the test report shall confirm the intended operation at the supported PICC to PCD bit rates tested for Test procedure 1 and Test procedure 2.

The used test conditions shall be mentioned in the test report.

7.1.5 Load modulation reception for PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$

7.1.5.1 Purpose

This test is used to verify that a PCD correctly detects the load modulation of a PICC which conforms to ISO/IEC 14443-2 for PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$, if supported.

7.1.5.2 Procedure

a) Tune the Reference PICC to 13,56 MHz as described in 5.5.2.4 and switch the jumper J1 to position "c" and the jumper J2 to position "b".

b) Place the Reference PICC at a particular position in the PCD operating volume.

c) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at connector CON3 of V_{load} as defined in Table 3.

d) Increase the modulation signal amplitude at CON1 to produce responses until the PCD detects at least 10 of them consecutively.

e) Place the Reference PICC in the DUT position on the Test PCD assembly.

f) Adjust the Test PCD assembly to produce a field strength H which gives the same voltage at CON3 and note the corresponding field strength by reading the calibration coil voltage.

g) Measure the Reference PICC load modulation amplitude V_{LMA} as described in 7.2.1 and compare it with $V_{LMA,\,min,\,PCD}$ associated with the noted field strength. This measured V_{LMA} defines the PCD sensitivity criterion in order to compare with $V_{LMA,\,min,\,PCD}$ to perform these test measurements.

h) Repeat steps b) to g) for various positions within the operating volume for PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$, if supported.

i) Repeat steps a) to h) with Reference PICC tuned to resonance frequency 15 MHz.

Any position in which the PCD sensitivity is above $V_{LMA,\,min,\,PCD}$ shall be considered out of the operating volume.

The test coverage may be expanded by using additional resonance frequencies below 13,56 MHz such as 12 MHz and 10 MHz.

The PCD sensitivity should be below $V_{LMA,\,min,\,PCD}$ to ensure good reception of the load modulation.

NOTE This test does not check that the PCD reception is independent of the phase of the load modulation. Consequently, it cannot guarantee the correct reception of any PICC conformant with ISO/IEC 14443-2.

7.1.5.3 Test report

The test report shall give the PCD load modulation sensitivity for the tested positions.

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7.1.6 PCD EMD immunity test

7.1.6.1 Purpose

The purpose of this test is to determine whether the PCD is insensitive to any load modulation amplitude below $V_{E,\,PCD}$ for all supported PICC to PCD bit rates.

7.1.6.2 Procedure

a) Tune the Reference PICC to 13,56 MHz as described in 5.5.2.4 and switch the jumper J1 to position "c".

b) Switch the jumper J2 to position "a" or to position "b" according to the tested PICC to PCD bit rate and place the Reference PICC at a designated position in the PCD operating volume.

c) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at CON3 of V_{load} as defined in Table 12.

d) Send the test pattern as shown in Figure 14. The test pattern is a valid standard frame including one single byte (01011101)b. The initial load modulation amplitude V_{EMD} of the test pattern shall be sufficiently low so that the PCD detects the PICC answer sent in step e).

e) Immediately after this test pattern, applying no gap, send the appropriate PICC answer to the PCD command with a PICC V_{LMA}, measured as defined in 7.2.1, of a value higher, e.g. twice the minimum value for the applied field strength H.

f) Increase V_{EMD} by adjusting the voltage at CON1 until the PCD does no longer detect the answer correctly. This may be determined by monitoring the next PCD command following the PICC answer; see Figure 14.

g) Place the Reference PICC into the DUT position on the Test PCD assembly.

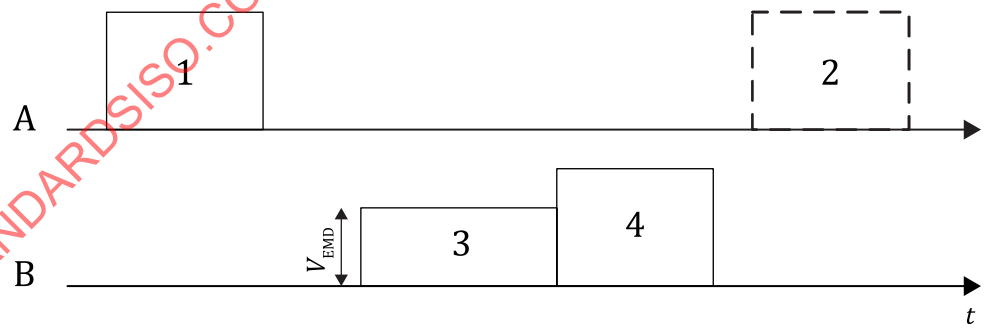
h) Adjust the Test PCD assembly to produce a field strength H which gives the same voltage at CON3 and note the corresponding field strength by reading the calibration coil voltage.

i) Derive the current value of V_{EMD} on the Reference PICC by applying the power versus time measurement as described in 5.7.2.

j) Compare this measured V_{EMD} value with $V_{E,\,PCD}$.

k) Repeat steps b) to j) for other designated positions within the operating volume.

l) Repeat steps b) to k) for all supported PICC to PCD bit rates.



Key

A PCD

B reference PICC

1 PCD command

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2 next PCD command
3 test pattern
4 PICC answer

Figure 14 — PCD immunity test (common for Type A and Type B)

7.1.6.3 Test report

The test report shall state whether the PCD was insensitive to any load modulation amplitude below $V_{E,\,PCD}$ for all supported PICC to PCD bit rates.

7.2 PICC tests

7.2.1 PICC transmission

7.2.1.1 Purpose

The purpose of this test is to verify that the PICC transmission conforms with the PICC requirements specified in ISO/IEC 14443-2 for all mandatory and supported optional PICC to PCD bit rates within the operating field range $[H_{min}, H_{max}]$.

7.2.1.2 Conditions

This test shall be done at ambient, minimum and maximum temperatures. If minimum and maximum temperatures are not provided in PICC test conditions, the PICC transmission test shall be performed only at ambient temperature.

7.2.1.3 Procedure

Step 1:

The load modulation test circuit of Figure 2 and the Test PCD assembly of Figure 3 defined for the PICC class (see ISO/IEC 14443-2:2020, 8.2.2.2) are used. If the PICC does not claim to meet the requirements of one particular PICC class as specified in ISO/IEC 14443-1, then use the Test PCD assembly 1.

Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil. Connect the output of the load modulation test circuit of Figure 2 to a signal acquiring device. The 10 Ω potentiometer P1 shall be trimmed to minimize the residual carrier. This signal shall be at least 40 dB lower than the signal obtained by shorting one sense coil. Additionally connect the output of the calibration coil (see Figure 1 and Figure 3) to the same signal acquiring device as the load modulation test circuit.

Step 2:

The DUT shall be placed in the DUT position (see Figure 3). If the PICC meets the requirements of one particular class as specified in ISO/IEC 14443-1, then its antenna shall be located within the zone defined for its PICC class centered in sense coil a. If the PICC does not claim to meet the requirements of one particular class as specified in ISO/IEC 14443-1, then its antenna shall be located within the external rectangle defined for “Class 1” centered in sense coil a. The RF drive into the Test PCD antenna shall be re-adjusted to the required field strength.

For each PICC to PCD bit rate supported by the PICC, the Test PCD shall put the PICC in the PROTOCOL state. An I-block shall be sent by the Test PCD to obtain a response from the PICC of at least the length defined in Table 13 for that PICC to PCD bit rate (TEST_COMMAND4 and TEST_RESPONSE4 fit this purpose). If this frame length is not supported by the PICC, its maximum supported frame length shall be used.

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Table 13 — PICC transmission minimum frame length definition

PICC to PCD bit rate	Minimum frame length [bytes]
$f_c/128$	128
$f_c/64$	256
$f_c/32$	512
$f_c/16$	1024
$f_c/8$	2048
$f_c/4$	4096
$f_c/2$	4096

NOTE These minimum frame lengths stem from the memory size of the signal acquiring device and can be increased in the future.

Display the whole PICC response of both, calibration coil and load modulation test circuit, including at least 200 carrier periods before the first and 20 carrier periods after the last modulation of the PICC on the signal acquiring device and store the sampled data of calibration coil and load modulation test circuit in separate files for analysis by computer programs as defined in Annex F and Annex N.

Load modulation amplitude computation:

Fourier transform with a Bartlett window exactly six subcarrier cycles of the sampled modulation waveform using suitable computer software (as the one given in Annex F). Use a discrete Fourier transformation with a scaling such that a pure sinusoidal signal results in its peak magnitude. In order to minimize transient effects, avoid analysing a subcarrier cycle immediately following a non-modulating period or a phase shift of the subcarrier. The discrete Fourier transformation shall be done at the sidebands frequencies generated by the DUT, i.e., $f_c + f_s$ and $f_c - f_s$.

Amplitude and phase drift computation:

Use the PICC amplitude and phase drift analysis tool defined in Annex N.

This test procedure shall be repeated 5 times. The test apparatus shall generate the carrier frequency f_c as defined in ISO/IEC 14443-2:2020, 6.2:

a) once at the lower limit of the allowed range,

b) 3 times in the middle of the allowed range and

c) once at the upper limit of the allowed range.

Before each repetition the test apparatus shall perform a field reset of at least 5 ms.

7.2.1.4 Test report

The test report shall state:

a) Conformance of the PICC load modulation amplitude V_{LMA} with the requirements defined in ISO/IEC 14443-2:

   1) For PICC to PCD bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$, if supported, the resulting peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ shall be above $V_{LMA,\ min,\ PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.2.

   2) For PICC to PCD bit rates of $f_c/8$, $f_c/4$ and $f_c/2$, if supported, the average value resulting from the peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ shall be above $V_{LMA,\ min,\ PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.2.

   3) For all mandatory and supported optional PICC to PCD bit rates, the average value resulting from the peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ shall be below $V_{LMA,\ max,\ PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.2.

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4) For all mandatory and supported optional PICC to PCD bit rates, the parameter $V_{|MS1-US|}$ shall be above $V_{LMA,\ min,\ PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.2.

b) Conformance of the phase parameters $\emptyset_{LM,\ INTRA}$ and $\emptyset_{LM,\ INTER}$ of the PICC with the requirements defined ISO/IEC 14443-2:

1) For all mandatory and supported optional PICC to PCD bit rates using a subcarrier of $f_c/16$, $\emptyset_{LM,\ INTRA}$ should be less than $\emptyset_{LM,\ INTRA,\ max\ ,PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.3.

2) For all mandatory and supported optional PICC to PCD bit rates using a subcarrier of $f_c/16$, $\emptyset_{LM,\ INTER}$ shall be less than $\emptyset_{LM,\ INTER,\ max\ ,PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.3.

3) For all supported optional PICC to PCD bit rates using a subcarrier higher than $f_c/16$, $\emptyset_{LM,\ INTRA}$ should be less than $\emptyset_{LM,\ INTRA,\ max\ ,PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.3.

4) For all supported optional PICC to PCD bit rates using a subcarrier higher than $f_c/16$, $\emptyset_{LM,\ INTER}$ should be less than $\emptyset_{LM,\ INTER,\ max\ ,PICC}$ as defined in ISO/IEC 14443-2:2020, 8.2.2.3.

c) Based on the state information retrieved in N.9.1, conformance with ISO/IEC 14443-2 of the following parameters of the PICC:

1) For PICC Type A responses using a bit rate of $f_c/128$, the duration of an etu, the number of subcarrier periods per etu, whether 50 % of an etu are modulated with the subcarrier and the start of communication.

2) For PICC Type A responses using an optional bit rate higher than $f_c/128$ and a subcarrier of $f_c/16$, if supported, the duration of an etu, the bit representation and coding and the start of communication.

3) For PICC Type B responses using a subcarrier of $f_c/16$, the duration of an etu, and the bit representation and coding.

NOTE For PICC Type B responses, TR1, SOF, character encoding, EGT and EOF are tested in Annex G.

d) Furthermore, the test report shall:

1) give the measured peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ and the applied fields and modulations;

2) give the measured phase characteristics; and

3) confirm the intended operation at the mandatory PICC to PCD bit rate of $f_c/128$ and all supported optional PICC to PCD bit rates.

The used test conditions shall be mentioned in the test report.

7.2.2 PICC EMD level and low EMD time test

7.2.2.1 Purpose

The purpose of this test is to determine that the PICC does not generate an electromagnetic disturbance amplitude V_{EMD} higher than $V_{E,\ PICC}$ during $t_{E,\ PICC}$ as specified in ISO/IEC 14443-2 with the exceptions defined therein for all mandatory and supported optional PICC to PCD bit rates within the operating field range $[H_{min}, H_{max}]$.

NOTE 1 The low EMD time $t_{E,\ PICC}$ is a function of FDT/TR0 as defined in ISO/IEC 14443-3:2018, 8.2.

NOTE 2 The EMD limit $V_{E,\ PICC}$ is a function of the field strength.

7.2.2.2 Noise requirements

In order to ensure a high dynamic range and sufficient sensitivity to EMD, the noise floor precondition test defined in 5.7.3 shall be performed before this test.

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7.2.2.3 Test commands

The PICC EMD test shall be performed for ISO/IEC 14443-3 commands. Depending on the PICC application, additional higher layer commands shall be included in the test plan.

7.2.2.4 Procedure

This test shall be done at least applying H_{min} and $H_{max.}$ Using the Test PCD assembly, perform the following steps.

a) Adjust the RF power delivered by the signal generator to the Test PCD antenna to the required field strength as measured by the calibration coil.

b) Place the DUT into the DUT position. The RF drive into the Test PCD antenna shall be readjusted to the required field strength if necessary.

c) Reset the PICC by switching the RF field off and on; then if necessary send a transition of sequence commands to put the PICC into the TIS (see G.3.3.2.2 for PICC Type A and G.4.4.2.2 for PICC Type B).

d) Send the command to be tested.

e) Record the sense coil's signal for a time period of at least 200 µs before the start of PICC subcarrier generation. Additionally, record at least 50 µs after the first detected subcarrier in order to determine precisely the position of the PICC answer.

f) Determine the value of $t_{E,\ PICC}$ from the acquired signal: if the PCD modulation is present on the trace then measure the time between the last rising edge of PCD modulation and the start of PICC subcarrier generation and calculate $t_{E,\ PICC}$ with the formula given in ISO/IEC 14443-3:2018, 8.2; if the PCD modulation is not present on the trace then $t_{E,\ PICC}$ equals its maximum value defined in ISO/IEC 14443-3:2018, 8.2.

g) Compute the signal power at the frequencies $f_c + f_s$ and $f_c - f_s$ as a function of time as defined in 5.7.2.

h) Compute the maximum signal out of the two results obtained in g).

i) Determine the time t_{START} corresponding to half of the amplitude of the maximum signal obtained in h) during the rising edge of PICC transmission. Check if the amplitude of the maximum signal obtained in h) during the time period $[t_{START} - t_{E,\ PICC};\ t_{START} - 1/f_s]$ conforms with the requirements defined in ISO/IEC 14443-2.

j) Repeat steps d) to i) for the next test command.

k) Repeat steps d) to j) for all supported PICC to PCD bit rates.

7.2.2.5 Test report

The test report shall state whether the PICC EMD level during $t_{E,\ PICC}$ conforms with the requirements defined in ISO/IEC 14443-2 for all supported PICC to PCD bit rates.

Furthermore, the test report shall give the measured maximum electromagnetic disturbance levels of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ during $t_{E,\ PICC}$. A graph showing EMD levels during $t_{E,\ PICC}$ should be incorporated in the report in case the test fails.

7.2.3 PICC reception

7.2.3.1 Purpose

The purpose of this test is to verify the ability of the PICC to receive the PCD commands under the conditions as specified in ISO/IEC 14443-2 for all mandatory and supported optional PCD to PICC bit rates within the operating field range $[H_{min}, H_{max}]$.

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7.2.3.2 General conditions

The test conditions shall be checked using the analysis tool defined in Annex E with the DUT in the DUT position. If at least one parameter is not within the tolerances defined in 4.3, the test conditions shall be readjusted.

The Test PCD assembly may use a pre-equalization method to achieve some of the test conditions defined in Table 14, Table 15, Table 16 and Table 17.

For a frame size higher than 256 bytes, a frame with error correction as defined in ISO/IEC 14443-4 should be used.

7.2.3.3 PICC Type A for PCD to PICC bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$

7.2.3.3.1 Test conditions

The test conditions for a PCD to PICC bit rate of $f_c/128$ are specified in Table 14.

Table 14 — PICC Type A test conditions for a PCD to PICC bit rate of $f_c/128$

Test condition	t_1	t_2	t_3	t_4	PCD field envelope during 60 % of t_2[a]	Overshoot
1	$41/f_c$	$6/f_c$	$17/f_c$	$7/f_c$	0,5 %	0 % (100 % of $H_{INITIAL}$)
2	$27{,}5/f_c$	$25{,}5/f_c$	$10/f_c$	$6/f_c$	0,5 %	10 % (110 % of $H_{INITIAL}$)
3	$41/f_c$	$13/f_c$	$2/f_c$		0,5 %	10 % (110 % of $H_{INITIAL}$)
4	$40/f_c$	$7/f_c$	$16/f_c$	$6/f_c$	4 %	0 % (100 % of $H_{INITIAL}$)
5	$28{,}5/f_c$	$26/f_c$	$10/f_c$	$6/f_c$	4 %	10 % (110 % of $H_{INITIAL}$)

[a] During the remaining 40 % of t_2, the PCD field envelope shall be at least the defined value.

All of these test conditions shall be tested at least using H_{min} and H_{max}.

The test conditions for PCD to PICC bit rates of $f_c/64$, $f_c/32$ and $f_c/16$ are specified for each bit rate in Table 15.

Table 15 — PICC Type A test conditions for PCD to PICC bit rates of $f_c/64$, $f_c/32$ and $f_c/16$

PCD to PICC bit rate	Test condition	t_1	t_5	t_6	a	h_{ovs}
$f_c/64$	1	$20/f_c$	$13/f_c$	$12/f_c$	0,2	0 %
	2	$16/f_c$	$15/f_c$	$10/f_c$	0	6,4 %
	3	$20/f_c$	$14/f_c$	$2/f_c$	0	10,1 %
$f_c/32$	1	$10/f_c$	$6/f_c$	$10/f_c$	0,4	0 %
	2	$8/f_c$	$7/f_c$	$9/f_c$	0	6,1 %
	3	$10/f_c$	$6/f_c$	$2/f_c$	0	9,9 %
$f_c/16$	1	$5/f_c$	$2{,}5/f_c$	$6/f_c$	0,6	0 %
	2	$4/f_c$	$3/f_c$	$5{,}5/f_c$	0,2	4,8 %
	3	$5/f_c$	$2{,}5/f_c$	$2/f_c$	0,2	7,3 %

All of these test conditions shall be tested at least using H_{min} and H_{max}.

7.2.3.3.2 Procedure

Under all of the test conditions defined in Table 14 the PICC shall answer to a REQA with ATQA.

Under test conditions 2 and 3 defined in Table 14 the PICC shall answer to REQA with ATQA and to WUPA with ATQA respecting the frame delay time as defined in ISO/IEC 14443-3:2018, 6.2.1.1, where the frame delay time shall be determined by the method defined in Annex B.

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For each optional PCD to PICC bit rate supported by the PICC, the PICC shall operate under all of the conditions defined in Table 15 after selection of that optional PCD to PICC bit rate. The PICC shall respond correctly to an I-block transmitted at that optional PCD to PICC bit rate.

For each optional PCD to PICC bit rate in combination with a PICC to PCD bit rate of $f_c/128$, the PICC shall operate under each of the test conditions 2 and 3 defined in Table 15 after selection of that optional PCD to PICC bit rate. The PICC shall respond to an I-block with (0)b as last bit and an I-block with (1)b as last bit transmitted at that optional PCD to PICC bit rate respecting the frame delay time defined in in ISO/IEC 14443-3:2018, 6.2.1.1, where the frame delay time shall be determined by the method defined in Annex B.

7.2.3.4 PICC Type B for PCD to PICC bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$

7.2.3.4.1 Test conditions

The test conditions for each bit rate are defined in Table 16.

Table 16 — PICC Type B test conditions for PCD to PICC bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$

PCD to PICC bit rate	Test condition	t_f	t_r	h_f	h_r	m	b
$f_c/128$	1	$17/f_c$	$17/f_c$	0 %	0 %	7 %	0,869
	2	$2/f_c$	$11/f_c$	1,4 %	1 %	7 %	0,869
	3	$11/f_c$	$2/f_c$	1 %	1,4 %	7 %	0,869
	4	$17/f_c$	$17/f_c$	0 %	0 %	15 %	0,739
	5	$2/f_c$	$11/f_c$	2,7 %	1,9 %	15 %	0,739
	6	$11/f_c$	$2/f_c$	1,9 %	2,7 %	15 %	0,739
$f_c/64$	1	$14/f_c$	$14/f_c$	0 %	0 %	7 %	0,869
	2	$2/f_c$	$9/f_c$	1,3 %	1 %	7 %	0,869
	3	$9/f_c$	$2/f_c$	1 %	1,3 %	7 %	0,869
	4	$14/f_c$	$14/f_c$	0 %	0 %	15 %	0,739
	5	$2/f_c$	$9/f_c$	2,7 %	1,9 %	15 %	0,739
	6	$9/f_c$	$2/f_c$	1,9 %	2,7 %	15 %	0,739
$f_c/32$	1	$11/f_c$	$11/f_c$	0 %	0 %	7 %	0,869
	2	$2/f_c$	$7,5/f_c$	1,3 %	0,9 %	7 %	0,869
	3	$7,5/f_c$	$2/f_c$	0,9 %	1,3 %	7 %	0,869
	4	$11/f_c$	$11/f_c$	0 %	0 %	15 %	0,739
	5	$2/f_c$	$7,5/f_c$	2,6 %	1,9 %	15 %	0,739
	6	$7,5/f_c$	$2/f_c$	1,9 %	2,6 %	15 %	0,739
$f_c/16$	1	$8/f_c$	$8/f_c$	0 %	0 %	7 %	0,869
	2	$2/f_c$	$6/f_c$	1,3 %	0,9 %	7 %	0,869
	3	$6/f_c$	$2/f_c$	0,9 %	1,3 %	7 %	0,869
	4	$8/f_c$	$8/f_c$	0 %	0 %	15 %	0,739
	5	$2/f_c$	$6/f_c$	2,5 %	1,8 %	15 %	0,739
	6	$6/f_c$	$2/f_c$	1,8 %	2,5 %	15 %	0,739

All of these test conditions shall be tested at least using H_{min} and H_{max}.

7.2.3.4.2 Procedure

Under all of the test conditions defined in Table 16, the PICC operating at a bit rate of $f_c/128$ shall answer to a REQB with ATQB.

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For each optional PCD to PICC bit rate supported by the PICC, the PICC shall operate under each of the test conditions defined in Table 16 after selection of that optional PCD to PICC bit rate. This PICC shall respond correctly to an I-block transmitted at that optional PCD to PICC bit rate.

7.2.3.5 PICC Type A or Type B for PCD to PICC bit rates of $f_c/8$, $f_c/4$ and $f_c/2$

7.2.3.5.1 Test conditions

Six test conditions are defined for each bit rate in Table 17.

Table 17 — PICC test conditions for PCD to PICC bit rates of $f_c/8$, $f_c/4$ and $f_c/2$

PCD to PICC bit rate	Test condition	t_f	t_r	h_f	h_r	m	b
$f_c/8$	1	$6/f_c$	$6/f_c$	0 %	0 %	8 %	0,852
	2	$2/f_c$	$5/f_c$	1,4 %	1 %	8 %	0,852
	3	$5/f_c$	$2/f_c$	1 %	1,4 %	8 %	0,852
	4	$6/f_c$	$6/f_c$	0 %	0 %	21 %	0,653
	5	$2/f_c$	$5/f_c$	3,2 %	2,2 %	21 %	0,653
	6	$5/f_c$	$2/f_c$	2,2 %	3,2 %	21 %	0,653
$f_c/4$	1	$4/f_c$	$4/f_c$	0 %	0 %	8 %	0,852
	2	$2/f_c$	$4/f_c$	1,2 %	0,8 %	8 %	0,852
	3	$4/f_c$	$2/f_c$	0,8 %	1,2 %	8 %	0,852
	4	$4/f_c$	$4/f_c$	0 %	0 %	21 %	0,653
	5	$2/f_c$	$4/f_c$	2,9 %	1,9 %	21 %	0,653
	6	$4/f_c$	$2/f_c$	1,9 %	2,9 %	21 %	0,653
$f_c/2$	1	$3/f_c$	$3/f_c$	0 %	0 %	8 %	0,852
	2	$2/f_c$	$3/f_c$	1,1 %	0,8 %	8 %	0,852
	3	$3/f_c$	$2/f_c$	0,8 %	1,1 %	8 %	0,852
	4	$3/f_c$	$3/f_c$	0 %	0 %	21 %	0,653
	5	$2/f_c$	$3/f_c$	2,5 %	1,9 %	21 %	0,653
	6	$3/f_c$	$2/f_c$	1,9 %	2,5 %	21 %	0,653

These six test conditions shall be tested at least using H_{min} and H_{max}.

7.2.3.5.2 Procedure

For each optional PCD to PICC bit rate supported by the PICC, the PICC shall operate under each of the test conditions defined in Table 17 after selection of that optional PCD to PICC bit rate. This PICC shall respond correctly to an I-block transmitted at that optional PCD to PICC bit rate.

7.2.3.6 PICC Type A or Type B for PCD to PICC bit rates of $3f_c/4$, f_c, $3f_c/2$ and $2f_c$

See K.2.2.1.

7.2.3.7 Test report

The test report shall confirm the intended operation at the mandatory $f_c/128$ bit rate. For PICCs supporting one or more of the optional PCD to PICC bit rates, the test report shall confirm the intended operation at the supported bit rates.

The used test conditions shall be mentioned in the test report.

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7.2.4 PICC resonance frequency

7.2.4.1 Purpose

The test may be used to measure the resonance frequency of a PICC.

When two or more PICCs are placed in the same PCD energizing field, the resonance frequency of each PICC decreases.

Care should be taken in designing each PICC resonance frequency.

The resonance frequency may depend on the field strength used during the measurement.

7.2.4.2 Procedure

The resonance frequency of a PICC is measured by using an impedance analyser or a network analyser or a LCR-meter connected to a calibration coil. The PICC should be placed on the calibration coil at a distance of 10 mm, with the axes of the two coils being congruent. The resonance frequency is that frequency at which the resistive part of the measured complex impedance is at maximum.

7.2.4.3 Test report

When applied the test report shall give the PICC resonance frequency and the measurement conditions.

7.2.5 PICC maximum loading effect

7.2.5.1 Purpose

The purpose of this test is to verify that the loading of the PICC conforms to ISO/IEC 14443-2.

7.2.5.2 General conditions

For this test, the R_{ext} values of the impedance matching networks specified in Annex A shall be reduced to 0,94 Ω for the impedance matching network 1 and to 0,54 Ω for the impedance matching network 2. The values of the capacitors shall be adjusted accordingly.

7.2.5.3 Procedure

7.2.5.3.1 Preparation

Depending on the claimed PICC class, select:

a) the relevant H_{min} as defined in ISO/IEC 14443-2:2020, Table 2;

b) the relevant Reference PICC as defined in Table 12 and its voltage V_{load};

c) the relevant Test PCD assembly as defined in Table 12.

If the PICC does not claim any particular PICC class as specified in ISO/IEC 14443-1, then PICC parameters, test apparatus and circuits in accordance with ISO/IEC 14443-2:2020, 6.3 shall be used for this test.

The PICC loading effect at H_{min} shall be measured using the Test PCD assembly. It shall be less than the loading effect of the selected Reference PICC tuned to 13,56 MHz and calibrated to obtain V_{load} at CON3 at H_{min}.

7.2.5.3.2 Default procedure

The default procedure of this substitution method is as follows.

a) Tune the selected Reference PICC to 13,56 MHz as described in 5.5.2.4.

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b) Calibrate the Test PCD assembly to produce the H_{min} operating condition on the calibration coil.

c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of V_{load} measured at CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a DC voltage of V_{load} at CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary. R2 value should be between R2min and R2max as defined in Table 12. Check this range at least once before using the alternative method.

d) Remove the Reference PICC. The unloaded field strength when Reference PICC 1 using a V_{load} of 4,5 V is removed should be between 1,65 A/m and 1,85 A/m. The unloaded field strength when Reference PICC 2 or Reference PICC 3 is removed should be between 1,58 A/m and 1,70 A/m. The unloaded field strength when Reference PICC 1 using a V_{load} of 6 V is removed should be between 1,70 A/m and 1,90 A/m.

e) Place the DUT into the DUT position on the Test PCD assembly.

f) Measure the field strength monitored by the calibration coil. This field strength shall be greater than H_{min}.

7.2.5.3.3 Extended procedure

If PICC Class 1 parameters were used and if the field strength measured in step f) of 7.2.5.3.2 was not greater than H_{min}, then the following extended procedure may be used to measure the PICC loading effect:

a) repeat steps b) to f) of 7.2.5.3.2 using Reference PICC 1 configured for a V_{load} of 6 V instead of the voltage defined in Table 12;

NOTE 1 The warning about R2 value in 7.2.5.3.2 is not applicable in this case.

b) repeat the PICC transmission test as defined in 7.2.1 with a field strength of H_{min} – 0,2 A/m (rms) instead of H_{min} as defined in ISO/IEC 14443-2:2020 Table 2, using the PICC V_{LMA} limits defined for H_{min}, as defined in ISO/IEC 14443-2:2020, Table 22;

c) repeat the PICC EMD level and low EMD time test as defined in 7.2.2 with a field strength of H_{min} – 0,2 A/m (rms) instead of H_{min} as defined in ISO/IEC 14443-2:2020, Table 2 using the $V_{E,\ PICC}$ limit defined for H_{min} as defined in ISO/IEC 14443-2:2020, 10.2;

d) repeat the PICC reception test as defined in 7.2.3 with a field strength of H_{min} – 0,2 A/m (rms) instead of H_{min} as defined in ISO/IEC 14443-2:2020, Table 2, using for PICC Type B the modulation index m defined for H_{min} as defined in ISO/IEC 14443-2:2020, 9.1.2; and

e) repeat the PICC operating field strength test as defined in 7.2.6 with a field strength of H_{min} – 0,2 A/m (rms) instead of H_{min} as defined in ISO/IEC 14443-2:2020, Table 2.

NOTE 2 This extended procedure checks that a slightly higher PICC loading effect is compensated by a slightly lower PICC minimum operating field strength.

7.2.5.4 Test report

If the extended procedure has not been used, the test result is only PASS if the field strength measured in step f) is greater than H_{min}, otherwise the test result is FAIL.

If the extended procedure has been used, the test result is only PASS if the field strength measured in step f) is greater than H_{min} (using Reference PICC 1 configured for a DC voltage V_{load} of 6 V), and if:

a) the PICC transmission test as defined in 7.2.1;

b) the PICC EMD level and low EMD time test as defined in 7.2.2;

c) the PICC reception test as defined in 7.2.3; and

d) the PICC operating field strength test as defined in 7.2.6

are PASS with a field strength of H_{min} – 0,2 A/m (rms) instead of H_{min}, otherwise the test result is FAIL.

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The test report shall give the value of the measured field strength and the V_{load} value used.

7.2.6 PICC operating field strength test

7.2.6.1 Purpose

This test verifies that the PICC operates as intended for all mandatory and supported optional PCD to PICC bit rates within the operating field range [H_{min}, H_{max}]

7.2.6.2 Conditions

This test shall be done at least at ambient, minimum and maximum temperatures applying H_{min} and H_{max}. If minimum and maximum temperatures are not provided in PICC test conditions, PICC operating field strength test shall be performed only at ambient temperature.

When the test condition is both H_{max} and maximum temperature, the PICC should be put in horizontal position. The impact of the ventilation (if any) should be minimized during the test in order to limit the PICC's heat dissipation. The test shall be preceded with a one-minute PICC exposition to a field strength of H_{max} without any field shut-off so that the PICC chip has reached its maximum temperature when the test starts. The air temperature value during test execution shall remain within ±3 °C of the nominal value.

7.2.6.3 Procedure

For each PCD to PICC bit rate supported by the PICC, the following command sequence shall be used for this procedure using the test conditions defined in 7.2.6.2.

a) Activate the PICC as described in G.5.1.2 and execute the appropriate bit rates selection sequence, if applicable.

b) Run TEST_COMMAND_SEQUENCE1.

7.2.6.4 Test report

The test report shall confirm the intended operation at the mandatory $f_c/128$ bit rate. For PICCs supporting one or more of the optional PCD to PICC bit rates the test report shall confirm the intended operation at the supported PCD to PICC bit rates.

The used test conditions shall be mentioned in the test report.

7.3 Test methods for bit rates of $3f_c/4$, f_c, $3f_c/2$ and $2f_c$ from PCD to PICC

Annex K shall apply.

7.4 PXD tests

PCD and PICC tests shall be applied as follows:

a) when the PXD is in PCD Mode, tests defined in 7.1 and, if applicable, 7.3 shall be applied;

b) when the PXD is in PICC Mode, tests defined in 7.2 and, if applicable, 7.3 shall be applied.

NOTE In automatic mode alternation, the PXD can be forced into the required mode.

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8 Test of ISO/IEC 14443-3 and ISO/IEC 14443-4 parameters

8.1 PCD tests

8.1.1 PCD EMD recovery test

8.1.1.1 Purpose

The purpose of this test is to determine whether the PCD is disturbed by a test pattern sent $t_{E, PCD}$ before the PICC answer for all supported PICC to PCD bit rates.

8.1.1.2 Procedure

a) The UT performs the protocol activation procedure according to H.1.9.2 for Type A or H.1.9.3 for Type B. During activation, the LT will not declare support of any framing options nor frames with error correction.

b) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

c) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

d) The LT sends in sequence, as illustrated in Figure 15 using the $t_{E, PCD}$ associated with minimum FDT/TR0:

NOTE 1 The low EMD time $t_{E, PCD}$ is a function of FDT/TR0 as defined in ISO/IEC 14443-3:2018, 8.2.

1) a test pattern, which starts sending the two data bits b1 = (0)b followed by b2 = (1)b in a valid way to the PCD, but interrupts immediately after the second bit sent, as illustrated in Figure 16 for Type A and Figure 17 for Type B;

2) a period with no load modulation for a duration of $t_{E, PCD}$;

3) the appropriate answer to the PCD command.

NOTE 2 As the minimum TR0 is shorter than the test pattern duration, in step d) 1) the test pattern can start before the end of the PCD command or the overlapping part of the test pattern can be omitted.

e) Check if the PCD behaves in the same way as if there was no test pattern. This may be determined by monitoring the next PCD command following the PICC answer, see Figure 15.

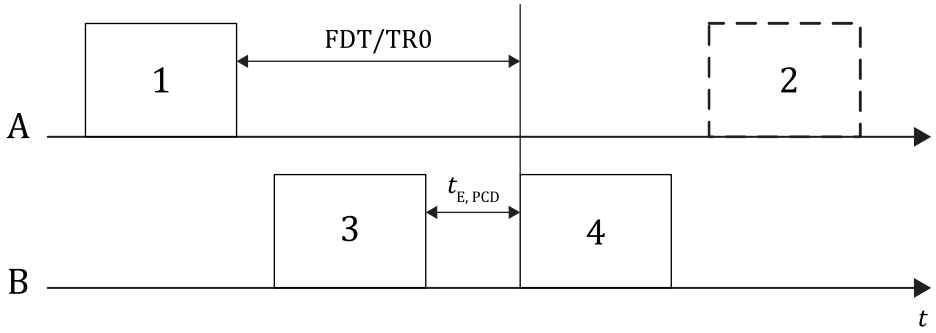
f) Repeat steps d) and e) 10 times.

g) Repeat steps d) to f) replacing minimum FDT/TR0 with maximum FDT/TR0.

h) Repeat steps a) to g) for all supported PICC to PCD bit rates.

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Key

A PCD
B reference PICC
1 PCD command
2 next PCD command
3 test pattern
4 PICC answer

Figure 15 — EMD recovery test sequence (common for Type A and Type B)

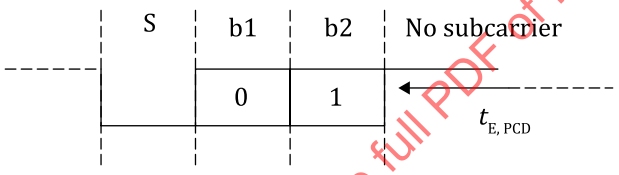


Figure 16 — Test pattern for the EMD recovery test (Type A)

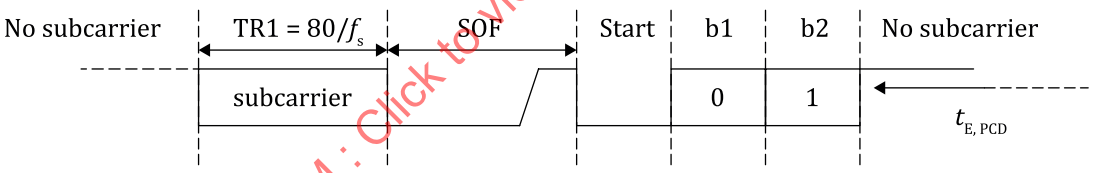


Figure 17 — Test pattern for the EMD recovery test (Type B)

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8.1.1.3 Test report

The test report shall report whether the PCD was not disturbed by the test pattern sent $t_{E, PCD}$ before the PICC answer (or was able to recover from the test pattern) for all supported PICC to PCD bit rates.

8.1.2 Additional PCD tests

Additional PCD tests of ISO/IEC 14443-3 and ISO/IEC 14443-4 parameters shall be as defined in Annex H, Annex I and Annex L.

In order to continue the scenario as specified, the PCD-test-apparatus shall adapt its behaviour in reaction to any frames sent by the IUT before the PCD commands specified in the test, unless otherwise specified.

EXAMPLE 1 The PCD-test-apparatus ignores commands sent by the IUT which are not defined in ISO/IEC 14443 series.

EXAMPLE 2 The PCD-test-apparatus adapts its behaviour in case the IUT performs a presence check.

EXAMPLE 3 The PCD-test-apparatus adapts its behaviour in case the IUT sends S(PARAMETERS) which are not specified in the scenario.

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8.2 PICC tests

PICC tests of ISO/IEC 14443-3 and ISO/IEC 14443-4 parameters shall be as defined in Annex G and Annex L.

Unless otherwise specified, the PICC-test-apparatus shall adapt its behaviour in reaction to any PICC response in the following cases:

a) If the PICC sends one or several S(WTX) requests before the expected I-block, the PICC-test-apparatus shall adapt by sending necessary S(WTX) responses to continue the scenario as specified.

b) If the PICC response is chained, the PICC-test-apparatus shall adapt by sending necessary R(ACK) to continue the scenario as specified.

c) If the length of a frame sent by the PICC-test-apparatus exceeds FSC for Type A or maximum frame size for Type B, the PICC-test-apparatus shall adapt by chaining to continue the scenario as specified.

8.3 PXD tests

8.3.1 PCD and PICC Modes

PCD and PICC tests shall be applied as follows:

a) when the PXD is in PCD Mode, tests defined in 8.1 shall be applied;

b) when the PXD is in PICC Mode, tests defined in 8.2 shall be applied.

NOTE In automatic mode alternation, the PXD can be forced into the required mode.

8.3.2 Automatic mode alternation

8.3.2.1 General

The tests defined in this subclause apply only to PXD supporting automatic mode alternation.

One cycle is defined as the duration between two consecutive beginnings of PCD Mode (RF field on).

8.3.2.2 PCD Mode and PICC Mode alternation cycle

8.3.2.2.1 Purpose

This test checks that:

a) each cycle does not last longer than t_{cyc};

b) in each cycle, the PICC Mode lasts longer than PCD Mode; and

c) the PICC Mode duration varies randomly and differs by at least t_{diff}.

8.3.2.2.2 Conditions

The PXD should not be in close proximity to another PXD, PCD or PICC.

8.3.2.2.3 Procedure

The RF field of the PXD shall be monitored and evaluated for at least 10 consecutive cycles:

a) Ensure that the PXD is in automatic Mode alternation;

b) Measure all RF field on and RF field off durations.

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8.3.2.2.4 Test report

The test result is PASS if all the following conditions are met:

a) no cycle lasts more than t_{cyc};

b) for each t_{cyc} the PICC Mode duration (RF field off) is longer than the PCD Mode duration (RF field on);

c) the PICC Mode durations vary;

d) the minimum and maximum PICC Mode durations differ by at least t_{diff}.

Otherwise the test result is FAIL.

NOTE 1 The appreciation of the randomness of the PICC Mode duration can be done with common statistical methods.

NOTE 2 Due to statistical reasons the test result can be FAIL and the test can be repeated.

8.3.3 PCD Mode

8.3.3.1 Polling

8.3.3.1.1 Purpose

This test checks that the PXD in automatic mode alternation polls for PICCs Type A and Type B as defined in ISO/IEC 14443-3:2018, 5.2 in each cycle of PCD Mode.

8.3.3.1.2 Conditions

The PXD should not be in close proximity to another PXD, PCD or PICC.

8.3.3.1.3 Procedure

All modulations during PCD Mode shall be monitored, and the timings between the Request commands shall be measured for at least 10 consecutive cycles.

a) Ensure that the PXD is in automatic alternation mode.

b) Monitor all Request commands during PCD Mode.

c) Measure timings before and between each command.

8.3.3.1.4 Test report

The test result is PASS if all the following conditions are met in each cycle:

a) at least one REQA/WUPA command is sent by the PXD;

b) at least one REQB/WUPB command is sent by the PXD;

c) the duration of unmodulated field before at least one of the REQA/WUPA commands is more than 5 ms;

d) the duration of unmodulated field before at least one of the REQB/WUPB commands is more than 5 ms.

Otherwise the test result is FAIL.

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8.3.3.2 End of PCD Mode

8.3.3.2.1 Purpose

This test checks that the PXD in automatic mode alternation leaves the PCD Mode after processing of a PICC, and resumes its automatic mode alternation with the PICC Mode first.

8.3.3.2.2 Conditions

The PCD-test-apparatus shall be used.

8.3.3.2.3 Procedure

Perform the following steps:

a) Place the PCD-test-apparatus in the operating volume of the PXD.

b) Send responses to all anticollision commands sent by the PXD until the PCD-test-apparatus is in ACTIVE or PROTOCOL state.

c) Do not answer any further PXD commands.

8.3.3.2.4 Test report

The test result is PASS if the PXD resumes its automatic mode alternation, possibly after application of the error handling or PICC presence check rules, with the PICC Mode first, otherwise the test result is FAIL.

8.3.4 PICC Mode

8.3.4.1 Reaction to polling

8.3.4.1.1 Purpose

This test checks that the PXD in automatic mode alternation responds to Type A or Type B Request commands as defined in ISO/IEC 14443-3:2018, 5.2 in each cycle of PICC Mode.

8.3.4.1.2 Conditions

The PICC-test-apparatus shall be used.

8.3.4.1.3 Procedure 1

Perform the following steps:

a) Switch the PICC-test-apparatus RF operating field off.

b) Place the PXD into the test position of the PICC-test-apparatus and ensure that the PXD is in automatic alternation mode.

c) Switch the PICC-test-apparatus RF operating field on while the PXD RF field is on.

d) Send a REQA command 5 ms after the start of PICC Mode (PXD RF field off).

e) Send a REQB command 5 ms after the end the REQA command.

f) Record the presence and the content of the PXD response.

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8.3.4.1.4 Procedure 2

Perform the following steps:

a) Switch the PICC-test-apparatus RF operating field off.

b) Place the PXD into the test position of the PICC-test-apparatus and ensure that the PXD is in automatic alternation mode.

c) Switch the PICC-test-apparatus RF operating field on while the PXD RF field is on.

d) Send a REQB command 5 ms after the start of PICC Mode (PXD RF field off).

e) Send a REQA command 5 ms after the end the REQB command.

f) Record the presence and the content of the PXD response.

8.3.4.1.5 Test report

The test result is PASS if the PXD response is one of the following:

a) ATQA in each of the two procedures (PICC Type A mode);

b) ATQB in each of the two procedures (PICC Type B mode);

c) ATQA in Procedure 1 and ATQB in Procedure 2 (PICC Type A and Type B mode).

Otherwise the test result is FAIL.

8.3.4.2 PICC Mode duration and exit conditions

8.3.4.2.1 Purpose

This test checks that, after reception of a valid REQA/WUPA command or REQB/WUPB command, the PXD in automatic mode alternation does not go in PCD Mode before a POWER-OFF state.

8.3.4.2.2 Conditions

The PICC-test-apparatus shall be used.

8.3.4.2.3 Procedure

Perform the following steps:

a) Switch the PICC-test-apparatus RF operating field on.

b) Ensure that the PXD is in automatic alternation mode and place the PXD into the test position of the PICC-test-apparatus.

c) Send a REQA command at least 5 ms after the start of PICC Mode (PXD RF field off).

d) Send a REQB command 5 ms after the end of the REQA command if there is no answer to the REQA command.

e) Keep the PICC-test-apparatus RF field on for more than 2 s.

f) Continue with anticollision commands to put the PXD in ACTIVE or PROTOCOL state and check the PXD responses.

g) Send a HALT or S(DESELECT) command to put the PXD in HALT state.

h) Keep the PICC-test-apparatus RF field on for more than 2 s.

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i) Send a Request command of the communication signal interface which was answered in step c) or d) and check there is no PXD response.

j) Send a Wake-up command of the communication signal interface which was answered in step c) or d) and check there is a PXD response.

k) Switch the PICC-test-apparatus RF operating field off.

l) Check that the automatic alternation resumes in less than 1 s by monitoring the PXD RF field.

8.3.4.2.4 Test report

The test result is PASS if all steps of the procedure succeed, otherwise the test result is FAIL.

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Annex A
(normative)

Test PCD antennas

A.1 Test PCD antenna 1

A.1.1 Test PCD antenna 1 layout including impedance matching network 1

Figure A.1 and Figure A.2 illustrate the Test PCD antenna 1 layout including the impedance matching network 1 at its recommended position.

The antenna coil track width is 1,8 mm (except for through-plated holes).

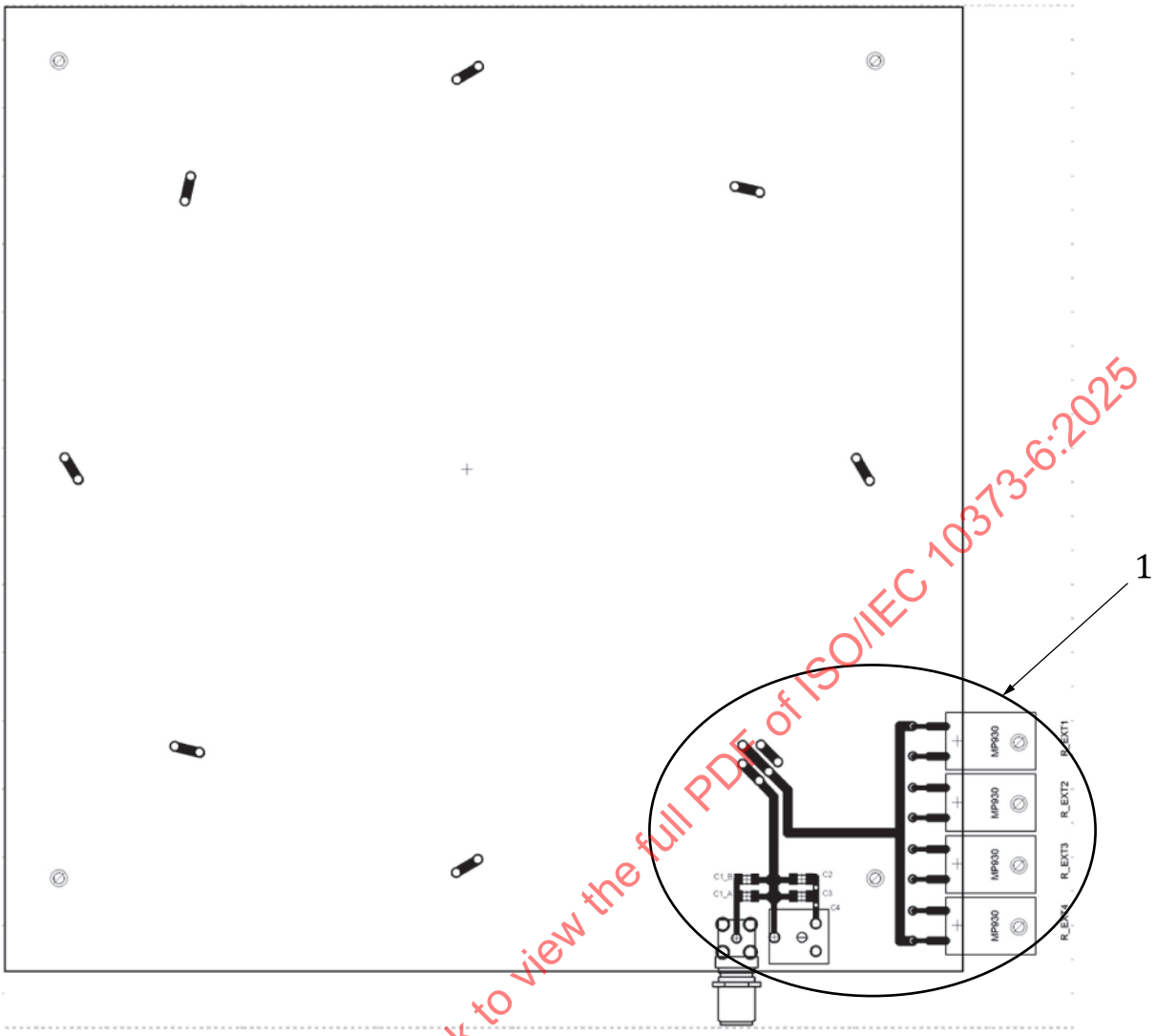
Starting from the impedance matching network 1, there are crossovers every 45°.

Printed circuit board: FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

NOTE The layout of the impedance matching network 1 is informative.

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Key

1 impedance matching network 1

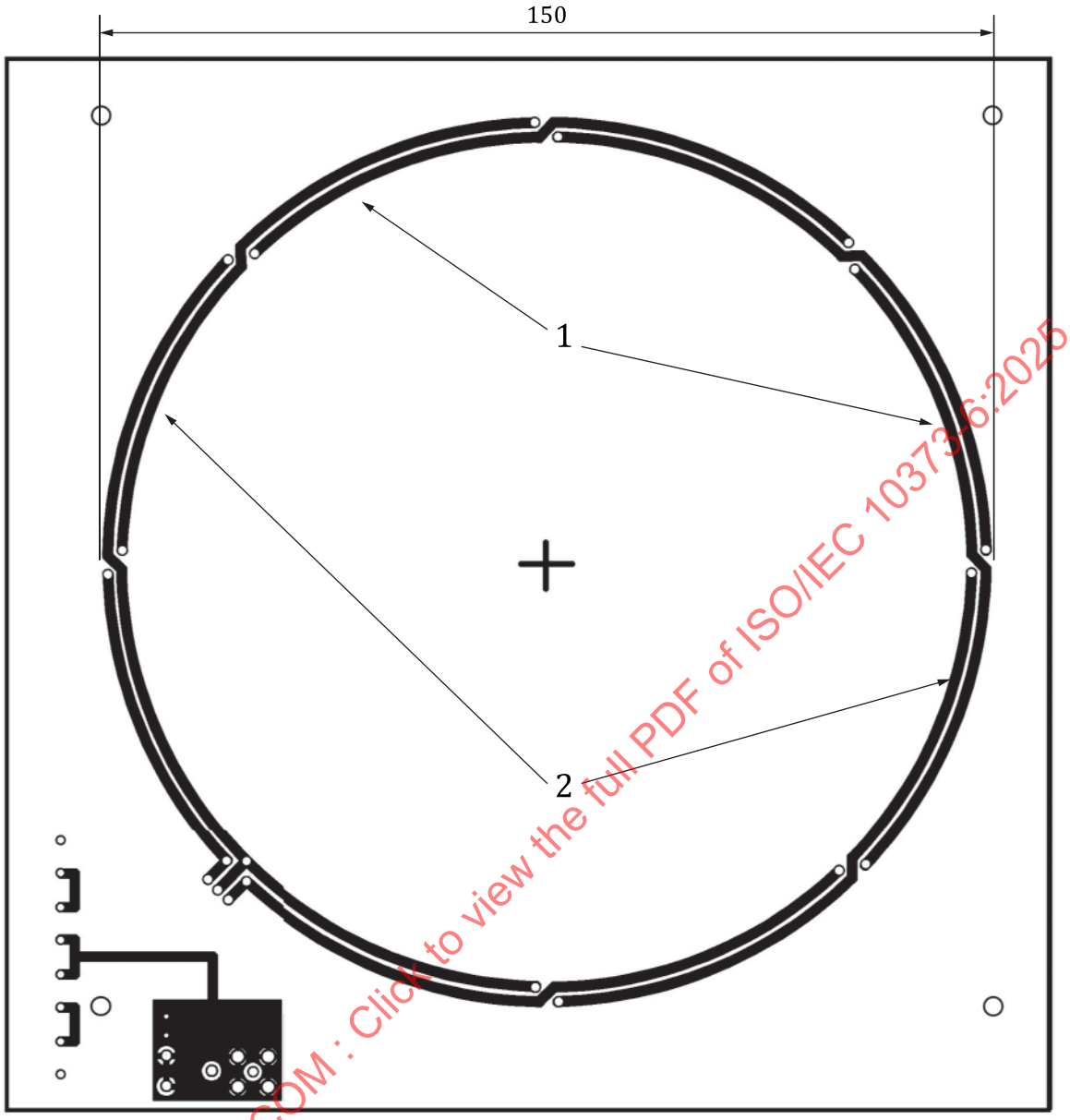
NOTE Drawing is not to scale.

Figure A.1 — Test PCD antenna 1 layout including impedance matching network 1 (view from front)

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Dimensions in millimetres



Key

1 antenna coil

2 ground compensation coil

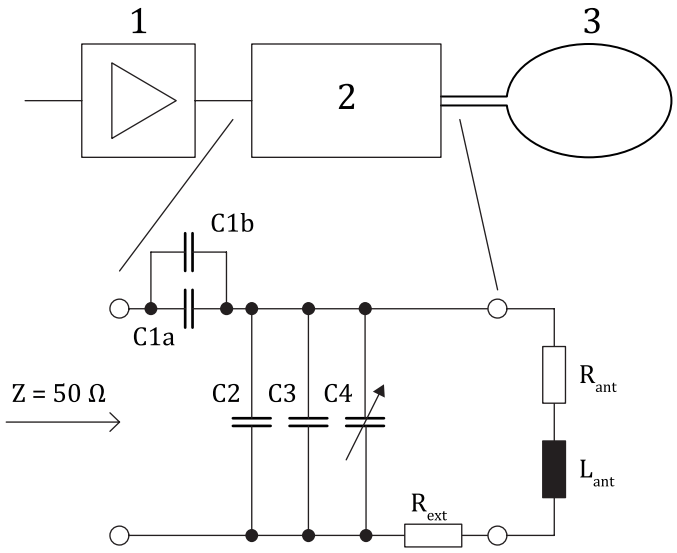
Figure A.2 — Test PCD antenna 1 layout including impedance matching network 1 (view from back)

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A.1.2 Impedance matching network 1

The circuitry of the impedance matching network 1 is specified in Figure A.3, where (R_{ant}, L_{ant}) represent the antenna impedance. The capacitors C1a, C1b, C2 and C3 have fixed values. The input impedance phase can be adjusted with the variable capacitor C4.

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Components list

	Value	Unit	Remarks
C1a	82	pF	Voltage range 200 V
C1b	8,2	pF	Voltage range 200 V
C2	150	pF	Voltage range 200 V
C3	10	pF	Voltage range 200 V
C4	2-27	pF	Voltage range 200 V
R_{ext}	4,7	Ω	Power range 20 W

Key

1 linear low distortion variable output 50 Ω power driver
2 impedance matching network 1
3 antenna coil

Figure A.3 — Impedance matching network 1

NOTE 1 The tolerance of the matched antenna impedance is ±5 Ω and ±10°.

NOTE 2 The power and voltage ranges include a safety margin.

NOTE 3 R_{ext} can be built by a parallel circuit of each two resistors of 4,7 Ω 5 W in series.

NOTE 4 R_{ext} is preferably connected in the ground path of the antenna as drawn in Figure A.3.

NOTE 5 The parasitic capacitance of the antenna is not shown in Figure A.3.

A.2 Test PCD antenna 2

A.2.1 Test PCD antenna 2 layout including impedance matching network 2

Figure A.4 and Figure A.5 illustrate the Test PCD antenna 2 layout including the impedance matching network 2 at its recommended position.

The antenna coil track width is 1,8 mm (except for through-plated holes).

Starting from the impedance matching network 2 there are crossovers every 45°.

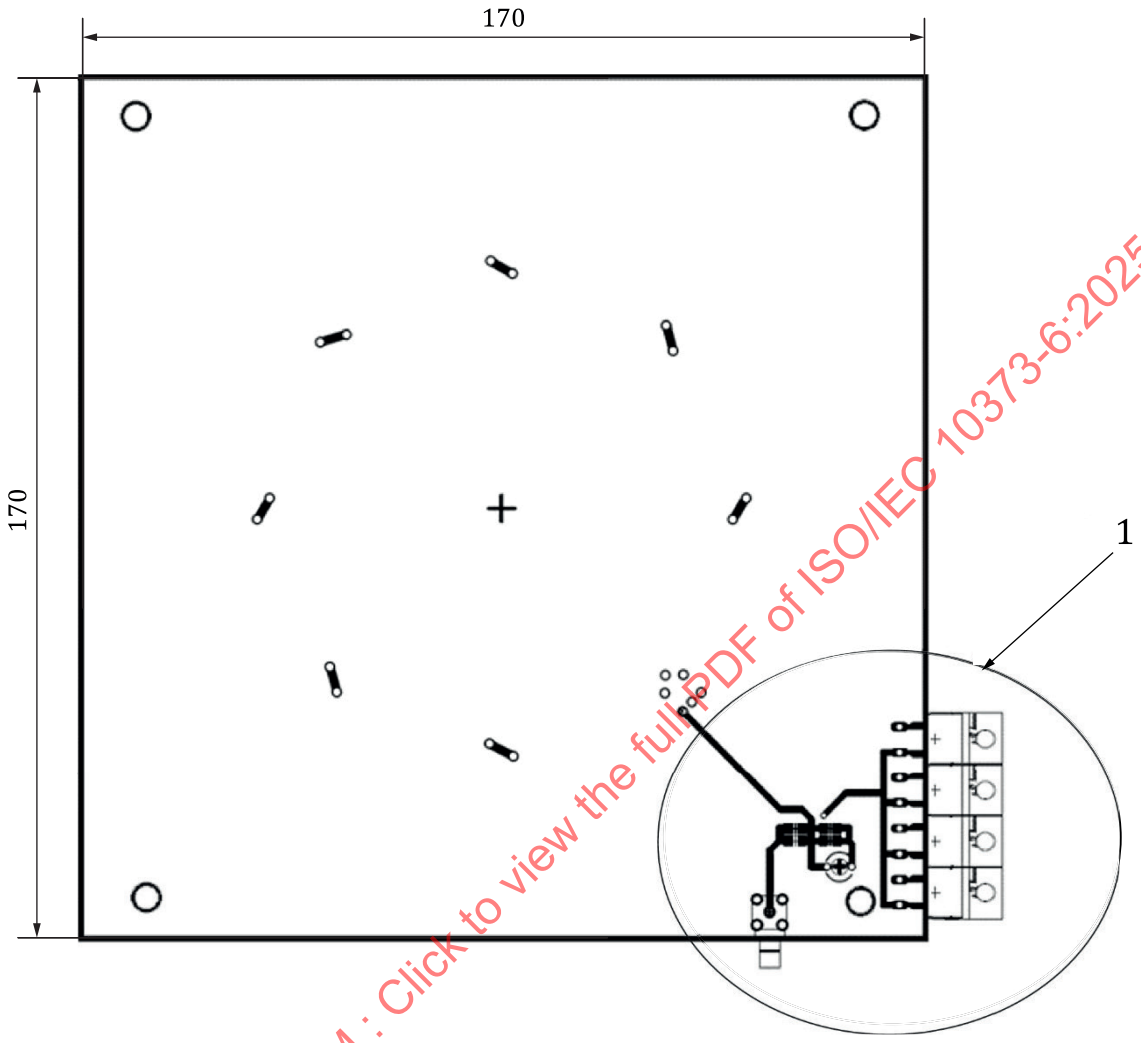
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Printed circuit board: FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

NOTE The layout and the position of the impedance matching network 2 are informative.

Dimensions in millimetres



Key

1 impedance matching network 2

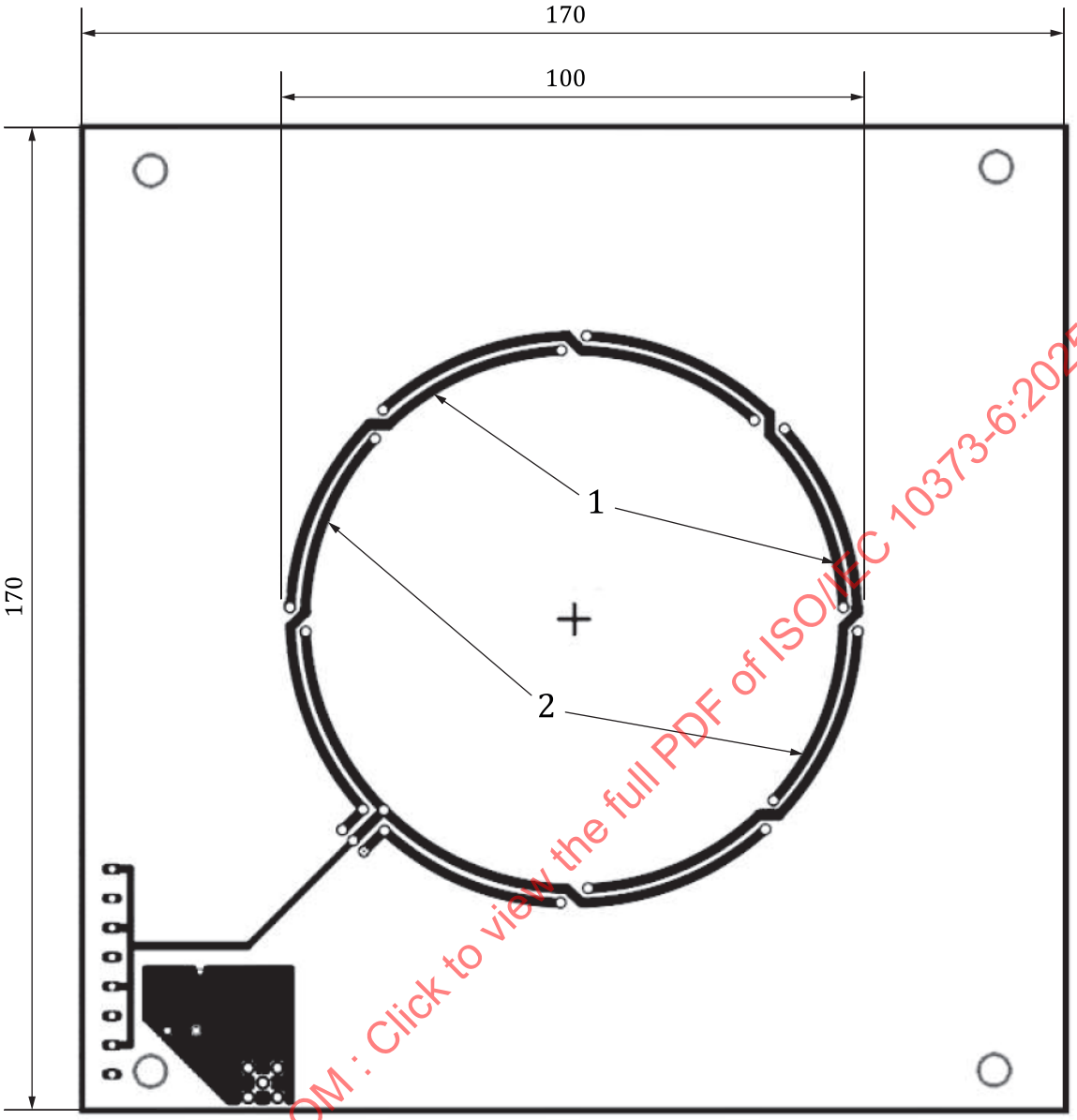
NOTE Printed circuit board outside dimensions are informative.

Figure A.4 — Test PCD antenna 2 layout including impedance matching network 2 (view from front)

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Dimensions in millimetres



Key

1 antenna coil

2 ground compensation coil

NOTE Printed circuit board outside dimensions are informative.

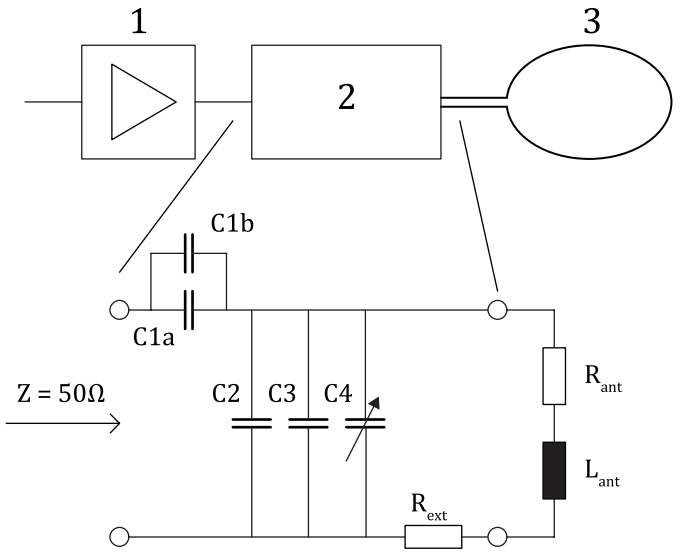
Figure A.5 — Test PCD antenna 2 layout including impedance matching network 2 (view from back)

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A.2.2 Impedance matching network 2

The circuitry of the impedance matching network 2 is specified in Figure A.6, where (R_{ant}, L_{ant}) represent the antenna impedance. The capacitors C1a, C1b, C2 and C3 have fixed values. The input impedance phase can be adjusted with the variable capacitor C4.

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Components list

	Value	Unit	Remarks
C1a	100	pF	Voltage range 200 V
C1b	12	pF	Voltage range 200 V
C2	270	pF	Voltage range 200 V
C3	18	pF	Voltage range 200 V
C4	2-27	pF	Voltage range 200 V
R_{ext}	2,7	Ω	Power range 20 W

Key

1 linear low distortion variable output 50 Ω power driver

2 impedance matching network 2

3 antenna coil

Figure A.6 — Impedance matching network 2

NOTE 1 The tolerance of the matched antenna impedance is ±5 Ω and ±10°.

NOTE 2 The power and voltage ranges include a safety margin.

NOTE 3 R_{ext} can be built either by a parallel circuit of each two resistors of 2,7 Ω 5 W in series each or by a parallel circuit of 10 Ω, 10 Ω, 10 Ω and 15 Ω, 5 W.

NOTE 4 R_{ext} is preferably connected in the ground path of the antenna as drawn in Figure A.6.

NOTE 5 The parasitic capacitance of the antenna is not shown in Figure A.6.

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Annex B
(normative)

PICC Type A FDT determination method

B.1 Overview

The working principle of the PICC Type A FDT determination method is illustrated in Figure B.1.

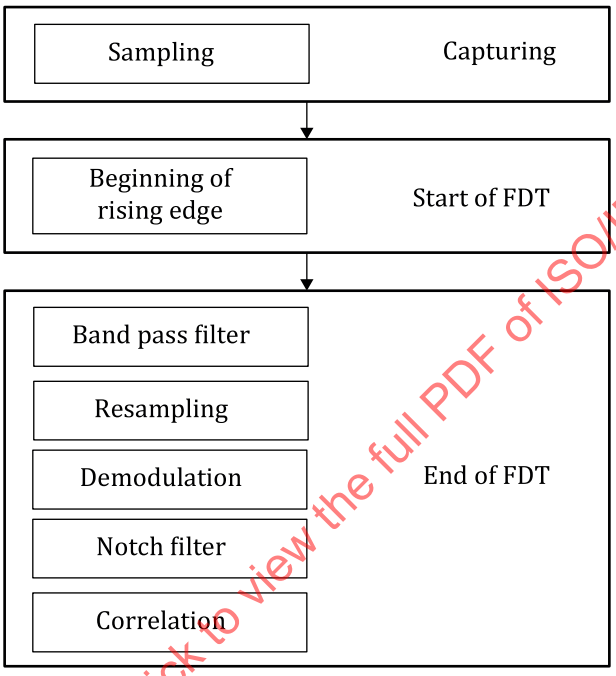


Figure B.1 — FDT determination method block diagram

Each block is described in following clauses.

NOTE The intrinsic uncertainty of the method is $\pm 0{,}5/f_c$.

B.2 Capturing

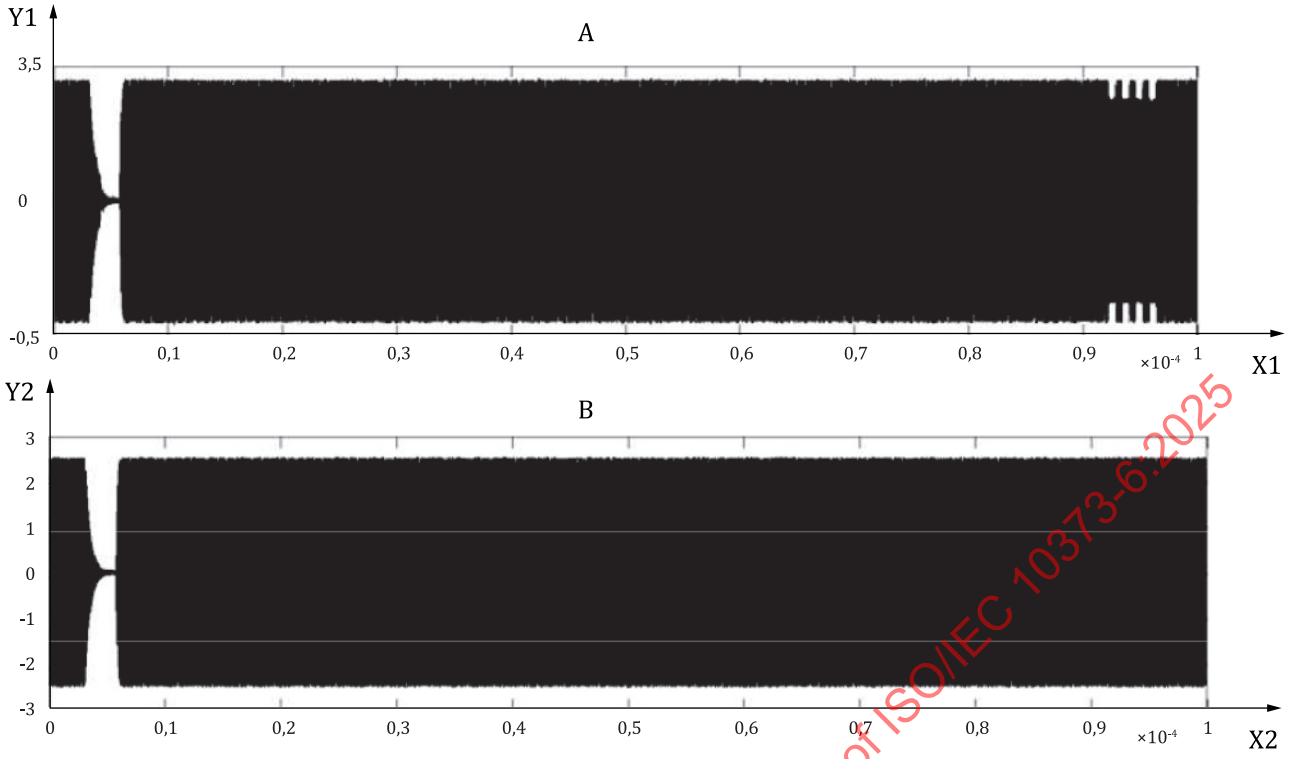
The digital sampling device/oscilloscope used for signal capturing shall fulfill the requirements defined in 5.2.

The time and voltage data as captured by both the calibration coil and the load modulation test circuit (also known as sense coils), with at least 128 carrier periods before the last pause transmitted by the PCD and at least 128 carrier periods after the PICC start of communication shall be transferred to a suitable computer. Both, the calibration coil and the load modulation test circuit signals, shall be captured by the same digital sampling device as illustrated in Figure B.2.

The signal processing afterwards shall use the actual $1/f_c$ derived from the calibration coil signal as time basis.

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Key

X_1 time (s)
Y_1 amplitude (V)
X_2 time (s)
Y_2 amplitude (V)
A graph: signal from sense coils
B graph: signal from calibration coil

Figure B.2 — Example signals captured for FDT determination

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B.3 Determination of the Start of FDT

The captured calibration coil signal shall be used to determine the beginning of the rising edge of the last pause transmitted by the PCD. The method described in Annex E shall be used.

B.4 Determination of the End of FDT

B.4.1 General

The captured calibration coil and sense coils signals shall be processed as described in the following clauses.

B.4.2 Band pass filter

The calibration coil and sense coils signals shall be filtered as specified in E.3.1.

B.4.3 Resampling

The filtered calibration coil and sense coils signals shall be resampled to an integer number multiple of f_c using linear interpolation. The integer number shall be at least 37.

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B.4.4 Demodulation

The resampled sense coils signal shall be demodulated by the resampled calibration coil signal, to which phase shifts of 0°, 45°, 90° and 135° shall be applied, as shown in Figure B.3.

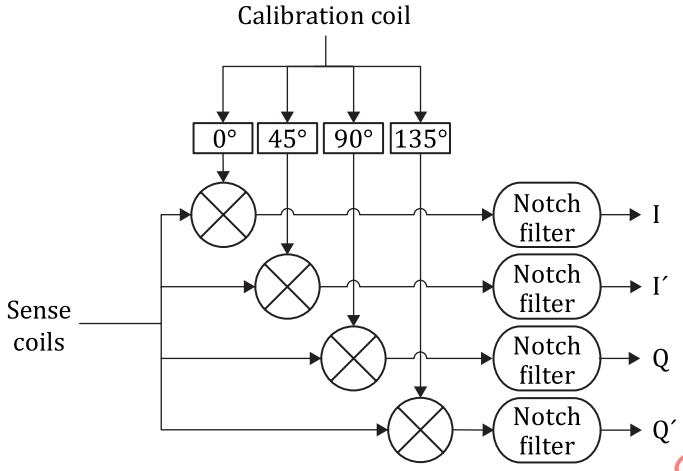


Figure B.3 — Demodulation scheme

B.4.5 Notch filter

The filter as specified in E.5.1 shall be applied to the demodulated signals in the following way:

a) after filtering the demodulated signals in forward direction, the filtered signals shall be reversed and filtered again;

b) after second filtering, the signals shall be reversed again to obtain signals I, I´, Q and Q´ (see Figure B.3).

B.4.6 Correlation

Each of the signals I, I´, Q and Q´ shall be cross-correlated with the signal shown in Figure B.4. From both the positive correlation maximum and negative correlation minimum of all correlation results, the later occurrence represents the center of the PICC start of communication. From this moment, $64/f_c$ shall be subtracted to get the first modulation edge of the PICC response.

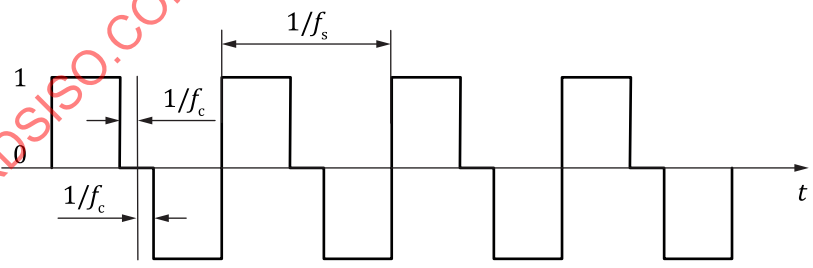


Figure B.4 — Correlation signal

B.5 Program of the FDT determination method

This informative program written in the high-level interpreted programming language GNU Octave gives an example for the implementation of the FDT determination method.

It is published separately and can be found at https://standards.iso.org/iso-iec/10373/-6/ed-5/en/.

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Annex C
(normative)

Sense coils

C.1 Sense coils layout

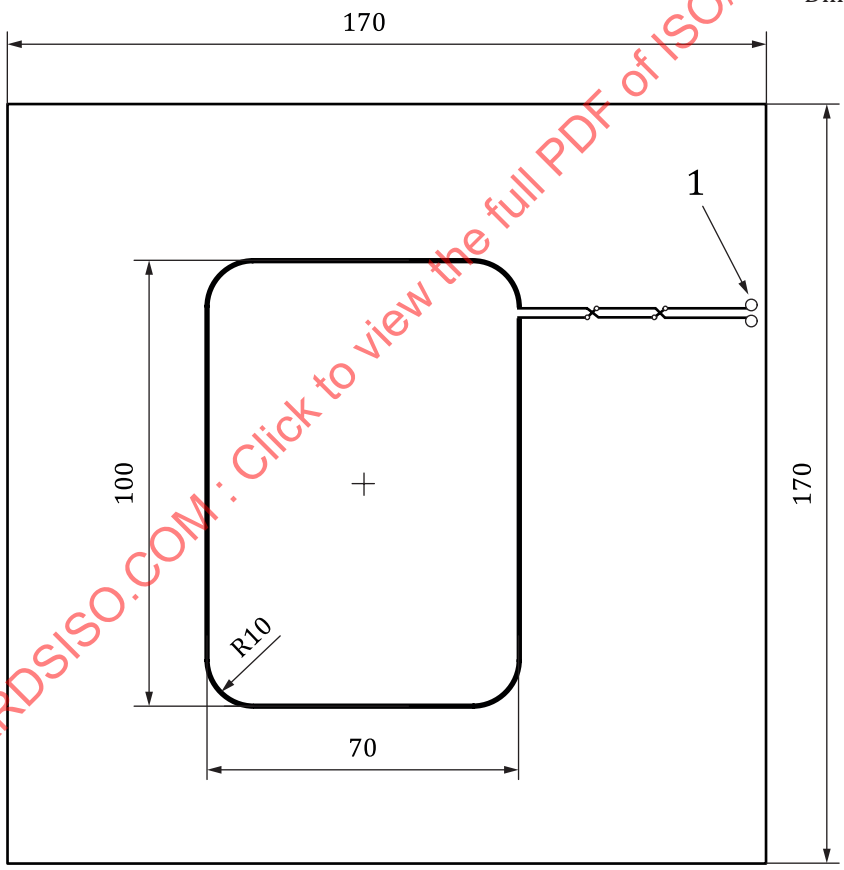
C.1.1 Sense coils 1 layout

Figure C.1 illustrates the sense coils 1 layout.

The sense coil track width is 0,5 mm with relative tolerance ±20 % (except for through-plated holes). Size of the coils refers to the outer dimensions.

Printed circuit board: FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

Dimensions in millimetres



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Key

1 connections

NOTE Printed circuit board outside dimensions are informative.

Figure C.1 — Sense coils 1 (a and b) layout

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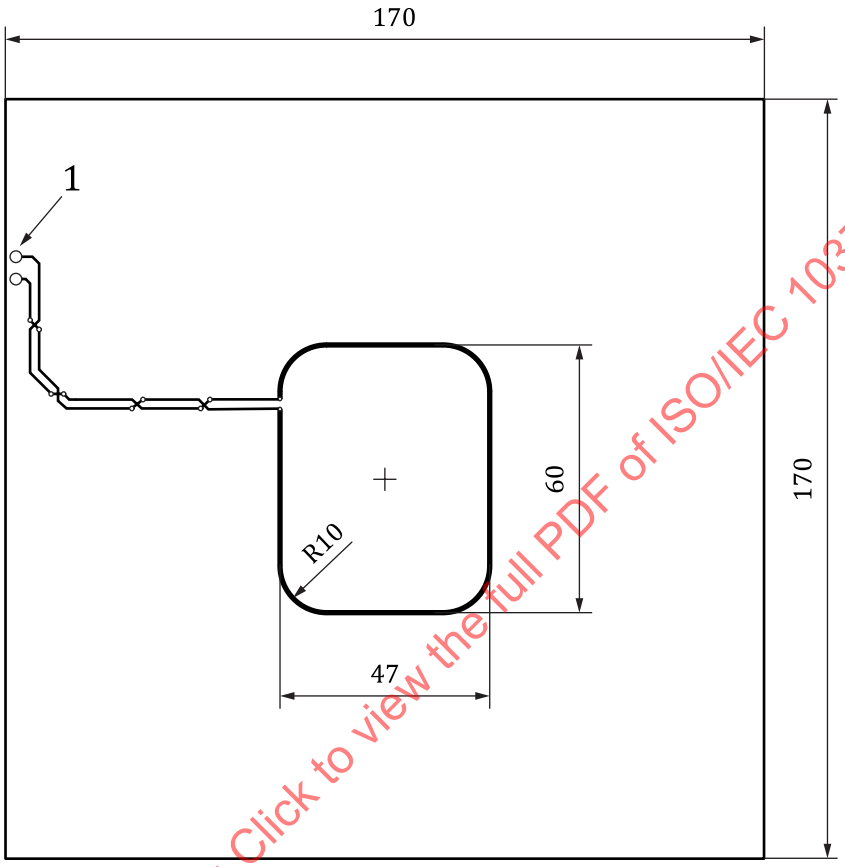
C.1.2 Sense coils 2 layout

Figure C.2 illustrates the sense coils 2 layout.

The sense coil track width is 0,5 mm with relative tolerance ±20 % (except for through-plated holes). Size of the coils refers to the outer dimensions.

Printed circuit board: FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

Dimensions in millimetres



Key

1 connections

NOTE Printed circuit board outside dimensions are informative.

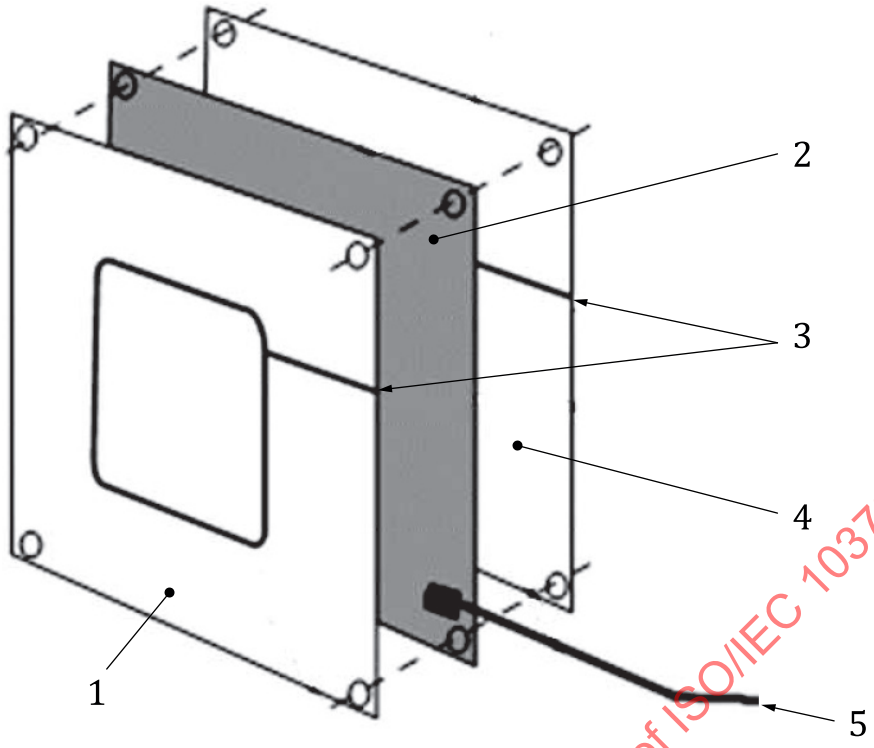
Figure C.2 — Sense coils 2 (a and b) layout

C.1.3 Sense coils assembly

Figure C.3 illustrates the sense coils assembly.

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Key

1 sense coil b
2 test PCD antenna
3 connections
4 sense coil a
5 13,56 MHz signal

Figure C.3 — Sense coils assembly

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Annex D
(normative)

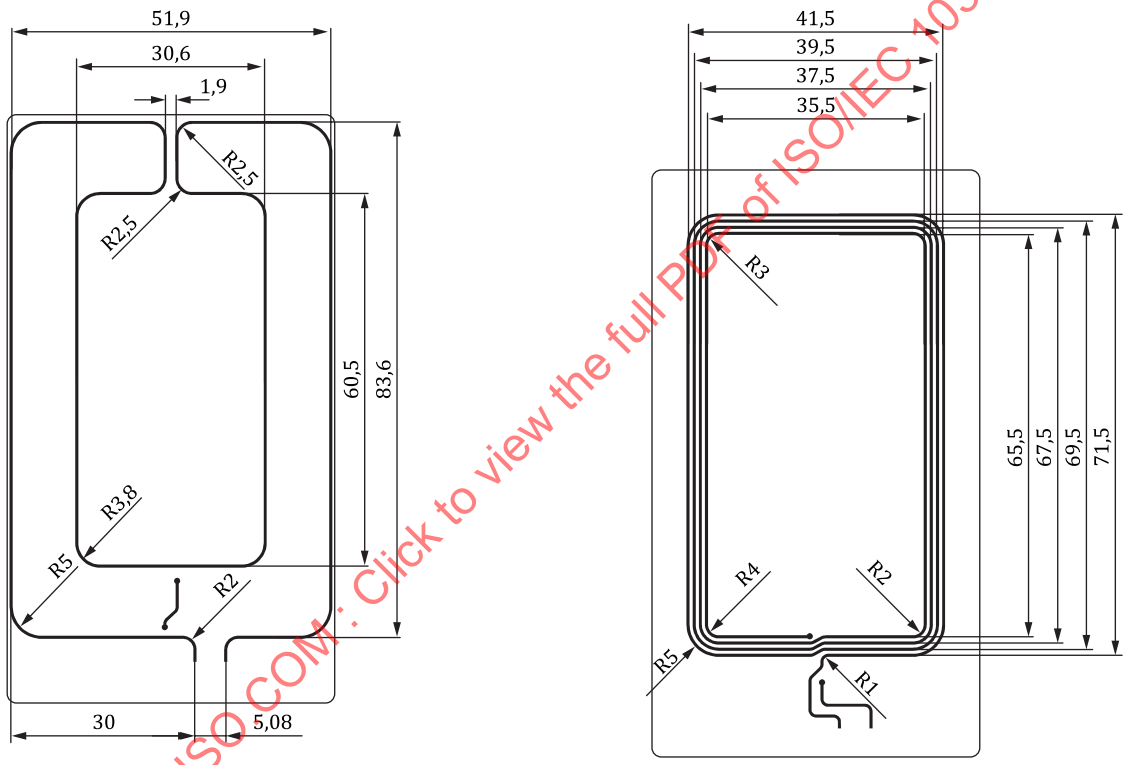
Reference PICCs and Active Reference PICCs

D.1 Reference PICCs

D.1.1 Reference PICC 1 coil layouts

Figure D.1 specifies the Reference PICC 1 pick up coil and main coil layouts.

Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.1 — Reference PICC 1 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The two coils track width and spacing shall be 0,5 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

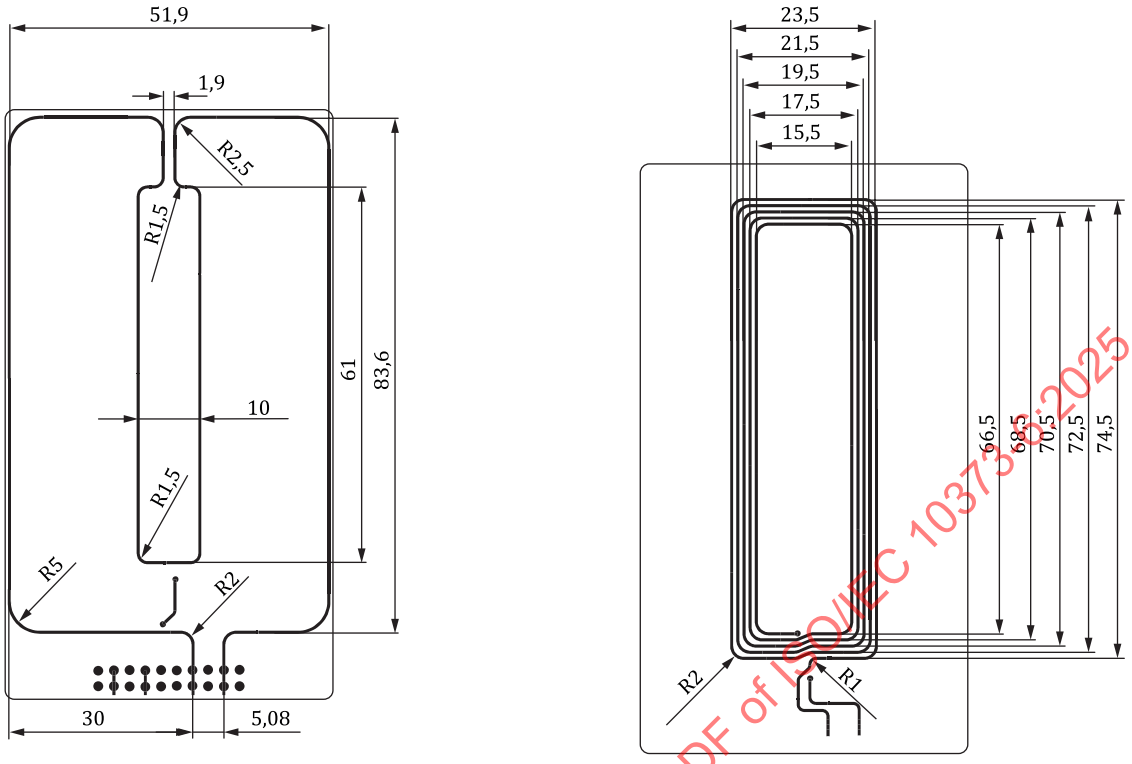
D.1.2 Reference PICC 2 coil layouts

Figure D.2 specifies the Reference PICC 2 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.2 — Reference PICC 2 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The two coils track width and spacing shall be 0,5 mm with a relative tolerance of ±20 %.

All main coil corners radii shall be 2 mm.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

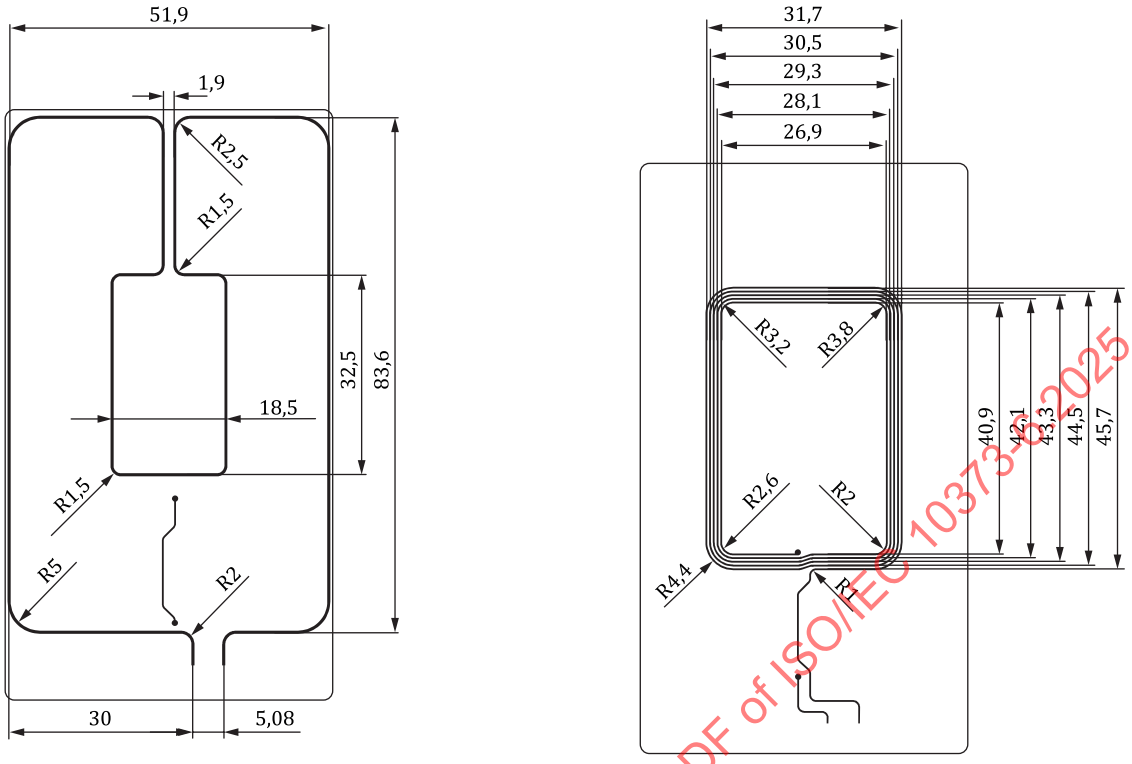
D.1.3 Reference PICC 3 coil layouts

Figure D.3 specifies the Reference PICC 3 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.3 — Reference PICC 3 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The pick up coil track width shall be 0,5 mm with a relative tolerance of ±20 %.

The main coil track width and spacing shall be 0,3 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

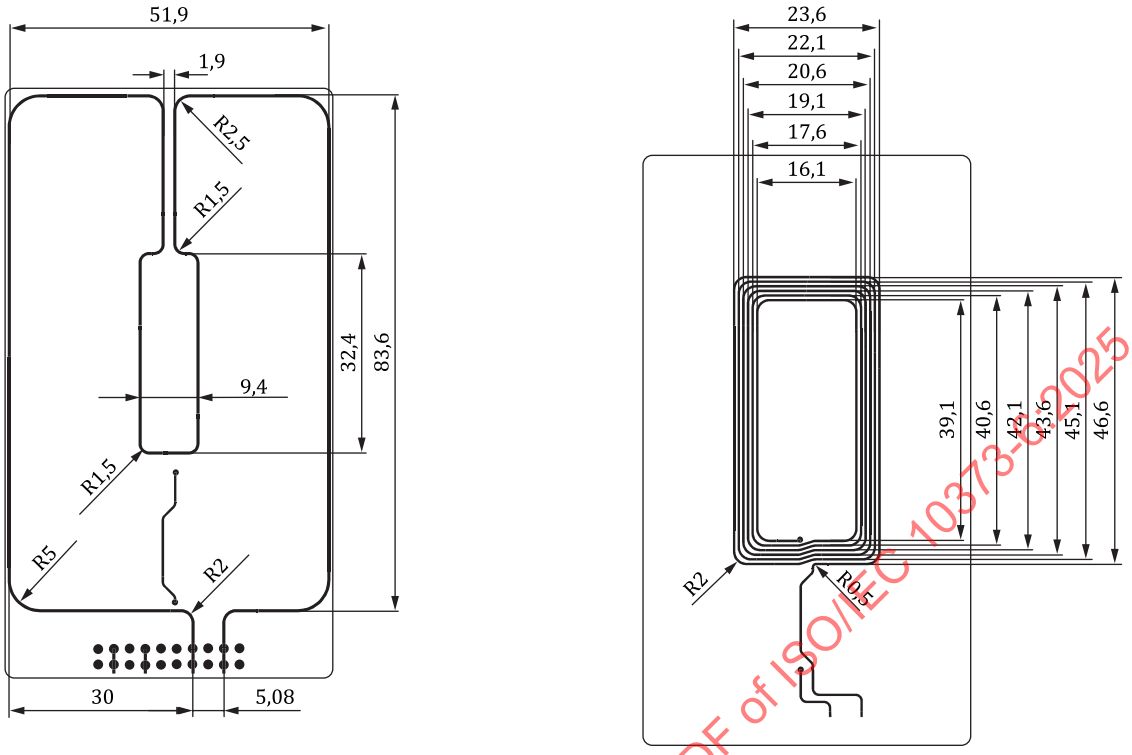
D.1.4 Reference PICC 4 coil layouts

Figure D.4 specifies the Reference PICC 4 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.4 — Reference PICC 4 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The pick up coil track width shall be 0,5 mm with a relative tolerance of ±20 %.

All main coil corners radii shall be 2 mm.

The main coil track width shall be 0,4 mm and the spacing shall be 0,35 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

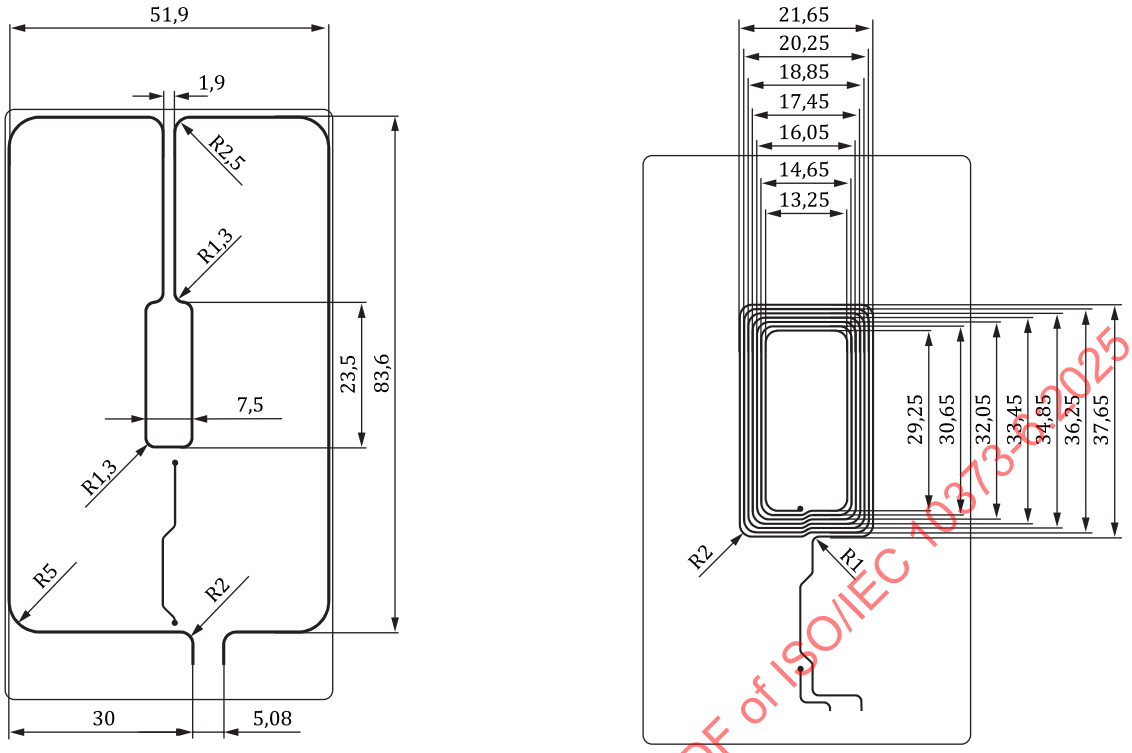
D.1.5 Reference PICC 5 coil layouts

Figure D.5 specifies the Reference PICC 5 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.5 — Reference PICC 5 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The pick up coil track width shall be 0,5 mm with a relative tolerance of ±20 %.

All main coil corners radii shall be 2 mm.

The main coil track width and spacing shall be 0,35 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

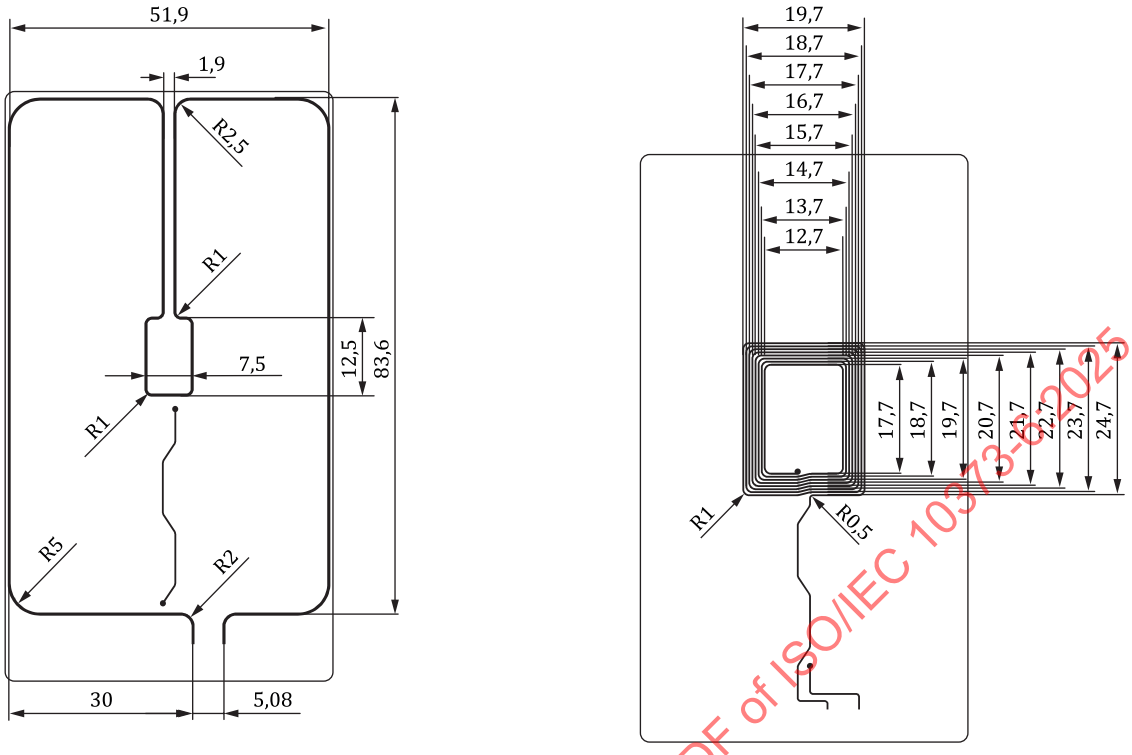
D.1.6 Reference PICC 6 coil layouts

Figure D.6 specifies the Reference PICC 6 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.6 — Reference PICC 6 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The pick up coil track width shall be 0,5 mm with a relative tolerance of ±20 %.

All main coil corners radii shall be 1 mm.

The main coil track width shall be 0,3 mm and the spacing shall be 0,2 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

D.2 Active Reference PICCs

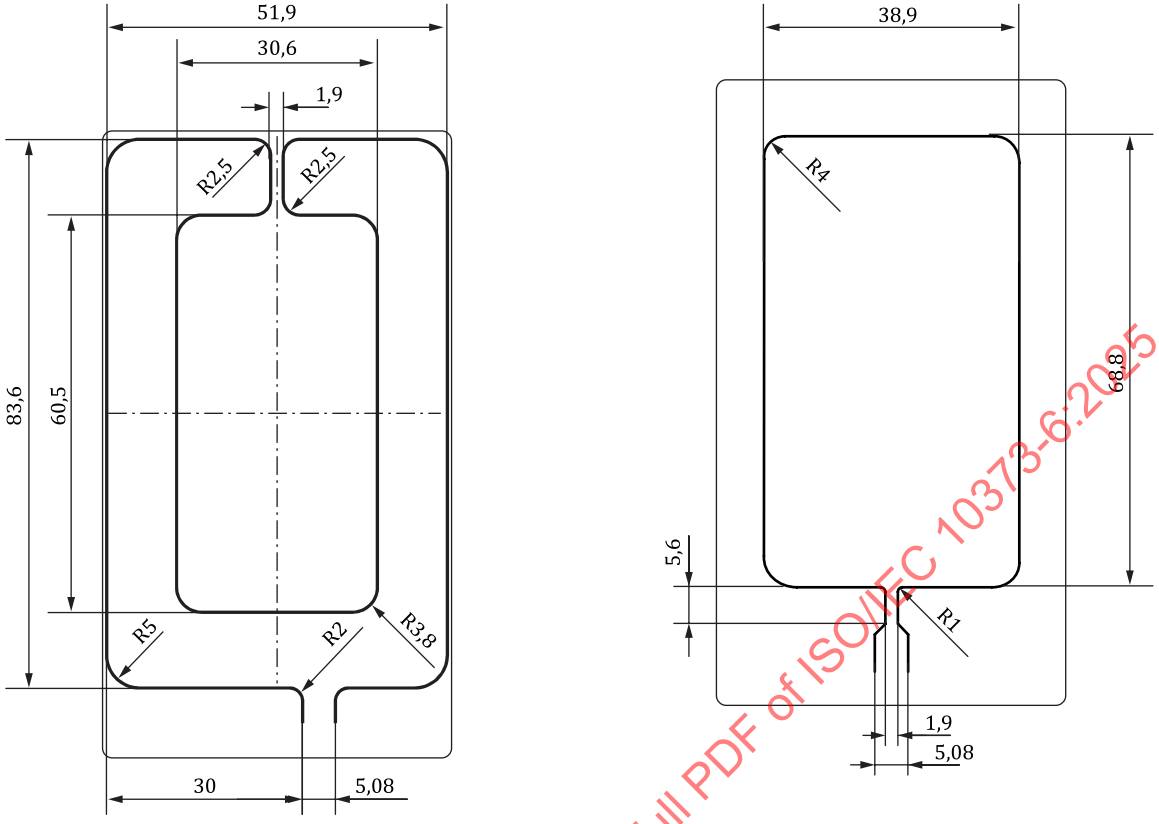
D.2.1 Active Reference PICC 1 coil layouts

Figure D.7 specifies the Active Reference PICC 1 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.7 — Active Reference PICC 1 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The two coils track width and the spacing shall be 0,5 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

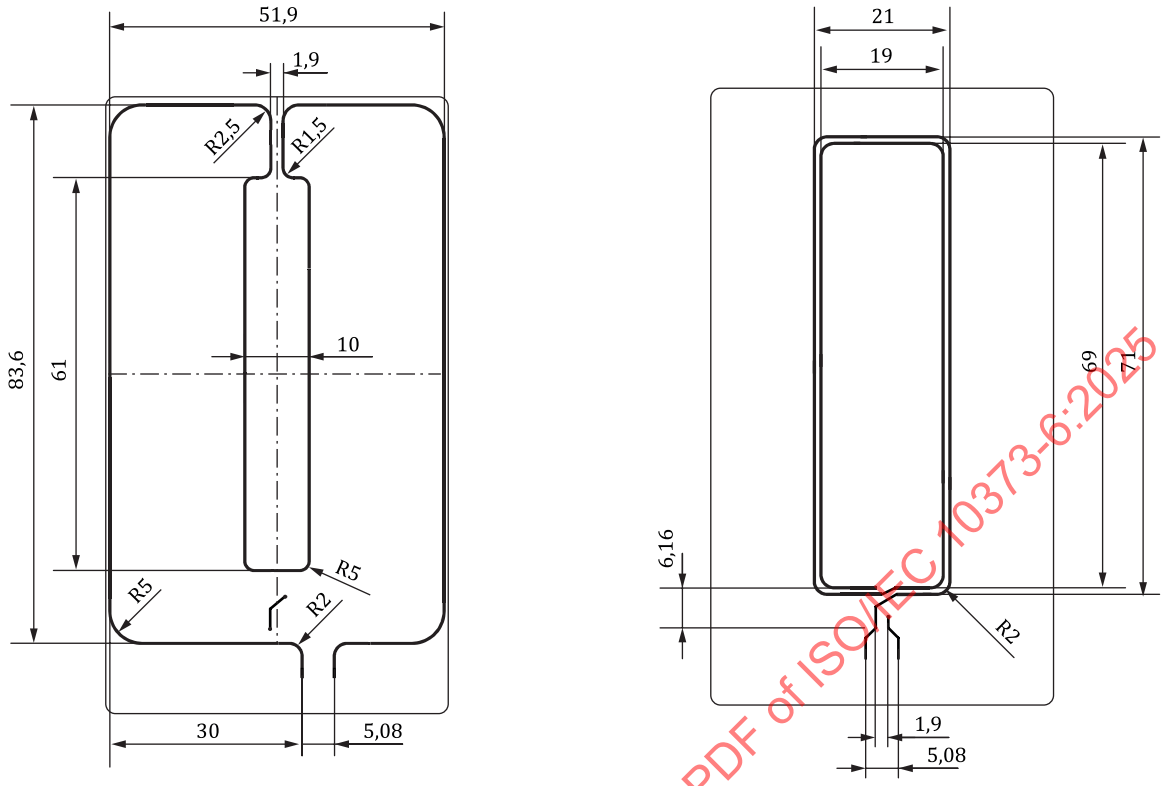
D.2.2 Active Reference PICC 2 coil layouts

Figure D.8 specifies the Active Reference PICC 2 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.8 — Active Reference PICC 2 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The two coils track width and the spacing shall be 0,5 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

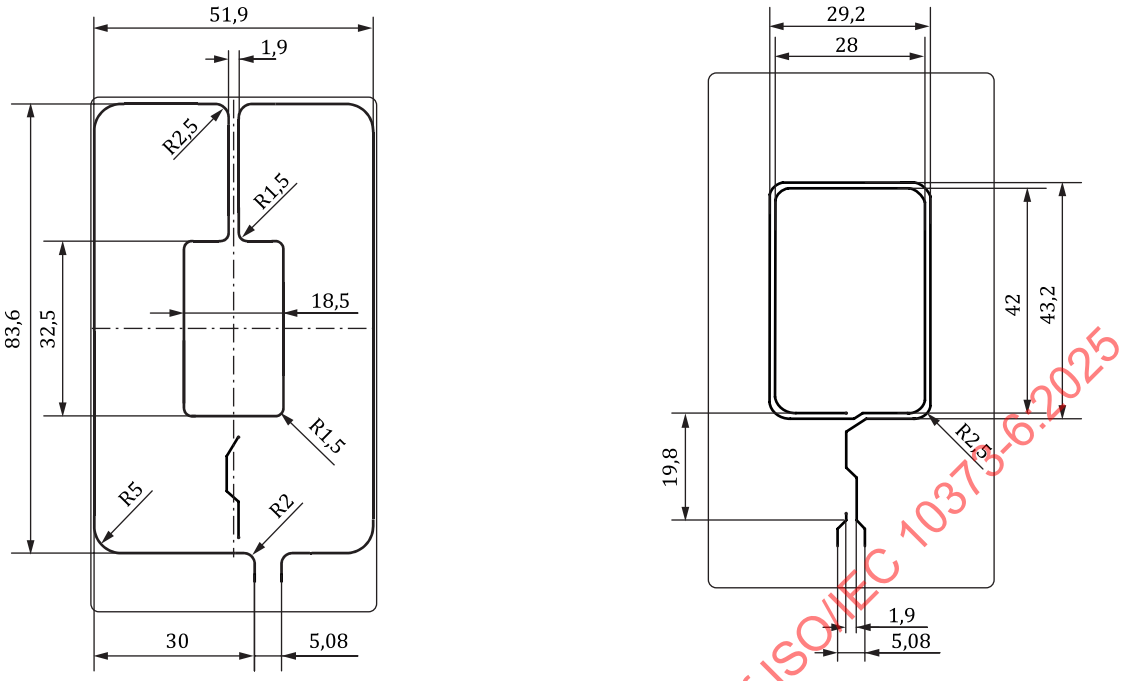
D.2.3 Active Reference PICC 3 coil layouts

Figure D.9 specifies the Active Reference PICC 3 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.9 — Active Reference PICC 3 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The two coils track width and the spacing shall be 0,3 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

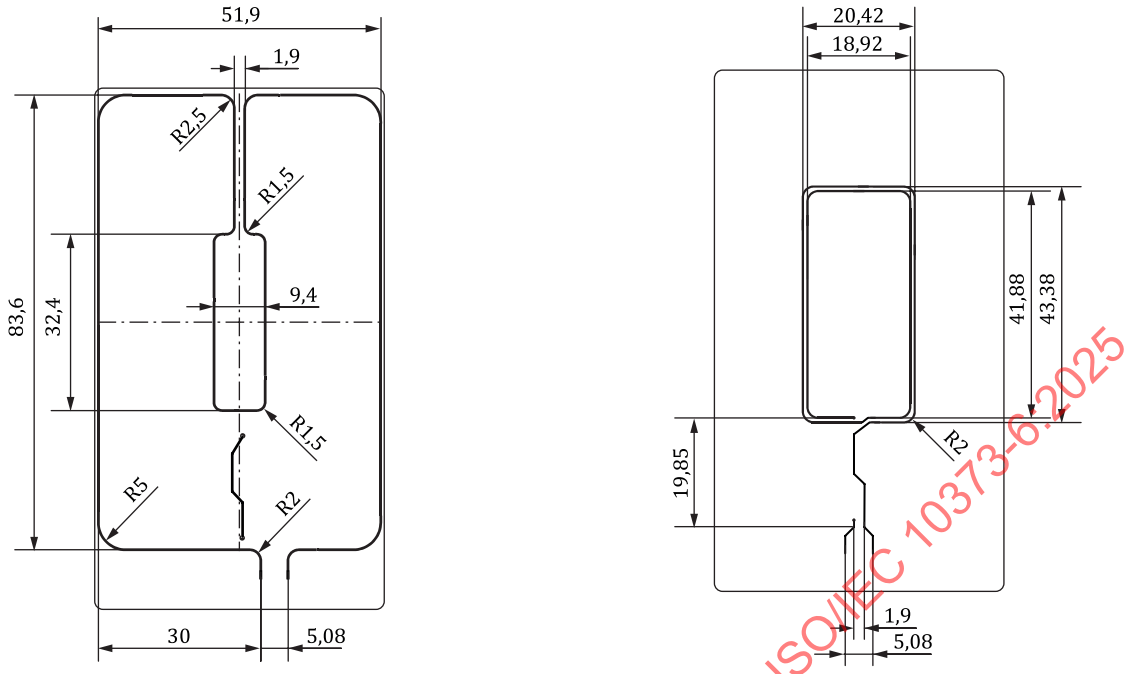
D.2.4 Active Reference PICC 4 coil layouts

Figure D.10 specifies the Active Reference PICC 4 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil

b) View from back, main coil

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.10 — Active Reference PICC 4 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The two coils track width shall be 0,4 mm and the spacing shall be 0,35 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

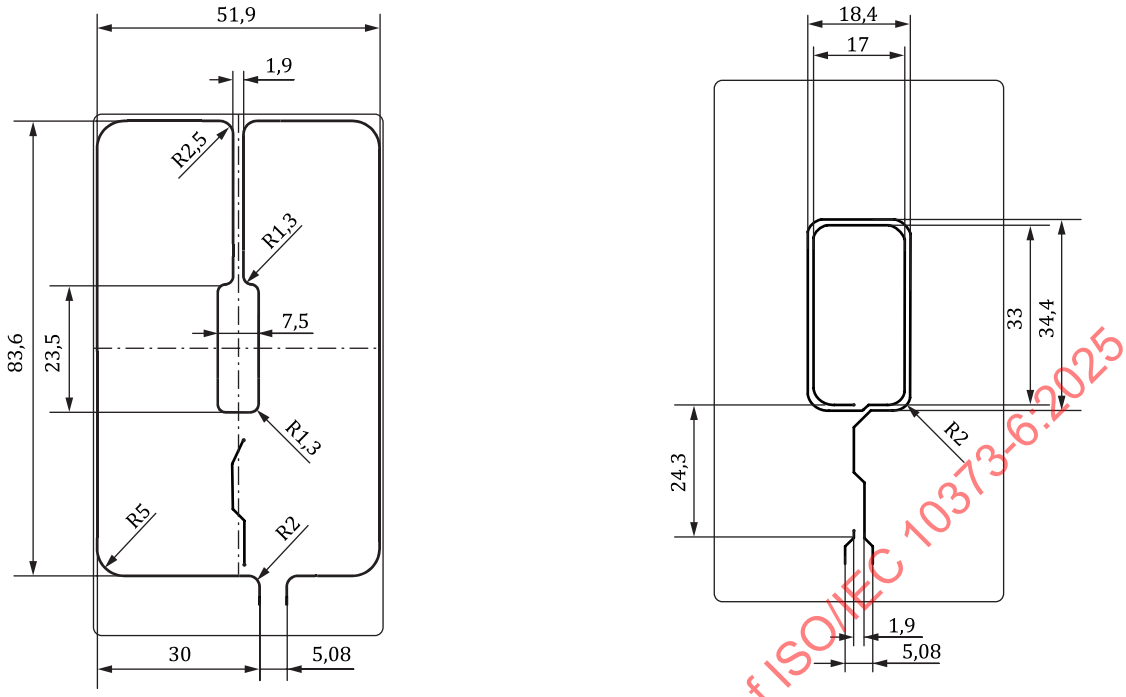
D.2.5 Active Reference PICC 5 coil layouts

Figure D.11 specifies the Active Reference PICC 5 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil **b) View from back, main coil**

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.11 — Active Reference PICC 5 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The two coils track width and the spacing shall be 0,35 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

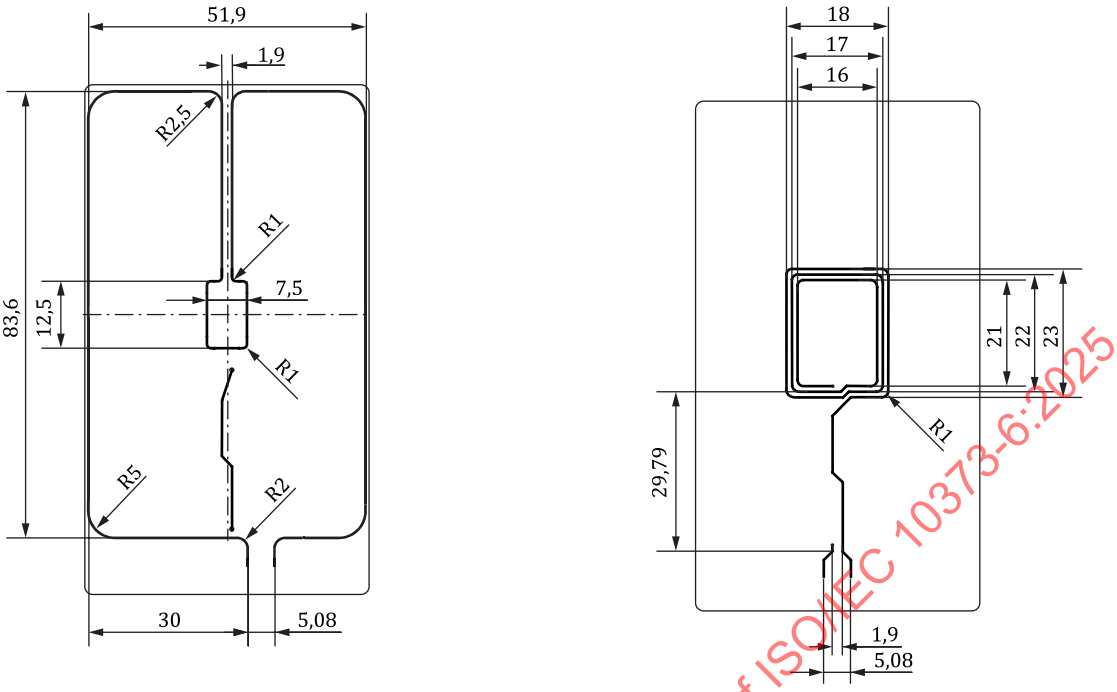
D.2.6 Active Reference PICC 6 coil layouts

Figure D.12 specifies the Active Reference PICC 6 pick up coil and main coil layouts.

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Dimensions in millimetres



a) View from front, pick up coil

b) View from back, main coil

NOTE Dimensions of coil tracks refer to coil track center.

Figure D.12 — Active Reference PICC 6 pick up coil and main coil layouts

The pick up coil and the main coil shall be concentric.

The two coils track width shall be 0,3 mm and the spacing shall be 0,2 mm with a relative tolerance of ±20 %.

Printed circuit board: FR4 material, thickness 0,76 mm with a relative tolerance of ±10 %, double sided with 35 µm copper.

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Annex E
(normative)

PCD modulation index *m* and waveform analysis tool

E.1 Overview

The working principle of the PCD modulation index *m* and waveform analysis tool is illustrated in Figure E.1.

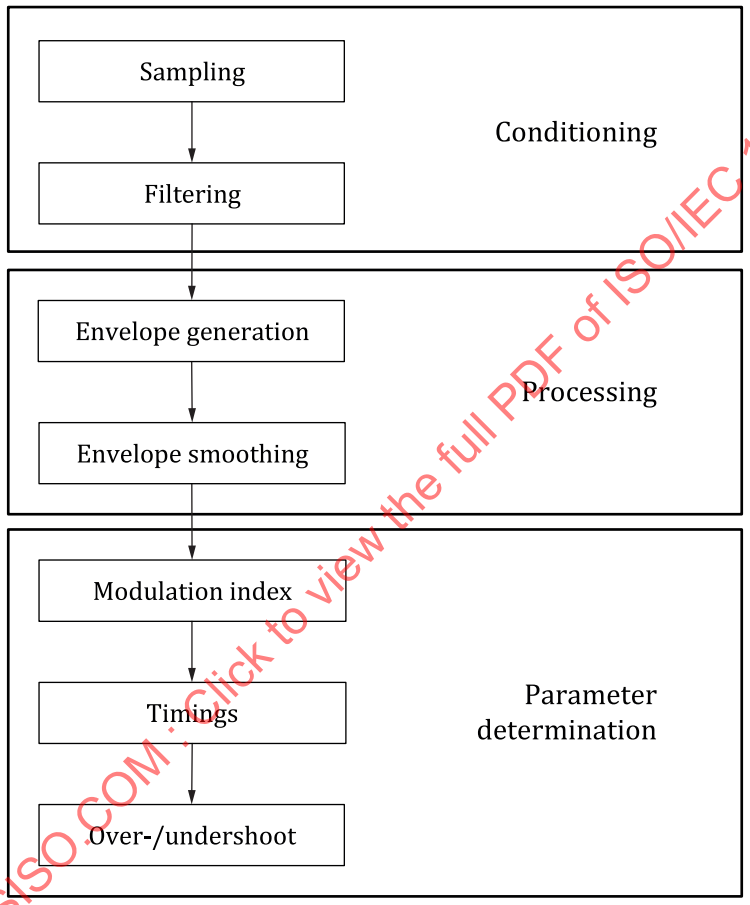


Figure E.1 — PCD modulation index *m* and waveform analysis tool block diagram

Each block is described in the following clauses.

E.2 Sampling

E.2.1 Sampling for PCD to PICC bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$

The oscilloscope used for signal capturing shall fulfill the requirements defined in 5.2.

The time and voltage data of one modulation pulse (see Figure E.2) shall be transferred to a suitable computer.

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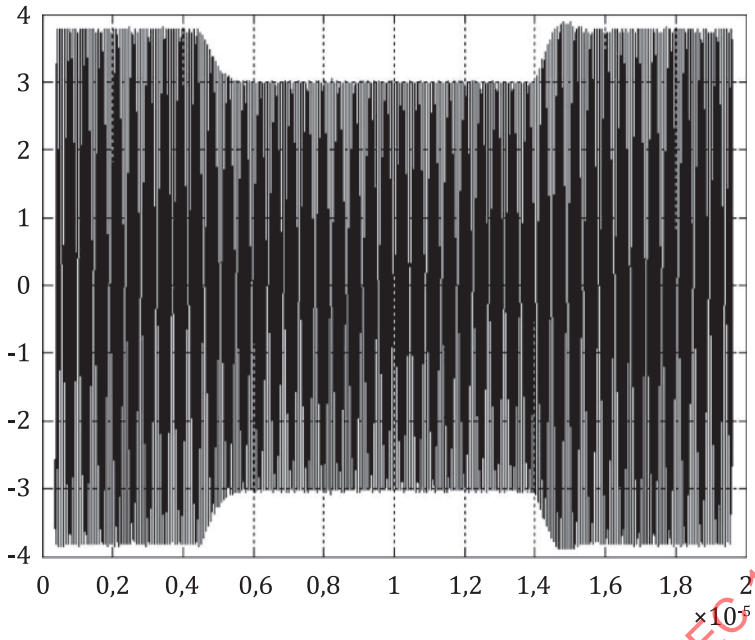


Figure E.2 — Modulation pulse

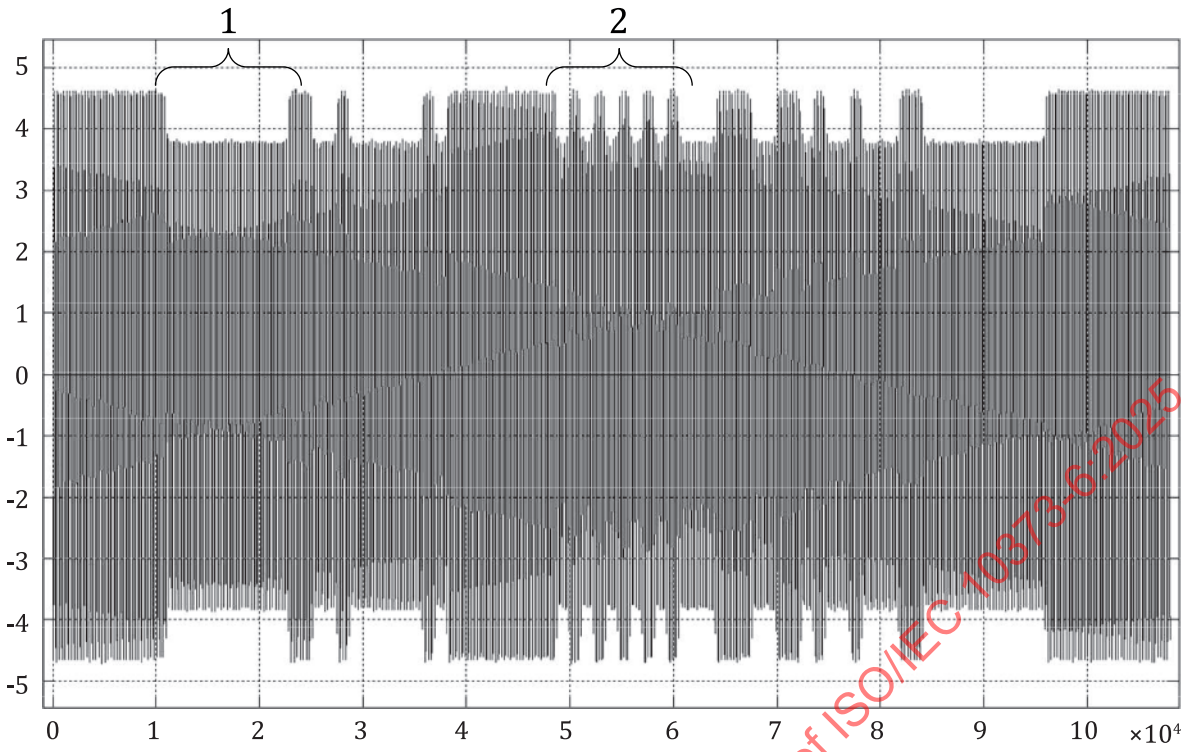
E.2.2 Sampling for PCD to PICC bit rates of $f_c/8$, $f_c/4$ and $f_c/2$

The oscilloscope used for signal capturing shall fulfill the requirements defined in 5.2.

The time and voltage data of a PCD frame containing short and long modulation pulses (preferably a complete S(DESELECT) command) as illustrated in Figure E.3, with at least 20 carrier periods before the first and after the last modulation pulse, shall be transferred to a suitable computer.

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Key

1 long modulation pulse (SOF low)

2 short modulation pulses (10101010)b

Figure E.3 — Modulation pulses

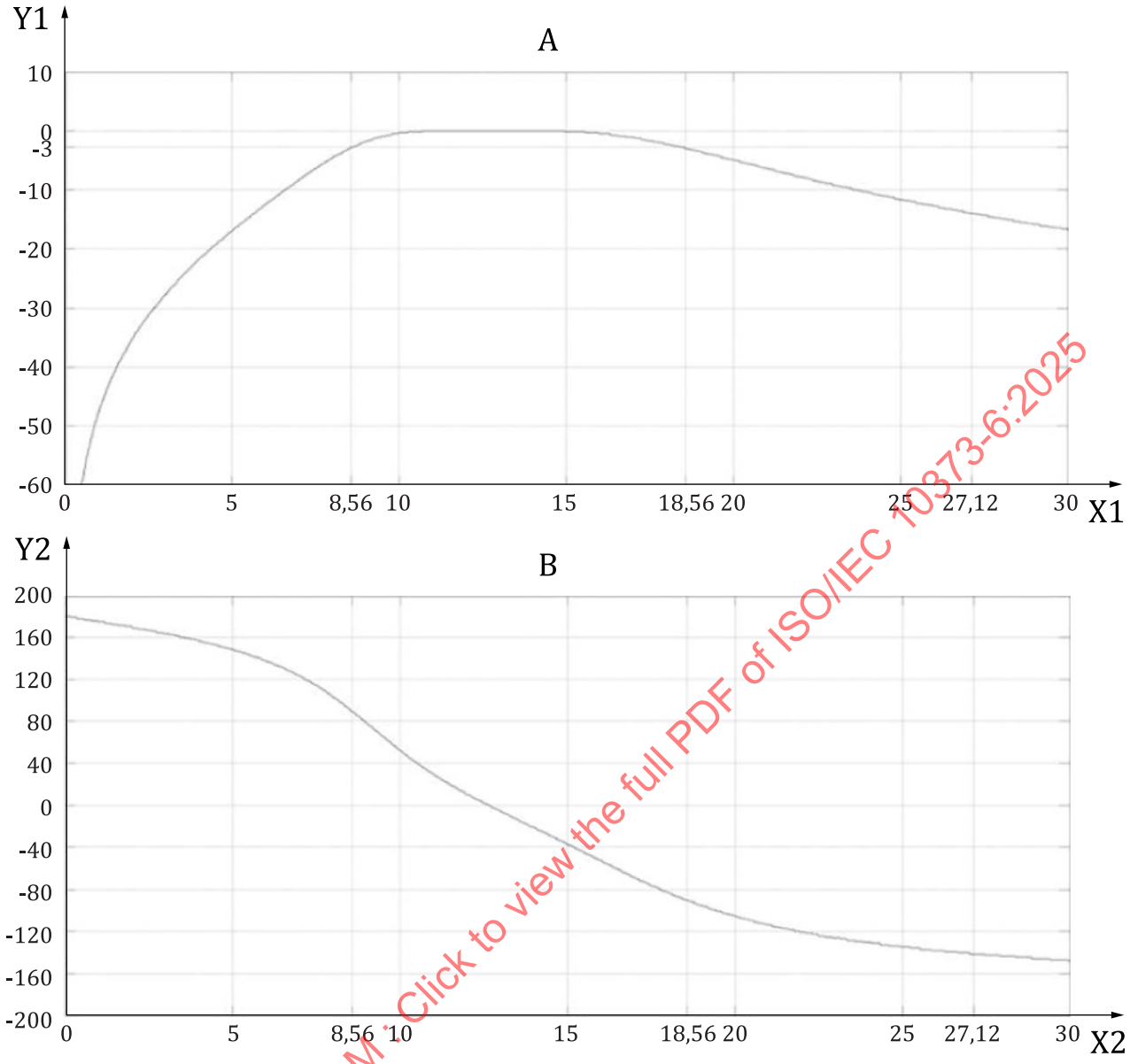
E.3 Filtering

E.3.1 Filtering for PCD to PICC bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$

A 4th order, Butterworth type band pass filter with center frequency of 13,56 MHz and 10 MHz 3 dB bandwidth shall be used for filtering the DC and higher harmonic components. The filter characteristic is illustrated in Figure E.4.

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Key

X_1 frequency (MHz)
Y_1 magnitude (dB)
X_2 frequency (MHz)
Y_2 phase (degree)
A graph: filter magnitude characteristics
B graph: filter phase characteristics

Figure E.4 — Filter characteristics

E.3.2 Filtering for PCD to PICC bit rates of $f_c/8$, $f_c/4$ and $f_c/2$

A 4th order, Butterworth type band pass filter with center frequency of 13,56 MHz and 15 MHz 3 dB bandwidth shall be used for filtering the DC and higher harmonic components.

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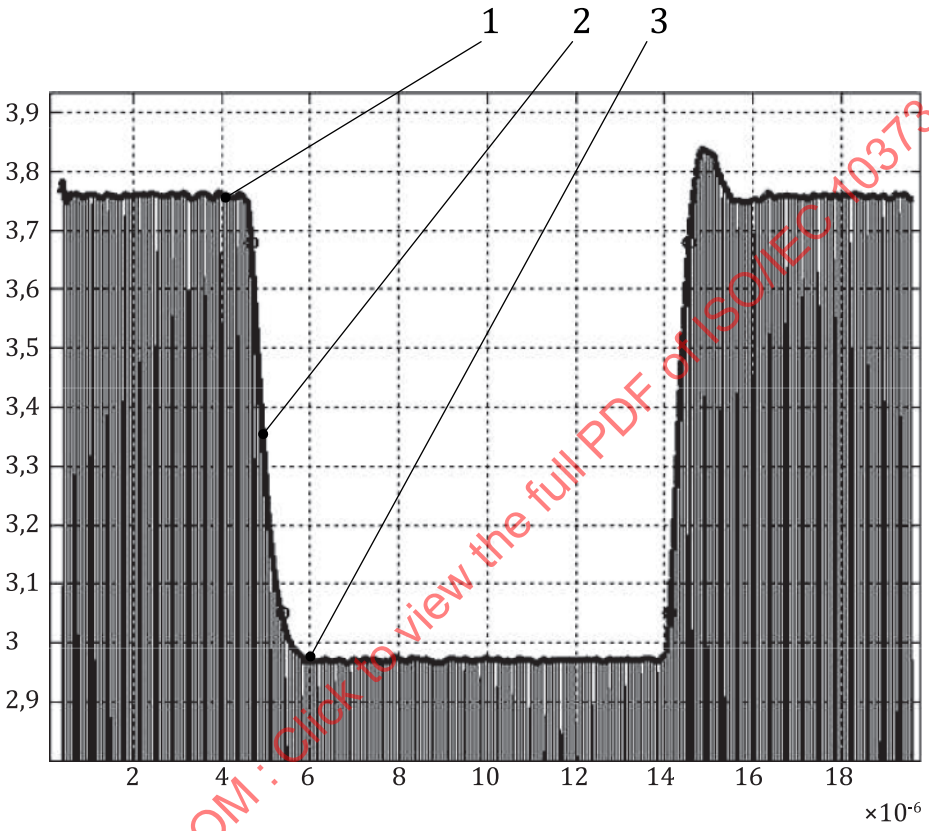
E.4 Envelope generation

The filtered signal shall be Hilbert transformed and the magnitude of this complex transform represents the signal envelope.

E.5 Envelope smoothing

E.5.1 Envelope smoothing for PCD to PICC bit rates of $f_c/128$, $f_c/64$, $f_c/32$ and $f_c/16$

The signal envelope shall be smoothened with a moving average filter and the filter period shall be one carrier period. The smoothened envelope signal is illustrated in Figure E.5.



Key

1 initial envelope signal amplitude
2 envelope signal, smoothened
3 modulated envelope signal amplitude

Figure E.5 — Envelope smoothing

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E.5.2 Envelope smoothing for PCD to PICC bit rates of $f_c/8$, $f_c/4$ and $f_c/2$

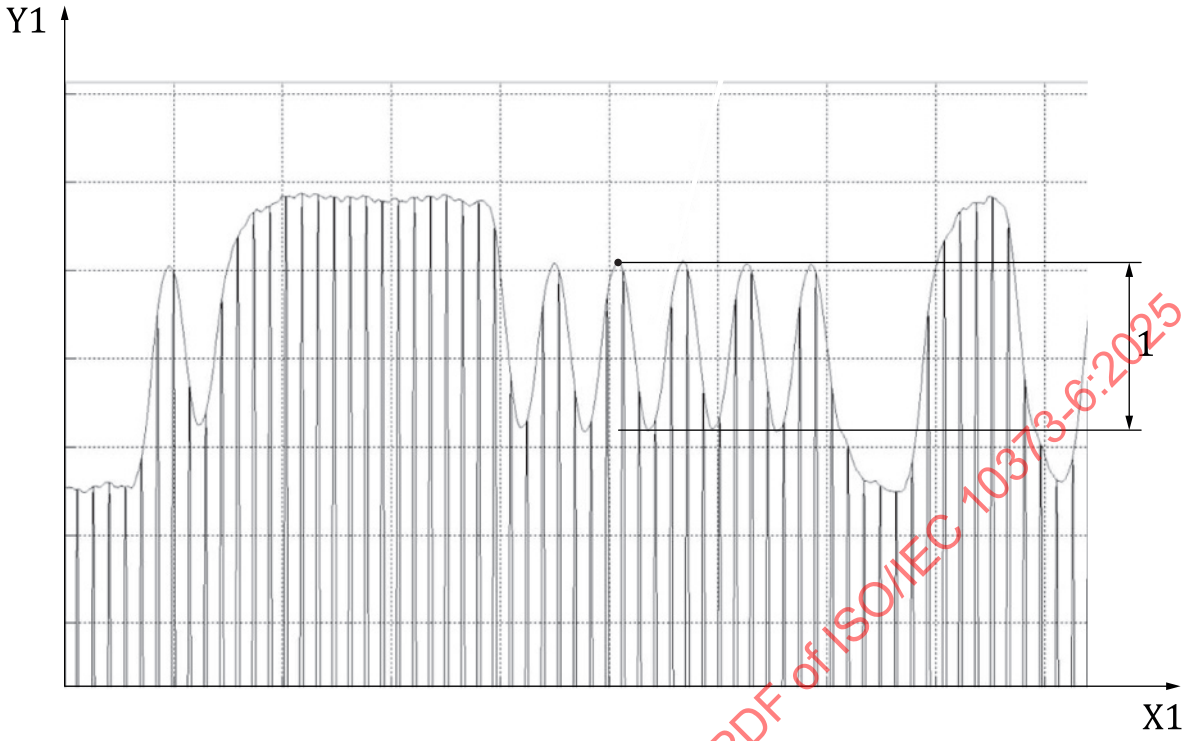
No smoothing of the signal envelope shall be applied.

E.6 Modulation index *m* determination

The initial and modulated envelope signal amplitudes shall be determined by calculating the histogram of the smoothened envelope signal. The most frequent values correspond to the initial and modulated envelope signal amplitude. For Type A modulation signals only the initial envelope signal amplitude shall be determined using the histogram approach.

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For PCD to PICC bit rates of $f_c/8$, $f_c/4$ and $f_c/2$ the minimum value of modulation index m shall be determined within the complete PCD frame (see Figure E.6). The PCD frame shall contain (10101010)b.



Key

X1 time

Y1 amplitude

1 minimum value of modulation index m

Figure E.6 — Minimum value of modulation index *m*

The rise and fall times should be determined according to the definitions in ISO/IEC 14443-2.

For PCD to PICC bit rates of $f_c/8$, $f_c/4$ and $f_c/2$ the timings shall be determined at positions with long modulation pulse positions, e.g., t_f at transition to SOF low and t_r at transition to EOF high.

E.7 Overshoot and undershoot determination

The envelope signal shall be smoothened by a moving average filter over 3 carrier periods before determining the overshoot and undershoot values according to the definitions in ISO/IEC 14443-2.

E.8 Program of the PCD modulation index *m* and waveform analysis tool

This informative program written in ANSI C language gives an example for the implementation of the PCD modulation index m and waveform analysis tool.

It is published separately and can be found at https://standards.iso.org/iso-iec/10373/-6/ed-5/en/.

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Annex F
(informative)

Program for the evaluation of the load modulation amplitude

This program written in ANSI C language gives an example for the calculation of the amplitude of the load modulation.

It is published separately and can be found at https://standards.iso.org/iso-iec/10373/-6/ed-5/en/.

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Annex G
(normative)

Additional PICC test methods

G.1 PICC-test-apparatus and accessories

G.1.1 General

This clause defines the test apparatus and test circuits for verifying the operation of a PICC according to ISO/IEC 14443-3. The test apparatus includes the following:

a) calibration coil (see 5.3);

b) Test PCD assembly (see 5.4);

c) digital sampling oscilloscope (see 5.2).

Care shall be taken to ensure that the results are not affected by the RF performance of the test circuits.

G.1.2 Emulating the I/O protocol

The PICC-test-apparatus shall be able to emulate the Type A and Type B protocols, which are required to test a PICC.

G.1.3 Generating the I/O character timing in reception mode

The PICC-test-apparatus shall be able to generate the I/O bit stream according to ISO/IEC 14443-3. Timing parameters: start bit length, guard time, bit width, request guard time, start of frame width, end of frame width shall be configurable.

G.1.4 Measuring and monitoring the RF I/O protocol

The PICC-test-apparatus shall be able to measure and monitor the timing of the logical low and high states of the RF Input/Receive line relative to the clock frequency. The PICC-test-apparatus shall be able to monitor the PICC subcarrier.

G.1.5 Protocol Analysis

The PICC-test-apparatus shall be able to analyse the I/O-bit stream in accordance with protocol Type A and Type B as specified in ISO/IEC 14443-3 and ISO/IEC 14443-4 and extract the logical data flow for further protocol analysis.

G.1.6 RFU fields and values

RFU fields should be constantly monitored during the testing and shall always be verified to contain the assigned default value. A test shall be FAIL and the tested PICC shall be declared non-conformant in case an RFU field is not set to its default value at any time.

Functional fields should be constantly monitored during the testing and shall always be verified to contain only functional values documented in the standard or proprietary values documented in the standard. A test shall be FAIL and the tested PICC shall be declared non-conformant in case a functional field is not set to said values (and thus is set to an RFU or restricted value) at any time.

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G.1.7 Measuring timing

G.1.7.1 Timing measurements

The PICC-test-apparatus shall continuously monitor the following frame format and timing values:

a) for PICC Type A:

   1) frame delay time PCD to PICC (see ISO/IEC 14443-3:2018, 6.2.1.1), with respect to the minimum FDT and the maximum FDT (= FWT), where the use of the determination method defined in Annex B is not mandatory;

   2) frame formats (see ISO/IEC 14443-3:2018, 6.2.3);

   3) frame waiting time (see ISO/IEC 14443-4:2018, 7.3).

b) for PICC Type B:

   1) character, frame format and timing (see ISO/IEC 14443-3:2018, 7.1);

   2) frame waiting time (see ISO/IEC 14443-4:2018, 7.3).

A test shall be FAIL and the tested PICC shall be declared non-conformant in case one of the listed timing constraints is violated.

G.1.7.2 Timing measurement report

Fill Table G.78 for PICC Type A or Table G.79 for PICC Type B, or both, with the measured timing values.

G.2 General considerations

G.2.1 Use of test commands

For the test commands defined in 3.2, the PICC-test-apparatus shall take into account the following rules.

a) On TEST_COMMAND2 and TEST_RESPONSE2: If the PICC does not support any command expecting a response consisting of n chained I-blocks, the scenarios using TEST_COMMAND2 are not applicable.

b) On TEST_COMMAND3 and TEST_RESPONSE3: If the PICC does not support any command needing more than FWT time for execution, the scenarios using TEST_COMMAND3 are not applicable.

G.2.2 Relationship of test methods versus base standard requirement

Table G.1 lists the applicable tests for PICCs Type A.

Table G.2 lists the applicable tests for PICCs Type B.

Table G.3 lists the applicable tests for both PICCs Type A and Type B.

The ISO/IEC 14443-4 PICC should also conform with ISO/IEC 14443-3 and should be subjected to both the ISO/IEC 14443-3 and ISO/IEC 14443-4 tests for the applicable communication signal interface.

A PICC conformant with ISO/IEC 14443-3 but not with ISO/IEC 14443-4 and in ACTIVE or ACTIVE* state (see G.3.3.7, G.3.3.12 and G.4.4.7) may respond with any frame (including Mute) to frames not related to ISO/IEC 14443-3.

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Table G.1 — Test methods for logical operation of the PICC Type A protocol

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	Name	Base standard	Clause(s)
G.3.2	Polling	ISO/IEC 14443-3:2018	5.2
G.3.3	Testing of the PICC Type A state transitions	ISO/IEC 14443-3:2018	6.3, 6.4, 6.5
G.3.4	Handling of Type A anticollision	ISO/IEC 14443-3:2018	6.4.2
G.3.5	Handling of RATS	ISO/IEC 14443-4:2018	5.7.1.2
G.3.6	Handling of PPS request	ISO/IEC 14443-4:2018	5.7.2.2
G.3.7	Handling of FSD	ISO/IEC 14443-4:2018	5.7
G.3.8	Handling of frame delay time PICC to PCD and SFGT	ISO/IEC 14443-3:2018 ISO/IEC 14443-4:2018	6.2.1 5.3.5
G.3.9	PICC bit rates capability	ISO/IEC 14443-3:2018	6.1, 6.2

Table G.2 — Test methods for logical operation of the PICC Type B protocol

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	Name	Base standard	Clause(s)
G.4.2	Polling	ISO/IEC 14443-3:2018	5.2
G.4.3	PICC framing and bit rates capability	ISO/IEC 14443-3:2018	7.1
G.4.4	Testing of the PICC Type B state transitions	ISO/IEC 14443-3:2018	7.4 to 7.12
G.4.5	Handling of Type B anticollision	ISO/IEC 14443-3:2018	7.4 to 7.12
G.4.6	Handling of ATTRIB	ISO/IEC 14443-3:2018	7.10
G.4.7	Handling of Maximum Frame Size	ISO/IEC 14443-3:2018	7.10.4
G.4.8	Handling of TR2 and SFGT	ISO/IEC 14443-3:2018 ISO/IEC 14443-3:2018	7.9.4.4 7.9.4.7

Table G.3 — Test methods for logical operation of PICC Type A or Type B

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	Name	Base standard	Clause(s)
G.5.2	PICC reaction to ISO/IEC 14443-4 scenarios	ISO/IEC 14443-4:2018	Clause 7
G.5.3	Handling of PICC error detection	ISO/IEC 14443-4:2018	7.6.7
G.5.4	PICC reaction on CID	ISO/IEC 14443-4:2018	7.2.2.2
G.5.5	PICC reaction on NAD	ISO/IEC 14443-4:2018	7.2.2.3
G.5.6	PICC reaction on S(PARAMETERS) blocks	ISO/IEC 14443-4:2018	7.6.1

G.3 Test method for initialization of the PICC Type A

G.3.1 General

The tests in this subclause determine whether a PICC Type A conforms to ISO/IEC 14443-3 and the protocol activation sequence in ISO/IEC 14443-4:2018, Clause 5. If conformance with ISO/IEC 14443-4 is not required, all tests containing ISO/IEC 14443-4 commands need not be applied.

G.3.2 Scenario G.1: Polling

G.3.2.1 Scope

This test is to determine the behaviour of the PICC Type A on receiving REQA commands according to ISO/IEC 14443-3:2018, 5.2.

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G.3.2.2 Procedure

Perform the following steps for 3 different field strengths of H_{min}, $(H_{min} + H_{max})/2$ and H_{max} as specified for the respective PICC class:

a) Place the PICC into the field and adjust it.

b) Switch the RF operating field off for a minimum time for resetting a PICC (see ISO/IEC 14443-3:2018, 5.2.5).

c) Switch the RF operating field on.

d) Do delay of 5 ms and send a valid REQA command.

e) Record the presence and the content of the PICC response.

f) Switch the RF operating field off for a minimum time for resetting a PICC (see ISO/IEC 14443-3:2018, 5.2.5).

g) Switch the RF operating field on.

h) Wait 5 ms and send a valid REQB command (using Type B modulation and bit coding).

i) Wait 5 ms and send a valid REQA command.

j) Record the presence and the content of the PICC response.

G.3.2.3 Test report

The test is:

a) PASS only when the PICC's response is a valid ATQA in both steps e) and j); and

b) FAIL in any other case.

G.3.3 Testing of the PICC Type A state transitions

G.3.3.1 Scope

These tests verify the correct implementation of the PICC Type A state diagram as described in ISO/IEC 14443-3:2018, 6.3.

G.3.3.2 General test outline

G.3.3.2.1 General

For an exhaustive test of the PICC Type A state machine, the correctness of every possible state transition at every state shall be verified. Verifying a specific state using a specific state transition will be done as follows.

First, reset the PICC and place it in the TIS. This is one of the states from StateSet where the transitions (T) shall be verified. Then execute a transition (T) from TransitionSet. After execution of the state transition, check if the PICC is in the expected TTS. There is a difficulty in how to perform this check, because it is impossible to directly inspect the state machine of the PICC. The solution to this problem is to make some additional state transitions and checking the answer of the PICC. The transitions for this purpose are selected in such way that the state can be determined from the PICC answers as precisely as possible.

G.3.3.2.2 Functions for putting the PICC in the TIS

Putting the PICC into the TIS will be done by a sequence of transition commands specified in the following tables. The general method is as follows:

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In order to put the PICC into the TIS, look up the corresponding state transition sequence in Table G.4. Then successively apply the state transitions described in the State Transition Sequence column by looking up the corresponding commands in Table G.5. Always check the content and integrity of the PICC response.

Table G.4 — State transition sequence table

TIS	State transition sequence
POWER-OFF	—
IDLE[a]	POWER-OFF → IDLE
READY(1)	POWER-OFF → IDLE → READY(1)
READY(2)	POWER-OFF → IDLE → READY(1) → READY(2)
READY(3)	POWER-OFF → IDLE → READY(1) → READY(2) → READY(3)
ACTIVE	POWER-OFF → IDLE → READY(1) → … → READY(CascadeLevels) → ACTIVE
PROTOCOL	POWER-OFF → IDLE → READY(1) → … → READY(CascadeLevels) → ACTIVE → PROTOCOL
HALT	POWER-OFF → IDLE → READY(1) → …→ READY(CascadeLevels) → ACTIVE → HALT
READY*(1)	POWER-OFF → IDLE → READY(1) → … → READY(CascadeLevels) → ACTIVE → HALT → READY*(1)
READY*(2)	POWER-OFF → IDLE → READY(1) → … → READY(CascadeLevels) → ACTIVE → HALT → READY*(1) → READY*(2)
READY*(3)	POWER-OFF → IDLE → READY(1) → … → READY(CascadeLevels) → ACTIVE → HALT → READY*(1) → READY*(2) → READY*(3)
ACTIVE*	POWER-OFF → IDLE → READY(1) → …→ READY(CascadeLevels) → ACTIVE → HALT → READY*(1) → … → READY*(CascadeLevels) → ACTIVE*

[a] IDLE state may be reached from ACTIVE state.

Table G.5 — State transition table

State → Next state	PICC-test-apparatus		PICC
POWER-OFF → IDLE	Power On (RF Field on)	→	
		←	Mute
IDLE → READY(1)	REQA	→	
		←	ATQA
READY(1) → READY(2)	SELECT(1)[a]	→	
		←	SAK (cascade)
READY(2) → READY(3)	SELECT(2)[a]	→	
		←	SAK (cascade)
READY(CascadeLevels) → ACTIVE	SELECT (CascadeLevels)[a]	→	
		←	SAK (complete)
ACTIVE → PROTOCOL	RATS(0,0)	→	
		←	ATS
ACTIVE → HALT	HLTA	→	
		←	Mute
HALT → READY*(1)	WUPA	→	
		←	ATQA
READY*(1) → READY*(2)	SELECT(1)	→	
		←	SAK (cascade)

[a] If the PICC UID is unknown, SELECT command may be preceded with an anticollision command to retrieve the PICC UID.

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Table G.5 *(continued)*

State → Next state	PICC-test-apparatus		PICC
READY*(2) → READY*(3)	SELECT(2)	→	
		←	SAK(cascade)
READY*(CascadeLevels) →ACTIVE*	SELECT (CascadeLevels)	→	
		←	SAK (complete)
ACTIVE → IDLE	REQA	→	
		←	Mute
[a] If the PICC UID is unknown, SELECT command may be preceded with an anticollision command to retrieve the PICC UID.			

G.3.3.2.3 Functions for checking the validity of the TTS

G.3.3.2.3.1 General

Table G.6 describes the state transitions, which are used to check whether the PICC is in the state S. The content of the PICC answer (i.e. ATQA, SAK ...) should be thoroughly checked for ISO/IEC 14443-3 and ISO/IEC 14443-4 conformance. Note that these tests can cause the PICC to change its state.

G.3.3.2.3.2 Distinguishing READY (I) and ACTIVE states

The READY(I)/READY*(I) states and the ACTIVE/ACTIVE* states cannot be distinguished with one test run. In order to distinguish the "*"-states from the non-"*"-states, perform the following steps:

a) Rerun the test a second time, without checking the TTS.

b) Send REQA command. The PICC response shall be Mute.

c) Send REQA command.

d) If the PICC response is Mute then the PICC state was a "*"-state.

e) Else the PICC was a non-"*"-state.

G.3.3.2.3.3 Distinguishing HALT state

The HALT state cannot be distinguished from READY*(I) state and from ACTIVE* state with one test run. In order to distinguish the HALT state perform the following steps:

a) Rerun the test a second time, without checking the TTS.

b) Send WUPA command. The PICC response shall be ATQA.

Table G.6 — Checking the TTS

State S	PICC-test-apparatus		PICC
IDLE	REQA	→	
		←	ATQA[a]
READY(I), I < CascadeLevels	SELECT(I)	→	
		←	SAK (cascade)
READY(I), I = CascadeLevels	SELECT(I)	→	
		←	SAK (complete)
ACTIVE	RATS (0,0)	→	
		←	ATS
PROTOCOL	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
[a] If the PICC UID is known, send an anticollision command to retrieve the PICC UID. Check that the PICC UID has not changed.			

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Table G.6 *(continued)*

State S	PICC-test-apparatus		PICC
HALT	REQA	→	
		←	Mute
	WUPA	→	
		←	ATQA[a]
READY*(I), I < CascadeLevels	SELECT (I)	→	
		←	SAK (cascade)
READY*(I), I = CascadeLevels	SELECT (I)	→	
		←	SAK (complete)
ACTIVE*	RATS(0,0)	→	
		←	ATS

[a] If the PICC UID is known, send an anticollision command to retrieve the PICC UID. Check that the PICC UID has not changed.

NOTE The block number can be 0 or 1 dependent on block numbering rules, see ISO/IEC 14443-4:2018, 7.6.4.

G.3.3.3 Scenario G.2: Behaviour of the PICC Type A in the IDLE state

G.3.3.3.1 Scope

This test is to determine the behaviour of the PICC Type A in the IDLE state according to ISO/IEC 14443-3:2018, 6.3.2.

G.3.3.3.2 Procedure

Perform the following steps for every row of Table G.7:

a) Put the PICC into IDLE state. If the UID is unknown, put the PICC in ACTIVE state to retrieve its UID and then put it into IDLE state using ACTIVE → IDLE state transition. Check that the value "88" of the cascade tag CT is not used for uid0 in single size UID.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.7 — Transitions from IDLE state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		READY(1)
		←	ATQA	
WUPA	WUPA	→		READY(1)
		←	ATQA	
HLTA	HLTA	→		IDLE
		←	Mute	
AC (empty)	('93 20')	→		IDLE
		←	Mute	
AC	('93' NVB $UIDTX_1$[[1..n_1]])[a]	→		IDLE
		←	Mute	
nAC	('93' NVB ~$UIDTX_1$[[1.. n_1]])[a]	→		IDLE
		←	Mute	

[a] Let $1 \le n_1 \le 32$.

[b] The value is sent in a standard frame and not in a short frame.

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Table G.7 *(continued)*

Transition	PICC-test-apparatus		PICC	TTS
SELECT	SELECT(1)	→		IDLE
		←	Mute	
nSELECT	('93 70' ~UIDTX$_1$[[1..32]] BCC CRC_A)	→		IDLE
		←	Mute	
RATS	RATS(0,0)	→		IDLE
		←	Mute	
PPS	PPS(0,0,0)	→		IDLE
		←	Mute	
ISO/IEC 14443-4 command	I(0)$_0$(TEST_COMMAND1(1))	→		IDLE
		←	Mute	
DESELECT	S(DESELECT)	→		IDLE
		←	Mute	
Error condition	('26')[b]	→		IDLE
		←	Mute	
Short frames containing all RFU values	Short frames containing all RFU values	→		IDLE
		←	Mute	

[a] Let $1 \leq n_1 \leq 32$.

[b] The value is sent in a standard frame and not in a short frame.

G.3.3.3.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.3.3.4 Scenario G.3: Behaviour of the PICC Type A in the READY(1) state

G.3.3.4.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY state on cascade level 1 according to ISO/IEC 14443-3:2018, 6.3.3.

G.3.3.4.2 Procedure

Perform the following steps for all PICCs and every row of Table G.8:

a) Put the PICC into READY(1) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

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Table G.8 — Transitions from READY(1) state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		IDLE
		←	Mute	
WUPA	WUPA	→		IDLE
		←	Mute	
HLTA	HLTA	→		IDLE
		←	Mute	
AC (wrong parity bit)[g]	('93 20', wrong parity bit)	→		IDLE
		←	Mute	
SELECT[f] (wrong parity bit)[g]	SELECT(1) with wrong parity bit	→		IDLE
		←	Mute	
AC (empty)	('93 20')	→		READY(1)
		←	$UIDTX_1[[1..32]]$ BCC	
AC[f] (split after (0)b)	('93' NVB $UIDTX_1[[1..n_1]]$)[a]	→		READY(1)
		←	if $n_1 = 32$ then (BCC) else ($UIDTX_1[[n_1+1..32]]$ BCC)[a]	
AC[f] (split after (1)b)	('93' NVB $UIDTX_1[[1..n_2]]$)[b]	→		READY(1)
		←	if $n_2 = 32$ then (BCC) else ($UIDTX_1[[n_2+1..32]]$ BCC)[b]	
nAC[f] (wrong UID)	('93' NVB ~$UIDTX_1[[1..n_3]]$)[e]	→		IDLE
		←	Mute	
SELECT[f]	SELECT(1)	→		ACTIVE or READY[d]
		←	SAK[c]	
nSELECT[f] (wrong UID)	('93 70' ~$UIDTX_1$ BCC CRC_A)	→		IDLE
		←	Mute	
Error condition	('93 70' $UIDTX_1$ BCC ~CRC)	→		IDLE
		←	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		IDLE
		←	Mute	
DESELECT	S(DESELECT)	→		IDLE
		←	Mute	
RATS	RATS(0,0)	→		IDLE
		←	Mute	
PPS	PPS(0,0,0)	→		IDLE
		←	Mute	

[a] Let $1 \le n_1 \le 32$, $UIDTX_1[[n_1]] = 0$. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, $UIDTX_1[[n_2]] = 1$. If such a number does not exist, the test may be skipped.

[c] Cascade bit of SAK shall be (0)b for single size UID PICCs and (1)b for double and triple size UID PICCs and shall be coherent with both the value of uid0 ('88' for the cascade tag or not) and the UID size declared by b8b7 of ATQA.

[d] Single size UID PICC shall be in ACTIVE state; double and triple size UID PICCs shall be in READY state.

[e] Let $1 \le n_3 \le 32$.

[f] If the PICC UID is unknown, it may be retrieved by putting the PICC in ACTIVE state, and then applying ACTIVE → IDLE, IDLE → READY(1) and READY(1) → READY(2) state transitions.

[g] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

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G.3.3.4.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.3.3.5 Scenario G.4: Behaviour of the PICC Type A in the READY(2) state

G.3.3.5.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY state on cascade level 2 according to ISO/IEC 14443-3:2018, 6.3.3. This test is only for PICCs with double or triple size UID.

G.3.3.5.2 Procedure

Perform the following steps for all PICCs with double and triple size UID and every row of Table G.9:

a) Put the PICC into READY(2) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.9 — Transitions from READY(2) state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		IDLE
		←	Mute	
WUPA	WUPA	→		IDLE
		←	Mute	
HLTA	HLTA	→		IDLE
		←	Mute	
AC (wrong parity bit)[g]	('95 20', wrong parity bit)	→		IDLE
		←	Mute	
SELECT[f] (wrong parity bit)[g]	SELECT(2) with wrong parity bit	→		IDLE
		←	Mute	
AC (empty)	('95 20')	→		READY(2)
		←	$UIDTX_2$[[1..32]] BCC	

[a] Let $1 \le n_1 \le 32$, $UIDTX_2[[n_1]] = 0$. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, $UIDTX_2[[n_2]] = 1$. If such a number does not exist, the test may be skipped.

[c] Cascade bit of SAK shall be (0)b for double size UID PICCs and (1)b for triple size UID PICCs and shall be coherent with both the value of uid0 ("88" for the cascade tag or not) and the UID size declared by b8b7 of ATQA.

[d] Double size UID PICCs shall be in ACTIVE state; triple size UID PICCs shall be in READY state.

[e] Let $1 \le n_3 \le 32$.

[f] If the PICC UID is unknown, it may be retrieved by putting the PICC in ACTIVE state, and then applying ACTIVE → IDLE, IDLE → READY(1) and READY(1) → READY(2) state transitions.

[g] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

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Table G.9 *(continued)*

Transition	PICC-test-apparatus		PICC	TTS
AC[f] (split after (0)b)	('95' NVB UIDTX$_2$[[1..n$_1$]])[a]	→		READY(2)
		←	if n$_1$ = 32 then (BCC) else (UIDTX$_2$[[n$_1$+1..32]] BCC) [a]	
AC[f] (split after (1)b)	('95' NVB UIDTX$_2$[[1..n$_2$]])[b]	→		READY(2)
		←	if n$_2$ = 32 then (BCC) else (UIDTX$_2$[[n$_2$+1..32]] BCC) [b]	
nAC[f] (wrong UID)	('95' NVB ~UIDTX$_2$[[1..n$_3$]])[e]	→		IDLE
		←	Mute	
SELECT[f]	SELECT(2)	→		ACTIVE or READY[d]
		←	SAK[c]	
nSELECT[f] (wrong UID)	('95 70' ~UIDTX$_2$ BCC CRC_A)	→		IDLE
		←	Mute	
Error condition	('95 70' UIDTX$_2$ BCC ~CRC)	→		IDLE
		←	Mute	
ISO/IEC 14443-4 command	I(0)$_0$(TEST_COMMAND1(1))	→		IDLE
		←	Mute	
DESELECT	S(DESELECT)	→		IDLE
		←	Mute	
RATS	RATS(0,0)	→		IDLE
		←	Mute	
PPS	PPS(0,0,0)	→		IDLE
		←	Mute	

[a] Let $1 \le n_1 \le 32$, UIDTX$_2$[[n$_1$]] = 0. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, UIDTX$_2$[[n$_2$]] = 1. If such a number does not exist, the test may be skipped.

[c] Cascade bit of SAK shall be (0)b for double size UID PICCs and (1)b for triple size UID PICCs and shall be coherent with both the value of uid0 ("88" for the cascade tag or not) and the UID size declared by b8b7 of ATQA.

[d] Double size UID PICCs shall be in ACTIVE state; triple size UID PICCs shall be in READY state.

[e] Let $1 \le n_3 \le 32$.

[f] If the PICC UID is unknown, it may be retrieved by putting the PICC in ACTIVE state, and then applying ACTIVE → IDLE, IDLE → READY(1) and READY(1) → READY(2) state transitions.

[g] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

G.3.3.5.3 Test report

The test is:

a) N/A when the PICC has a single size UID;

b) PASS when the PICC has a double or a triple size UID and only when it responds as indicated in the procedure; and

c) FAIL in any other case.

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G.3.3.6 Scenario G.5: Behaviour of the PICC Type A in the READY(3) state

G.3.3.6.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY state according to ISO/IEC 14443-3:2018, 6.3.3. This test is only for PICCs with triple size UID.

G.3.3.6.2 Procedure

Perform the following steps for all PICCs with triple size UID and every row of Table G.10:

a) Put the PICC into READY(3) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.10 — Transitions from READY(3) state

Transitions	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		IDLE
		←	Mute	
WUPA	WUPA	→		IDLE
		←	Mute	
HLTA	HLTA	→		IDLE
		←	Mute	
AC (wrong parity bit)[e]	('97 20', wrong parity bit)	→		IDLE
		←	Mute	
SELECT[d] (wrong parity bit)[e]	SELECT(3) with wrong parity bit	→		IDLE
		←	Mute	
AC (empty)	('97 20')	→		READY(3)
		←	$UIDTX_3[[1..32]]$ BCC	
AC[d] (split after (0)b)	('97' NVB $UIDTX_3[[1..n_1]]$)[a]	→		READY(3)
		←	if $n_1 = 32$ then (BCC) else ($UIDTX_3[[n_1+1..32]]$ BCC)[a]	
AC[d] (split after (1)b)	('97' NVB $UIDTX_3[[1..n_2]]$)[b]	→		READY(3)
		←	if $n_2 = 32$ then (BCC) else ($UIDTX_3[[n_2+1..32]]$ BCC)[b]	
nAC[d] (wrong UID)	('97' NVB ~$UIDTX_3[[1..n_3]]$)[c]	→		IDLE
		←	Mute	
SELECT[d]	SELECT(3)	→		ACTIVE
		←	SAK (complete)	

[a] Let $1 \le n_1 \le 32$, UIDTX3[[n_1]] = 0. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, UIDTX3[[n_2]] = 1. If such a number does not exist, the test may be skipped.

[c] Let $1 \le n_3 \le 32$.

[d] If the PICC UID is unknown, it may be retrieved by putting the PICC in ACTIVE state, and then applying ACTIVE → IDLE, IDLE → READY(1), READY(1) → READY(2) and READY(2) → READY(3) state transitions.

[e] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

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Table G.10 *(continued)*

Transitions	PICC-test-apparatus		PICC	TTS
nSELECT[d] (wrong UID)	('97 70' ~UIDTX$_3$ BCC CRC_A)	→		IDLE
		←	Mute	
Error condition	('97 70' UIDTX$_3$ BCC ~CRC)	→		IDLE
		←	Mute	
ISO/IEC 14443-4 command	I(0)$_0$(TEST_COMMAND1(1))	→		IDLE
		←	Mute	
DESELECT	S(DESELECT)	→		IDLE
		←	Mute	
RATS	RATS(0,0)	→		IDLE
		←	Mute	
PPS	PPS(0,0,0)	→		IDLE
		←	Mute	

[a] Let $1 \le n_1 \le 32$, UIDTX3[[n_1]] = 0. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, UIDTX3[[n_2]] = 1. If such a number does not exist, the test may be skipped.

[c] Let $1 \le n_3 \le 32$.

[d] If the PICC UID is unknown, it may be retrieved by putting the PICC in ACTIVE state, and then applying ACTIVE → IDLE, IDLE → READY(1), READY(1) → READY(2) and READY(2) → READY(3) state transitions.

[e] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

G.3.3.6.3 Test report

The test is:

a) N/A when the PICC has a single or double size UID;

b) PASS when the PICC has a triple size UID and only when it responds as indicated in the procedure; and

c) FAIL in any other case.

G.3.3.7 Scenario G.6: Behaviour of the PICC Type A in the ACTIVE state

G.3.3.7.1 Scope

This test is to determine the behaviour of the PICC Type A in the ACTIVE state according to ISO/IEC 14443-3:2018, 6.3.4.

G.3.3.7.2 Procedure

Perform the following steps for every row of Table G.11:

a) Put the PICC into ACTIVE state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

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Table G.11 — Transitions from ACTIVE state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		IDLE
		←	Mute	
WUPA	WUPA	→		IDLE
		←	Mute	
AC	('93' NVB $UIDTX_1[[1..n_1]]$)[a]	→		IDLE
		←	Mute[b]	
nAC	('93' NVB ~$UIDTX_1[[1..n_1]]$)[a]	→		IDLE
		←	Mute[b]	
HLTA	HLTA	→		HALT
		←	Mute	
SELECT	SELECT(1)	→		IDLE
		←	Mute[b]	
nSELECT	('93 70' ~$UIDTX_1$ BCC CRC_A)	→		IDLE
		←	Mute[b]	
RATS	RATS(0,0)	→		PROTOCOL
		←	ATS	
Error condition	('E0 00' ~CRC)	→		IDLE
		←	Mute[b]	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		IDLE
		←	Mute[b]	
DESELECT	S(DESELECT)	→		IDLE
		←	Mute[b]	
PPS	PPS(0,0,0)	→		IDLE
		←	Mute[b]	
RATS (wrong parity bit)[c]	RATS(0,0) with wrong parity bit	→		IDLE
		←	Mute[b]	
Type B command	REQB	→	Mute	IDLE or ACTIVE[d]
		←		
AC (empty)	('93 20')	→		IDLE
		←	Mute	
RATS with all FSDI RFU values	RATS(0,all FSDI RFU values)	→		PROTOCOL
		←	ATS	
RATS with CID RFU value	RATS(15,0)	→		IDLE
		←	Mute[b]	

[a] Let $1 \le n_1 \le 32$.

[b] Mute or proprietary response.

[c] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

[d] Check first IDLE state as TTS. If TTS is not IDLE state, rerun the test a second time to check ACTIVE state.

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G.3.3.7.3 Test report

The test is

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

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G.3.3.8 Scenario G.7: Behaviour of the PICC Type A in the HALT state

G.3.3.8.1 Scope

This test is to determine the behaviour of the PICC Type A in the HALT state according to ISO/IEC 14443-3:2018, 6.3.5.

G.3.3.8.2 Procedure

Perform the following steps for every row of Table G.12:

a) Put the PICC into HALT state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.12 — Transitions from HALT state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		HALT
		←	Mute	
WUPA	WUPA	→		READY*(1)
		←	ATQA	
HLTA	HLTA	→		HALT
		←	Mute	
AC (empty)	(‘93 20’)	→		HALT
		←	Mute	
AC	(‘93’ NVB $UIDTX_1[[1..n_1]]$)[a]	→		HALT
		←	Mute	
nAC	(‘93’ NVB ~$UIDTX_1[[1..n_1]]$)[a]	→		HALT
		←	Mute	
SELECT	SELECT(1)	→		HALT
		←	Mute	
nSELECT	(‘93 70’ ~$UIDTX_1$ BCC CRC_A)	→		HALT
		←	Mute	
RATS	RATS(0,0)	→		HALT
		←	Mute	
Error condition	(‘52’) in the standard frame	→		HALT
		←	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		HALT
		←	Mute	
DESELECT	S(DESELECT)	→		HALT
		←	Mute	
PPS	PPS(0,0,0)	→		HALT
		←	Mute	

[a] Let $1 \leq n_1 \leq 32$.

G.3.3.8.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

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b) FAIL in any other case.

G.3.3.9 Scenario G.8: Behaviour of the PICC Type A in the READY*(1) state

G.3.3.9.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY* state of cascade level 1 according to ISO/IEC 14443-3:2018, 6.3.6.

G.3.3.9.2 Procedure

Perform the following steps for every row of Table G.13:

a) Put the PICC into READY*(1) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check that the PICC is in the TTS.

Table G.13 — Transitions from READY*(1) state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		HALT
		←	Mute	
WUPA	WUPA	→		HALT
		←	Mute	
HLTA	HLTA	→		HALT
		←	Mute	
AC (wrong parity bit)[f]	('93 20', wrong parity bit)	→		HALT
		←	Mute	
SELECT (wrong parity bit)[f]	SELECT(1) with wrong parity bit	→		HALT
		←	Mute	
AC (empty)	('93 20')	→		READY*(1)
		←	$UIDTX_1[[1..32]]$ BCC	
AC (split after (0)b)	('93' NVB $UIDTX_1[[1..n_1]]$)[a]	→		READY*(1)
		←	if $n_1 = 32$ then (BCC) else ($UIDTX_1[[n_1+1..32]]$ BCC)[a]	
AC (split after (1)b)	('93' NVB $UIDTX_1[[1..n_2]]$)[b]	→		READY*(1)
		←	if $n_2 = 32$ then (BCC) else ($UIDTX_1[[n_2+1..32]]$ BCC)[b]	
nAC (wrong UID)	('93' NVB ~$UIDTX_1[[1..n_3]]$)[e]	→		HALT
		←	Mute	

[a] Let $1 \le n_1 \le 32$, $UIDTX_1[[n_1]] = 0$. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, $UIDTX_1[[n_2]] = 1$. If such a number does not exist, the test may be skipped.

[c] Cascade bit of SAK shall be (0)b for single size UID PICCs and (1)b for double and triple size UID PICCs and shall be coherent with both the value of uid0 ('88' for the cascade tag or not) and the UID size declared by b8b7 of ATQA.

[d] Single size UID PICCs shall be in ACTIVE* state; double and triple size UID PICCs should be in READY* state.

[e] Let $1 \le n_3 \le 32$.

[f] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

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Table G.13 *(continued)*

Transition	PICC-test-apparatus		PICC	TTS
SELECT	SELECT(1)	→		ACTIVE *or READY*[d]
		←	SAK[c]	
nSELECT (wrong UID)	(‘93 70’ ~UIDTX$_1$ BCC CRC_A)	→		HALT
		←	Mute	
Error condition	(‘93 70’ UIDTX$_1$ BCC ~CRC)	→		HALT
		←	Mute	
ISO/IEC 14443-4 command	I(0)$_0$(TEST_COMMAND1(1))	→		HALT
		←	Mute	
DESELECT	S(DESELECT)	→		HALT
		←	Mute	
RATS	RATS(0,0)	→		HALT
		←	Mute	
PPS	PPS(0,0,0)	→		HALT
		←	Mute	

[a] Let $1 \le n_1 \le 32$, UIDTX$_1$[[n_1]] = 0. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, UIDTX$_1$[[n_2]] = 1. If such a number does not exist, the test may be skipped.

[c] Cascade bit of SAK shall be (0)b for single size UID PICCs and (1)b for double and triple size UID PICCs and shall be coherent with both the value of uid0 ('88' for the cascade tag or not) and the UID size declared by b8b7 of ATQA.

[d] Single size UID PICCs shall be in ACTIVE* state; double and triple size UID PICCs should be in READY* state.

[e] Let $1 \le n_3 \le 32$.

[f] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

G.3.3.9.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.3.3.10 Scenario G.9: Behaviour of the PICC Type A in the READY*(2) state

G.3.3.10.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY* state of cascade level 2 according to ISO/IEC 14443-3:2018, 6.3.6. This test only applies to PICCs with double or triple size UID.

G.3.3.10.2 Procedure

Perform the following steps for every row of Table G.14:

a) Put the PICC into READY*(2) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

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Table G.14 — Transitions from READY*(2) state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		HALT
		←	Mute	
WUPA	WUPA	→		HALT
		←	Mute	
HLTA	HLTA	→		HALT
		←	Mute	
AC (wrong parity bit)[f]	('95 20', wrong parity bit)	→		HALT
		←	Mute	
SELECT (wrong parity bit)[f]	SELECT(2) with wrong parity bit	→		HALT
		←	Mute	
AC (empty)	('95 20')	→		READY*(2)
		←	$UIDTX_2$[[1..32]] BCC	
AC (split after (0)b)	('95' NVB $UIDTX_2$[[1..n_1]])[a]	→		READY*(2)
		←	if n_1 = 32 then (BCC) else ($UIDTX_2$[[n_1+1..32]] BCC)[a]	
AC (split after (1)b)	('95' NVB $UIDTX_2$[[1..n_2]])[b]	→		READY*(2)
		←	if n_2 = 32 then (BCC) else ($UIDTX_2$[[n_2+1..32]] BCC)[b]	
nAC (wrong UID)	('95' NVB ~$UIDTX_2$[[1..n_3]]) [e]	→		HALT
		←	Mute	
SELECT	SELECT(2)	→		ACTIVE or READY[d]
		←	SAK[c]	
nSELECT (wrong UID)	('95 70' ~$UIDTX_2$ BCC CRC_A)	→		HALT
		←	Mute	
Error condition	('95 70' $UIDTX_2$ BCC ~CRC)	→		HALT
		←	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		HALT
		←	Mute	
DESELECT	S(DESELECT)	→		HALT
		←	Mute	
RATS	RATS(0,0)	→		HALT
		←	Mute	
PPS	PPS(0,0,0)	→		HALT
		←	Mute	

[a] Let $1 \le n_1 \le 32$, $UIDTX_2$[[n_1]] = 0. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, $UIDTX_2$[[n_2]] = 1. If such a number does not exist, the test may be skipped.

[c] Cascade bit of SAK shall be (0)b for double size UID PICCs and (1)b for triple size UID PICCs and shall be coherent with both the value of uid0 ('88' for the cascade tag or not) and the UID size declared by b8b7 of ATQA.

[d] Double size UID PICCs shall be in ACTIVE state; triple size UID PICCs shall be in READY state.

[e] Let $1 \le n_3 \le 32$.

[f] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

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G.3.3.10.3 Test report

The test is:

a) N/A when the PICC has a single size UID;

b) PASS when the PICC has a double or triple size UID and only when it responds as indicated in the procedure; and

c) FAIL in any other case.

G.3.3.11 Scenario G.10: Behaviour of the PICC Type A in the READY*(3) state

G.3.3.11.1 Scope

This test is to determine the behaviour of the PICC Type A in the READY* state of cascade level 3 according to ISO/IEC 14443-3:2018, 6.3.6. This test is only for PICCs with triple size UID.

G.3.3.11.2 Procedure

Perform the following steps for every row of Table G.15:

a) Put the PICC into READY*(3) state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.15 — Transitions from READY*(3) state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		HALT
		←	Mute	
WUPA	WUPA	→		HALT
		←	Mute	
HLTA	HLTA	→		HALT
		←	Mute	
AC (wrong parity bit)[d]	(‘97 20’, wrong parity bit)	→		HALT
		←	Mute	
SELECT (wrong parity bit)[d]	SELECT(3) with wrong parity bit	→		HALT
		←	Mute	
AC (empty)	(‘97 20’)	→		READY*(3)
		←	$UIDTX_3[[1..32]]$ BCC	
AC (split after (0)b)	(‘97’ NVB $UIDTX_3[[1..n_1]]$)[a]	→		READY*(3)
		←	if $n_1 = 32$ then (BCC) else ($UIDTX_3[[n_1+1..32]]$ BCC)[a]	

[a] Let $1 \le n_1 \le 32$, UIDTX3[[n_1]] = 0. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, UIDTX3[[n_2]] = 1. If such a number does not exist, the test may be skipped.

[c] Let $1 \le n_3 \le 32$.

[d] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

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Table G.15 *(continued)*

Transition	PICC-test-apparatus		PICC	TTS

AC
(split after (1)b)
	('97' NVB $UIDTX_3[[1..n_2]]$)[b]	→
		←
			if n_2 = 32 then
			(BCC)
			else
			($UIDTX_3[[n_2+1..32]]$ BCC)[b]
				READY*(3)

nAC (wrong UID)	('97' NVB ~$UIDTX_3[[1..n_3]]$)[c]	→ ←	Mute	HALT
SELECT	SELECT(3)	→ ←	SAK (complete)	ACTIVE*
nSELECT (wrong UID)	('97 70' ~$UIDTX_3$ BCC CRC_A)	→ ←	Mute	HALT
Error condition	('97 70' $UIDTX_3$ BCC ~CRC)	→ ←	Mute	HALT
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→ ←	Mute	HALT
DESELECT	S(DESELECT)	→ ←	Mute	HALT
RATS	RATS(0,0)	→ ←	Mute	HALT
PPS	PPS(0,0,0)	→ ←	Mute	HALT

[a] Let $1 \le n_1 \le 32$, UIDTX3[[n_1]] = 0. If such a number does not exist, the test may be skipped.

[b] Let $1 \le n_2 \le 32$, UIDTX3[[n_2]] = 1. If such a number does not exist, the test may be skipped.

[c] Let $1 \le n_3 \le 32$.

[d] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

G.3.3.11.3 Test report

The test is:

a) N/A when the PICC has a single or double size UID;

b) PASS when the PICC has a triple size UID and only when it responds as indicated in the procedure; and

c) FAIL in any other case.

G.3.3.12 Scenario G.11: Behaviour of the PICC Type A in the ACTIVE* state

G.3.3.12.1 Scope

This test is to determine the behaviour of the PICC Type A in the ACTIVE* state according to ISO/IEC 14443-3:2018, 6.3.7.

G.3.3.12.2 Procedure

Perform the following steps for every row of Table G.16:

a) Put the PICC into ACTIVE* state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

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d) Check if the PICC is in the TTS.

Table G.16 — Transitions from ACTIVE* state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		HALT
		←	Mute	
WUPA	WUPA	→		HALT
		←	Mute	
HLTA	HLTA	→		HALT
		←	Mute	
AC	('93' NVB $UIDTX_1[[1..n_1]]$)[a]	→		HALT
		←	Mute[b]	
nAC	('93' NVB ~$UIDTX_1[[1..n_1]]$)[a]	→		HALT
		←	Mute[b]	
SELECT	SELECT(1)	→		HALT
		←	Mute[b]	
nSELECT	('93 70' ~$UIDTX_1$ BCC CRC_A)	→		HALT
		←	Mute[b]	
RATS	RATS(0,0)	→		PROTOCOL
		←	ATS	
Error condition	('E0 00' ~CRC)	→		HALT
		←	Mute[b]	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		HALT
		←	Mute[b]	
DESELECT	S(DESELECT)	→		HALT
		←	Mute[b]	
PPS	PPS(0,0,0)	→		HALT
		←	Mute[b]	
RATS (wrong parity bit)[c]	RATS(0,0) with wrong parity bit	→		HALT
		←	Mute[b]	
Type B command	REQB	→		HALT or ACTIVE*[d]
		←	Mute	
AC (empty)	('93 20')	→		HALT
		←	Mute	

[a] Let $1 \leq n_1 \leq 32$.

[b] Mute or proprietary response.

[c] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

[d] Check first HALT state as TTS. If TTS is not HALT state, rerun the test a second time to check ACTIVE* state.

G.3.3.12.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

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G.3.3.13 Scenario G.12: Behaviour of the PICC Type A in the PROTOCOL state

G.3.3.13.1 Scope

This test is to determine the behaviour of the PICC Type A in the PROTOCOL state according to ISO/IEC 14443-3:2018, 6.3.8. This test shall ensure that the activated PICC does not respond to any anticollision or initialization command.

G.3.3.13.2 Procedure

Perform the following steps for every row of Table G.17:

a) Put the PICC into PROTOCOL state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.17 — Transitions from PROTOCOL state

Transition	PICC-test-apparatus		PICC	TTS
REQA	REQA	→		PROTOCOL
		←	Mute	
WUPA	WUPA	→		PROTOCOL
		←	Mute	
AC	(‘93’ NVB $UIDTX_1$[[1..n_1]])[a]	→		PROTOCOL
		←	Mute	
nAC	(‘93’ NVB ~$UIDTX_1$[[1..n_1]])[a]	→		PROTOCOL
		←	Mute	
HLTA	HLTA	→		PROTOCOL
		←	Mute	
SELECT	SELECT(1)	→		PROTOCOL
		←	Mute	
nSELECT	(‘93 70’ ~$UIDTX_1$ BCC CRC_A)	→		PROTOCOL
		←	Mute	
RATS	RATS(0,0)	→		PROTOCOL
		←	Mute	
Error condition	S(DESELECT, ~CRC)	→		PROTOCOL
		←	Mute	
DESELECT	S(DESELECT)	→		HALT
		←	S(DESELECT)	
PPS	PPS(0,0,0)	→		PROTOCOL
		←	Mute, or PPS response[b]	

[a] Let $1 \leq n_1 \leq 32$.

[b] PPS response is returned if the PICC supports PPS.

[c] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

[d] Check first IDLE state as TTS. If TTS is not IDLE state, rerun the test a second time to check PROTOCOL state.

[e] PPS response is returned only if the PICC supports PPS and applies the RFU error handling as defined in ISO/IEC 14443-3:2018, 5.3.

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Table G.17 *(continued)*

Transition	PICC-test-apparatus		PICC	TTS
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		PROTOCOL
		←	$I(0)_0$ (TEST_RESPONSE1(1))	
DESELECT (wrong parity bit)[c]	S(DESELECT) with wrong parity bit	→		PROTOCOL
		←	Mute	
ISO/IEC 14443-4 command (wrong parity bit)[c]	$I(0)_0$(TEST_COMMAND1(1)) with wrong parity bit	→		PROTOCOL
		←	Mute	
Type B command	REQB	→		IDLE or PROTOCOL[d]
		←	Mute	
AC (empty)	('93 20')	→		PROTOCOL
		←	Mute	
PPS with all PPS0 RFU values	PPS(0,0,0) with all PPS0 RFU value	→		PROTOCOL
		←	Mute, or PPS response[e]	
ISO/IEC 14443-4 command (RFU block type)	$I(0)_0$(TEST_COMMAND1(1)) with block type set to (01)b	→		PROTOCOL
		←	Mute	

[a] Let $1 \leq n_1 \leq 32$.

[b] PPS response is returned if the PICC supports PPS.

[c] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

[d] Check first IDLE state as TTS. If TTS is not IDLE state, rerun the test a second time to check PROTOCOL state.

[e] PPS response is returned only if the PICC supports PPS and applies the RFU error handling as defined in ISO/IEC 14443-3:2018, 5.3.

G.3.3.13.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.3.4 Scenario G.13: Handling of Type A anticollision

G.3.4.1 Scope

This test is to perform a full bitwise anticollision loop according to ISO/IEC 14443-3:2018, 6.5.3.

G.3.4.2 Procedure

a) Put the PICC into the field.

b) Put the PICC into READY(1) state.

c) Execute AnticollisionA.

d) Put the PICC into READY*(1) state.

e) Execute AnticollisionA.

Pseudo code: Type A anticollision procedure:

```
1    Procedure AnticollisionA
2    // TPDUSend and TPDURecv are PCD specific functions
```

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```
3     // to send and receive frames
4     for c = 1 to CascadeLevels do
5       TPDUSend (SELECT(c) 20)
6       if TPDURecv() ≠ (UIDTXc[[1..32]] BCC) then return FAIL
7       // anticollision over UID bits
8       for p = 1 to 32 do
9         // enter desired cascade level
10        if c ≥ 2 then TPDUSend(SELECT(1))
11        if c = 3 then TPDUSend(SELECT(2))
12        // anticollision with matched bit
13        NVB[[1..4]] = (p + 16) mod 8
14        NVB[[5..8]] = (p + 16) div 8
15        TPDUSend (SELECT(c) NVB UIDTXc[[1..p]])
16        if TPDURecv() ≠ (UIDTXc[[p+1..32]] BCC) then return FAIL
17        // anticollision with unmatched bit
18        TPDUSend(SELECT(c) NVB UIDTXc[[1..p-1]] ~UIDTXc[[p]])
19        if TPDURecv() ≠ Mute then return FAIL
20        // re-enter READY(1) (resp. READY*(1)) state
21        TPDUSend (WUPA)
22      end for
23    end for
24    return PASS
```

G.3.4.3 Test report

The test is:

a) PASS only when every Anticollision Test procedure returns PASS, and

b) FAIL when any Anticollision Test returns the value FAIL.

G.3.5 Handling of RATS

Handling of RATS is tested in G.3.3.7 and G.3.3.12.

Scenario G.14: RATS after wrong RATS

This scenario, which was defined in former editions of this document, is no longer present.

Scenario G.15: RATS after RATS

This scenario, which was defined in former editions of this document, is no longer present.

G.3.6 Handling of PPS request

G.3.6.1 Scope

This test is to determine the handling of the PPS request by the PICC Type A according to ISO/IEC 14443-4:2018, 5.7.2.2.

G.3.6.2 Procedure

For each of the scenarios described in Table G.18, Table G.19 and Table G.20, perform the following steps:

a) Put the PICC into PROTOCOL state.

b) Send the command as described under the PICC-test-apparatus column in each scenario.

c) Check that the response of the PICC conforms to the one given in the PICC column.

d) Check if the PICC is in PROTOCOL state.

Scenario G.16: PPS without parameter change

This scenario, which was defined in former editions of this document, is no longer present.

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Table G.18 — Scenario G.17: PPS without PPS1

PICC-test-apparatus		PICC
('D0 01' CRC_A)	→	
	←	Mute or ('D0' CRC_A)[a]

[a] Both responses are valid.

Table G.19 — Scenario G.18: PPS after PPS

PICC-test-apparatus		PICC
PPS(0,0,0)	→	
	←	Mute or ('D0' CRC_A)[a]
PPS(0,0,0)	→	
	←	Mute

[a] Response depends on whether the PICC supports PPS or not. If the PICC does not support any changeable parameters it may not support the PPS request because the PCD shall not send PPS to such a PICC (see ISO/IEC 14443-4:2018, 5.1, 6th dash).

Table G.20 — Scenario G.19: PPS after unreceived PPS

PICC-test-apparatus		PICC
('D0 11 00' ~CRC)	→	
	←	Mute
PPS(0,0,0)	→	
	←	Mute

G.3.6.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.3.7 Scenario G.20: Handling of FSD

G.3.7.1 Scope

This test is to determine if the PICC Type A respects the FSD value as negotiated by the RATS according to ISO/IEC 14443-4:2018, 5.2.

G.3.7.2 Procedure

Perform the following steps for each FSDI defined in ISO/IEC 14443-4 including all RFU values:

a) Put the PICC into ACTIVE state.

b) Send the RATS(0, fsdi) command with parameter fsdi as in the particular test.

c) Check that the PICC answer is a valid ATS and that its size does not exceed FSD.

d) Carry out additional sequences if required by the PICC to be ready to accept TEST_COMMAND2(2).

e) Send the I-block $I(0)_0$(TEST_COMMAND2(2)).

f) Check that the size of the I-block sent by the PICC is ≤ FSD.

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G.3.7.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure, and

b) FAIL in any other case.

G.3.8 Handling of frame delay time PICC to PCD and SFGT

G.3.8.1 Scope

This test is to determine if the PICC Type A respects the minimum frame delay time PICC to PCD defined in ISO/IEC14443-3:2018, 6.2.1.2 and SFGT defined in ISO/IEC 14443-4:2018, 5.3.5.

G.3.8.2 Procedure

The procedure shall be repeated at a bit rate of $f_c/128$ in both directions and at the maximum bit rates supported by the PICC in each direction.

Perform the following steps for Scenario G.71:

a) Put the PICC into IDLE state.

b) For each step in the scenario do:

   1) Send the command as described in the PICC-test-apparatus column of Table G.21 respecting the timing condition described in the frame delay time PICC to PCD column.

   2) Check that the PICC response matches the one of the PICC column of Table G.21.

c) End for.

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Table G.21 — Scenario G.71: Handling of frame delay time PICC to PCD and SFGT

Step	Frame delay time PICC to PCD	PICC-test-apparatus		PICC
1	—	REQA	→	
			←	ATQA
2	Minimum frame delay time PICC to PCD + $50/f_c$[a]	AC(1)	→	
			←	$UIDTX_1$ BCC
3	$(1172 + 50)/f_c$[a]	SELECT(1)	→	
			←	SAK (cascade) or SAK (complete)
4[b]	$(1172 + 50)/f_c$[a]	AC(2)	→	
			←	$UIDTX_2$ BCC
5[b]	$(1172 + 50)/f_c$[a]	SELECT(2)	→	
			←	SAK (cascade) or SAK (complete)
6[c]	$(1172 + 50)/f_c$[a]	AC(3)	→	
			←	$UIDTX_3$ BCC
7[c]	$(1172 + 50)/f_c$[a]	SELECT(3)	→	
			←	SAK (complete)
8	$(1172 + 50)/f_c$[a]	RATS(0,0)	→	
			←	ATS
9	$(1172 + 50)/f_c$ if SFGI=0 or SFGT + $50/f_c$[a]	PPS(0,dri,dsi)[d]	→	
			←	PPS response
10	$(1172 + 50)/f_c$ if SFGI=0 or SFGT + $50/f_c$[a,e]	$I(0)_0$(TEST_COMMAND1(1))	→	
			←	$I(0)_0$(TEST_RESPONSE1(1))[f]
11	$(1172 + 50)/f_c$[a]	$I(0)_1$(TEST_COMMAND3)	→	
			←	S(WTX)(WTXM)
12	$(1172 + 50)/f_c$[a]	S(WTX)(WTXM)	→	
			←	$I(0)_1$(TEST_RESPONSE3)[g]

[a] The applied frame delay time PICC to PCD shall have a maximum tolerance of $\pm 25/f_c$.

[b] This step is sent only for a PICC with UID size 2 or 3.

[c] This step is sent only for a PICC with UID size 3.

[d] PPS request is sent for bit rate > $f_c/128$. Configure PPS request with appropriate dsi and dri corresponding to the maximum bit rates supported by the PICC in each direction. Skip this step if the PICC does not support any changeable parameters in the ATS.

[e] If the previous step has been skipped since the PICC does not support any changeable parameters in the ATS, SFGI applies to this step.

[f] S(WTX) request(s) may be sent by the PICC. The PICC-test-apparatus shall acknowledge each S(WTX) request with an S(WTX) response until receiving the PICC response. There is no specific requirement on frame delay time PICC to PCD for the S(WTX) response(s).

[g] Additional S(WTX) request(s) may be sent by the PICC. The PICC-test-apparatus shall acknowledge each S(WTX) request with an S(WTX) response until receiving the PICC response. There is no specific requirement on frame delay time PICC to PCD for the S(WTX) response(s).

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G.3.8.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure, and

b) FAIL in any other case.

Report the measured timings in Table G.78.

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G.3.9 Scenario G.72: PICC bit rates capability

G.3.9.1 Scope

This test verifies the handling of the PICC Type A bit rate negotiation and the handling of the RFU bits in PPS0 and PPS1 as defined in ISO/IEC 14443-4.

G.3.9.2 Procedure

G.3.9.2.1 Sequencing

The scenario in G.3.9.2.2 shall be carried out in the following sequences:

a) The scenario skipping steps e) to h) shall be repeated for all combinations of PCD to PICC and PICC to PCD supported bit rates negociated by PPS. All of the RFU bits of PPS0 shall be set to (1)b at least once.

b) The scenario skipping step c) shall be repeated for all combinations of PCD to PICC and PICC to PCD supported bit rates negotiated by S(PARAMETERS) blocks if supported by the PICC. All of the RFU bits during bit rate negotiation in steps e) to h) shall be set to (1)b at least once.

G.3.9.2.2 Scenario

Perform the following steps:

a) Put the PICC into IDLE state.

b) Put the PICC in PROTOCOL state.

c) Send the appropriate PPS request and check the PPS response.

With any of the RFU bits in PPS0 set to (1)b, PPS response is returned only if the PICC applies the RFU error handling as defined in ISO/IEC 14443-3:2018, 5.3. Otherwise, the PICC will not change its bit rate.

d) Check that the PICC responses are valid. Record the presence, content and timing of the PICC responses.

e) Send an S(PARAMETERS) block indicating Bit rates request.

f) Check PICC answer. If the PICC supports S(PARAMETERS) blocks, the PICC responds with an S(PARAMETERS) block containing values for all supported parameters. If the PICC does not support S(PARAMETERS) it stays mute; skip steps g) and h).

g) Send an S(PARAMETERS) block to activate selected communication parameters (bit rates).

h) Check that the PICC response is a valid S(PARAMETERS) block to acknowledge the activated parameters.

i) Send the I-block $I(0)_0$(TEST_COMMAND1(1)). Record the presence, frame format, content and timing of the PICC response.

j) Send the S(DESELECT) command.

k) Check that the PICC response is a valid S(DESELECT). Record the presence, frame format, content and timing of the PICC response.

l) Send a WUPA command.

m) Check that the PICC response is a valid ATQA. Record the presence, frame format, content and timing of the PICC response.

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G.3.9.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.4 Test method for initialization of the PICC Type B

G.4.1 General

This subclause is to test if the PICC Type B conforms to ISO/IEC 14443-3. If conformance with ISO/IEC 14443-4 is not required all tests containing ISO/IEC 14443-4 commands need not be applied.

If the PICC does not support the REQB/WUPB with N > 1 nor the Slot-MARKER command (see ISO/IEC 14443-3:2018, 7.6.1) all tests containing these commands need not be applied.

G.4.2 Scenario G.21: Polling

G.4.2.1 Scope

This test is to determine the behaviour of the PICC Type B on receiving of REQB according to ISO/IEC 14443-3:2018, 5.2.

G.4.2.2 Procedure

Perform the following steps for 3 different field strengths of H_{min}, $(H_{min} + H_{max})/2$ and H_{max} as specified for the respective PICC class:

a) Place the PICC into the field and adjust it.

b) Switch the RF operating field off for a minimum time for resetting a PICC in accordance with ISO/IEC 14443-3:2018, 5.2.5.

c) Switch the RF operating field on.

d) Wait 5 ms and send a valid REQB(1) command.

e) Record the presence and the content of the PICC response.

f) Switch the RF operating field off for a minimum time for resetting a PICC in accordance with ISO/IEC 14443-3:2018, 5.2.5.

g) Switch the RF operating field on.

h) Wait 5 ms and send a valid REQA command (with Type A modulation).

i) Wait 5 ms and send a valid REQB(1) command.

j) Record the presence and the content of the PICC response.

G.4.2.3 Test report

The test is:

a) PASS only when the PICC's response is a valid ATQB in both steps e) and j); and

b) FAIL when the PICC's response isn't a valid ATQB in any of steps e) or j).

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G.4.3 Scenario G.22: PICC framing and bit rates capability

G.4.3.1 Scope

This test verifies the handling of the PICC Type B bit rate negotiation as defined in ISO/IEC 14443-3 and ISO/IEC 14443-4.

G.4.3.2 Procedure

G.4.3.2.1 Sequencing

The scenario in G.4.3.2.2 shall be carried out in the following sequences:

a) The scenario skipping steps g) to j) shall be repeated for all combinations of PCD to PICC and PICC to PCD supported bit rates negotiated by ATTRIB.

b) The scenario shall be repeated for all combinations of PCD to PICC and PICC to PCD supported bit rates negotiated by S(PARAMETERS) if supported by the PICC. In step e), b8 to b5 of Param 2 shall be set to (0000)b.

G.4.3.2.2 Scenario

Perform the following steps:

Perform the following steps for each row of Table G.22:

a) Put the PICC into IDLE state.

b) Set the frame parameters of the PICC-test-apparatus according to Table G.22.

c) Send a REQB command.

d) Check that the PICC response is a valid ATQB. Record the presence, frame format, content and timing of the PICC response.

e) Send the appropriate ATTRIB(0, 0) command.

f) Check that the PICC response is a valid Answer to ATTRIB(0). Record the presence, frame format, content and timing of the PICC response.

g) Send an S(PARAMETERS) block to send Bit rates request.

h) Check PICC answer. If the PICC supports S(PARAMETERS) blocks, the PICC responds with an S(PARAMETERS) block containing values for all supported parameters. If the PICC does not support S(PARAMETERS) it stays mute; skip steps i) and j).

i) Send an S(PARAMETERS) block to activate selected communication parameters (bit rates and framing options).

j) Check that the PICC response is a valid S(PARAMETERS) block to acknowledge the activated parameters.

k) Send the I-block $I(0)_0$(TEST_COMMAND1(1)). Record the presence, frame format, content and timing of the PICC response.

l) Send the S(DESELECT) command.

m) Check that the PICC response is a valid S(DESELECT). Record the presence, frame format, content and timing of the PICC response.

n) Send a WUPB command.

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o) Check that the PICC response is a valid ATQB. Record the presence, frame format, content and timing of the PICC response.

Table G.22 — Type B PCD to PICC frame parameters

Test No.	EGT [etu]	SOF low [etu]	SOF high [etu]	EOF [etu]	Min. TR0 coding	Min. TR1 coding	EOF handling coding	SOF handling coding	Framing options (b2b1)[a]	Bit boundaries[b]	
										Rising edge [$1/f_c$]	Falling edge [$1/f_c$]
1	0	10,5	2,5	10,5	(00)b	(00)b	(0)b	(0)b	(00)b	0	0
2	0	10 – 1/16	2 – 1/8	10 – 1/16	(00)b	(00)b	(0)b	(0)b	(00)b	0	0
3	5,5[c d]	10 – 1/16	2 – 1/8	10 – 1/16	(00)b	(00)b	(0)b	(0)b	(00)b	0	0
4	0	11 + 1/8	2 – 1/8	10 – 1/16	(00)b	(00)b	(0)b	(0)b	(00)b	0	0
5	0	10 – 1/16	3 + 1/8	10 – 1/16	(00)b	(00)b	(0)b	(0)b	(00)b	0	0
6	6[c e]	11 + 1/8	3 + 1/8	11 + 1/8	(00)b	(00)b	(0)b	(0)b	(00)b	0	0
7	0	10 – 1/16	2 – 1/8	10 – 1/16	(00)b	(00)b	(0)b	(0)b	(00)b	–8[f]	–8[g]
8	0	10 – 1/16	2 – 1/8	10 – 1/16	(00)b	(00)b	(0)b	(0)b	(00)b	+8[h]	+8[i]
9	0	10 – 1/16	2 – 1/8	10 – 1/16	(00)b	(00)b	(0)b	(0)b	(00)b	–8[f]	+8[i]
10	0	10 – 1/16	2 – 1/8	10 – 1/16	(00)b	(00)b	(0)b	(0)b	(00)b	+8[h]	–8[g]
11	0	10,5	2,5	10,5	(00)b	(01)b	(0)b	(0)b	(00)b	0	0
12	0	10,5	2,5	10,5	(00)b	(10)b	(0)b	(0)b	(00)b	0	0
13	0	10,5	2,5	10,5	(01)b	(00)b	(0)b	(0)b	(00)b	0	0
14	0	10,5	2,5	10,5	(01)b	(01)b	(0)b	(0)b	(00)b	0	0
15	0	10,5	2,5	10,5	(01)b	(10)b	(0)b	(0)b	(00)b	0	0
16	0	10,5	2,5	10,5	(10)b	(00)b	(0)b	(0)b	(00)b	0	0
17	0	10,5	2,5	10,5	(10)b	(01)b	(0)b	(0)b	(00)b	0	0
18	0	10,5	2,5	10,5	(10)b	(10)b	(0)b	(0)b	(00)b	0	0
19	0	10,5	2,5	10,5	(00)b	(00)b	(0)b	(1)b	(00)b	0	0
20	0	10,5	2,5	10,5	(00)b	(00)b	(1)b	(0)b	(00)b	0	0
21	0	10,5	2,5	10,5	(00)b	(00)b	(1)b	(1)b	(00)b	0	0
22	0	10,5	2,5	10,5	(00)b	(00)b	(0)b	(0)b	(01)b	0	0
23	0	10,5	2,5	10,5	(00)b	(00)b	(0)b	(0)b	(10)b	0	0
24	0	10,5	2,5	10,5	(11)b	(11)b	(0)b	(0)b	(00)b	0	0
25	0	10,5	2,5	10,5	(00)b	(00)b	(0)b	(0)b	(00)b[j]	0	0

[a] Only applicable if PICC supports at least one framing options.

[b] Bit boundaries is applied on b2 of the first byte of I-block $I(0)_0$(TEST_COMMAND1(1)). For bit rates higher than $f_c/16$, bit boundaries shall occur at nominal bit positions.

[c] Not applicable for bit rates higher than $f_c/16$.

[d] Applies to all characters except between the last character and EOF where EGT of 0 will be used.

[e] Applies to all characters and also between the last character and EOF.

[f] Apply -4 for $f_c/64$, -2 for $f_c/32$ and –1 for $f_c/16$.

[g] Apply –1 for $f_c/64$, $f_c/32$ and $f_c/16$.

[h] Apply +4 for $f_c/64$, +2 for $f_c/32$ and +1 for $f_c/16$.

[i] Apply +1 for $f_c/64$, $f_c/32$ and $f_c/16$.

[j] All RFU bits in the 1st byte of the framing options shall be set to (1)b, the 2nd byte set to 'FF'. All RFU bits during bit rate negotiation in steps g) to j) shall be set to (1)b.

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G.4.3.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure, and

b) FAIL in any other case.

Report the measured timings in Table G.79.

G.4.4 Testing of the PICC Type B state transitions

G.4.4.1 General

These tests are to verify the correct implementation of the PICC Type B state diagram as described in ISO/IEC 14443-3:2018, 7.4.

G.4.4.2 General test outline

G.4.4.2.1 General

This is the same procedure as described for the PICC Type A (see G.3.3.2).

G.4.4.2.2 Functions to set the PICC in TIS

Putting the PICC into the TIS will be done by a sequence of transition commands specified in the following tables. The general method is as follows:

In order to put the PICC into the TIS, look up the corresponding sequence in Table G.23. Then successively apply the state transitions described in this column by looking up the corresponding commands in Table G.24. Always check the content and integrity of the PICC response.

Table G.23 — State transition sequence

TIS	State Transition Sequence
POWER-OFF	—
IDLE[a]	POWER-OFF → IDLE
READY-REQUESTED	POWER-OFF → IDLE → READY-REQUESTED
READY-DECLARED	POWER-OFF → IDLE → READY-DECLARED
PROTOCOL	POWER-OFF → IDLE → READY-DECLARED → PROTOCOL
HALT	POWER-OFF → IDLE → READY-DECLARED → HALT

[a] IDLE state may be reached from READY-DECLARED state.

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Table G.24 — State transition

State → Next State	PICC-test-apparatus		PICC
POWER-OFF → IDLE	Power On (RF operating field on)	→	
		←	Mute
IDLE → READY-REQUESTED	REQB(16)	→	
		←	Mute[a]
IDLE → READY-DECLARED	REQB(1)	→	
		←	ATQB
READY-DECLARED → HALT	HLTB	→	
		←	'00' CRC_B
READY-DECLARED → PROTOCOL	ATTRIB(0, 0)	→	
		←	Answer to ATTRIB(0)
READY-DECLARED → IDLE	REQB(1, nAFI)	→	
		←	Mute

[a] In case the PICC has selected slot 1, the REQB command shall be reissued until the PICC doesn't answer ATQB.

G.4.4.2.3 Functions for checking the validity of the TTS

Table G.25 describes the state transitions, which are used to check whether the PICC is in the state S. The content of the PICC answer (i.e. ATQB...) should be thoroughly checked for ISO/IEC 14443-3 and ISO/IEC 14443-4 conformance.

NOTE 1 The tests can cause the PICC to change its state.

Table G.25 — Checking the TTS

TTS	PICC-test-apparatus		PICC
IDLE	REQB(1)	→	
		←	ATQB[b]
READY-REQUESTED	SLOTMARKER (n)[a]	→	
		←	ATQB[b]
READY-DECLARED	ATTRIB(0, 0)	→	
		←	Answer to ATTRIB(0)
PROTOCOL	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
HALT	REQB(1)	→	
		←	Mute
	WUPB(1)	→	
		←	ATQB[b]

[a] Since the selected PICC slot is unknown, the Slot-MARKER command shall be reissued with different slot values until an ATQB is received.

[b] If the PUPI is known, check that PUPI has not changed.

NOTE 2 The block number can be 0 or 1 dependent on block numbering rules, see ISO/IEC 14443-4:2018, 7.6.4.

G.4.4.3 Scenario G.23: Behaviour of the PICC Type B in the IDLE state

G.4.4.3.1 Scope

This test is to determine the behaviour of the PICC Type B in the IDLE state according to ISO/IEC 14443-3:2018, 7.4.4.

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G.4.4.3.2 Procedure

Perform the following steps for every row of Table G.26:

a) Put the PICC into IDLE state. If the PUPI is unknown, put the PICC in READY-DECLARED state to retrieve its PUPI and put it in IDLE state using READY-DECLARED → IDLE state transition.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.26 — Transitions from IDLE state

Transition	PICC-test-apparatus		PICC	TTS
REQB[d]	REQB(1)	→		READY-DECLARED
		←	ATQB	
WUPB[d]	WUPB(1)	→		READY-DECLARED
		←	ATQB	
REQB (wrong CRC)	('05 00 00' ~CRC)	→		IDLE
		←	Mute	
WUPB (wrong CRC)	('05 00 08' ~CRC)	→		IDLE
		←	Mute	
HLTB	HLTB	→		IDLE
		←	Mute	
ATTRIB	ATTRIB(0, 0)	→		IDLE
		←	Mute	
Slot-MARKER	SLOTMARKER(n)[a]	→		IDLE
		←	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		IDLE
		←	Mute	
DESELECT	S(DESELECT)	→		IDLE
		←	Mute	
REQB[e] (Unmatched AFI)	REQB(1,nAFI)	→		IDLE
		←	Mute	
WUPB[e] (Unmatched AFI)	WUPB(1,nAFI)	→		IDLE
		←	Mute	
HLTB (Unmatched PUPI)	HLTB(~PUPI)	→		IDLE
		←	Mute	
ATTRIB (Unmatched PUPI)	ATTRIB(0, 0, ~PUPI)	→		IDLE
		←	Mute	
REQB[c]	REQB(16)[b]	→		READY-REQUESTED
		←	Mute	

[a] n shall run through all values 2 ≤ n ≤ 16.

[b] Nevertheless, there is statistically a probability of 1/16 so that the PICC answers ATQB and goes to READY-DECLARED sub-state.

[c] If the PICC does not support the REQB/WUPB with N > 1 (see ISO/IEC 14443-3:2018, 7.6.1) the test need not be applied.

[d] All matched AFIs as defined by the PICC manufacturer shall be tested.

[e] Any unmatched AFI values, also values which are currently RFU, should be tested.

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Table G.26 *(continued)*

Transition	PICC-test-apparatus		PICC	TTS
WUPB[c]	WUPB(16)[b]	→		READY-REQUESTED
		←	Mute	
REQB with all PARAM (b8,b7,b6) RFU values	REQB(1) with all PARAM (b8,b7,b6) RFU values	→		READY-DECLARED
		←	ATQB	
REQB with all N RFU values	REQB(all N RFU values)[b]	→		READY-REQUESTED
		←	Mute	

[a] n shall run through all values 2 ≤ n ≤ 16.

[b] Nevertheless, there is statistically a probability of 1/16 so that the PICC answers ATQB and goes to READY-DECLARED sub-state.

[c] If the PICC does not support the REQB/WUPB with N > 1 (see ISO/IEC 14443-3:2018, 7.6.1) the test need not be applied.

[d] All matched AFIs as defined by the PICC manufacturer shall be tested.

[e] Any unmatched AFI values, also values which are currently RFU, should be tested.

G.4.4.3.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.4.4.4 Scenario G.24: Behaviour of the PICC Type B in the READY-REQUESTED sub-state

G.4.4.4.1 General

If the PICC does not support the REQB/WUPB with N > 1 nor the Slot-MARKER command (see ISO/IEC 14443-3:2018, 7.6.1) this scenario need not be applied.

G.4.4.4.2 Scope

This test is to determine the behaviour of the PICC Type B in the READY-REQUESTED sub-state according to ISO/IEC 14443-3:2018, 7.4.5.

G.4.4.4.3 Procedure

Perform the following steps for every row of Table G.27:

a) Put the PICC into READY-REQUESTED state. If the PUPI is unknown, put the PICC in READY-DECLARED state to retrieve the PICC PUPI and put it in IDLE state before performing the step a).

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

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Table G.27 — Transitions from READY-REQUESTED sub-state

Transition	PICC-test-apparatus		PICC	TTS
REQB[d]	REQB(1)	→		READY-DECLARED
		←	ATQB	
WUPB[d]	WUPB(1)	→		READY-DECLARED
		←	ATQB	
REQB (wrong CRC)	('05 00 00' ~CRC)	→		READY-REQUESTED
		←	Mute	
WUPB (wrong CRC)	('05 00 08' ~CRC)	→		READY-REQUESTED
		←	Mute	
HLTB	HLTB	→		READY-REQUESTED
		←	Mute	
ATTRIB	ATTRIB(0, 0)	→		READY-REQUESTED
		←	Mute	
Slot-MARKER	SLOTMARKER(n)[a]	→		READY-DECLARED
		←	ATQB or Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		READY-REQUESTED
		←	Mute	
DESELECT	S(DESELECT)	→		READY-REQUESTED
		←	Mute	
REQB	REQB(16)[b]	→		READY-REQUESTED
		←	Mute	
WUPB	WUPB(16)[b]	→		READY-REQUESTED
		←	Mute	
REQB[e] (unmatched AFI)	REQB(1,nAFI)	→		IDLE[c]
		←	Mute	
WUPB[e] (unmatched AFI)	WUPB(1,nAFI)	→		IDLE[c]
		←	Mute	
HLTB (unmatched PUPI)	HLTB(~PUPI)	→		READY-REQUESTED
		←	Mute	
ATTRIB (unmatched PUPI)	ATTRIB(0, 0, ~PUPI)	→		READY-REQUESTED
		←	Mute	

[a] n shall run through all values $2 \leq n \leq 16$. The PICC shall respond ATQB at exactly one value of n, else Mute.

[b] Nevertheless, there is statistically a probability of 1/16 so that the PICC answers ATQB and goes to READY-DECLARED sub-state.

[c] Send all Slot-MARKER commands and verify that there is no response before checking the IDLE state.

[d] All matched AFIs as defined by the PICC manufacturer shall be tested.

[e] Any unmatched AFI values, also values which are currently RFU, should be tested.

G.4.4.4.4 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure, and

b) FAIL in any other case.

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G.4.4.5 Scenario G.25: Behaviour of the PICC Type B in the READY-DECLARED sub-state

G.4.4.5.1 Scope

This test is to determine the behaviour of the PICC Type B in the READY-DECLARED sub-state according to ISO/IEC 14443-3:2018, 7.4.6.

G.4.4.5.2 Procedure

Perform the following steps for every row of Table G.28:

a) Put the PICC into READY-DECLARED sub-state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.28 — Transitions from READY-DECLARED sub-state

Transition	PICC-test-apparatus		PICC	TTS
REQB[e]	REQB(1)	→		READY-DECLARED
		←	ATQB	
WUPB[e]	WUPB(1)	→		READY-DECLARED
		←	ATQB	
REQB (wrong CRC)	('05 00 00' ~CRC)	→		READY-DECLARED
		←	Mute	
WUPB (wrong CRC)	('05 00 08' ~CRC)	→		READY-DECLARED
		←	Mute	
HLTB	HLTB	→		HALT
		←	('00' CRC_B)	
ATTRIB	ATTRIB(0, 0)	→		PROTOCOL
		←	Answer to ATTRIB(0)	
Slot-MARKER	SLOTMARKER(n)[a]	→		READY-DECLARED
		←	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		READY-DECLARED
		←	Mute	
DESELECT	S(DESELECT)	→		READY-DECLARED
		←	Mute	
REQB[b]	REQB(16)[c]	→		READY-REQUESTED
		←	Mute	
WUPB[b]	WUPB(16)[c]	→		READY-REQUESTED
		←	Mute	
HLTB (unmatched PUPI)	HLTB(~PUPI)	→		READY-DECLARED
		←	Mute	

[a] n shall run through all values $2 \leq n \leq 16$.

[b] If the PICC does not support the REQB/WUPB with N > 1 (see ISO/IEC 14443-3:2018, 7.6.1) the test need not be applied.

[c] Nevertheless, there is statistically a probability of 1/16 so that the PICC answers ATQB and goes to READY-DECLARED sub-state.

[d] Send ATTRIB command and verify that there is no response before checking the IDLE state.

[e] All matched AFIs as defined by the PICC manufacturer shall be tested.

[f] Any unmatched AFI values, also values which are currently RFU, should be tested.

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Table G.28 *(continued)*

Transition	PICC-test-apparatus		PICC	TTS
ATTRIB (unmatched PUPI)	ATTRIB(0, 0, ~PUPI)	→		READY-DECLARED
		←	Mute	
REQB[f] (unmatched AFI)	REQB(1,nAFI)	→		IDLE[d]
		←	Mute	
WUPB[f] (Unmatched AFI)	WUPB(1,nAFI)	→		IDLE[d]
		←	Mute	
ATTRIB with all Param 1 (b2,b1) RFU values	ATTRIB(0, 0) with Param 1 (b2,b1) set to RFU values	→		PROTOCOL
		←	Answer to ATTRIB(0)	
ATTRIB with Param 1 (b8 to b5) RFU value	ATTRIB(0, 0) with Param 1 (b8,b7,b6,b5) set to (1,1,1,1)	→		PROTOCOL
		←	Answer to ATTRIB(0)	
ATTRIB with all Param 2 (b4 to b1) RFU values	ATTRIB(0, with Param 2 (b,b3,b2,b1) set to RFU values)	→		PROTOCOL
		←	Answer to ATTRIB(0)	
ATTRIB with Param 3 (b4) RFU value	ATTRIB(0, 0) with Param 3 (b4) set to (1)b	→		PROTOCOL
		←	Answer to ATTRIB(0)	
ATTRIB with Param 3 (b3,b2) values	ATTRIB(0, 0) with all Param 3 (b3,b2) values different to ATQB Protocol_Type (b3,b2) value	→		PROTOCOL
		←	Answer to ATTRIB(0)	
ATTRIB with Param 3 (b8 to b5) RFU values	ATTRIB(0, 0) with Param 3 (b8,b7,b6,b5) set to RFU values	→		READY-DECLARED
		←	Mute	
ATTRIB with Param 4 CID RFU value	ATTRIB(15, 0)	→		READY-DECLARED
		←	Mute	
ATTRIB with all Param 4 (b8 to b5) RFU values	ATTRIB(0, 0) with Param 4 (b8,b7,b6,b5) set to RFU values	→		PROTOCOL
		←	Answer to ATTRIB(0)	

[a] n shall run through all values 2 ≤ n ≤ 16.

[b] If the PICC does not support the REQB/WUPB with N > 1 (see ISO/IEC 14443-3:2018, 7.6.1) the test need not be applied.

[c] Nevertheless, there is statistically a probability of 1/16 so that the PICC answers ATQB and goes to READY-DECLARED sub-state.

[d] Send ATTRIB command and verify that there is no response before checking the IDLE state.

[e] All matched AFIs as defined by the PICC manufacturer shall be tested.

[f] Any unmatched AFI values, also values which are currently RFU, should be tested.

G.4.4.5.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.4.4.6 Scenario G.26: Behaviour of the PICC Type B in the HALT state

G.4.4.6.1 Scope

This test is to determine the behaviour of the PICC Type B in the HALT state according to ISO/IEC 14443-3:2018, 7.4.8.

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G.4.4.6.2 Procedure

Perform the following steps for every row of Table G.29:

a) Put the PICC into HALT state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.29 — Transitions from HALT state

Transition	PICC-test-apparatus		PICC	TTS
REQB[d]	REQB(1)	→		HALT
		←	Mute	
WUPB[d]	WUPB(1)	→		READY-DECLARED
		←	ATQB	
WUPB (wrong CRC)	('05 00 08' ~CRC)	→		HALT
		←	Mute	
HLTB	HLTB	→		HALT
		←	Mute	
ATTRIB	ATTRIB(0, 0)	→		HALT
		←	Mute	
Slot-MARKER	SLOTMARKER(n)[a]	→		HALT
		←	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		HALT
		←	Mute	
DESELECT	S(DESELECT)	→		HALT
		←	Mute	
WUPB[e] (Unmatched AFI)	WUPB(1,nAFI)	→		IDLE
		←	Mute	
REQB[e] (Unmatched AFI)	REQB(1,nAFI)	→		HALT
		←	Mute	
HLTB (Unmatched PUPI)	HLTB(~PUPI)	→		HALT
		←	Mute	
ATTRIB (Unmatched PUPI)	ATTRIB(0, 0, ~PUPI)	→		HALT
		←	Mute	
WUPB[b]	WUPB(16)[c]	→		READY-REQUESTED
		←	Mute	

[a] n shall run through all values 2 ≤ n ≤ 16.

[b] If the PICC does not support the REQB/WUPB with N > 1 (see ISO/IEC 14443-3:2018, 7.6.1), the test need not be applied.

[c] Nevertheless, there is statistically a probability of 1/16 so that the PICC answers ATQB and goes to READY-DECLARED sub-state.

[d] All matched AFIs as defined by the PICC manufacturer shall be tested.

[e] Any unmatched AFI value, also values which are RFU, should be tested.

G.4.4.6.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

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G.4.4.7 Scenario G.27: Behaviour of the PICC Type B in the PROTOCOL state

G.4.4.7.1 Scope

This test is to determine the behaviour of the PICC Type B in the PROTOCOL state according to ISO/IEC 14443-3:2018, 7.4.7. This test shall ensure that the activated PICC does not respond to any initialization command.

G.4.4.7.2 Procedure

Perform the following steps for every row of Table G.30:

a) Put the PICC into PROTOCOL state.

b) Perform the state transition by sending the command as indicated in the PICC-test-apparatus column.

c) Check if the PICC response is as indicated in the PICC column.

d) Check if the PICC is in the TTS.

Table G.30 — Transitions from PROTOCOL state

Transition	PICC-test-apparatus		PICC	TTS
REQB[b]	REQB(1)	→		PROTOCOL
		←	Mute	
WUPB[b]	WUPB(1)	→		PROTOCOL
		←	Mute	
REQB (wrong CRC)	('05 00 00' ~CRC)	→		PROTOCOL
		←	Mute	
WUPB (wrong CRC)	('05 00 08' ~CRC)	→		PROTOCOL
		←	Mute	
HLTB	HLTB	→		PROTOCOL
		←	Mute	
ATTRIB	ATTRIB(0, 0)	→		PROTOCOL
		←	Mute	
Slot-MARKER	SLOTMARKER(n)[a]	→		PROTOCOL
		←	Mute	
ISO/IEC 14443-4 command	$I(0)_0$(TEST_COMMAND1(1))	→		PROTOCOL
		←	$I(0)_0$(TEST_RESPONSE1(1))	
DESELECT	S(DESELECT)	→		HALT
		←	S(DESELECT)	
WUPB[c] (unmatched AFI)	WUPB(1,nAFI)	→		PROTOCOL
		←	Mute	
REQB[c] (unmatched AFI)	REQB(1,nAFI)	→		PROTOCOL
		←	Mute	

[a] n shall run through all values 2 ≤ n ≤ 16.

[b] All matched AFIs as defined by the PICC manufacturer shall be tested.

[c] Any unmatched AFI values, also values which are currently RFU, should be tested.

[d] Check first IDLE state as TTS. If TTS is not IDLE state, rerun the test a second time to check PROTOCOL state.

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Table G.30 *(continued)*

Transition	PICC-test-apparatus		PICC	TTS
HLTB (unmatched PUPI)	HLTB(~PUPI)	→		PROTOCOL
		←	Mute	
ATTRIB (unmatched PUPI)	ATTRIB(0, 0, ~PUPI)	→		PROTOCOL
		←	Mute	
Type A command	REQA	→		IDLE or PROTOCOL[d]
		←	Mute	

[a] n shall run through all values 2 ≤ n ≤ 16.

[b] All matched AFIs as defined by the PICC manufacturer shall be tested.

[c] Any unmatched AFI values, also values which are currently RFU, should be tested.

[d] Check first IDLE state as TTS. If TTS is not IDLE state, rerun the test a second time to check PROTOCOL state.

G.4.4.7.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.4.5 Scenario G.28: Handling of Type B anticollision

G.4.5.1 Scope

The purpose of this test is to determine the handling of a PICC Type B anticollision according to ISO/IEC 14443-3:2018, 7.4.1.

The core of this test is the procedure AnticollisionB(N, outparam chi2) which is defined in the pseudo code below. The procedure performs 256 REQB(N) commands and following Slot-MARKER commands and counts how many times each of the N slots has been selected by the PICC. The procedure also checks if the PICC has mapped each REQB(N) request to exactly one slot. If this is not the case the test returns FAIL.

Since Type B anticollision is based on random selection of the slots, statistical methods shall be used for verification. As it is the nature of all statistical tests, this test can fail even in the case the PICC behaves correctly. This failure is called a "Type I error" in statistical terms. This error cannot be completely avoided. Instead, the probability of its occurrence can be controlled by the so called "significance value" α. This means, the smaller α, the less probable the "Type I error". However, this does not mean that one should select α as small as possible. This is because the smaller α is, the more probable is that the test passes a bad PICC (i.e. a PICC that doesn't select the slots with the right probability). In statistical terms this is called a "Type II error".

The PICC shall additionally select each of the N slots with equal probability (i.e. 1/N). In order to verify this, the statistical χ^2-test on all slots shall be performed. The result of this test is the value chi2 which shall be compared against the $\chi^2_{\alpha,N-1}$ quintile.

G.4.5.2 Procedure

If one of the statistical tests fails in step e) the test lab may rerun the test for this parameter N.

Perform the following steps for each value N = 2, 4, 8, 16.

a) Set the significance level α to 0,005 and look up from Table G.31 the corresponding $\chi^2_{\alpha,N-1}$ quintile. Other choices of α according to Table G.31 are optional for the test applicants.

b) Reset the PICC.

c) Execute AnticollisionB(N, chi2).

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d) If AnticollisionB returns FAIL, fail the test.

e) If chi2 ≤ $\chi^2_{\alpha,N-1}$ then the test is PASS else the test is FAIL.

Table G.31 — α quintile values

α	$\chi^2_{\alpha,N-1}$			
	$\chi^2_{\alpha,1}$	$\chi^2_{\alpha,3}$	$\chi^2_{\alpha,7}$	$\chi^2_{\alpha,15}$
0,1 (optional)	2,706	6,251	12,017	22,307
0,05 (optional)	3,841	7,815	14,067	24,996
0,01 (optional)	6,635	11,345	18,475	30,578
0,005	7,879	12,838	20,278	32,801

Pseudo code: Type B anticollision procedure

```
1   Procedure AnticollisionB(N, chi2)
3   // TPDUSend and TPDURecv are PCD specific functions
4   // to send and receive TPDU frames
5   //
6   // probability for selecting slot
7   p = 1/N
8   //
9   // clear slot counters
10  for i from 1 to N do
11    Slots[i] = 0
12  endfor
13  //
14  // collect data
15  for i from 1 to 256 do
16    Reset the PICC
17    TPDUSend (REQB(N))
18    if TPDURecv() = ATQB then
19      Slots[1] = Slots[1]+1
20    endif
21    for j from 2 to N do
22      TPDUSend (SLOTMARKER(j))
23      if TPDURecv () = ATQB then
24        Slots[j] = Slots[j]+1
25      endif
26    endfor
27  endfor
28  //
29  // check that exactly
30  // one slot has been selected at each run
31  cnt = 0
32  for i from 1 to N do
33    cnt = cnt + Slots[i]
34  endfor
35 if cnt ≠ 256 then
36    return FAIL
37  endif
38  Chi2 = 0
39  for i from 1 to N do
40    chi2 = chi2 + Slots[i]*Slots[i]
41  endfor
42  chi2 = chi2*N/256 - 256
43  return PASS
```

G.4.5.3 Test report

The test is:

a) PASS only when every Anticollision Test procedure returns PASS; and

b) FAIL when any Anticollision Test procedure returns the value FAIL.

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G.4.6 Handling of ATTRIB

G.4.6.1 Scope

This test is to determine the behaviour of the PICC Type B on ATTRIB command according to ISO/IEC 14443-3:2018, 7.10.

G.4.6.2 Procedure

For each of the scenarios described in Table G.32 and Table G.33, perform the following steps:

a) Put the PICC into READY-DECLARED sub-state.

b) Send the command sequence as described in the PICC-test-apparatus column.

c) Check that the response of the PICC conforms with the one given in the PICC column.

d) Check if the PICC is in PROTOCOL state.

Table G.32 — Scenario G.29: ATTRIB with wrong PUPI

PICC-test-apparatus		PICC
ATTRIB(0, 0, ~PUPI)	→	
	←	Mute
ATTRIB(0, 0)	→	
	←	Answer to ATTRIB(0)

Table G.33 — Scenario G.30: ATTRIB after wrong ATTRIB

PICC-test-apparatus		PICC
ATTRIB(0, 0, ~CRC)	→	
	←	Mute
ATTRIB(0, 0)	→	
	←	Answer to ATTRIB(0)

G.4.6.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.4.7 Scenario G.31: Handling of Maximum Frame Size

G.4.7.1 Scope

This test is to determine if the PICC Type B respects the Maximum Frame Size as negotiated by the ATTRIB according to ISO/IEC 14443-3:2018, 7.10.4.

G.4.7.2 Procedure

Perform the following steps for each Maximum Frame Size Code in ATTRIB as defined in ISO/IEC 14443-3 including RFU values:

a) Put the PICC into READY-DECLARED sub-state as described in G.4.4.2.2.

b) Send the ATTRIB(0, fsdi) command with parameter fsdi as in the particular test.

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c) Check if the PICC answer is Answer to ATTRIB(0).

d) Carry out additional sequences if required by the PICC to be ready to accept TEST_COMMAND2(2).

e) Send the I-block $I(0)_0$(TEST_COMMAND2(2)).

f) Check if the size of the I-block response of the PICC response is does not exceed the Maximum Frame Size.

G.4.7.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.4.8 Handling of TR2 and SFGT

G.4.8.1 Scope

This test is to determine if the PICC Type B respects the minimum TR2 according ISO/IEC 14443-3:2018, 7.9.4.4 and SFGT according ISO/IEC 14443-3:2018, 7.9.4.7.

G.4.8.2 Procedure

The procedure shall be repeated at a bit rate of $f_c/128$ in both directions and at the maximum bit rates supported by the PICC in each direction.

Perform the following steps of the scenario described in Table G.34:

a) Put the PICC into IDLE state.

b) For each step in the scenario do:

   1) Send the command as described in the PICC-test-apparatus column respecting the timing condition described in the TR2 column.

   2) Check that the PICC response matches the one of the PICC column.

c) End for.

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Table G.34 — Scenario G.73: Handling of TR2 and SFGT

Step	TR2 to apply	PICC-test-apparatus		PICC
1	—	REQB(1)[a]	→	
			←	ATQB or Extended ATQB
2	—	WUPB(1)[a]	→	
			←	ATQB or Extended ATQB
3	Minimum TR2 + $50/f_c$[b,c]	ATTRIB(0, 0)	→	
			←	Answer to ATTRIB
4	Minimum TR2 + $50/f_c$[b,c] or SFGT + $50/f_c$[c,d]	$I(0)_0$(TEST_COMMAND1(1))	→	
			←	$I(0)_0$(TEST_RESPONSE1(1))[e]
5	Minimum TR2 + $50/f_c$[b,c]	$I(0)_1$(TEST_COMMAND3)	→	
			←	S(WTX)(WTXM)
6	Minimum TR2 + $50/f_c$[b,c]	S(WTX)(WTXM)	→	
			←	$I(0)_1$(TEST_RESPONSE3)[f]

[a] Bit 5 of PARAM is set to 1 (PICC-test-apparatus supports the extended ATQB).

[b] Minimum TR2 is set as given in the ATQB.

[c] The applied TR2 or SFGT shall have a maximum tolerance of $\pm 25/f_c$.

[d] If the PICC has responded with extended ATQB.

[e] S(WTX) request(s) may be sent by the PICC. The PICC-test-apparatus shall acknowledge each S(WTX) request with an S(WTX) response until receiving the PICC response. There is no specific requirement on TR2 for the S(WTX) response(s).

[f] Additional S(WTX) request(s) may be sent by the PICC. The PICC-test-apparatus shall acknowledge each S(WTX) request with an S(WTX) response until receiving the PICC response. There is no specific requirement on TR2 for the S(WTX) response(s).

G.4.8.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure; and

b) FAIL in any other case.

G.5 Test methods for logical operation of the PICC Type A or Type B

G.5.1 General

G.5.1.1 General

This subclause contains tests verifying that the activated PICC conforms to the ISO/IEC 14443-4. This subclause applies to PICC Type A and Type B.

G.5.1.2 PICC activation process

G.5.1.2.1 General

PICC activation is the process of putting the PICC in the state where protocol blocks defined in ISO/IEC 14443-4 may be exchanged. This process is dependent on the PICC communication signal interface.

G.5.1.2.2 Activation of the PICC Type A

a) Put the PICC into ACTIVE state as described in G.3.3.2.2.

b) Send RATS(cid, fsdi).

c) Check that the PICC response is a valid ATS.

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G.5.1.2.3 Activation of the PICC Type B

a) Put the PICC into READY-DECLARED sub-state as described in G.4.4.2.2.

b) Send ATTRIB(cid, fsdi).

c) Check that the PICC response is a valid Answer to ATTRIB(cid).

G.5.2 PICC reaction to ISO/IEC 14443-4 scenarios

G.5.2.1 Scope

This test is to determine the behaviour of the PICC according to ISO/IEC 14443-4:2018, Clause 7. This test uses implementations of the protocol scenarios of ISO/IEC 14443-4:2018, Annex B.

G.5.2.2 Procedure

For each of the scenarios described in Table G.35 to Table G.58, perform the following steps:

a) Activate the PICC as described in G.5.1.2, use CID = 0.

b) For each step in the scenario do:

   1) Send the command as described in the PICC-test-apparatus column.

   2) Check that the PICC response matches the one of the PICC column.

c) End for.

Table G.35 — Scenario G.32: Exchange of I-blocks

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
2	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.36 — Scenario G.33: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	→	
		←	S(WTX)(WTXM)
2	S(WTX)(WTXM)	→	
		←	$I(0)_0$(TEST_RESPONSE3)
3	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

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Table G.37 — Scenario G.34: DESELECT

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
2	S(DESELECT)	→	
		←	S(DESELECT)
3	REQA or REQB(1)[a]	→	
		←	Mute
4	WUPA or WUPB(1)[a]	→	
		←	ATQA or ATQB[a]

[a] For the PICC Type A, the left option shall be used. For the PICC Type B, the right option shall be used.

Table G.38 — Scenario G.35: PCD uses chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$(TEST_COMMAND1$(2)_1$)	→	
		←	$R(ACK)_0$
2	$I(0)_1$(TEST_COMMAND1$(2)_2$)	→	
		←	$I(0)_1$(TEST_RESPONSE1(2))
3	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))

Table G.39 — Scenario G.36: PICC uses chaining

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(2))	→	
		←	$I(1)_0$(TEST_RESPONSE2$(2)_1$)
2	$R(ACK)_1$	→	
		←	$I(0)_1$(TEST_RESPONSE2$(2)_2$)
3	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))

Table G.40 — Scenario G.37: Start of protocol

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1), ~CRC)	→	
		←	Mute
2	$R(NAK)_0$	→	
		←	$R(ACK)_1$
3	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
4	$I(0)_1$(TEST_COMMAND1(1))	→	$I(0)_1$(TEST_RESPONSE1(1))
		←	

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Table G.41 — Scenario G.38: Exchange of I-blocks

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
2	$I(0)_1$(TEST_COMMAND1(1), ~CRC)	→	
		←	Mute
3	$R(NAK)_1$	→	
		←	$R(ACK)_0$
4	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))
5	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))

Table G.42 — Scenario G.39: Exchange of I-blocks 1

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
2	$R(NAK)_0$	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
3	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.43 — Scenario G.40: Exchange of I-blocks 2

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
2	$R(NAK, \sim CRC)_0$	→	
		←	Mute
3	$R(NAK)_0$	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
4	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.44 — Scenario G.41: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	→	
		←	S(WTX)(WTXM)
2	$R(NAK)_0$	→	
		←	S(WTX)(WTXM)
3	S(WTX)(WTXM)	→	
		←	$I(0)_0$(TEST_RESPONSE3)
4	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

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Table G.45 — Scenario G.42: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	→	
		←	S(WTX)(WTXM)
2	$R(NAK, \sim CRC)_0$	→	
		←	Mute
3	$R(NAK)_0$	→	
		←	S(WTX)(WTXM)
4	S(WTX)(WTXM)	→	
		←	$I(0)_0$(TEST_RESPONSE3)
5	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.46 — Scenario G.43: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	→	
		←	S(WTX)(WTXM)
2	S(WTX)(WTXM, ~CRC)	→	
		←	Mute
3	$R(NAK)_0$	→	
		←	S(WTX)(WTXM)
4	S(WTX)(WTXM)	→	
		←	$I(0)_0$(TEST_RESPONSE3)
5	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.47 — Scenario G.74: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	→	
		←	S(WTX)(WTXM)
2	S(WTX) (WTXM, wrong parity bit)[a]	→	
		←	Mute
3	$R(NAK)_0$	→	
		←	S(WTX)(WTXM)
4	S(WTX)(WTXM)	→	
		←	$I(0)_0$(TEST_RESPONSE3)
5	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

[a] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit

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Table G.48 — Scenario G.44: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	→	
		←	S(WTX)(WTXM)
2	S(WTX)(WTXM)	→	
		←	$I(0)_0$(TEST_RESPONSE3)
3	$R(NAK)_0$	→	
		←	$I(0)_0$(TEST_RESPONSE3)
4	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.49 — Scenario G.45: Request for waiting time extension

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3)	→	
		←	S(WTX)(WTXM)
2	S(WTX)(WTXM)	→	
		←	$I(0)_0$ (TEST_RESPONSE3)
3	$R(NAK, \sim CRC)_0$	→	
		←	Mute
4	$R(NAK)_0$	→	
		←	$I(0)_0$ (TEST_RESPONSE3)
5	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.50 — Scenario G.46: DESELECT

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
2	S(DESELECT, ~CRC)	→	
		←	Mute
3	S(DESELECT)	→	
		←	S(DESELECT)
4	REQA or REQB(1)[a]	→	
		←	Mute
5	WUPA or WUPB(1)[a]	→	
		←	ATQA or ATQB[a]

[a] For the PICC Type A, the left option shall be used. For the PICC Type B, the right option shall be used.

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Table G.51 — Scenario G.47: PCD uses chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$(TEST_COMMAND1(3)$_1$)	→	
		←	$R(ACK)_0$
2	$R(NAK)_0$	→	
		←	$R(ACK)_0$
3	$I(1)_1$(TEST_COMMAND1(3)$_2$)	→	
		←	$R(ACK)_1$
4	$I(0)_0$(TEST_COMMAND1(3)$_3$)	→	
		←	$I(0)_0$(TEST_RESPONSE1(3))
5	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.52 — Scenario G.48: PCD uses chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$(TEST_COMMAND1(3)$_1$)	→	
		←	$R(ACK)_0$
2	$I(1)_1$(TEST_COMMAND1(3)$_2$, ~CRC)	→	
		←	Mute
3	$R(NAK)_1$	→	
		←	$R(ACK)_0$
4	$I(1)_1$(TEST_COMMAND1(3)$_2$)	→	
		←	$R(ACK)_1$
5	$I(0)_0$(TEST_COMMAND1(3)$_3$)	→	
		←	$I(0)_0$(TEST_RESPONSE1(3))
6	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.53 — Scenario G.49: PCD uses chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$ (TEST_COMMAND1(3)$_1$)	→	
		←	$R(ACK)_0$
2	$R(NAK, \sim CRC)_0$	→	
		←	Mute
3	$R(NAK)_0$	→	
		←	$R(ACK)_0$
4	$I(1)_1$(TEST_COMMAND1(3)$_2$)	→	
		←	$R(ACK)_1$
5	$I(0)_0$(TEST_COMMAND1(3)$_3$)	→	
		←	$I(0)_0$ (TEST_RESPONSE1(3))
6	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

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Table G.54 — Scenario G.50: PICC uses chaining

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(3))	→	
		←	$I(1)_0$(TEST_RESPONSE2(3)$_1$)
2	R(ACK, ~CRC)$_1$	→	
		←	Mute
3	$R(ACK)_1$	→	
		←	$I(1)_1$(TEST_RESPONSE2(3)$_2$)
4	$R(ACK)_0$	→	
		←	$I(0)_0$(TEST_RESPONSE2(3)$_3$)
5	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.55 — Scenario G.51: PICC uses chaining

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(3))	→	
		←	$I(1)_0$(TEST_RESPONSE2(3)$_1$)
2	$R(ACK)_1$	→	
		←	$I(1)_1$(TEST_RESPONSE2(3)$_2$)
3	$R(ACK)_1$	→	
		←	$I(1)_1$(TEST_RESPONSE2(3)$_2$)
4	$R(ACK)_0$	→	
		←	$I(0)_0$(TEST_RESPONSE2(3)$_3$)
5	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

Table G.56 — Scenario G.52: PICC uses chaining

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(2))	→	
		←	$I(1)_0$(TEST_RESPONSE2(2)$_1$)
2	$R(NAK)_0$	→	
		←	$I(1)_0$(TEST_RESPONSE2(2)$_1$)
3	$R(ACK)_1$	→	
		←	$I(0)_1$(TEST_RESPONSE2(2)$_2$)
4	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))

Table G.57 — Scenario G.53: PICC Presence Check Method 1

Step	PICC-test-apparatus		PICC
1	$I(0)_0$()	→	
		←	$I(0)_0$() or $I(0)_0$(inf)
2	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))
3	$I(0)_0$()	→	
		←	$I(0)_0$() or $I(0)_0$(inf)

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Table G.58 — Scenario G.54: PICC Presence Check Method 2

Step	PICC-test-apparatus		PICC
1	$R(NAK)_0$	→	
		←	$R(ACK)_1$
2	$R(NAK)_0$	→	
		←	$R(ACK)_1$
3	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
4	$R(NAK)_1$	→	
		←	R(ACK)0
5	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))

G.5.2.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure, and

b) FAIL in any other case.

G.5.3 Handling of PICC error detection

G.5.3.1 Scope

This test is to determine the error detection mechanism of the PICC as described in ISO/IEC 14443-4:2018, 7.6.7.

G.5.3.2 Procedure

For each of the scenarios described in Table G.59, Table G.60, Table G.61 and Table G.62, perform the following steps:

a) Place the PICC into the field.

b) Activate the PICC as described in G.5.1.2, use CID = 0.

c) For each step in scenario do:

   1) Send the command as described in the PICC-test-apparatus column.

   2) Check if the PICC response is as described in the PICC column.

d) End for.

Table G.59 — Scenario G.55: Wrong CRC on I-block

Step	PICC-test-apparatus		PICC	Comment
1	$I(0)_0$(TEST_COMMAND1(1), ~CRC)	→		ISO/IEC 14443-4:2018, 7.6.7.1 a)
		←	Mute	
2	$I(0)_0$(TEST_COMMAND1(1))	→		
		←	$I(0)_0$(TEST_RESPONSE1(1))	

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Table G.60 — Scenario G.56: Wrong CRC on chained I-block

Step	PICC-test-apparatus		PICC	Comment
1	$I(1)_0$(TEST_COMMAND1(2)$_1$)	→		
		←	$R(ACK)_0$	
2	$I(0)_1$(TEST_COMMAND1(2)$_2$, ~CRC)	→		ISO/IEC 14443-4:2018, 7.6.7.1 a)
		←	Mute	
3	$I(0)_1$(TEST_COMMAND1(2)$_2$)	→		
		←	$I(0)_1$(TEST_RESPONSE1(2))	

Table G.61 — Scenario G.57: Wrong CRC on S(WTX)-block

Step	PICC-test-apparatus		PICC	Comment
1	$I(0)_0$(TEST_COMMAND3)	→		
		←	S(WTX)(WTXM)	
2	S(WTX)(WTXM, ~CRC)	→		ISO/IEC 14443-4:2018, 7.6.7.1 a)
		←	Mute	
3	S(WTX)(WTXM)	→		
		←	$I(0)_0$(TEST_RESPONSE3)	

Table G.62 — Scenario G.75: RFU block type

Step	PICC-test-apparatus		PICC	Comment
1	$I(0)_0$(TEST_COMMAND1(1), RFU block type	→		ISO/IEC 14443-4:2018, 7.2.2.1
		←	Mute	
2	$I(0)_0$(TEST_COMMAND1(1))	→		
		←	$I(0)_0$(TEST_RESPONSE1(1))	

G.5.3.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure, and

b) FAIL in any other case.

G.5.4 PICC reaction on CID

G.5.4.1 Scope

This test is to determine the reaction of the PICC to CID coding according to ISO/IEC 14443-4:2018, 7.2.2.2.

G.5.4.2 Procedure

For each of the scenarios described in Table G.65 to Table G.70, perform the following steps. Use the proper CID test case table depending upon whether the PICC supports CID or not.

For each row in the CID test case tables Table G.63 or Table G.64 do:

a) Activate the PICC with cid_{ass} as indicated in the column Assigned CID.

b) Perform a block exchange as described in the corresponding scenario. Use the cid_{cmd} as described in the Command CID column in the CID test case table.

c) Check if the PICC response matches with the response as in the PICC column in the scenario. If two response options are indicated for the PICC, then the unique expected response will be determined from the expected PICC response column in the CID test case table.

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Table G.63 — CID test cases (for PICCs which support CID)

Test No.[a]	Assigned CID (cid_{ass})	Command CID (cid_{cmd})	Expected PICC response
1	1	1	Response 1 of the scenario
2	0	0	Response 1 of the scenario
3	0	NO CID	Response 1 of the scenario
4	1	NO CID	Response 2 of the scenario (Mute)
5	0	1	Response 2 of the scenario (Mute)
6	1	0	Response 2 of the scenario (Mute)
7	2	1	Response 2 of the scenario (Mute)
8	1	1 with (b6,b5) = (01)b	Response 2 of the scenario (Mute)
9	1	1 with (b6,b5) = (10)b	Response 2 of the scenario (Mute)
10	1	1 with (b6,b5) = (11)b	Response 2 of the scenario (Mute)

[a] Each test shall be carried out with each of the scenarios described.

Table G.64 — CID test cases (for PICCs which do not support CID)

Test No.[a]	Assigned CID (cid_{ass})	Command CID (cid_{cmd})	Expected PICC response
1	0	0	Response 2 of the scenario (Mute)
2	0	NO CID	Response 1 of the scenario
3	0	1	Response 2 of the scenario (Mute)
4[b]	1	NO CID	Response 1 of the scenario

[a] Each test shall be carried out with each of the scenarios described.

[b] Applies to PICC Type A only.

Table G.65 — Scenario G.58: CID on I-block

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1), CID = cid_{cmd})	→ ←	Response 1: $I(0)_0$(TEST_RESPONSE1(1), CID = cid_{cmd}) Response 2: Mute[a]

[a] Response 1 or response 2 according to Table G.58 or Table G.59.

Table G.66 — Scenario G.59: CID on I-block with chaining

Step	PICC-test-apparatus		PICC
1	$I(1)_0$ (TEST_COMMAND1$(2)_1$,CID = cid_{cmd})	→ ←	Response 1: R(ACK, CID = cid_{cmd})$_0$ Response 2: Mute[a]

[a] Response 1 or response 2 according to Table G.58 or Table G.59.

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Table G.67 — Scenario G.60: CID on R-block

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(3), CID[a] = cid_{ass})	→	
		←	$I(1)_0$(TEST_RESPONSE2(3)$_1$, CID = cid_{ass})
2	R(ACK, CID[a] = cid_{cmd})$_1$	→	
		←	Response 1: $I(1)_1$ (TEST_RESPONSE2(3)$_2$, CID = cid_{cmd}) Response 2: Mute[b]

[a] For PICC not supporting CID, use no CID.

[b] Response 1 or response 2 according to Table G.58 or Table G.59.

Test No. 3 of Table G.92 shall be omitted for this scenario.

Table G.68 — Scenario G.61: CID on S(WTX)-block

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND3, CID[a] = cid_{ass})	→	
		←	S(WTX)(WTXM, CID = cid_{ass})
2	S(WTX)(WTXM, CID[a] = cid_{cmd})	→	
		←	Response 1: $I(0)_0$(TEST_RESPONSE3, CID[a] = cid_{cmd}) Response 2: Mute[b]

[a] For PICC not supporting CID, use no CID.

[b] Response 1 or response 2 according to Table G.58 or Table G.59.

Test No. 3 of Table G.92 shall be omitted for this scenario

Table G.69 — Scenario G.62: CID on S(DESELECT)-block

Step	PICC-test-apparatus		PICC
1	S(DESELECT, CID = cid_{cmd})	→	
		←	Response 1: S(DESELECT, CID = cid_{cmd}) Response 2: Mute[a]

[a] Response 1 or response 2 according to Table G.58 or Table G.59.

Table G.70 — Scenario G.66: CID on S(PARAMETERS)-block

Step	PICC-test-apparatus		PICC
1	S(PARAMETERS, CID = cid_{cmd})	→	
		←	Response 1: S(PARAMETERS, CID = cid_{cmd}) Response 2: Mute[a]

[a] If the PICC supports S(PARAMETERS) response 1 or response 2 in accordance with Table G.58 or Table G.59. Else always response 2.

G.5.4.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure, and

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b) FAIL in any other case.

G.5.5 PICC reaction on NAD

G.5.5.1 Scope

This test is to determine the reaction of the PICC to NAD coding according to ISO/IEC 14443-4:2018, 7.2.2.3.

G.5.5.2 Procedure

For each of the scenarios described in Table G.71, Table G.72 and Table G.73, perform the following steps:

Activate the PICC as described in clause PICC activation process G.5.1.2, use CID = 0 and FSDI = 0.

For each step in the scenario do:

a) Send the command as described in the PICC-test-apparatus column.

b) Check that the PICC response matches the one of the PICC column.

Let n be an arbitrary value of a valid NAD with b4 and b8 set to (0)b.

Table G.71 — Scenario G.63: NAD on I-block (for PICCs supporting NAD)

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1), NAD = n)	→	
		←	$I(0)_0$(TEST_RESPONSE1(1), containing NAD)

Table G.72 — Scenario G.64: NAD on chained I-block (for PICCs supporting NAD)

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND2(3), NAD = n)	→	
		←	$I(1)_0$(TEST_RESPONSE2(3)$_1$, containing NAD)
2	$R(ACK)_1$	→	
		←	$I(1)_1$(TEST_RESPONSE2(3)$_2$, not containing NAD)

Table G.73 — Scenario G.65: NAD on I-block (for PICCs not supporting NAD)

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1), NAD = n)	→	
		←	Mute

G.5.5.3 Test report

The test is:

a) N/A when the scenario is not applicable for the PICC,

b) PASS when the scenario is applicable for the PICC and only when the PICC's response is as indicated in the procedure, and

c) FAIL in any other case.

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G.5.6 PICC reaction on S(PARAMETERS) blocks

G.5.6.1 Scope

This test is to determine the behaviour of the PICC according to ISO/IEC 14443-4:2018, 7.6.1. This test uses implementations of the protocol scenarios of ISO/IEC 14443-4:2018, B.2.6.

G.5.6.2 Procedure

For each of the scenarios described in Table G.74 to Table G.77, perform the following steps:

a) Activate the PICC as described in G.5.1.2, use CID = 0.

b) For each step in the scenario do:

   1) Send the command as described in the PICC-test-apparatus column.

   2) Check that the PICC response matches the one of the PICC column. If the PICC does not support S(PARAMETERS), the PICC shall stay Mute on every S(PARAMETER) request.

c) End for.

Table G.74 — Scenario G.67: Exchange of additional parameters

Step	PICC-test-apparatus		PICC
1	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
2	S(PARAMETERS) tag 'A0', length '00', value not present	→	
		←	S(PARAMETERS)[a]
3	$I(0)_1$(TEST_COMMAND1(1))	→	
		←	$I(0)_1$(TEST_RESPONSE1(1))
[a] If the PICC does not support S(PARAMETERS), it shall stay Mute.			

Table G.75 — Scenario G.68: Exchange of additional parameters

Step	PICC-test-apparatus		PICC
1	S(PARAMETERS) tag 'A0', length '00', value not present	→	
		←	S(PARAMETERS)[a]
2	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
[a] If the PICC does not support S(PARAMETERS), it shall stay Mute.			

Table G.76 — Scenario G.69: Exchange of additional parameters

Step	PICC-test-apparatus		PICC
1	S(PARAMETERS) tag 'A0', length '00', value not present	→	
		←	S(PARAMETERS)[a]
2	S(PARAMETERS) tag 'A0', length '00', value not present	→	
		←	S(PARAMETERS)[a]
3	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))
[a] If the PICC does not support S(PARAMETERS), it shall stay Mute.			

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Table G.77 — Scenario G.70: Exchange of additional parameters

Step	PICC-test-apparatus		PICC
1	S(PARAMETERS, ~CRC)	→	
		←	Mute
2	S(PARAMETERS) tag 'A0', length '00', value not present	→	
		←	S(PARAMETERS)[a]
3	$I(0)_0$(TEST_COMMAND1(1))	→	
		←	$I(0)_0$(TEST_RESPONSE1(1))

[a] If the PICC does not support S(PARAMETERS), it shall stay Mute.

G.5.6.3 Test report

The test is:

a) PASS only when the PICC responds as indicated in the procedure, and

b) FAIL in any other case.

G.5.7 PICC supporting Type A and Type B

G.5.7.1 Purpose

This test checks that, if the PICC supports Type A and Type B, then it stays locked in the communication signal interface of the first processed Request command until POWER-OFF state (after Answer to Request of one communication signal interface, the other communication signal interface is disabled until the PICC enters POWER-OFF state).

G.5.7.2 Conditions

The PICC-test-apparatus shall be used.

G.5.7.3 Procedure

Perform the following steps:

a) Place the PICC into the test position of the PICC-test-apparatus.

b) Switch the PICC-test-apparatus RF operating field on and wait at least 5 ms.

c) Send a WUPA command and check there is a valid PICC response.

d) Keep the PICC-test-apparatus RF field on for more than 1 s.

e) Send a sequence of 10 WUPB commands and check there is no PICC response.

f) Switch the RF operating field off for a minimum time for resetting a PICC (see ISO/IEC 14443-3:2018, 5.2.4)

g) Switch the PICC-test-apparatus RF operating field on and wait at least 5 ms.

h) Send a WUPB command and check there is a valid PICC response.

i) Keep the PICC-test-apparatus RF field on for more than 1 s.

j) Send a sequence of 10 WUPA commands and check there is no PICC response.

G.5.7.4 Test report

The test result is PASS if all steps of the procedure succeed, otherwise the test result is FAIL.

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G.6 Reported results

The results of the tests shall be reported in Table G.78 to Table G.82.

Table G.78 — Type A specific timing table

No	Parameter		Reference	Measured values [$1/f_c$]		Test result PASS or FAIL or N/A
				Min	Max	
1	Frame delay time PCD to PICC (for REQA, WUPA, ANTICOLLISION and SELECT commands)		ISO/IEC 14443-3:2018, 6.2.1.1			
2	Activation frame waiting time (for RATS command and PPS request)		ISO/IEC 14443-4:2018, 5.6 ISO/IEC 14443-3:2018, 6.2.1.1			
3	Frame waiting time (for S(DESELECT) and S(PARAMETERS) blocks)		ISO/IEC 14443-4:2018, 7.3 ISO/IEC 14443-4:2018, 8.1 ISO/IEC 14443-3:2018, 6.2.1.1			
4	Frame delay time PCD to PICC (for frames other than in previous rows)		ISO/IEC 14443-4:2018, 7.3 ISO/IEC 14443-3:2018, 6.2.1.1	—	—	—
	PCD to PICC bit rate	**PICC to PCD bit rate**		—	—	—
	$f_c/128$	$f_c/128$		a	a	
	$f_c/64$			a	a	
	$f_c/32$			a	a	
	$f_c/16$			a	a	
	$f_c/128$ or $f_c/64$ or $f_c/32$ or $f_c/16$ or $f_c/8$ or $f_c/4$ or $f_c/2$ or $3f_c/4$ or $3f_c/2$ or $2f_c$	$f_c/64$ or $f_c/32$ or $f_c/16$ or $f_c/8$ or $f_c/4$ or $f_c/2$				
5	Start of communication[b]		ISO/IEC 14443-2:2020, 8.2.6.2			

[a] PICC response shall conform with ISO/IEC 14443-3:2018, 6.2.1.1. The integer value n corresponding to the measured value shall be additionally indicated.

[b] Start of communication concerns only PICC to PCD bit rates higher than $f_c/128$.

Table G.79 — Type B specific timing table

No	Parameter	Reference	Measured values [etu] or [$1/f_s$] or [$1/f_c$] depending on the requirements		Test result PASS or FAIL or N/A
			Min	Max	
1	SOF low	ISO/IEC 14443-3:2018, 7.1.4			
2	SOF high	ISO/IEC 14443-3:2018, 7.1.4			
3	EOF low	ISO/IEC 14443-3:2018, 7.1.5			
4	EGT PICC to PCD	ISO/IEC 14443-3:2018, 7.1.2			
5	TR0 for ATQB	ISO/IEC 14443-3:2018, 7.1.6, ISO/IEC 14443-3:2018, 7.10.3			
6	TR1 for ATQB	ISO/IEC 14443-3:2018, 7.1.6, ISO/IEC 14443-3:2018, 7.10.3			
7	TR0 except for ATQB and S(DESELECT) response	ISO/IEC 14443-3:2018, 7.1.6, ISO/IEC 14443-3:2018, 7.10.3			

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Table G.79 *(continued)*

No	Parameter	Reference	Measured values [etu] or [$1/f_s$] or [$1/f_c$] depending on the requirements		Test result PASS or FAIL or N/A
			Min	Max	
8	TR1 not for ATQB	ISO/IEC 14443-3:2018, 7.1.6, ISO/IEC 14443-3:2018, 7.10.3			
9	f_s to OFF	ISO/IEC 14443-3:2018, 7.1.7			
10	Deactivation frame waiting time (TR0+TR1)	ISO/IEC 14443-3:2018, 7.1.6, ISO/IEC 14443-4:2018, 8.1			

Table G.80 — Reported results for Type A specific test methods

Test method from ISO/IEC 10373-6		Scenario numbers	Test result
Clause	Parameter	ISO/IEC 10373-6	PASS or FAIL or N/A
G.3.2	Polling	Scenario G.1	
G.3.3	Testing of the PICC Type A state transitions	Scenario G.2	
		Scenario G.3	
		Scenario G.4	
		Scenario G.5	
		Scenario G.6	
		Scenario G.7	
		Scenario G.8	
		Scenario G.9	
		Scenario G.10	
		Scenario G.11d	
		Scenario G.12	
G.3.4	Handling of Type A anticollision	Scenario G.13	
G.3.6	Handling of PPS request	Scenario G.17	
		Scenario G.18	
		Scenario G.19	
G.3.7	Handling of FSD	Scenario G.20	
G.3.8	Handling of frame delay time PICC to PCD and SFGT	Scenario G.71	
G.3.9	PICC bit rates capability	Scenario G.72	

Table G.81 — Reported results for Type B specific test methods

Test method from ISO/IEC 10373-6		Scenario numbers	Test result
Clause	Parameter	ISO/IEC 10373-6	PASS or FAIL or N/A
G.4.2	Polling	Scenario G.21	
G.4.3	PICC framing and bit rates capability	Scenario G.22	
G.4.4	Testing of the PICC Type B state transitions	Scenario G.23	
		Scenario G.24	
		Scenario G.25	
		Scenario G.26	

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Table G.81 *(continued)*

Test method from ISO/IEC 10373-6		Scenario numbers	Test result
Clause	**Parameter**	**ISO/IEC 10373-6**	**PASS or FAIL or N/A**
		Scenario G.27	
G.4.5	Handling of Type B anticollision	Scenario G.28	
G.4.6	Handling of ATTRIB	Scenario G.29	
		Scenario G.30	
G.4.7	Handling of Maximum Frame Size	Scenario G.31	
G.4.8	Handling of TR2 and SFGT	Scenario G.73	

Table G.82 — Reported results for test methods for logical operation of the PICC Type A or Type B

Test method from ISO/IEC 10373-6		Scenario numbers	Test result
Clause	**Parameter**	**ISO/IEC 10373-6**	**PASS or FAIL or N/A**
G.5.2	PICC reaction to ISO/IEC 14443-4 scenarios	Scenario G.32	
		Scenario G.33	
		Scenario G.34	
		Scenario G.35	
		Scenario G.36	
		Scenario G.37	
		Scenario G.38	
		Scenario G.39	
		Scenario G.40	
		Scenario G.41	
		Scenario G.42	
		Scenario G.43	
		Scenario G.74	
		Scenario G.44	
		Scenario G.45	
		Scenario G.46	
		Scenario G.47	
		Scenario G.48	
		Scenario G.49	
		Scenario G.50	
		Scenario G.51	
		Scenario G.52	
		Scenario G.53	
		Scenario G.54	
G.5.3	Handling of PICC error detection	Scenario G.55	
		Scenario G.56	
		Scenario G.57	
		Scenario G.75	
G.5.4	PICC reaction on CID	Scenario G.58	

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Table G.82 *(continued)*

Test method from ISO/IEC 10373-6		Scenario numbers	Test result
Clause	**Parameter**	**ISO/IEC 10373-6**	**PASS or FAIL or N/A**
		Scenario G.59	
		Scenario G.60	
		Scenario G.61	
		Scenario G.62	
		Scenario G.66	
G.5.5	PICC reaction on NAD	Scenario G.63	
		Scenario G.64	
		Scenario G.65	
G.5.6	PICC reaction on S(PARAMETERS) blocks	Scenario G.67	
		Scenario G.68	
		Scenario G.69	
		Scenario G.70	
G.5.7	PICC supporting Type A and Type B		

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Annex H
(normative)

Additional PCD test methods

H.1 PCD-test-apparatus and accessories

H.1.1 General

This clause defines the PCD-test-apparatus and test circuits for verifying the operation of the PCD according to ISO/IEC 14443-3 and ISO/IEC 14443-4.

H.1.2 Test method

The ISO/IEC 9646 abstract model is chosen and the local test method is used for the testing of the ISO/IEC 14443 protocol between the IUT and the LT.

H.1.3 PCD-test-apparatus structure

The PCD-test-apparatus consists of two parts (see Figure H.1), the UT (may be a computer with a host interface suitable for the IUT) and the LT.

In some arrangements, for instance when a PCD is embedded in a product, the control of the IUT by the UT may be limited. In such cases some scenarios may not be applicable.

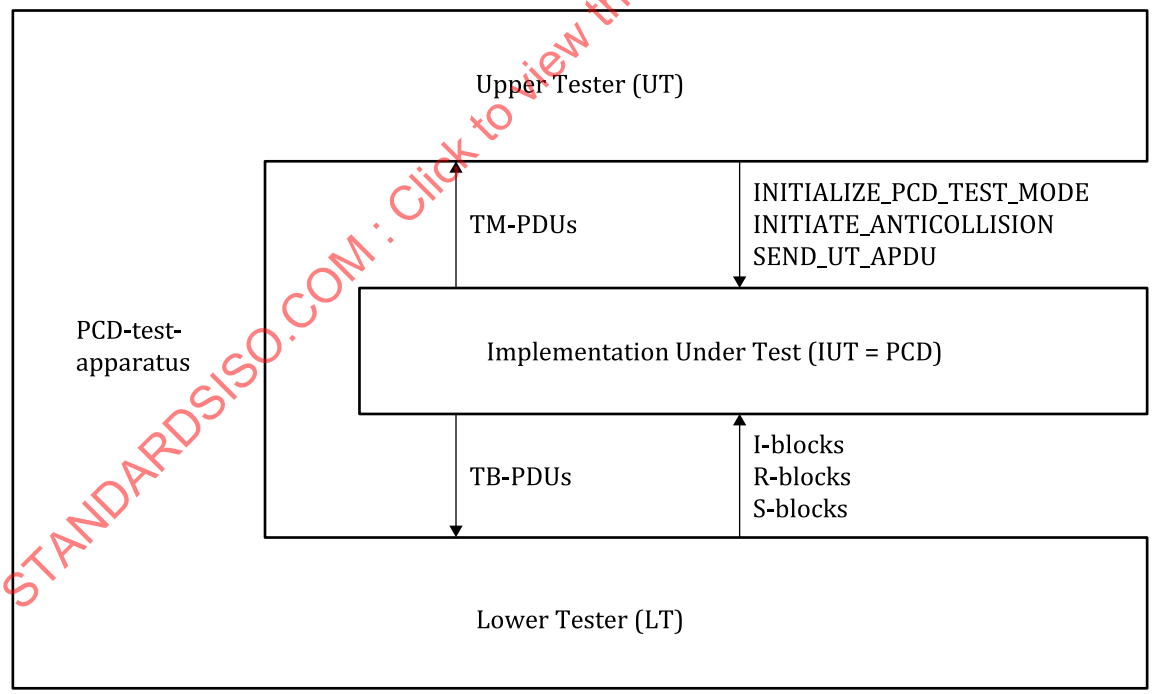


Figure H.1 — Conceptual tester architecture

The LT part of the PCD-test-apparatus includes:

a) a PICC emulation hardware and software device capable of emulating of Type A and Type B protocols;

b) a digital sampling oscilloscope (see 5.2).

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H.1.4 PCD-test-apparatus interface

The UT and the IUT communicate with the TM-PDU. The definition of TM-PDUs is implementation dependent and provided by the IUT manufacturer and shall initiate the actions required in Table H.1.

Table H.1 — Logical interface commands

No.	TM-PDU name	Required IUT action
1	INITIALIZE_PCD_TEST_MODE	Return to Power On state (The IUT is expected to enter to anticollision loop). The IUT returns the result code of its action to the UT.
2	INITIATE_ANTICOLLISION	Initiate anticollision sequence (if the IUT starts the anticollision sequence automatically upon initialize, the sequence can be empty). The IUT returns the result code of its action to the UT.
3	SEND_UT_APDU[ab]	Transmit the UT_APDU through the RF interface to LT and return the IUT result code of its action to the UT. The response from the IUT shall include the answer of LT to the UT_APDU sent.
[a] The size of the command UT_APDU shall not exceed the PCDs internal output buffer size as defined in Table 3.		
[b] The size of the response UT_APDU shall not exceed the PCDs internal input buffer size as defined in Table 3.		

The PCD-test-apparatus shall be able to initialize the IUT utility information provided by the IUT manufacturer over the UT interface and to configure itself to perform the necessary procedures, protocols and analysis over its LT interface.

H.1.5 Emulating the I/O protocol

The PCD-test-apparatus at its LT interface shall be able to emulate the protocol Type A and Type B and PICC applications, which are required to run the scenario. The LT shall be able to break the transmitted packets into chained blocks with the required length.

It shall be possible to configure the LT to simulate different options:

a) NAD and CID configuration;

b) frame size, bit rates and any other parameter as required for the implementation of the test methods.

H.1.6 Generating the I/O character timing in transmission mode

The PCD-test-apparatus at its LT interface shall be able to generate the I/O bit stream according to ISO/IEC 14443-3. Timing parameters: start bit duration, Extra Guard Time EGT (Type B only), bit duration, frame delay time, start of frame width and end of frame width shall be configurable.

For the purpose of tests of Type A, the LT shall be capable of simulating a bit collision at a selected bit position(s).

H.1.7 Measuring and monitoring the RF I/O protocol

H.1.7.1 Timing measurements

The PCD-test-apparatus shall continuously monitor the following frame format and timing values:

a) for PCD Type A:

   1) frame delay time PICC to PCD (see ISO/IEC 14443-3:2018, 6.2.1.2);

   2) frame formats (see ISO/IEC 14443-3:2018, 6.2.3);

b) for PCD Type B:

   1) character, frame format and timing (see ISO/IEC 14443-3:2018, 7.1).

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A test shall be FAIL and the IUT shall be declared non-conformant in case one of the listed timing constraints is violated.

H.1.7.2 Timing measurement report

Fill Table H.36 for Type A and Table H.37 for Type B with the measured timing values.

H.1.8 Protocol analysis

The PCD-test-apparatus shall be able to analyse the I/O-bit stream at its LT interface in accordance with protocol Type A and Type B as specified in ISO/IEC 14443-3 and ISO/IEC 14443-4 and extract the logical data flow for further protocol analysis.

H.1.9 Protocol activation procedure

H.1.9.1 Activation procedure for anticollision test methods

Activate the LT by the following sequence:

a) Configure the LT to emulate the Type A or Type B protocol.

b) The UT sends INITIALIZE_PCD_TEST_MODE TM-PDU to the PCD.

c) The UT sends INITIATE_ANTICOLLISION TM-PDU to the PCD.

H.1.9.2 Activation procedure for Type A protocol test methods

Activate the LT by the following sequence:

a) Configure the LT to emulate the Type A protocol.

b) The UT sends INITIALIZE_PCD_TEST_MODE TM-PDU to the PCD.

c) The UT sends INITIATE_ANTICOLLISION TM-PDU to the PCD. The PCD shall apply the anticollision sequence as defined in ISO/IEC 14443-3:2018, Clause 6 (request, anticollision loop and select). The PCD shall apply the protocol activation sequence as defined in ISO/IEC 14443-4:2018, Clause 5.

d) The PCD reports to the UT the result of the activation procedure.

H.1.9.3 Activation procedure for Type B protocol test methods

Activate the LT by the following sequence:

a) Configure the LT to emulate the Type B protocol.

b) The UT sends INITIALIZE_PCD_TEST_MODE TM-PDU to the PCD.

c) The UT sends INITIATE_ANTICOLLISION TM-PDU to the PCD. The PCD shall apply the anticollision sequence as defined in ISO/IEC 14443-3:2018, Clause 7.

d) The PCD reports to the UT the result of the activation procedure.

H.1.10 Scenario

H.1.10.1 Description

Testing of the PCD as defined in this document requires a scenario to be executed. This scenario is a "typical protocol and application specific communication", dependent on the protocol and application specific functionality foreseen for the normal use of and implemented in the PCD.

The typical scenario is the set of command TM-PDUs defined in H.1.4.

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The scenario shall be defined by the entity carrying out these tests and shall be documented with the test results. The scenario shall encompass a representative subset or, if practical, the full functionality of the PCD expected to be utilized during normal use.

The UT_APDU to be sent may be one from the following:

a) UT_TEST_COMMAND1, decided by the PCD-test-apparatus, specifies the default instruction for scenarios not needing PCD chaining. (In case PCD decides anyway to chain, the scenario should be adapted accordingly by the test laboratory);

b) UT_TEST_COMMAND2, decided by the PCD-test-apparatus, specifies the default instruction for scenarios dealing with PCD chaining.

H.1.10.2 Scenario example

The typical scenario may be as follows:

```
INITIALIZE_PCD_TEST_MODE
INITIATE_ANTICOLLISION
SEND_UT_APDU (UT_TEST_COMMAND1)
SEND_UT_APDU (UT_TEST_COMMAND2)
….
```

H.1.11 UT, LT and PCD behaviour

The following items summarize the behaviour of the UT, the LT and the PCD:

a) The UT runs the activation procedure as defined in H.1.9.

b) If the activation procedure went wrong, the PCD goes to exception processing. This exception processing may include reporting the error to the UT.

c) In case of anticollision test methods, the PCD-test-apparatus ends the test at this point. For protocol test methods the UT continues to the next step.

d) The UT sends the first command UT_APDU to the PCD.

e) The PCD is expected to transfer this command UT_APDU to the LT using TB-PDUs. The PCD splits the current UT_APDU into the appropriate TB-PDUs, sends the first block to the LT and awaits the response block. The PCD manages communication blocks according to ISO/IEC 14443-4, which may also include S(PARAMETERS) exchange.

f) The command UT_APDU is received by the LT. The LT sends the response UT_APDU to the PCD. The LT manages communication blocks (TB-PDUs) according to ISO/IEC 14443-4 (the LT may use chaining mechanism at any time even if not mandated by either PCD or PICC maximum frame size). The PCD is expected to transfer response UT_APDU, received from the LT, back to the UT.

g) If the command failed at protocol level (i.e. error detected by the PCD), the PCD goes to exception processing. Exception processing may include error reporting to the UT.

h) If the command succeeded, the PCD reports the UT about successful result. In this case, if the scenario defines additional UT_APDU to be sent to the LT, the UT sends the next UT_APDU to the PCD. This loop continues until the last test UT_APDU is sent.

H.1.12 Relationship of test methods versus base standard requirement

All tests in Table H.2, Table H.3 and Table H.4 shall be executed and their results reported in the relevant tables in H.6.

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Table H.2 — Type A specific test methods

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	**Name**	**Base standard**	**Clause**
H.2.1	Frame delay time PICC to PCD	ISO/IEC 14443-3:2018	6.2.1.2
H.2.2	Request Guard Time	ISO/IEC 14443-3:2018	6.2.2
H.2.3	Handling of bit collision during ATQA	ISO/IEC 14443-3:2018	6.5.2
H.2.4	Handling of anticollision loop	ISO/IEC 14443-3:2018	6.5.3
H.2.5	Handling of RATS and ATS	ISO/IEC 14443-4:2018	5.7.1.1
H.2.6	Handling of PPS response	ISO/IEC 14443-4:2018	5.7.2.1
H.2.7	Frame size selection mechanism	ISO/IEC 14443-4:2018	5.3.3
H.2.8	Handling of Start-up Frame Guard Time	ISO/IEC 14443-4:2018	5.3.5
H.2.9	Handling of the CID during activation by the PCD	ISO/IEC 14443-4:2018	5.7.3
H.2.10	Handling of parity bit	ISO/IEC 14443-3:2018	6.2.3.2

Table H.3 — Type B specific test methods

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	**Name**	**Base standard**	**Clause**
H.3.2	Frame size selection mechanism	ISO/IEC 14443-3:2018	7.9
H.3.3	Handling of the CID during activation by the PCD	ISO/IEC 14443-3:2018	7.10
H.3.4	Frame delay time PICC to PCD (TR2)	ISO/IEC 14443-3:2018	7.9.4.4
H.3.5	Handling of Start-up Frame Guard Time	ISO/IEC 14443-3:2018	7.9.4.7
H.3.6	Type B PCD framing tests	ISO/IEC 14443-3:2018	7.1
H.3.7	Handling of Protocol_Type RFU value	ISO/IEC 14443-3:2018	7.9.4.4

Table H.4 — Test methods for logical operation

Test method from ISO/IEC 10373-6		Corresponding requirement	
Clause	**Name**	**Base standard**	**Clause**
H.4.2	Handling of polling	ISO/IEC 14443-3:2018	Clause 5
H.4.3	Reaction of the PCD to request for waiting time extension	ISO/IEC 14443-4:2018	7.4
H.4.4	Error detection and recovery	ISO/IEC 14443-4:2018	7.6.7
H.4.5	Handling of NAD during chaining	ISO/IEC 14443-4:2018	7.2.2.3

H.2 Type A specific test methods

H.2.1 Frame delay time PICC to PCD

H.2.1.1 Scope

The purpose of this test is to determine the timing between a PICC frame and the next PCD frame.

H.2.1.2 Apparatus

See H.2.

H.2.1.3 Procedure

Place the LT into the PCD operating volume.

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During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command.

c) The LT answers with ATQA indicating bit frame anticollision and UID size: single (bits b8 and b7 equal (00)b).

d) The PCD shall send ANTICOLLISION command '93 20' (cascade level 1).

e) The LT answers with UID CL1 (uid0 uid1 uid2 uid3 BCC).

f) The PCD shall send SELECT command '93 70' uid0 uid1 uid2 uid3 BCC CRC_A.

g) The LT answers with SAK indicating that UID is complete (b3 = (0)b) and that PICC is conformant with ISO/IEC 14443-4 (b6 = (1)b).

h) The PCD shall send a valid RATS command.

i) The LT answers with a valid ATS (T0 = '77', TA(1)='77', TB(1) = 'A0', TC(1) = '02', no historical bytes).

j) The PCD may send a PPS request. In that case, the LT answers with a valid PPS response.

k) The PCD may send a S(PARAMETERS) request. In that case, the LT answers with S(PARAMETERS) response.

l) The PCD shall return the result code, in accordance with Table H.1, of its action to the UT.

m) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

n) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

o) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

p) The PCD is expected to transfer the response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

q) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

r) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

s) The LT sends S(WTX) request using any valid WTXM.

t) The PCD shall send S(WTX) response using the same WTXM as in the S(WTX) request. If it does not meet the expected response, end the test at this point.

u) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

v) Measure the time between the last modulation transmitted by the LT and the first pause transmitted by the PCD (see ISO/IEC 14443-3:2018, 6.2.1.2) for each command.

Table H.5 gives part of the procedure as a scenario.

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Table H.5 — Scenario H.27: Frame delay time PICC to PCD

PCD		LT
REQA/WUPA	→	
	←	ATQA (single size UID)
ANTICOLLISION command Level 1 ('93 20')	→	
	←	UID CL1 (uid0 uid1 uid2 uid3 BCC)
SELECT command ('93 70' uid0 uid1 uid2 uid3 BCC CRC_A)	→	
	←	SAK (UID complete, PICC conformant with ISO/IEC 14443-4)
RATS command (e.g.'E0 01' CRC_A)	→	
	←	ATS (T0= '77', TA(1)='77', TB(1)='A0', TC(1)= '02', no historical bytes)
PPS request	→	
	←	PPS response
S(PARAMETERS)	→	
	←	S(PARAMETERS)
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1)
$I(0)_1$(INF = UT_TEST_COMMAND1)	→	
	←	S(WTX) request
S(WTX) response	→	
	←	$I(0)_1$(INF = answer to UT_TEST_COMMAND1)

H.2.1.4 Test report

The test is:

a) PASS only when the PCD's frame delay time PICC to PCD always exceeds the minimum value defined in ISO/IEC 14443-3:2018, 6.2.1.2., and

b) FAIL in any other case.

Fill item 1 of Table H.36 with the minimum measured value of frame delay time PICC to PCD.

H.2.2 Request Guard Time

H.2.2.1 Scope

The purpose of this test is to determine the Request Guard Time of two consecutive REQA/WUPA commands. This test is relevant for PCDs, which send consecutive REQA/WUPA.

H.2.2.2 Apparatus

See H.2.

H.2.2.3 Procedure

Place the LT into the PCD operating volume.

During the following procedure, the RF Input/Receive data shall be continuously monitored and verified correct according to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

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Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command. The LT remains Mute.

c) The LT waits until the PCD sends a valid REQA/WUPA command. The LT remains Mute.

d) Measure the time between the start bits of two consecutive REQA/WUPA (see ISO/IEC 14443-3:2018, 6.2.2).

H.2.2.4 Test report

The test is:

a) PASS only when the PCD's Request Guard Time always exceed the minimum value defined in ISO/IEC°14443-3:2018, 6.2.2, and

b) FAIL in any other case.

Fill item 2 in Table H.36 with the measured value of Request Guard Time.

H.2.3 Handling of bit collision during ATQA

H.2.3.1 Scope

The purpose of this test is to determine the handling of bit collision during ATQA by the PCD.

H.2.3.2 Apparatus

See H.1.

H.2.3.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command.

c) Maintain the LT to answer with ATQA using simulation of the bit collision at bit N (N from 1 up to 16). Collision at a bit causes a collision also in associated parity bit.

H.2.3.4 Test report

The test is:

a) PASS only when the PCD starts the bit frame oriented anticollision loop or resets the operating field, and

b) FAIL in any other case.

H.2.4 Handling of anticollision loop

H.2.4.1 Scope

The purpose of this test is to determine the correct handling of the bit anticollision loop according to ISO/IEC 14443-3:2018, 6.5.3.

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H.2.4.2 Apparatus

See H.1.

H.2.4.3 Procedure

H.2.4.3.1 General

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

H.2.4.3.2 Procedure 1 (single size UID)

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command.

c) The LT answers with ATQA indicating bit frame anticollision and UID size: single (bits b8 and b7 equal (00)b).

d) The PCD shall send ANTICOLLISION command '93 20' (cascade level 1).

e) The LT answers with UID CL1 (uid0 uid1 uid2 uid3 BCC).

f) The PCD shall send SELECT command '93 70' uid0 uid1 uid2 uid3 BCC CRC_A.

g) The LT answers with SAK (cascade bit is cleared, b3 = (0)b), indicating that UID is complete.

h) Repeat the procedure using ATQA = 'FF30' in step c).

i) Repeat the procedure using ATQA = 'FFF0' in step c).

j) Repeat the procedure using uid0 = 'F8' in step e).

Table H.6 gives part of the procedure as a scenario.

Table H.6 — Scenario H.1: Handling of anticollision loop for PICC with single size UID (Procedure 1)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		
		←	ATQA (single size UID)	1
ANTICOLLISION Level 1	ANTICOLLISION command Level 1 ('93 20')	→		
		←	UID CL1 (uid0 uid1 uid2 uid3 BCC)	2
SELECT	SELECT command ('93 70' uid0 uid1 uid2 uid3 BCC CRC_A)	→		
		←	SAK(complete)	3

H.2.4.3.3 Procedure 2 (double size UID)

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command.

c) The LT answers with ATQA indicating bit frame anticollision and UID size: double (bits b8 and b7 equal (01)b).

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d) The PCD shall send ANTICOLLISION command '93 20' (cascade level 1).

e) The LT answers with UID CL1 ('88' uid0 uid1 uid2 BCC).

f) The PCD shall send SELECT command '93 70 88' uid0 uid1 uid2 BCC CRC_A.

g) The LT answers with SAK (cascade bit is set, b3 = (1)b).

h) The PCD shall increase the cascade level and shall send ANTICOLLISION command '95 20' (cascade level 2).

i) The LT answers with UID CL2 (uid3 uid4 uid5 uid6 BCC).

j) The PCD shall send SELECT command '95 70' uid3 uid4 uid5 uid6 BCC CRC_A.

k) The LT answers with SAK (cascade bit is cleared, b3 = (0)b), indicating that UID is complete.

l) Repeat the procedure using ATQA = 'FF70' in step c).

m) Repeat the procedure using ATQA = 'FFF0' in step c).

Table H.7 gives part of the procedure as a scenario.

Table H.7 — Scenario H.2: Handling of anticollision loop for PICC with double size UID (Procedure 2)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		
		←	ATQA (double size UID)	1
ANTICOLLISION Level 1	ANTICOLLISION command Level 1 ('93 20')	→		
		←	UID CL1 ('88' uid0 uid1 uid2 BCC)	2
SELECT	SELECT command ('93 70 88' uid0 uid1 uid2 BCC CRC_A)	→		
		←	SAK(cascade)	3
ANTICOLLISION Level 2	ANTICOLLISION command Level 2 ('95 20')	→		
		←	UID CL2 (uid3 uid4 uid5 uid6 BCC)	4
SELECT	SELECT command ('95 70' uid3 uid4 uid5 uid6 BCC CRC_A)	→		
		←	SAK(complete)	5

H.2.4.3.4 Procedure 3 (triple size UID)

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command.

c) The LT answers with ATQA indicating bit frame anticollision and UID size: triple (bits b8 and b7 equal (10)b).

d) The PCD shall send ANTICOLLISION command '93 20' (cascade level 1).

e) The LT answers with UID CL1 ('88' uid0 uid1 uid2 BCC).

f) The PCD shall send SELECT command '93 70 88' uid0 uid1 uid2 BCC CRC_A.

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g) The LT answers with SAK (cascade bit is set, b3 = (1)b).

h) The PCD shall increase the cascade level and shall send ANTICOLLISION command '95 20' (cascade level 2).

i) The LT answers with UID CL2 ('88' uid3 uid4 uid5 BCC).

j) The PCD shall send SELECT command '95 70 88' uid3 uid4 uid5 BCC CRC_A.

k) The LT answers with SAK (cascade bit is set, b3 = (1)b).

l) The PCD shall increase the cascade level and shall send ANTICOLLISION command '97 20' (cascade level 3).

m) The LT answers with UID CL3 (uid6 uid7 uid8 uid9 BCC).

n) The PCD shall send SELECT command '97 70' uid6 uid7 uid8 uid9 BCC CRC_A.

o) The LT answers with SAK (cascade bit is cleared, b3 = (0)b), indicating that UID is complete.

p) Repeat the procedure using ATQA = 'FFB0' in step c).

q) Repeat the procedure using ATQA = 'FFF0' in step c).

Table H.8 gives part of the procedure as a scenario.

Table H.8 — Scenario H.3: Handling of anticollision loop for PICC with triple size UID (Procedure 3)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		
		←	ATQA (triple size UID)	1
ANTICOLLISION Level 1	ANTICOLLISION command Level 1 ('93 20')	→		
		←	UID CL1 ('88' uid0 uid1 uid2 BCC)	2
SELECT	SELECT command ('93 70 88' uid0 uid1 uid2 BCC CRC_A)	→		3
		←	SAK(cascade)	
ANTICOLLISION Level 2	ANTICOLLISION command Level 2 ('95 20')	→		
		←	UID CL2 ('88' uid3 uid4 uid5 BCC)	4
SELECT	SELECT command ('95 70 88' uid3 uid4 uid5 BCC CRC_A)	→		
		←	SAK(cascade)	5
ANTICOLLISION Level 3	ANTICOLLISION command Level 3 ('97 20')	→		
		←	UID CL3 (uid6 uid7 uid8 uid9 BCC)	6
SELECT	SELECT command ('97 70' uid6 uid7 uid8 uid9 BCC CRC_A)	→		
		←	SAK(complete)	7

H.2.4.3.5 Procedure 4 (full bitwise anticollision, single size UID)

This procedure is only applicable to PCDs supporting Type A collision resolution (see Table 3).

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Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA or WUPA command.

c) The LT answers with ATQA indicating bit frame anticollision and UID size: single (bits b8 and b7 equal (00)b).

d) The PCD shall send ANTICOLLISION command: '93 20'.

e) The LT answers by a stream of 40 bits by emulating a collision on every bit, including parity bits.

f) Repeat the steps g) to h) for values k from 1 to 31.

g) The PCD shall send ANTICOLLISION command: '93' NVB $UIDTX_1$[[1..k]], where $UIDTX_1$[[1..k–1]] either is empty (i.e. k = 1) or contains the value already known by the PCD and $UIDTX_1$[[k]] is an arbitrary bit selected by the PCD.

h) The LT answers by a stream of 40 minus k bits by emulating a collision on every bit, including parity bits.

i) The PCD may optionally send ANTICOLLISION command: '93 60' $UIDTX_1$[[1..32]]. In this case the LT answers with BCC.

NOTE This optional ANTICOLLISON command does not change the Stage number.

j) The PCD shall send SELECT command '93 70' $UIDTX_1$[[1..32]] BCC CRC_A. Note that the PCD has to calculate the BCC if it has not run the optional step i).

k) The LT answers with SAK (cascade bit is cleared, b3 = (0)b), indicating that UID is complete.

Table H.9 gives part of the procedure as a scenario.

Table H.9 — Scenario H.4: Handling of full bitwise anticollision loop for PICC (Procedure 4)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		
		←	ATQA (single size UID)	1
ANTICOLLISION	ANTICOLLISION command ('93 20')	→		
		←	40 bits full collision frame	2
ANTICOLLISION (k bits $UID_{PARTIAL}$) 1 ≤ k ≤ 31	ANTICOLLISION command ('93' NVB $UIDTX_1$[[1..k]])	→		
		←	40 minus k bits collision frame	k+2
OPTIONAL ANTICOLLISION (32 bits $UID_{PARTIAL}$)	ANTICOLLISION command ('93 60' $UIDTX_1$[[1..32]])	→		
		←	(BCC)	
SELECT	SELECT command ('93 70' $UIDTX_1$[[1..32]] BCC CRC_A)	→		
		←	SAK(complete)	34

H.2.4.3.6 Procedure 5 (detection of full bitwise anticollision loop for PICC)

This procedure is only applicable to PCDs not supporting Type A collision resolution (see Table 3).

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command

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c) The LT answers with ATQA indicating bit frame anticollision and UID size: single (bits b8 and b7 equal (00)b).

d) The PCD shall send ANTICOLLISION command: '93 20'.

e) The LT answers by a stream of 40 bits by emulating a collision on every bit, including parity bits.

f) The PCD shall reset the operating field.

Table H.10 gives part of the procedure as a scenario.

Table H.10 — Scenario H.34: Detection of full bitwise anticollision loop for PICC (Procedure 5)

Test	PCD		LT	Stage
REQA/WUPA	REQA/WUPA	→		
		←	ATQA (single size UID)	1
ANTICOLLISION	ANTICOLLISION command ('93 20')	→		
		←	40 bits full collision frame	2
RESET	Reset of the operating field	→		

H.2.4.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches each applicable procedure expected scenario, and

b) FAIL in any other case.

H.2.5 Handling of RATS and ATS

H.2.5.1 Scope

The purpose of this test is to determine the handling of RATS and ATS by the PCD according to ISO/IEC 14443-4:2018, 5.7.1.1.

H.2.5.2 Apparatus

See H.1.

H.2.5.3 Procedure

H.2.5.3.1 General

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

NOTE 1 Procedure 1 (Scenario H.5: Handling of RATS and ATS), which was defined in former editions of this document, is no longer present.

NOTE 2 Procedure 3 (Scenario H.7: Handling of RATS and ATS), which was defined in former editions of this document, is no longer present.

H.2.5.3.2 Procedure 2

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT answers relevant anticollision messages and waits until the PCD sends a valid RATS command.

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c) The LT answers with a valid ATS without TA byte.

d) The PCD shall return the result code, in accordance with Table H.1, of its action to the UT.

e) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

f) The PCD is expected to send any I-block (including empty) to the LT, possibly after PICC presence check sequences.

Table H.11 gives part of the procedure as a scenario.

Table H.11 — Scenario H.6: Handling of RATS and ATS, Procedure 2

Test	PCD		LT
Correct ATS	RATS command (e.g.'E0 01' CRC_A)	→	
		←	ATS
Continue operation	Any I-block (including empty)	→	

H.2.5.3.3 Procedure 4

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command.

c) The LT answers with ATQA indicating bit frame anticollision and UID size: single (bits b8 and b7 equal (00)b) and proprietary bits b12 to b9 set to (0000)b.

d) The PCD shall send ANTICOLLISION command '93 20' (cascade level 1).

e) The LT answers with UID CL1 (uid0 uid1 uid2 uid3 BCC).

f) The PCD shall send SELECT command '93 70' uid0 uid1 uid2 uid3 BCC CRC_A.

g) The LT answers with SAK (b3 = (0)b, b6=(1)b, all other bits are set to (0)b).

h) The PCD shall send a valid RATS command.

i) Repeat the procedure using SAK (b3 = (0)b, b6=(1)b, all other bits are set to (1)b) at step g) and using ATQA with proprietary bits b12 to b9 set to (1111)b at step a).

Table H.12 gives part of the procedure as a scenario.

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Table H.12 — Scenario H.30: Handling of RATS and ATS, Procedure 4

PCD		LT
REQA/WUPA	→	
	←	ATQA (single size UID, proprietary bits b12 to b9 set to (0)b) or ATQA (single size UID, proprietary bits b12 to b9 set to (1)b)[a]
ANTICOLLISION command Level 1 ('93 20')	→	
	←	UID CL1 (uid0 uid1 uid2 uid3 BCC)
SELECT command ('93 70' uid0 uid1 uid2 uid3 BCC CRC_A)	→	
	←	SAK(b3=(0)b, b6=(1)b, all other bits are set to (0)b) or SAK(b3=(0)b, b6=(1)b, all other bits are set to (1)b)[a]
RATS command (e.g.'E0 01' CRC_A)[b]	→	

[a] Determined in step i).

[b] The PCD may send "proprietary" commands before sending RATS.

H.2.5.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches each procedure expected scenario, and

b) FAIL in any other case.

H.2.6 Handling of PPS response

Handling of PPS response is tested in I.3.1.

Scenario H.8: Handling of PPS request and response, Procedure 1

This scenario, which was defined in former editions of this document, is no longer present.

Scenario H.9: Handling of PPS request and response, Procedure 2

This scenario, which was defined in former editions of this document, is no longer present.

H.2.7 Frame size selection mechanism

H.2.7.1 Scope

The purpose of this test is to verify the correct handling of transmitted frame size and RFU values in T0.

The transmitted frames shall not be longer than indicated by FSCI.

This test shall be executed only for FSC values less than the PCD's internal input buffer size (see Table 3) and at least for FSCI set to '0', 'D', 'E', 'F' and FSCI set to the coding which results in the largest FSC value below the PCD's internal input buffer size.

H.2.7.2 Apparatus

See H.1.

H.2.7.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

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Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT answers relevant anticollision messages and waits until the PCD sends a valid RATS command.

c) The LT answers with a valid ATS. For the purpose of this test, the LT returns format byte T0 equal '70' (see ISO/IEC 14443-4:2018, 5.3.3). In case there is a PPS request the LT will answer it before continuing with the next step.

d) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND2) to the PCD where the data length shall be more than the maximum size of a frame accepted by the LT.

e) The PCD shall send the following $I(1)_0$ block with maximum length of in accordance with FSCI.

Table H.13 gives part of the procedure as a scenario.

Table H.13 — Scenario H.10: Frame size selection mechanism

PCD		LT
RATS command (e.g. 'E0 01' CRC_A)	→	
	←	ATS, T0 = '70'
Optional PPS request is possible and would be processed by the LT before the I-block	→	
	←	PPS response in case of PPS request
$I(1)_0$ (maximum length in accordance with FSCI)	→	

H.2.7.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario for all tested FSCI values, and

b) FAIL in any other case.

H.2.8 Handling of Start-up Frame Guard Time

H.2.8.1 Scope

The purpose of this test is to determine the PCD transmission timing according to ISO/IEC 14443-4:2018, 5.3.5.

This test shall be executed for at least SFGI set to 0, 1, 14 and 15.

H.2.8.2 Apparatus

See H.1.

H.2.8.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT answers relevant anticollision messages and waits until the PCD sends a valid RATS command.

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c) The LT answers with a valid ATS.

d) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

e) The PCD shall send next block or a PPS request after a minimum delay of SFGT.

Table H.14 gives part of the procedure as a scenario.

Table H.14 — Scenario H.11: Start-up Frame Guard Time mechanism

PCD		LT
RATS command (e.g. 'E0 01' CRC_A)	→	
	←	ATS
PPS Request or next block, sent not earlier than SFGT	→	

H.2.8.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario for all tested SFGI values, and

b) FAIL in any other case.

Fill item 3 of Table H.36 with the measured values of the delay before the PCD next block or PPS request.

H.2.9 Handling of the CID during activation by the PCD

H.2.9.1 Scope

The purpose of this test is to determine the handling of the CID according to ISO/IEC 14443-4:2018, 5.7.3. This test shall be executed for at least CID set to 0, 1 and 14 if the CID can be chosen by the UT. Else, only the CID chosen by the PCD shall be used.

H.2.9.2 Apparatus

See H.1.

H.2.9.3 Procedure

Use the sequence a) to c) to put the PCD into the state required by this test.

a) Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

b) The UT performs the activation procedure according to H.1.9.1.

c) The LT answers relevant anticollision messages and waits until the PCD sends the RATS. The LT answers with ATS.

For each test from the scenario described in Table H.15, when supported by the PCD, use the sequence d) to h).

d) Put the PCD into the state required by this test.

e) The LT waits until the PCD applies the command as described in PCD column.

f) The LT answers as described in the LT column.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

h) The PCD is expected to send I-block to the LT applying the condition as described in the PCD column.

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Table H.15 — Scenario H.12: Handling of the CID

Test	PCD		LT
CID not equal to 0 and receive CID is supported	RATS (CID not equal 0)	→	
		←	ATS (CID supported)
	Any valid command using CID	→	
CID not equal to 0 and receive CID is not supported	RATS (CID not equal 0)	→	
		←	ATS (CID not supported)
	Any valid command without CID	→	
CID equal to 0 and receive CID is supported	RATS (CID = 0)	→	
		←	ATS (CID supported)
	Any valid command using CID = 0 or without CID	→	
CID equal to 0 and receive CID is not supported	RATS (CID = 0)	→	
		←	ATS (CID not supported)
	Any valid command without CID	→	
TC(1) RFU values	RATS (CID not equal to 0)	→	
		←	ATS (CID supported with (b8 t0 b3) = (111111)b
	Any valid command using CID	→	

H.2.9.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario, and

b) FAIL in any other case.

H.2.10 Handling of parity bit

H.2.10.1 Scope

The purpose of this test is to determine the behaviour of a PCD in Type A when receiving PICC messages with parity error according to ISO/IEC 14443-3:2018, 6.2.3.2.

H.2.10.2 Apparatus

See H.1.

H.2.10.3 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the protocol activation procedure according to H.1.9.2. Interface byte TA(1) is set to (00000000)b (only bit rate of f_c/128 in both directions).

b) The UT sends the SEND_UT_APDU (UT_TEST_COMMAND1) to the PCD.

c) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

d) The LT sends an erroneous I-block to the PCD with a wrong parity bit.

e) The PCD shall send $R(NAK)_0$.

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f) The LT sends again the erroneous block to the PCD.

g) The PCD either shall send $R(NAK)_0$ or shall send an S(DESELECT) request or shall reset the operating field.

Table H.16 gives part of the procedure as a scenario.

Table H.16 — Scenario H.31: Parity bit error in I-block

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1, wrong parity bit)[a]
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1, wrong parity bit)[a]
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC) or S(DESELECT) or reset of the operating field	→	

[a] The parity error is simulated on the first transmitted byte of the frame by reversing the parity bit.

NOTE There is no test at PICC to PCD bit rates higher than $f_c/128$ as the inverted parity bit of the last byte is considered as End of Communication.

H.2.10.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario, and

b) FAIL in any other case.

H.3 Type B specific test methods

H.3.1 Frame size selection mechanism

H.3.1.1 Scope

NOTE The I/O transmission timing test, which was defined in former editions of this document, is no longer present.

The purpose of this test is to analyse the frame size selection mechanism according to ISO/IEC 14443-3:2018, 7.9.

This test shall be executed only for maximum frame size values less than the PCD's internal input buffer size (see Table 3) and at least for Maximum Frame Size Code set to '0', 'D', 'E', 'F', and the Maximum Frame Size Code coding which results in the largest maximum frame size value below the PCD's internal input buffer size.

H.3.1.2 Apparatus

See H.1.

H.3.1.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

For each of the Maximum Frame Size Code in ATQB parameters, run the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

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b) The LT waits until the PCD sends a valid REQB/WUPB command.

c) The LT answers with ATQB. For the purpose of this test the LT returns in the second protocol info byte (see ISO/IEC 14443-3:2018, 7.9.4) the Maximum Frame Size Code in ATQB parameter and indicates conformance with ISO/IEC 14443-4.

d) The PCD shall send a valid ATTRIB command.

e) The LT sends Answer to ATTRIB.

f) The PCD shall return the result code, in accordance with Table H.1, of its action to the UT.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND2) to the PCD.

h) The PCD shall send an $I(1)_0$ block with its length not exceeding the maximum frame size resulting from the Maximum Frame Size Code in ATQB indicated by the PICC, as shown in the PCD column of Scenario H.13

Table H.17 gives part of the procedure as a scenario.

Table H.17 — Scenario H.13: Frame size selection mechanism

PCD		LT
REQB/WUPB	→	
	←	ATQB
ATTRIB command	→	
	←	Answer to ATTRIB
$I(1)_0$(INF = the first chain includes the first block of UT_TEST_COMMAND2), with its length not exceeding the maximum frame size of the LT.	→	

H.3.1.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario for all tested values of Maximum Frame Size Code in ATQB values, and

b) FAIL in any other case.

H.3.2 Handling of the CID during activation by the PCD

H.3.2.1 Scope

The purpose of this test is to determine the handling of the CID according to ISO/IEC 14443-3 and ISO/IEC 14443-4.

This test shall be executed for at least CID set to 0, 1 and 14 if the CID can be chosen by the UT. Else, only the CID chosen by the PCD shall be used.

H.3.2.2 Apparatus

See H.1.

H.3.2.3 Procedure

H.3.2.3.1 General

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

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H.3.2.3.2 Procedure 1

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends the REQB/WUPB command.

c) The LT sends ATQB with Frame Option bits (b2,b1) equal (00)b. It means: CID and NAD are not supported.

d) The LT waits until the PCD sends the ATTRIB command. The PCD shall send a valid ATTRIB command with Param 4 set to '00'.

e) The LT sends Answer to ATTRIB with CID value equals 0.

f) The PCD shall return the result code, in accordance with Table H.1, of its action to the UT.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

h) The PCD shall send the following I(0 or 1)$_0$ block without NAD and CID.

i) The LT remains MUTE.

j) The PCD shall send at least one R(NAK)$_0$ without NAD and CID.

k) The LT remains MUTE.

l) The PCD either shall send an S(DESELECT) request without NAD and CID or shall reset the operating field.

Table H.18 gives part of the procedure as a scenario.

Table H.18 — Scenario H.14: Handling of the CID, Procedure 1

PCD		LT
REQB/WUPB	→	
	←	ATQB Frame Option Bits (b2,b1) = (00)b
ATTRIB(0, fsdi)	→	
	←	Answer to ATTRIB
I(0 or 1)$_0$ without NAD and CID	→	
	←	Mute
R(NAK)$_0$ without NAD and CID	→	
	←	Mute
Optional R(NAK)$_0$ without NAD and CID	→	
	←	Mute
S(DESELECT) request without NAD and CID or reset of the operating field	→	

H.3.2.3.3 Procedure 2

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends the REQB/WUPB command.

c) The LT sends ATQB with Frame Option bits (b2,b1) equal (01)b. It means: CID is supported and NAD is not supported.

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d) The LT waits until the PCD sends the ATTRIB command. The PCD shall send a valid ATTRIB command, using a CID in the range from 0 to 14.

e) The LT sends Answer to ATTRIB with the CID value used in step d).

f) The PCD shall return the result code, in accordance with Table H.1, of its action to the UT.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

h) The PCD shall send the following $I(0 \text{ or } 1)_0$ block using the same CID value as in step d) or, optionally, using no CID if the value was 0 in step d), and without NAD.

i) The LT remains MUTE.

j) The PCD shall send at least one $R(NAK)_0$ with the same CID value as in step d) or, optionally, using no CID if the value was 0 in step d), and without NAD.

k) The LT remains MUTE.

l) The PCD either shall send S(DESELECT) request with the same CID value as in step d) or, optionally, using no CID if the value was 0 in step d), and without NAD or shall reset the operating field.

Table H.19 gives part of the procedure as a scenario.

Table H.19 — Scenario H.15: Handling of the CID, Procedure 2

PCD		LT
REQB/WUPB	→	
	←	ATQB Frame Option Bits (b2,b1) = (01)b
ATTRIB(CID = 'X', fsdi) with 'X' in the range of 0 to 14	→	
	←	Answer to ATTRIB
$I(0 \text{ or } 1)_0$ with [a] CID = 'X' and without NAD	→ ←	 Mute
$R(NAK)_0$ with [a] CID = 'X' and without NAD	→ ←	 Mute
Optional $R(NAK)_0$ with [a] CID = 'X' and without NAD	→ ←	 Mute
S(DESELECT) request with CID = 'X' and without NAD or reset the operating field	→	

[a] The PCD may optionally send no CID if CID was 0 in the ATTRIB command.

H.3.2.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches each procedure expected scenario, and

b) FAIL in any other case.

H.3.3 Frame delay time PICC to PCD (TR2)

H.3.3.1 Scope

The purpose of this test is to determine the timing between a PICC frame and the next PCD frame according to the minimum TR2 coding as defined in ISO/IEC 14443-3:2018, 7.9.4.4.

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This test shall be executed for all the minimum TR2 values:

a) b3 and b2 of Protocol_Type equal to (00)b;

b) b3 and b2 of Protocol_Type equal to (01)b;

c) b3 and b2 of Protocol_Type equal to (10)b;

d) b3 and b2 of Protocol_Type equal to (11)b.

H.3.3.2 Apparatus

See H.1.

H.3.3.3 Procedure

Place the LT into the PCD operating volume.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQB/WUPB command.

c) The LT answers with a valid ATQB coding the minimum TR2 as expected.

d) The PCD shall send a valid ATTRIB command.

e) The LT sends Answer to ATTRIB.

f) The PCD shall return the result code, in accordance with Table H.1, of its action to the UT.

g) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

h) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

i) The LT sends an I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

j) The PCD is expected to transfer the response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

k) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

l) The LT sends S(WTX) request using any valid WTXM.

m) The PCD shall send S(WTX) response using the same WTXM as in the S(WTX) request. If it does not meet the expected response, end the test at this point.

n) The LT sends an I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

o) Measure the time delay between the PICC EOF start and PCD SOF start (see ISO/IEC 14443-3:2018, 7.1.7) for each command.

Table H.20 gives part of the procedure as a scenario.

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Table H.20 — Scenario H.27: Frame delay time PICC to PCD (TR2)

PCD		LT
REQB/WUPB	→	
	←	ATQB (coding the minimum TR2 as expected)
ATTRIB command	→	
	←	Answer to ATTRIB
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1)
$I(0)_1$(INF = UT_TEST_COMMAND1)	→	
	←	S(WTX) request
S(WTX) response	→	
	←	$I(0)_1$(INF = answer to UT_TEST_COMMAND1)

H.3.3.4 Test report

The test is:

a) PASS only when the PCD's frame delay time PICC to PCD (TR2) always exceed the minimum value defined in ISO/IEC 14443-3:2018, 7.9.4.4, and

b) FAIL in any other case.

Fill item 6 of Table H.37 with the minimum measured value of frame delay time PICC to PCD (TR2).

H.3.4 Handling of Start-up Frame Guard Time

H.3.4.1 Scope

The purpose of this test is to determine the PCD transmission timing according to ISO/IEC 14443-3:2018, 7.9.4.7.

This test shall be executed for at least SFGI set to 0, 1, 14 and 15. The procedure shall be executed setting b4 to b1 of Extended ATQB byte to (1111)b at least once.

This test is applicable only if PCD supports Extended ATQB as described in ISO/IEC 14443-3:2018, 7.9.4.7.

H.3.4.2 Apparatus

See H.1.

H.3.4.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQB/WUPB command (b5 set to (1)b).

c) The LT answers with a valid extended ATQB coding the SFGI as expected.

d) The PCD shall send a valid ATTRIB command.

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e) The LT answers with a valid Answer to ATTRIB.

f) The UT sends the SEND_UT_APDU (UT_TEST_COMMAND1) to the PCD.

g) The PCD shall send the next block after a minimum delay of SFGT.

Table H.21 gives part of the procedure as a scenario.

Table H.21 — Scenario H.33: Handling of Start-up Frame Guard Time

PCD		LT
REQB/WUPB supporting Extended ATQB	→	
	←	Extended ATQB (coding the SFGI as expected)
ATTRIB command	→	
	←	Answer to ATTRIB
Next command (sent not earlier than SFGT)	→	

H.3.4.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario for all tested SFGI values, and

b) FAIL in any other case.

Fill item 7 of Table H.37 with the measured values of the delay before the PCD next block.

H.3.5 Type B PCD framing tests

H.3.5.1 Scope

The purpose of this test is to determine the behaviour of a PCD in Type B when receiving PICC messages according to ISO/IEC 14443-3:2018, 7.1.

H.3.5.2 Apparatus

See H.1.

H.3.5.3 Procedure

This procedure shall be repeated for combinations of PCD to PICC and PICC to PCD bit rates supported and selected by the PCD so that all supported bit rates in each direction are used at least once during the tests.

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

Perform the following steps for each row of Table H.22:

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQB/WUPB command.

c) The LT answers with a valid ATQB after setting the frame parameters of the LT according to Table H.35.

d) The PCD shall send a valid ATTRIB command.

e) The LT sends Answer to ATTRIB.

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f) The PCD shall return the answer to ATTRIB, in accordance with Table H.1, of its action to the UT.

g) The PCD may send an S(PARAMETERS) block to send Bit rates request, possibly after other S(PARAMETERS) exchanges. If not, skip steps h) to j).

h) The LT answers with an S(PARAMETERS) block that includes the framing options provided in Table H.18 and an appropriate combination of bit rates.

i) The PCD may send an S(PARAMETERS) activating bit rates and framing options. If not, skip step j).

j) The LT acknowledges the received S(PARAMETERS) block with an S(PARAMETERS) block response.

k) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

l) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

m) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

n) The PCD is expected to transfer the response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

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Table H.22 — PICC Type B to PCD frame parameters

Test No.	EGT [etu]	SOF low [etu]	SOF high [etu]	EOF [etu]	f_s to OFF [etu]	TR0	TR1	Framing options (b2b1)[a]
1	0	10,5	2,5	10,5	1	$1600/f_c$	$140/f_s$	(00)b
2	0	No SOF if "No SOF required" in ATTRIB from Answer to ATTRIB and following[b]	No SOF if "No SOF required" in ATTRIB from Answer to ATTRIB and following[b]	No EOF if "No EOF required" in ATTRIB from Answer to ATTRIB and following[b]	1	$1600/f_c$	$140/f_s$	(00)b
3	0	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	$2 - 1/f_s$ for $f_c/128$ $2 - 0,5/f_s$ for $f_c/64$ 2 for other	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	0	$1600/f_c$	$140/f_s$	(00)b
4	1,5[c]	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	$2 - 1/f_s$ for $f_c/128$ $2 - 0,5/f_s$ for $f_c/64$ 2 for other	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	$2 + 1/f_s$	$1600/f_c$	$140/f_s$	(00)b
5	0	$11 + 1/f_s$ for $f_c/128$ $11 + 0,5/f_s$ for $f_c/64$ 11 for other	$2 - 1/f_s$ for $f_c/128$ $2 - 0,5/f_s$ for $f_c/64$ 2 for other	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	0	$1600/f_c$	$140/f_s$	(00)b
6	0	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	$3 + 1/f_s$ for $f_c/128$ $3 + 0,5/f_s$ for $f_c/64$ 3 for other	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	0	$1600/f_c$	$140/f_s$	(00)b
7	2,125[c]	$11 + 1/f_s$ for $f_c/128$ $11 + 0,5/f_s$ for $f_c/64$ 11 for other	$3 + 1/f_s$ for $f_c/128$ $3 + 0,5/f_s$ for $f_c/64$ 3 for other	$11 + 1/f_s$ for $f_c/128$ $11 + 0,5/f_s$ for $f_c/64$ 11 for other	$2 + 1/f_s$	$1600/f_c$	$140/f_s$	(00)b
8	0	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	$2 - 1/f_s$ for $f_c/128$ $2 - 0,5/f_s$ for $f_c/64$ 2 for other	$10 - 1/f_s$ for $f_c/128$ $10 - 0,5/f_s$ for $f_c/64$ 10 for other	0	min TR0 $- 16/f_c$[e]	min TR1 $- 1/f_s$[f]	(00)b

[a] Only applicable if selected by the PCD.

[b] Only applicable at a bit rate of $f_c/128$.

[c] Applies to all characters except between the last character and EOF where EGT of 0 will be used.

[d] Applies to all characters and also between the last character and EOF.

[e] min TR0 is defined in ISO/IEC 14443-2:2020, 9.2.6 for ATQB and in ISO/IEC 14443-3:2018, 7.10.3.1 for other frames.

[f] min TR1 is defined in ISO/IEC 14443-2:2020, 9.2.6 for ATQB and in ISO/IEC 14443-3:2018, 7.10.3.2 for other frames.

[g] All RFU bits set to (1)b in the framing options byte.

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Table H.22 *(continued)*

Test No.	EGT [etu]	SOF low [etu]	SOF high [etu]	EOF [etu]	f_s to OFF [etu]	TR0	TR1	Framing options (b2b1)[a]
9	2,12 5[c]	11 + 1/f_s for f_c/128 11 + 0,5/f_s for f_c/64 11 for other	3 + 1/f_s for f_c/128 3 + 0,5/f_s for f_c/64 3 for other	11 + 1/f_s for f_c/128 11 + 0,5/f_s for f_c/64 11 for other	2 + 1/f_s	(256/f_s) × 2^{FWI} − TR1 + 16/f_c	200/f_s	(00)b
10	2,12 5[c]	11 + 1/f_s for f_c/128 11 + 0,5/f_s for f_c/64 11 for other	3 + 1/f_s for f_c/128 3 + 0,5/f_s for f_c/64 3 for other	11 + 1/f_s for f_c/128 11 + 0,5/f_s for f_c/64 11 for other	2 + 1/f_s	(256/f_s) × 2^{FWI} − TR1 + 16/f_c	min TR1 − 1/f_s[f]	(00)b
11	0	10 − 1/f_s for f_c/128 10 − 0,5/f_s for f_c/64 10 for other	2 − 1/f_s for f_c/128 2 − 0,5/f_s for f_c/64 2 for other	10 − 1/f_s for f_c/128 10 − 0,5/f_s for f_c/64 10 for other	0	min TR0 − 16/f_c[e]	200/f_s	(00)b
12	0	No SOF if requested in framing options with S-block	No SOF if requested in framing options with S-block	No EOF if requested in framing options with S-block	0	min TR0 − 16/f_c[e]	min TR1 − 1/f_s[f]	(10)b
13	0	10 − 1/f_s for f_c/128 10 − 0,5/f_s for f_c/64 10 for other	2 − 1/f_s for f_c/128 2 − 0,5/f_s for f_c/64 2 for other	10 − 1/f_s for f_c/128 10 − 0,5/f_s for f_c/64 10 for other	0	min TR0 − 16/f_c[e]	min TR1 − 1/f_s[f]	(01)b
14	0	10,5	2,5	10,5	1	1600/f_c	140/f_s	(00)b[g]

[a] Only applicable if selected by the PCD.

[b] Only applicable at a bit rate of f_c/128.

[c] Applies to all characters except between the last character and EOF where EGT of 0 will be used.

[d] Applies to all characters and also between the last character and EOF.

[e] min TR0 is defined in ISO/IEC 14443-2:2020, 9.2.6 for ATQB and in ISO/IEC 14443-3:2018, 7.10.3.1 for other frames.

[f] min TR1 is defined in ISO/IEC 14443-2:2020, 9.2.6 for ATQB and in ISO/IEC 14443-3:2018, 7.10.3.2 for other frames.

[g] All RFU bits set to (1)b in the framing options byte.

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H.3.5.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario for all tested frame parameters, and

b) FAIL in any other case.

H.3.6 Handling of Protocol_Type RFU value

H.3.6.1 Scope

The purpose of this test is to determine the behaviour of a PCD in Type B when receiving PICC messages containing Protocol_Type with b4 set to (1)b as defined in ISO/IEC 14443-3:2018, 7.9.4.4.

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H.3.6.2 Apparatus

See H.1.

H.3.6.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

Use the following sequence:

a) The UT performs the activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends the REQB/WUPB command.

c) The LT sends ATQB with Protocol_Type bit b4 set to (1)b.

d) The LT checks that the PCD does not continue communicating.

H.3.6.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario, and

b) FAIL in any other case.

H.4 Test method for logical operations of the PCD

H.4.1 General

All test methods described in this subclause, except H.4.2, shall be applied twice, once for Type A signal interface and once for Type B signal interface.

H.4.2 Handling of polling

H.4.2.1 Scope

The purpose of this test is to determine the behaviour of the PCD during polling. The conditions defined in ISO/IEC 14443-3:2018, 5.2.1 shall apply.

H.4.2.2 Apparatus

See H.1.

H.4.2.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

Use the following sequence:

a) The UT performs the protocol activation procedure according to H.1.9.1.

b) The LT waits until the PCD sends a valid REQA/WUPA command and a valid REQB/WUPB command, in any order and repetition.

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H.4.2.4 Test report

a) In case the PCD has committed to poll in order to detect PICCs requiring 5 ms (see Table 3) the test is:

   1) PASS only when the PCD sends at least one REQA/WUPA command (with at least 5 ms of unmodulated operating field before it) and at least one REQB/WUPB command (with at least 5 ms of unmodulated operating field before it), and

   2) FAIL in any other case.

b) Otherwise, the test is:

   1) PASS only when the PCD sends at least one REQA/WUPA command (with unmodulated operating field before it) and at least one REQB/WUPB command (with unmodulated operating field before it), and

   2) FAIL in any other case.

H.4.3 Reaction of the PCD to request for waiting time extension

H.4.3.1 Scope

The purpose of this test is to determine the behaviour of the PCD when the PICC uses a request for a waiting time extension (see ISO/IEC 14443-4:2018, 7.4). The mechanism of maintenance of WTX by the PCD is also tested.

This test shall be executed for the combinations of FWI and WTXM as shown in Table H.23, with TR0 and TR1 set to the default values in the LT for Type B.

Table H.23 — Tested combinations of FWI and WTXM

Combination	FWI	WTXM
1	0	1
2	0	3
3	0	59
4	1	1
5	1	3
6	1	59
7	14	1
8	14	3
9	14	59
10[a]	0	1
11[a]	8	59
13	15	1
14	15	59
15[b]	0	1

[a] (b8,b7) of INF field of S(WTX) request is set to (11)b

[b] (b4) of ADC is set to (1)b

H.4.3.2 Apparatus

See H.1.

H.4.3.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

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During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

The UT performs the protocol activation procedure according to H.1.9.2 for Type A or H.1.9.3 for Type B.

Use the following sequence:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) Set the following bit timing parameters at the LT:

   1) Frame waiting time (FWT): $(256 \times 16/f_c) \times 2^{FWI}$ (see ISO/IEC 14443-4:2018, 7.3)

   2) Extra Guard Time, Type B (EGT): the maximum value the PCD shall accept (see ISO/IEC 14443-3:2018, 7.1.2)

d) Just before FWT expiration, the LT sends S(WTX) request.

e) The PCD shall send S(WTX) response with INF(b6 to b1) = WTXM. If it does not meet the expected response, end the test at this point.

f) Set the following bit timing parameters at the LT:

   1) Temporary frame waiting time (FWT_{TEMP}): WTXM × $(256 \times 16/f_c) \times 2^{FWI}$ (see ISO/IEC 14443-4:2018, 7.3 and 7.4)

   2) Extra Guard Time, Type B (EGT): The maximum value the PCD shall accept (see ISO/IEC 14443-3:2018, 7.1.2)

g) Just before FWT_{TEMP} expiration, the LT sends the answer to the command UT_TEST_COMMAND1 sent in b).

h) The PCD is expected to transfer the response UT_APDU (answer to the command UT_TEST_COMMAND1) back to the UT.

i) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

j) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1. The PCD shall reset the FWT at this point.

k) The LT remains Mute for at least the expected FWT. This fact means FWT timeout for the PCD.

l) The PCD shall send an R(NAK) block only after FWT expires (ISO/IEC 14443-4:2018, 7.6.5.2).

m) Measure and record the time between the end of the PCD frame from step i) and start of PCD frame from step k).

NOTE Scenario H.16, which was defined in former editions of this document, is no longer present.

Table H.24 gives part of the procedure as a scenario.

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Table H.24 — Scenario H.17: PCD reaction to the LT waiting time extension request

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	S(WTX) request (sent just before FWT expiration) (WTXM belongs to the test set)
S(WTX) response	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1) (sent just before FWT_{TEMP} expiration)
$I(0)_1$(INF = UT_TEST_COMMAND1)	→	
	←	Mute
R(NAK)	→	

H.4.3.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches the expected scenario for all combinations of FWI and WTXM values as defined in H.4.3.1.

b) FAIL in any other case, e.g., when the answer to TEST_COMMAND_1 was not sent back to the UT or when the PCD sent the R(NAK) before FWT expired for at least one combination of FWI and WTXM as defined in H.4.3.1.

H.4.4 Error detection and recovery

H.4.4.1 Scope

The purpose of this test is to determine the behaviour of PCD when an error occurs according to ISO/IEC 14443-4:2018, 7.6.7.

NOTE In this subclause and the following subclauses, "erroneous block" is a frame with a wrong CRC.

H.4.4.2 Apparatus

See H.1.

H.4.4.3 Procedure

H.4.4.3.1 General

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

During the following procedure the RF Input/Receive data shall be continuously monitored and verified correct to ISO/IEC 14443-2. All signal transitions (level and timing) as well as the logical content of the communication shall be recorded.

The UT performs the protocol activation procedure according to H.1.9.2 for Type A or H.1.9.3 for Type B.

H.4.4.3.2 Procedure 1 (ISO/IEC 14443-4:2018, Annex B, Scenario 12)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

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c) The LT sends an erroneous I-block to the PCD.

d) The PCD shall send $R(NAK)_0$.

e) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

f) The PCD is expected to transfer the response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

Table H.25 gives part of the procedure as a scenario.

Table H.25 — Scenario H.18: Error detection and recovery of a transmission error by the PCD, Procedure 1

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1, ~CRC)
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1)

H.4.4.3.3 Procedure 2 (ISO/IEC 14443-4:2018, 7.6.5.2, rule 4)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends an erroneous block to the PCD.

d) The PCD shall send $R(NAK)_0$.

e) The LT sends a second erroneous block to the PCD.

f) The PCD either shall send $R(NAK)_0$ or shall send an S(DESELECT) request or shall reset the operating field.

Table H.26 gives part of the procedure as a scenario.

Table H.26 — Scenario H.19: Error detection and recovery of a transmission error by the PCD, Procedure 2

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1, ~ CRC)
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1, ~ CRC)
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC) or S(DESELECT) or reset of the operating field	→	

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H.4.4.3.4 Procedure 3 (ISO/IEC 14443-4:2018, 7.6.5.2, rule 4)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) Maintain the LT Mute.

d) The PCD shall send $R(NAK)_0$ at least once.

Table H.27 gives part of the procedure as a scenario.

Table H.27 — Scenario H.20: Error detection and recovery of a transmission error by the PCD, Procedure 3

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	Mute
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC)	→	
	←	Mute

H.4.4.3.5 Procedure 4 (ISO/IEC 14443-4:2018, 7.6.5.2, rule 7)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends $R(ACK)_0$ (because of infringement of protocol rules by the LT).

d) The PCD either shall send an S(DESELECT) request or shall reset the operating field.

Table H.28 gives part of the procedure as a scenario.

Table H.28 — Scenario H.21: Error detection and recovery of a transmission error by the PCD, Procedure 4

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$R(ACK)_0$ ('AA' CID CRC or 'A2' CRC)[a]
S(DESELECT) request or reset of the operating field	→	

[a] If the PCD block contains a CID, the left option shall be used, else the right option shall be used.

H.4.4.3.6 Procedure 5 (with chaining) (ISO/IEC 14443-4:2018, 7.6.5.2 rule 5, ISO/IEC 14443-4:2018, Annex B, Scenario 23)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT, with the INF field containing the UT_TEST_COMMAND1.

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c) The LT sends the first block $I(1)_0$ of the chain and waits for the PCD response.

d) The PCD shall send $R(ACK)_1$.

e) The LT sends an erroneous block $I(0)_1$ to the PCD.

f) The PCD shall send $R(ACK)_1$.

Table H.29 gives part of the procedure as a scenario.

Table H.29 — Scenario H.22: Error detection and recovery of a transmission error by the PCD, Procedure 5

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$I(1)_0$(INF = the first chain of the answer to UT_TEST_COMMAND1)
$R(ACK)_1$ ('AB' CID CRC or 'A3' CRC)	→	
	←	$I(0)_1$(INF = the last chain of the answer to UT_TEST_COMMAND1, ~CRC)
$R(ACK)_1$	→	

H.4.4.3.7 Procedure 6 (ISO/IEC 14443-4:2018, 7.6.5.2)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends an erroneous block to the PCD.

d) The PCD shall send $R(NAK)_0$.

e) The LT remains Mute.

f) The PCD either shall send $R(NAK)_0$ or shall send an S(DESELECT) request or shall reset the operating field.

Table H.30 gives part of the procedure as a scenario.

Table H.30 — Scenario H.23: Error detection and recovery of a transmission error by the PCD, Procedure 6

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1, ~ CRC)
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC)	→	
	←	Mute
$R(NAK)_0$ or S(DESELECT) request or reset of the operating field	→	

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H.4.4.3.8 Procedure 7 (ISO/IEC 14443-4:2018, 7.6.7, Annex B, Scenario 14)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends an erroneous S(WTX) request.

d) The PCD shall send $R(NAK)_0$.

e) The LT sends a valid S(WTX) request.

f) The PCD shall answer with S(WTX) response.

g) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

h) The PCD is expected to transfer this response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

Table H.31 gives part of the procedure as a scenario.

Table H.31 — Scenario H.24: Error detection and recovery of a transmission error by the PCD, Procedure 7

PCD		LT
$I(0)_0$ (INF = UT_TEST_COMMAND1)	→	
	←	S(WTX) request, ~CRC
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC)	→	
	←	S(WTX) request
S(WTX) response	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND1)

H.4.4.3.9 Procedure 8 (ISO/IEC 14443-4:2018, 7.6.7, Annex B, Scenario 17)

Procedure 8 and Scenario H.25, which were defined in former editions of this document, are no longer present.

H.4.4.3.10 Procedure 9 (with chaining) (see ISO/IEC 14443-4:2018, Annex B, Scenario 20)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND2(causing 3 chains)) to the PCD.

b) The LT waits until the PCD sends an I-block $I(1)_0$ to the LT, with the INF field the first chain of the UT_TEST_COMMAND2.

c) The LT sends an erroneous $R(ACK)_0$.

d) The PCD shall send $R(NAK)_0$.

e) The LT sends $R(ACK)_0$.

f) The PCD shall send the next block $I(1)_1$ of the chain.

g) The LT sends $R(ACK)_1$.

h) The PCD shall send the last block $I(0)_0$ of the chain .

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i) The LT sends I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND2) to the PCD.

j) The PCD is expected to transfer this response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

In case the UT cannot force the PCD to use 3 chains to send the TEST_COMMAND2, modify the expected procedure to reflect the test purpose which is to make sure that the block numbering and the chaining are properly executed after transmission error at step c).

Table H.32 gives part of the procedure as a scenario.

Table H.32 — Scenario H.26: Error detection and recovery of a transmission error by the PCD, Procedure 9

PCD		LT
$I(1)_0$(INF = the first chain of the UT_TEST_COMMAND2)	→	
	←	$R(ACK)_0$, ~CRC ('AA' CID '00 00' or 'A2 00 00')[a]
$R(NAK)_0$ ('BA' CID CRC or 'B2' CRC)	→	
	←	$R(ACK)_0$ ('AA' CID CRC or 'A2' CRC)[a]
$I(1)_1$(INF = the second chain of the UT_TEST_COMMAND2)	→	
	←	$R(ACK)_1$ ('AB' CID CRC or 'A3' CRC)[a]
$I(0)_0$(INF = the last chain of the UT_TEST_COMMAND2)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND2)

[a] If the PCD frame contains a CID, the left option shall be used, else the right option shall be used.

H.4.4.3.11 Procedure 10 (with chaining) (see ISO/IEC 14443-4:2018, Annex B, Scenario 21)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends SEND_UT_APDU(UT_TEST_COMMAND2(causing 3 chains)) to the PCD.

b) The LT waits until the PCD sends an I-block $I(1)_0$ to the LT, with the INF field the first chain of the UT_TEST_COMMAND2.

c) The LT sends $R(ACK)_0$.

d) The PCD shall send an I-block $I(1)_1$ to the LT.

e) The LT remains mute.

f) The PCD shall send $R(NAK)_1$.

g) The LT sends $R(ACK)_0$.

h) The PCD shall send the previous I-block $I(1)_1$ to the LT.

i) The LT sends $R(ACK)_1$.

j) The PCD shall send the last block $I(0)_0$ of the chain.

k) The LT sends an I-block (containing some response UT_APDU with answer to the UT_TEST_COMMAND2) to the PCD.

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l) The PCD is expected to transfer this response UT_APDU back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

In case the UT cannot force the PCD to use 3 chains to send the TEST_COMMAND2, modify the expected procedure to reflect the test purpose which is to make sure that the block numbering and the chaining are properly executed after Mute at step e).”

Table H.33 gives part of the procedure as a scenario.

Table H.33 — Scenario H.27: Error detection and recovery of a transmission error by the PCD, Procedure 10

PCD		LT
$I(1)_0$(INF = the first chain of the UT_TEST_COMMAND2)	→	
	←	$R(ACK)_0$ ('AA' CID CRC or 'A2' CRC)[a]
$I(1)_1$(INF = the second chain of the UT_TEST_COMMAND2)	→	
	←	Mute
$R(NAK)_1$ ('BB' CID CRC or 'B3' CRC)	→	
	←	$R(ACK)_0$ ('AA' CID CRC or 'A2' CRC)[a]
$I(1)_1$(INF = the second chain of the UT_TEST_COMMAND2)	→	
	←	$R(ACK)_1$ ('AB' CID CRC or 'A3' CRC)[a]
$I(0)_0$(INF = the last chain of the UT_TEST_COMMAND2)	→	
	←	$I(0)_0$(INF = answer to UT_TEST_COMMAND2)

[a] If the PCD block contains a CID, the left option shall be used, else the right option shall be used.

H.4.4.3.12 Procedure 11 (with chaining) (see ISO/IEC 14443-4:2018, Annex B, Scenario 24)

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block $I(0)_0$ to the LT, with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends I-block $I(1)_0$ indicating chaining.

d) The PCD shall send $R(ACK)_1$.

e) The LT sends erroneous I-block $I(1)_1$ to the PCD.

f) The PCD shall send $R(ACK)_1$.

g) The LT retransmits an I-block $I(1)_1$ without error.

h) The PCD shall send $R(ACK)_0$.

i) The LT sends the last block of the chain in I-block $I(0)_0$ (of its response UT_APDU with answer to the UT_TEST_COMMAND1) to the PCD.

j) The PCD is expected to transfer the response UT_APDU, containing all chaining segments, back to the UT. Check at the UT that this response UT_APDU block is correctly accepted.

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Table H.34 gives part of the procedure as a scenario.

Table H.34 — Scenario H.28: Error detection and recovery of a transmission error by the PCD, Procedure 11

PCD		LT
$I(0)_0$(INF = UT_TEST_COMMAND1)	→	
	←	$I(1)_0$(INF = the first chain of the answer to UT_TEST_COMMAND1)
$R(ACK)_1$ ('AB' CID CRC or 'A3' CRC)	→	
	←	$I(1)_1$(INF = the second chain of the answer to UT_TEST_COMMAND1, ~ CRC)
$R(ACK)_1$ ('AB' CID CRC or 'A3' CRC)	→	
	←	$I(1)_1$(INF = the second chain of the answer to UT_TEST_COMMAND1)
$R(ACK)_0$ ('AA' CID CRC or 'A2' CRC)	→	
	←	$I(0)_0$(INF = the last chain of the answer to UT_TEST_COMMAND1)

NOTE Procedure 12 (scenario H.29: ISO/IEC 14443-4:2018, 7.5.5.2, rule 8), which was defined in former editions of this document, is no longer present.

H.4.4.3.13 Procedure 13

Use the following sequence immediately after procedure H.4.4.3.1:

a) The UT sends the SEND_UT_APDU(UT_TEST_COMMAND1) to the PCD.

b) The LT waits until the PCD sends an I-block to the LT with the INF field containing the UT_TEST_COMMAND1.

c) The LT sends an S(WTX) request with WTXM set to 0.

d) The PCD either shall send an S(DESELECT) request or shall reset the operating field.

e) Repeat steps a) to d) twice sending S(WTX) request in step c) with WTXM set to 60 and 63.

f) Repeat steps a) to d) sending a block with block type set to (01)b in step c).

H.4.4.4 Test report

The test is:

a) PASS only when the PCD's behaviour matches each procedure expected scenario, and

b) FAIL in any other case.

H.4.5 Handling of NAD during chaining

H.4.5.1 Scope

The purpose of this test is to ensure that the PCD maintains NAD in the proper way.

H.4.5.2 Apparatus

See H.1.

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H.4.5.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.

Use the following sequence:

a) Configure the LT as one supporting NAD.

b) Repeat procedure from Scenario H.26.

H.4.5.4 Test report

The test is:

a) PASS when the PCD use the NAD in the first packet of chaining only or does not use NAD at all, and

b) FAIL in any other case.

H.5 Continuous monitoring of packets sent by the PCD

H.5.1 Scope

The purpose of this test is to ensure that the PCD does not set any RFU bits in any sent frame to any value other than the default value documented for such RFU bit. Further, the test shall also ensure that no field is ever set to RFU value. The test shall also ensure that the R-block and the S-block match the protocol definitions and that rules given regarding the first byte of the packet are not violated.

H.5.2 RFU fields

RFU fields shall be continuously monitored during the testing and shall always be verified to contain the assigned default value. A test shall be FAIL and the IUT shall be declared non-conformant in case an RFU field is not set to its default value at any time.

H.5.3 RFU values

Functional fields shall be continuously monitored during the testing and shall always be verified to contain only functional values documented in the standard or proprietary values documented as such in the standard. A test shall be FAIL and the IUT shall be declared non-conformant in case a functional field is not set to said values at any time.

H.5.4 R-block

R-block shall never contain an INF field (see ISO/IEC 14443-4:2018, 7.2.2.1).

H.5.5 S-block

An S-block shall have either

a) an INF field of one byte only when it is a WTX block, or

b) an INF field of n byte(s) (n ≥ 0) when it is a PARAMETERS block, or

c) no INF field otherwise

(see ISO/IEC 14443-4:2018, 7.2.2.1).

H.5.6 PCB

PCB byte shall contain allowed values (see ISO/IEC 14443-4:2018, 7.2.2 and ISO/IEC 14443-4:2018, Annex C).

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H.5.7 Type A initialization frames

Type A initialization frames shall contain allowed values (see ISO/IEC 14443-3:2018, 6.4.1 and 6.5.3.2).

H.5.8 Apparatus

See H.1.

H.5.9 Procedure

During all test procedures and scenarios the logical content of the communication shall always be recorded.

H.5.10 Test report

a) The test is PASS when the PCD behaves as follows:

   1) The PCD sets default values to RFU bits in all sent frames.

   2) The PCD does not set RFU value to any field.

   3) The PCD does not violate the length rules of R-block and S-block.

   4) The PCD does not violate the first byte coding rules of Block and Frame (as summarized in ISO/IEC 14443-4:2018, Annex C).

b) The test is FAIL in any other case, e.g., when the PCD behaves as follows:

   1) The PCD sets other than the default value to at least one RFU bit in any sent frame.

   2) The PCD sets any field to a RFU value.

   3) The PCD violates the length rules of R-block or S-block.

   4) The PCD violates the first byte coding rules of Block and Frame (as summarized in ISO/IEC 14443-4:2018, Annex C).

H.6 Reported results

The results of the tests shall be reported in Table H.35 to Table H.39.

Table H.35 — Type A specific timing table

No.	Parameter	Reference	Min value measured [$1/f_c$]	Test result PASS or FAIL or N/A
1	Frame delay time PICC to PCD	ISO/IEC 14443-3:2018, 6.2.1.2		
2	Request Guard Time	ISO/IEC 14443-3:2018, 6.2.2		
3	Start-up Frame Guard Time	ISO/IEC 14443-4:2018, 5.3.5	—	—
	SFGI = 0			
	SFGI = 1			
	SFGI = 14			

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Table H.36 — Type B specific timing table

No.	Parameter	Reference	Measured values [etu] or [$1/f_s$] or [$1/f_c$] depending on the requirements		Test result PASS or FAIL or N/A
			Min	Max	
1	SOF low	ISO/IEC 14443-3:2018, 7.1.4			
2	SOF high	ISO/IEC 14443-3:2018, 7.1.4			
3	EOF low	ISO/IEC 14443-3:2018, 7.1.5			
4	Bit boundaries for	ISO/IEC 14443-3:2018, 7.1.1	—	—	—
	the falling edge(s)				
	the rising edge(s)				
5	EGT PCD to PICC	ISO/IEC 14443-3:2018, 7.1.2			
6	TR2	ISO/IEC 14443-3:2018, 7.1.7	—	—	—
	(b3,b2) = (00)b				
	(b3,b2) = (01)b				
	(b3,b2) = (10)b				
	(b3,b2) = (11)b				
7	Start-up Frame Guard Time	ISO/IEC 14443-3:2018, 7.9.4.7	—	—	—
	SFGI = 0				
	SFGI = 1				
	SFGI = 14				

Table H.37 — Reported results for Type A specific test methods

Test method from ISO/IEC 10373-6		Scenario numbers	Test result
Clause	Parameter	ISO/IEC 10373-6	PASS or FAIL or N/A[a]
H.2.1	Frame delay time PICC to PCD	Scenario H.27	
H.2.2	Request Guard Time		
H.2.3	Handling of bit collision during ATQA		
H.2.4	Handling of anticollision loop	Scenario H.1	
		Scenario H.2	
		Scenario H.3	
		Scenario H.4	
		Scenario H.34	
H.2.5	Handling of RATS and ATS	Scenario H.6	
		Scenario H.30	
H.2.7	Frame size selection mechanism	Scenario H.10	
H.2.8	Handling of Start-up Frame Guard Time	Scenario H.11	
H.2.9	Handling of the CID during activation by the PCD	Scenario H.12	
H.2.10	Handling of parity bit	Scenario H.31	

[a] In case a test has several procedures indicate PASS only in case every individual procedure is PASS.

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Table H.38 — Reported results for Type B specific test methods

Test method from ISO/IEC 10373-6		Scenario numbers	Test result
Clause	**Parameter**	**ISO/IEC 10373-6**	**PASS or FAIL or N/A[a]**
H.3.2	Frame size selection mechanism	Scenario H.13	
H.3.3	Handling of the CID during activation by the PCD	Scenario H.14	
		Scenario H.15	
H.3.4	Frame delay time PICC to PCD (TR2)	Scenario H.32d	
H.3.5	Handling of Start-up Frame Guard Time	Scenario H.33	
H.3.6	Type B PCD framing tests		
H.3.7	Handling of Protocol_Type RFU value		

[a] In case a test has several procedures indicate PASS only in case every individual procedure is PASS.

Table H.39 — Reported results for test method for logical operations of the PCD

Test method from ISO/IEC 10373-6		Scenario numbers		Test result	
Clause	**Parameter**	**ISO/IEC 10373-6**	**ISO/IEC 14443-4:2018, Annex B**	**Type A PASS or FAIL or N/A[a]**	**Type B PASS or FAIL or N/A[a]**
H.4.2	Handling of polling				
H.4.3	Reaction of the PCD to request for waiting time extension	Scenario H.17			
H.4.4	Error detection and recovery	Scenario H.18	Scenario 12 "Exchange of I-blocks"		
		Scenario H.19			
		Scenario H.20			
		Scenario H.21			
		Scenario H.22	Scenario 23 "PICC uses chaining"		
		Scenario H.23			
		Scenario H.24	Scenario 14 "Request for waiting time extension"		
			Scenario 17 "Request for waiting time extension"		
		Scenario H.26	Scenario 20 "PCD uses chaining"		
		Scenario H.27	Scenario 21 "PCD uses chaining"		
		Scenario H.28	Scenario 24 "PICC uses chaining"		
H.4.5	Handling of NAD during chaining				
H.5	Continuous monitoring of packets sent by the PCD				

[a] In case a test has several procedures, indicate PASS only when each individual procedure is PASS.

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Table H.40 — PCD RFU report

Name	PCD command	RFU field/value	Value		Test result
			Default	Not allowed	PASS or FAIL or N/A
Short frame Type A	REQA/WUPA	RFU values		All values specified as RFU in ISO/IEC 14443-3:2018, Table 3	
SEL coding	SEL	RFU values		All values specified as RFU in ISO/IEC 14443-3:2018, Table 7	
AFI	REQB/WUPB	RFU values		All values specified as RFU in ISO/IEC 14443-3:2018, Table 22	
PARAM	REQB/WUPB	RFU field (b8 to b6)	(000)b	All other values	
		RFU values in number of slots (b3 to b1)		(101)b (110)b (111)b	
Param 1	ATTRIB	RFU field (b2 to b1)	(00)b	All other values	
Minimum TR0	ATTRIB	RFU values (b8 to b7)		(11)b	
Minimum TR1	ATTRIB	RFU values (b6 to b5)		(11)b	
Param 2	ATTRIB	RFU values (b4 to b1)		All values from '9'((1001)b) up to 'F'((1111)b)	
Param 3	ATTRIB	RFU field (b8 to b4)	(00000)b	All other values	
Param 4	ATTRIB	RFU field (b8 to b5)	(0000)b	All other values	
		RFU value (b4 to b1)		'F'((1111)b)	

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Annex I
(normative)

High bit rate selection test methods for PCD

I.1 Scope

The purpose of this test is to verify that the PCD properly executes the procedures for selection of bit rates higher than $f_c/128$, as specified:

a) for Type A in ISO/IEC 14443-4:2018, Clause 5;

b) for Type B in ISO/IEC 14443-3:2018, Clause 7;

c) for Type A or Type B using S(PARAMETERS) in ISO/IEC 14443-4:2018, Clause 9

and that the PCD properly applies the selected bit rates in both directions.

I.2 Apparatus

The PCD-test-apparatus as specified in H.1 shall be used. It shall be configurable to change the bit rate during the test procedure and shall be able to measure the bit rate used by the PCD on each stage of this test procedure.

I.3 Procedure

I.3.1 Procedure for Type A

I.3.1.1 General

Place the PCD-test-apparatus into the field of the PCD.

The following procedure shall be repeated for all values of interface byte TA(1) defined in Table I.1.

a) Run through activation sequence as defined in ISO/IEC 14443-3.

b) The PCD shall send a RATS command as defined in ISO/IEC 14443-4.

c) The PCD-test-apparatus answers with a valid ATS including TA(1) according to Table I.1.

d) The PCD may optionally send a PPS with a valid parameter setting for PPS1 byte according to Table I.1.

e) If the PCD has sent a PPS then the PCD-test-apparatus acknowledges the received PPS with a valid PPS response.

f) The PCD shall send $I(0)_0$ block using the bit rate selected. This block may also be $I(1)_0$, or R(NAK) in case of PICC presence check Method 2 a) as described in ISO/IEC 14443-4:2018, 7.6.6.2.

g) The PCD-test-apparatus sends a valid response using the bit rate selected. Check, if the answer from the PCD-test apparatus is accepted by the PCD.

h) If needed, the PCD-test-apparatus shall carry out additional sequences to achieve the conditions for the next step.

i) In the subsequent polling cycle, the PCD shall use a bit rate of $f_c/128$.

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