



SURFACE VEHICLE INFORMATION REPORT

J1938™**JUL2015**Issued 1988-10
Revised 2015-07

Superseding J1938 MAY1998

(R) Product Development Process and Checklist for Vehicle Electronic Systems

RATIONALE

This report is a major update to the original one dated 1998. It is much more comprehensive in its scope and detail. The main purpose is to condense information from a number of sources relating to the design of electronic modules. It is especially useful for some new players on the automotive electronics scene who may not know how to sort the “wheat from the chaff” and what to focus on.

TABLE OF CONTENTS

1.	SCOPE	4
2.	REFERENCES	4
2.1	Applicable Documents	4
2.1.1	SAE Publications	4
2.1.2	Military Specifications (latest versions)	4
2.2	Related Publications	5
2.2.1	ISO Publications	5
2.2.2	CISPR Publications	5
2.3	Other Publications	5
2.4	Technical Papers	5
2.5	Books, Handbooks	6
3.	CONTEMPORARY DESIGN/VALIDATION PERSPECTIVE	6
3.1	Test Related Issues	7
3.2	Test Effectiveness Example	7
3.3	Cost Reductions (CR)	8
3.4	Trouble Not Indicated (TNI's)	8
3.5	Sample Sizes	8
3.6	Reliability Prediction	8
4.	ROBUSTNESS VALIDATION (RV) PROCESS	9
4.1	Preliminary Assessment	10
4.2	Development Stage	10
4.2.1	General	10
4.2.2	SAE J2628 (Characterization, Conducted Immunity) Summary	12
4.3	Design Validation (DV) Readiness Evaluation	12
4.4	Design Validation (DV)	12
4.5	Product Validation (PV)	13
4.6	Conformity, TNI	13
4.7	Example of RV Process Results	14
5.	DESIGN CHECKLIST FOR MODULES	14
5.1	Component Selection/Application	14

SAE Technical Standards Board Rules provide that: "This report is published by SAE to advance the state of technical and engineering sciences. The use of this report is entirely voluntary, and its applicability and suitability for any particular use, including any patent infringement arising therefrom, is the sole responsibility of the user."

SAE reviews each technical report at least every five years at which time it may be revised, reaffirmed, stabilized, or cancelled. SAE invites your written comments and suggestions.

Copyright © 2015 SAE International

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without the prior written permission of SAE.

TO PLACE A DOCUMENT ORDER: Tel: 877-606-7323 (inside USA and Canada)
Tel: +1 724-776-4970 (outside USA)
Fax: 724-776-0790
Email: CustomerService@sae.org
http://www.sae.org

SAE WEB ADDRESS:

**SAE values your input. To provide feedback
on this Technical Report, please visit
http://www.sae.org/technical/standards/J1938_201507**

5.2	Components, Specific Devices	15
5.2.1	Resistors	15
5.2.2	Capacitors	15
5.2.3	Connectors/Interconnects	15
5.2.4	Printed Circuit Boards (PCB's), General	15
5.2.5	Thick film substrates	17
5.2.6	Transistors, Diodes, MOSFET's	17
5.2.7	Linear (Op Amps, etc)	17
5.2.8	Digital (microprocessors, etc.)	18
5.3	Circuit Design Checklist	18
5.3.1	General	18
5.3.2	Module Inputs	19
5.3.3	Module Outputs	20
5.3.4	Power Supply Related	20
5.3.5	Electrical overstress	20
5.3.6	Circuit Tolerance/Analysis	21
5.4	Software	21
5.5	Diagnostics	22
5.6	Repairability	22
5.7	Environmental (Non EMC)	22
5.7.1	General	22
5.7.2	Thermal Considerations (Components/Assemblies)	22
5.7.3	Vibration/Shock Considerations (Components/Assembly)	23
5.7.4	Humidity/Splash/Dust Considerations (Components/Assemblies)	23
5.7.5	Burn In *	24
5.8	Electromagnetic Compatibility (EMC)	24
5.8.1	Component (Module) Level	24
5.8.2	PCB Layout Rules for EMC	25
5.9	Miscellaneous Manufacturing Process Checklist	29
6.	NOTES	30
6.1	Revision Indicator	30
APPENDIX A	Example of thermal cycle Accelerated Test	31
Figure 1	Relative Contributions	3
Figure 4.1	Design margin plot from J2628	12
Figure 5.1	Sine approximation of pulse train	25
Figure 5.2	Filter example	27
Figure 5.3	IC cap layout	27
Figure 5.4	Example BGA with multiple powers	28
Figure 5.5	IC development layout	28
Figure 5.6	Simplified switching power supply schematic	29
Table 4.1	Development tests	11
Table 4.2	Actual example of time savings using RV process (radio)	14
Table 5.1	Grid inductance	26
Table A.1	Temperature profile	31

FOREWARD

The traditional approach to electronic system product development and validation is inherently not capable of finding many contemporary issues. The degree of analysis, modeling, simulation, testing and experience of the design/test staff varies widely among different OEM's and vendors. Another major part of product development is validation in a number of areas such as Functionality, Electromagnetic Compatibility (EMC) and Environmental testing. Although much time and expense is spent, using traditional approaches often leads to "feel good" results since the product "passes". Such a false sense of security is misleading since such validation methods can have serious deficiencies. These deficiencies may prevent detection of the types of concerns that exist in today's automotive electronic products.

Many specs were written when automotive electronics was not mature (lots of issues). Environmental and EMC specs evolved over many years (lots of baggage, old practices). These test methods have many limitations and compromises not appreciated by contemporary practitioners - simple pass-fail criteria can result in non-value work (test issues that are not real world concerns).

System Pareto Analysis - Top 3 Root Causes (mature OEM, Vendor). See Figure

1. Requirements not correct or unspecified ("Unrequirements")
2. System-Interface Issues
3. Trouble Not Indicated (TNI)

Many processes focus on D & E instead of top 3. Environmental Specs are wear out mechanism oriented - focused on component, solder joint and mechanical reliability. Major advances in component reliability, design-process maturity and solder capability have placed these down on Pareto List.

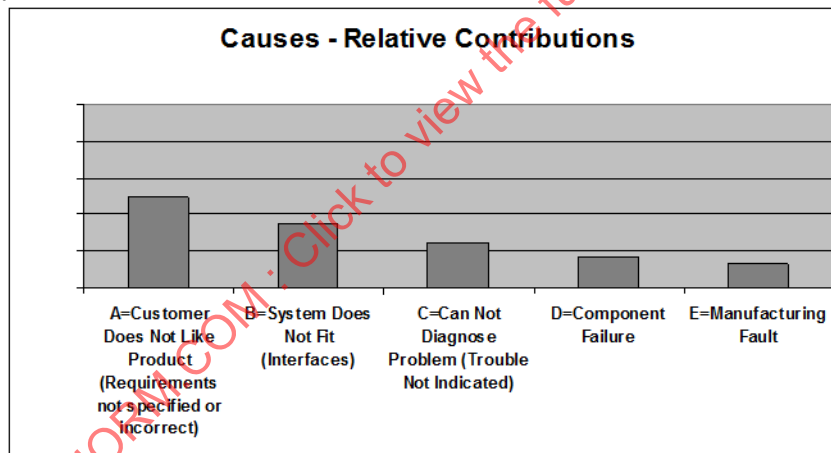


Figure 1 - Relative contributions

To provide information on a robust design process, a Handbook for Robustness Validation (SAE J1211) was recently published. It was developed by approximately 40 experts in the field (European and American).

It can be summarized by this quote from the SAE J1211 handbook.

"Robustness Validation relies first on knowledge-based modeling simulation and analysis methods to develop a highly capable design prior to building and testing physical parts; and then on test-to-failure (or acceptable degradation) and failure/defect susceptibility testing to confirm or identify robustness margins, to enable failure prediction and verify that manufacturing processes produce defect free parts. These techniques represent advancement beyond "test-to-pass" qualification plans which usually provide very little useful engineering information about failure modes, failure mechanisms and failure points".

To obtain a high degree of quality and reliability, a wide variety of subjects needs to be addressed when designing a vehicle electronic system. No single designer can be expected to have the experience necessary to consider all aspects of a design. Such experience is often spread throughout an organization and not concentrated on any one project. This report is meant to condense information from a number of sources to improve the quality and reliability of automotive electronics.

1. SCOPE

Since it is impossible to be all inclusive and cover every aspect of the design/validation process, this document can be used as a basis for preparation of a more comprehensive and detailed plan that reflects the accumulated "lessons learned" at a particular company. The following areas are addressed in this document:

1. Contemporary perspective including common validation issues and flaws.
2. A Robustness Validation (RV) process based on SAE J1211 handbook and SAE J2628.
3. Design checklists to aid in such a RV process.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of SAE publications shall apply.

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or +1 724-776-4970 (outside USA), www.sae.org.

SAE J551	Performance Levels and Methods of Measurement of Electromagnetic Radiation from Vehicles and Devices (30 to 1000 MHz)
SAE J1113	Electromagnetic Susceptibility Measurement Procedures for Vehicle Components (Except Aircraft)
SAE J1211	Handbook for Robustness Validation of Automotive Electrical/Electronic Modules
SAE J1455	Recommended Environmental Practices for Electronic Equipment Design in Heavy-Duty Vehicle Applications
SAE J1879	Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
SAE J2628	Characterization, Conducted Immunity

2.1.2 Military Specifications (latest versions)

Available from DODSSP, Subscription Services Desk, Building 4D, 700 Robins Avenue, Philadelphia, PA 19111-5094.

Mil-Std 202	Test Methods for Electronic and Electrical Component Parts
Mil-Std 810	Environmental Test Methods and Engineering Guidelines
Mil-Std 461	Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment.

2.2 Related Publications

The following publications are provided for information purposes only and are not a required part of this SAE Technical Report.

2.2.1 ISO Publications

Available from American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, Tel: 212-642-4900, www.ansi.org.

- ISO 11451 Vehicle Methods for Electrical Disturbances from Narrowband Radiated Electromagnetic Energy.
- ISO 11452 Electrical Disturbances by Narrowband Radiated Electromagnetic Energy, Component Test Methods.
- ISO 10605 Test Methods for Electrical Disturbances from Electrostatic Discharges.
- ISO 16750 Environmental Conditions and Testing for Electrical and Electronic Equipment.
- ISO 7637 Electrical Disturbance by Conduction and Coupling.

2.2.2 CISPR Publications

Available from American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, Tel: 212-642-4900, www.ansi.org.

- CISPR 25 Vehicles, Boats and Internal Combustion Engines, Radio Disturbance Characteristics, Limits and Methods of Measurement for the Protection of On-Board Receivers.

2.3 Other Standards

JEDEC (Joint Electron Device Engineering Council) Standards on electronic components, consumer electronics, electronic information, telecommunications, and internet security.

AEC (Automotive Electronics Council) Q100 (Failure Mechanism Based Stress Test Qualification for Integrated Circuits), Q101 (Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications), Q200 (Stress Test Qualification for passive Components) and other standards.

2.4 Technical Papers

1. IEEE EMC Symposium 2005, Comparison of ISO 7637 Transient Waveforms to Real World Automotive Transient Phenomena
2. Electrostatic Discharge Analysis of Multi-Layer Ceramic Capacitors, Cyrus Rostamzadeh , Hamidreza Dadgostar, Flavio Canavero, 2009 IEEE EMC Symposium.
3. Temperature and Voltage Variation of Ceramic Capacitors, or Why Your 4.7 μ F Capacitor Becomes a 0.33 μ F Capacitor, Mark Fortunato, Senior Principal Member of Technical Staff Maxim Integrated Products, Tutorial 5527
4. SAE 2009 - 01- 0294, Avoiding Electrical Overstress for Automotive Semiconductors by New Connecting Concepts, Christoph Thienel, Robert Bosch GmbH, Germany
5. A Fundamental Overview of Accelerated Testing Analytical Models, Hank Caruso, Abhijit Dasgupta, University of Maryland CALCE Center, College Park, Maryland, Journey of the Institute of IEST, Jan/Feb 1998, 1998 Proceedings Annual Reliability and Maintainability Symposium.
6. Comparison of Flex Cracking of Multilayer Ceramic Capacitors Assembled with Lead-Free and Eutectic Tin-Lead Solders, Mohammadreza Keimasi¹, Michael H. Azarian, and Michael Pecht

2.5 Books, Handbooks

1. Walker, The Design Analysis Handbook, ISBN 0-9641527-0-3. Provides a practical framework for integrating quality into the design process from start to finish. The methodology used is called Worst Case Analysis Plus (WCA+), a design-validation tool that demands thoroughness and analytical thinking by the user. A guide to assessing and validating circuit design. Presents processes and mathematical tools in a straightforward, real-world manner. Unique features of the approach include chapters on safety, bad science, and surviving high-pressure design projects.
2. Reinertsen, Managing the Design Factory, ISBN 0-684-83991-1. A methodical approach to consistently hit the "sweet spot" of quality, cost, and time in developing any product. Challenges many of the conventional approaches to product development - e.g., test failures are good (maximizes information), design reviews should not be done by part of team (independent evaluation by experts), etc. Full of practical techniques, concrete examples, and solid general principles, this is a real toolkit for product developers. Challenges the thinking of anyone involved in product development.
3. O'Conner, Kleyner, Practical Reliability Engineering, Ed 5, Wiley. With emphasis on practical aspects of engineering, this book has gained worldwide recognition through progressive editions as *the* essential reliability textbook. The fifth edition retains the unique balanced mixture of reliability theory and applications, thoroughly updated with the latest industry best practices.
4. Horowitz and Winfield, The Art of Electronics, ISBN 0-521-37095-7. Widely accepted as the authoritative text and reference on electronic circuit design, both analog and digital, this book revolutionized the teaching of electronics by emphasizing the methods actually used by circuit designers - a combination of some basic laws, rules of thumb, and a large bag of tricks. The result is a largely nonmathematical treatment that encourages circuit intuition, brainstorming, and simplified calculations of circuit values and performance.
5. Ott, Electromagnetic Compatibility Engineering, ISBN 978-0-470-18930-6. Completely revised, expanded, and updated version of Henry Ott's popular book "Noise Reduction Techniques in Electronic Systems". While maintaining and updating the core information such as cabling, grounding, filtering, shielding, digital circuit grounding and layout, and ESD that made the previous book such a wide success, this new book includes additional topics. Throughout the book, an emphasis is placed on cost-effective EMC designs, with the amount and complexity of mathematics kept to the strictest minimum.
6. Johnson, Graham, High Speed Digital Design, ISBN 0-13-395724-1. Focused on the field of knowledge lying between digital and analog circuit theory. The scope of the material covered includes signal reflection, crosstalk, and noise problems which occur in high speed digital machines (above 10MHz).

3. CONTEMPORARY DESIGN/VALIDATION PERSPECTIVE

Before developing a checklist, it is instructive to be aware of the limitations and history of automotive electronics validation to gain insight into why things are presently done in a certain manner. Such awareness is useful in the design process for a number of reasons including insight for making "hold or fold" decisions.

1. The traditional approach to product validation is to treat the different disciplines required separately. Such an approach often misses issues that cross discipline lines.
2. Market leaders know just "Meeting Spec" does not necessarily result in a quality product - Main goal is to satisfy the end customer and minimize field issues not just pass specs.
3. Component reliability and design practices have greatly improved over the early days of automotive electronics. Consequently, most electronic module issues are functionality, new design (including software) and workmanship related.

3.1 Test Related Issues

1. Originally, reliability for automotive electronics was poor so a lot of tests were “invented”. There were minimal design practices for automotive EMC.
2. As product complexity & technology grow the traditional “cookbook” approach is not effective at finding many real world concerns.
3. Testing methods have many limitations and compromises not appreciated by contemporary practitioners - don’t know when to “Hold or Fold”
4. Much testing addresses old issues with limited value add especially for modules that follow known basic design rules and are mature.
5. Different people looking at the same data can come up with quite different conclusions depending on their background, insight and flexibility.
6. Testing of representative modules often late in design cycle - need more simple development testing to identify issues early.
7. OEM test process is so complex, long and expensive that it diverts from “play” time to identify bugs early.
8. Simple pass-fail criteria (e.g., limit line) results in too much non value work (not real world issues).
9. Test Specs-Plans mainly “test for success” - cannot maximize information by maximizing success rate. Must have failures to maximize information.
10. Typical testing has major purpose of repeatability, not necessarily what is required to find real world issues (some tests require randomness).
11. Requirements validation (Hardware-Software) under ideal-pristine conditions. Does not sufficiently address system interactions, robustness. Many tests are idealized simulations of the real world.
12. There is such a large test infrastructure (equipment manufacturers, test labs, large OEM/Vendor departments) that it is extremely difficult to change present test methods and limits.
13. With a more focused plan (major emphasis on the analysis and development stages), overall test time and facilities can be reduced (> 50% possible) while being more effective and thorough.

"Testing alone is not sufficient for Design Verification ... Analysis compliments a test program by identifying problems that even the most rigorous testing can miss." (ref. The Design Analysis Handbook, Ed Walker).

3.2 Test Effectiveness Example

It is instructive to give an actual example of typical test method effectiveness. A study of 260 environmental testing anomalies over a 5 year time span for a major OEM supplier resulted in only 3 issues identified that would impact the field. Most issues = Test setup, unrepresentative module, limit incorrect, known concern before test, minor risk (would not result in field issue).

In a similar manner, field action case histories (not test issues), show that majority are functionality, design and workmanship issues.

3.3 Cost Reductions (CR)

Cost reductions are a necessary part of doing business but can be very expensive in the long run if not properly managed.

1. Overall cost save can be less than “booked” (engineering time-cost, warranty, field actions, customer satisfaction). One big recall can wipe out years of CR.
2. Diverts resources from original product. CR commonly > 50% of engineering resources.
3. Validation limited - often cookbook DV, test for success.
4. Best OEM's slowly introduce or phase-in radical new technology.

3.4 Trouble Not Indicated (TNI's)

TNI's are typically very high and can run over 50 % (sometimes > 80 %). One reason TNI's can be high is due to troubleshooting techniques at the dealer where part swapping may occur (once part taken from parts department, can't be returned).

Another reason they are so high is that field returns often use standard tests (e.g., environmental test such as thermal cycle) to try and identify the root cause. It is rare for these tests to identify root cause for reasons identified in section 3.1. In addition, the resources and time to find root cause are commonly not available. Often the root cause is a system issue which can be very difficult to investigate and requires expertise that crosses discipline boundaries. As a result a field return is often identified as TNI.

3.5 Sample Sizes

The preface in SAE J1211 puts sample size in perspective. By the mid 80's a test sample size of 6-24 units with zero failures is specified (90-95% reliability, confidence = 70-90%) which is about 5 to 20 failures / 10^6 hours. Not so good by today's standards. Today reliability is in ppm which translates to 0.05 failures / 10^6 hours range (test to pass). Reliability demonstration over 99.9 % would require thousands of units. It's evident that a smarter approach is required. Sample size, in most instances, do not need to be large for a number of reasons:

1. Most issues are functionality and design related so product responses are similar and can be found with fewer samples.
2. Large sample sizes divert attention from product evaluation (e.g., test complexity).
3. Use of focused testing (weaknesses via up-front analysis - tail testing) and measuring degradation (not just failures).
4. Allows increased monitoring, less facilities and less chamber loading (allows more focusing on product and not on test complexity "red herring" issues).
5. Combining stresses (e.g., thermal, electrical) also reduces sample size requirements.
6. Variables data (e.g., measuring degradation during test) requires fewer samples.
7. Use surrogate data from similar products to reduce number of tests.

3.6 Reliability Prediction

1. Electronics reliability predictions based on models can be non-value exercise if not used responsibly (e.g., no impact on design; just looking for a number).
2. From many years of automotive field experience, real issues would not be predicted from these prediction models.

3. Use of empirical models like Mil-Std 217 by automotive industry is limited. Typical Dept of Defense (DoD) use of Mil-Std 217F notice 2 and 217 Plus is limited to support logistics and analysis of alternate designs early in acquisition when empirical data on similar systems or from surrogate data sources are not available. The DoD also uses such methods as Physics of Failure, FMEA, reliability growth and reliability demonstration testing.
4. Life testing has limited capability since performed under conditions that often do not reflect the complexity of environmental stresses under end user operational conditions. The typical life test is done by making standard environmental tests longer (e.g., temperature cycling) and does not reflect the aforementioned complexity.
5. Only certain devices typically wear out or degrade - e.g., CD mechanism or Vacuum Fluorescent Display (VFD).
6. Since most electronics will not wear out in useful life of vehicle, should use degree of degradation as basis for life testing (e.g., idle current change, VFD brightness, change in design margins).
7. Robustness Validation process (section 4.0) more appropriate for 10yr/150k useful life estimation.
8. Using accelerating environmental testing has many limitations (ref 2.3.5). Based on idealistic equations with many assumptions.
 - Uses: Material trade-off studies, Comparisons of thermal and structural design alternatives, Order-of magnitude estimates of product wear-out rates, Evaluations of potential effects of possible design changes.
 - Risky uses: Exact predictions of product life, Precise contractual life requirements and warranty commitments, Generic assumptions for different products, Applying cyclic and steady-state models for transient load damage conditions

"It's much more important to have a reliable product than it is to claim to have a reliable product; i.e., the electronics reliability prediction paradigm is obsolete. Electronic product failures will be primarily due to process, workmanship and design problems." (ref. The Design Analysis Handbook, Ed Walker).

4. ROBUSTNESS VALIDATION (RV) PROCESS

There are many sources of information relating to electronics reliability and robustness. Some good examples are listed in section 2.4.1 to 2.4.3. However, this section focuses on the SAE J1211 Handbook. This recently published document addresses the Robustness Validation (RV) process that is gaining support (mostly in Europe at this time).

Much of this information can be obtained at <http://www.zvei.org/RobustnessValidation>. One can see from the following list of major sections, that it is quite comprehensive.

1. Information and communication flow
2. Mission profile
3. Knowledge matrix
4. Analysis, modeling and simulation
5. Intelligent testing
6. Manufacturing process robustness and its evaluation
7. Robustness indicator factor
8. Appendix A, B, C

A similar document, SAE J1879, was also recently issued which addresses the RV process at the semiconductor level.

At this point it is appropriate to make a distinction between verification and validation.

Verification: The evaluation of whether or not a product, service, or system complies with a regulation, requirement, specification, or imposed condition. It is often an internal process.

Validation: The assurance that a product, service, or system meets the needs of the customer and other identified stakeholders. It often involves acceptance and suitability with external customers.

Example:

- Verification = make sure shoe is size 10
- Validation = make sure foot is not size 8

These distinctions can be confusing and are often used interchangeably. For a module vendor, it is typical for validation testing to be basically the same as verification but just later in the design cycle on production units. For purposes of this document we will stick with the terms used in the SAE J1211 Handbook (Robustness Validation = prototype/development, design validation and production validation).

4.1 Preliminary Assessment.

Before RV can commence the following must be done to focus-tailor the process plan.

1. Review customer requirements, cost, timing
2. Evaluate process capability.
3. Determine mission profile: Determine electrical-mechanical-EMC environment, usage profile, life expectancy.
4. Analysis: Electrical (e.g., circuit worst case analysis - WCA), Thermal, Mechanical, New Technology, Changes, FMEA, quality history, etc
5. Identify potential weak spots to focus testing.
6. Design Reviews: Expert independent review.
7. Determine sample sizes: This is a major consideration since it determines test facility and staffing requirements. Sample size, in most instances, do not need to be large in the RV process for a number of reasons (Ref 3.5)

4.2 Development Stage

4.2.1 General

Of all the stages in RV, this is the most important for the following reasons:

1. Allows maximum flexibility to experiment
2. Allows sufficient reaction time
3. Stage where failures are good (maximizes information)
4. Should push product beyond spec limits to determine design margins.

Development testing may not be a large part of the typical validation plan. Typical plans usually focus on verifying that a product functions in a known way with a given set of input conditions (i.e., meets requirements). What is often missed are those other unwanted things that result from complex dynamic interactions of hardware-software, timing, throughput, electrical excursions, extreme operation, system interactions and interfaces. To be effective, the DUT should be tested in a sub-system configuration using realistic loads and interfaces.

The testing at this stage verifies product robustness in Electrical, Mechanical and Climatic categories. Potential weaknesses should be identified by stressing the product well beyond the specification limits. Failures are good since it maximizes the amount of information generated (ref 2.4.2). Failure analysis determines whether the results warrant a change in the design or are unrealistic (do not reflect the field environment).

In addition, to promote such evaluation, these development test methods should include simple and low cost techniques that require minimum lab facilities. They should be done with the design engineer present since some are not simply pass-fail tests but require product knowledge to evaluate the results. A list of such tests are summarized in the following table (most from the SAE J1211 handbook appendix B and/or SAE J2628). This table was developed by analyzing many actual field issues and devising methods to identify them. Such evaluations early in product development minimizes surprises later where it's much more difficult and costlier to change.

Table 4.1 - Development tests

Type	ID	Name	Description
General	G10	Internal Inspection (1)	Solder Joints, Connectors, etc. Use 10x magnifier.
	G20	Functionality (1)	Emphasis on Transition States.
Characterization	C10	Design Margins (1, 2)	Ramp Voltage, Upper-Lower Operating Limits (UOL, LOL) at Multiple Temps. Include C-20 During Test.
	C20	Interruptions, Transients (1, 2)	Random Power Interruptions, Transients
	C30	Power Dips (1, 2)	Dips From V-nom to (1-10) Volts, Various Pulse Widths
	C40	Current Draw (1, 2)	Monitor True RMS Current During Power On-Off, Multiple Temps.
	C50	Switch Input Noise (1, 2)	Random Noise Created by Chattering Relay
	C60	Overvoltage (4)	Monitor True RMS Current at 19V, 24V, Multiple Temps.
	C70	Reverse Battery Current (4)	Monitor True RMS Current at -14V
	C80	Oscillator Function (3)	Momentary Short Oscillator, Multiple Temps. Verify Automatic Recovery
Failure Modes	FM10	Shorts to Power-Ground (4)	0.3 Ω short, Monitor Current During Shorts
	FM20	Load Faults (1)	Opens, Partial Shorts in Certain Loads
	FM30	Leakage Resistance (1)	Pins tolerant to 50K Ω to Power or Ground
	FM40	Sneak Paths, Opens (1)	Open Power-Ground to DUT (at DUT)
EMC-RF	EMC10	RF Immunity (4)	Bulk Current Injection or Hand Held Transmitters (e.g., Cell Phone)
	EMC20	Emissions (4)	Current Probe on Harness or AM/FM Digital Radio
	EMC30	ESD (1, 4)	Pins = +/- 10kV, Controls = +/- 15kV
	EMC40	Crosstalk (4)	Noise From Chattering Relay Coupled by Parallel Wire
Environmental	ENV10	Moisture Immunity (1)	Apply Windex Directly to PCB. Verify No Combustion.
	ENV20	Mechanical Disturbance (1)	Tap with Plastic Hammer, Drop (15cm), Flexing of PCB
	ENV30	Resonant Search (1)	Identify Potential Vibration Issues
	ENV40	High Temp Exposure (1)	Monitor Suspect Hot Points. Hot Box if Applicable
	ENV50	Combined Envir Exposure (1)	High Temp-Humidity-Shock
(1) In SAE J1211 (2) In SAE J2628 (3) Not in SAE J1211, SAE J2628 or others (4) In other standards.			

4.2.2 SAE J2628 (Characterization, Conducted Immunity) Summary

This document establishes methods for characterizing the robustness of vehicle electronic modules to certain electrical and temperature environmental stresses using methods designed to address the deficiencies inherent in other commonly used validation methods. It is an extension of the philosophy detailed in the SAE J1211 handbook.

Addresses Major Issues:

1. Design Margins (see figure below).
2. Voltage Interruptions and Transients made by chattering relay (creates randomness) and inductance. Existing ISO type transients (e.g., ISO 7637) not realistic or effective (ref 2.3.1)
3. Voltage Dropouts and Dips due to poor connections and power system electrical loading.
4. Current Draw under a number of conditions.
5. Switch Input Noise, addresses non ideal characteristics of module mechanical switch type inputs (contact bounce and open/closed resistance).

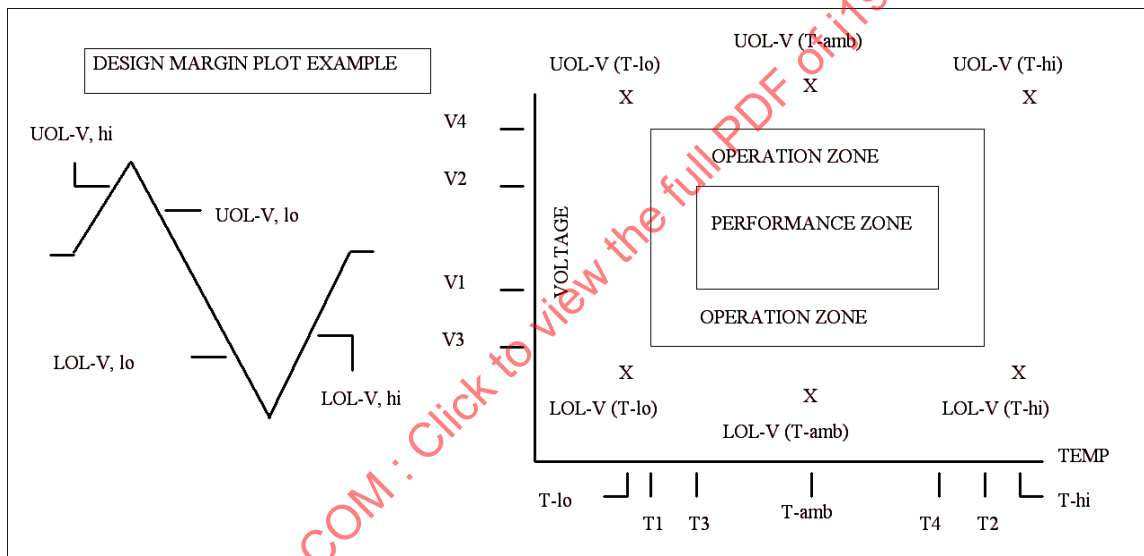


Figure 4.1 - Design margin plot from J2628

4.3 Design Validation (DV) Readiness Evaluation

Prior to DV testing, an assessment of the product shall be conducted by an independent "expert(s)". This expert must be knowledgeable in product design, manufacturing processes and testing. The result of this review is either OK or a list of minor-major issues. If the product is not considered ready, it can still proceed to DV but only after a risk assessment. With limited resources, such an approach is required to avoid a high retest rate. From past experience, this retest rate can be up to 80% if the product is not really ready for testing but just adhering to a project time schedule.

4.4 Design Validation (DV)

DV is done to assure the adequacy of the design in the vehicle environment. This is the stage that just meeting spec is considered sufficient ("test for success" oriented). However, testing beyond the spec limits is an essential part of this stage and addresses sample variability. However, only moderately exceed the specification limits (within physical limits of the module). This is one of the major difficulties in promoting the RV process since the traditional thinking is not accustomed to going beyond spec limits and the potential for anomalies that must be addressed - most OEM's and suppliers want "first pass success" (easy metric for performance reviews and meeting tight time schedules).

The DV is more focused on weaknesses or changes discovered in Analysis and Development stages. It references existing standards as much as possible, e.g., ISO 16750.

4.5 Product Validation (PV)

PV is done to assure that initial production parts as manufactured still meet design intent. Many RV concepts can be used to develop a more effective and efficient PV plan. Historically, the PV is similar or the same as DV. The process presented here emphasizes differences between DV and PV modules and the critical manufacturing processes that can affect design intent. PV should not be a repeat of DV, it should focus on what's different from DV and failure modes created by the manufacturing process. Such a process can save considerable time and cost.

4.6 Conformity, TNI

The purpose of these procedures is to sample a product on a periodic basis for concerns that may not be detected through the normal practices and test procedures at the electronics manufacturing plant including End of Line testing. Conformity test methods are used to track trends over time so that changes to the design, parts or processes can be detected. Besides periodic testing, using control charts on existing key parametric data can be used to detect changes. The development tests (ref 4.2) can be useful for this stage since they are relatively quick and effective. Similar procedures are also applicable for TNI investigation. Also consider use of Environmental Stress Screening (ESS) tailored to reduce infant mortality and precipitate process problems.

Some examples of the type of changes that may occur are:

1. IC Die shrink *
2. IC molding compound change.
3. New supplier.
4. Solder process/cleanliness change.
5. Part substitution with "equivalent" part. There can be differences in parts not reflected in the datasheet.
6. Counterfeit parts

* Early die shrinks with identical functions to reduce only the die size because of costs are no longer common. Newer chips contain mostly more complex functions with smaller structures which can't be shrunk without critical influences to their intrinsic parameters.

In addition:

1. Closed loop failure analysis and corrective action plan must be in place - concern description, define root cause, containment, corrective actions, verification of containment/corrective actions, prevent recurrence.
2. Analyze warranty returns - "non defective returns" often > 50% of returns. Normal reliability testing will often not find problems. Testing must emphasize module functionality (continuously monitored).

4.7 Example of RV Process Results

Table 4.2 - Actual example of time savings using RV process (radio)

	OEM Original Request (1)	RV – OEM Approved (2)
Analysis	Moderate	Similar but focused test plan
Development Test Time	None	24 h
DV Sample Size	12	6
DV Cumulative Test Time	3000 h	400 h
Durability Life Test	4800 h	300 h
Overall Test Time	7800 h	700 h
Note: Software validation and EMC additional		

(1) Cookbook approach (2) Mature product

5. DESIGN CHECKLIST FOR MODULES

The main purpose of this checklist is to provide a guide for ensuring that the many aspects of an electronic systems design and process are addressed. Such a list would be useful for design reviews, "fresh eyes" reviews and for education/training.

5.1 Component Selection/Application

One of the first major concerns for a reliable design is part selection and application. Vendor part quality is a major reliability concern. Efforts to use best in class suppliers cannot be overemphasized.

1. ____ Identify each aspect of the mission profile - environmental, durability.
2. ____ Identify critical reliability components and determine their special requirements - derating, screening, handling, failure mode response.
3. ____ Identify components to avoid – e.g., variable resistors if fixed can be used, hand inserted parts if auto insertion viable.
4. ____ Define part specifications - part sheets should reflect use in actual automotive environment. Spec sheets do not typically specify design margins from specified value so contact manufacturer.
5. ____ Determine which parts must be automotive grade - e.g., AEC Q100, 101, 200.
6. ____ Identify if semiconductor cooper wire bonding used - less proven for harsh, long life and high reliability applications.
7. ____ Address Electrostatic Discharge - most sensitive components, precautions, handling.
8. ____ Determine component tolerance assumptions for worst case analysis.
9. ____ Establish part availability and authenticity - program to avoid counterfeits.
10. ____ Define vendor quality/reliability control program.
11. ____ Determine Acceptable Quality Level (AQL) in Parts/Million (PPM) required - how verified.
12. ____ Address part obsolescence.

5.2 Components, Specific Devices

5.2.1 Resistors

1. ____ Consider failure modes - opens most common.
2. ____ Consider tolerances - initial, aging, over temp range.
3. ____ Use in Safe Operating Area. Derate for power dissipation voltage and temperature.
4. ____ Consider ESD sensitivity.

5.2.2 Capacitors

1. ____ Consider failure modes - e.g., shorts, value change most common
2. ____ Consider tolerances - initial, aging, temp (e.g., electrolytics can change dramatically over time/temperature).
3. ____ Use in Safe Operating Area - derate for DC operating voltage, transients, temperature, ripple current.
4. ____ Do not use less than 0805 size SMD for ESD control on module inputs/outputs (ref 2.3.2).
5. ____ Ensure that PCB flexure does not damage SMD caps (ref 2.3.6).
6. ____ No tantalum caps on "unlimited energy" nodes (battery).
7. ____ Use datasheet to determine actual ceramic capacitor value when DC applied (ref 2.3.3). For example, 0805, 10V cap value decreases over 50 % at 5V DC.

5.2.3 Connectors/Interconnects

1. ____ Address reliability concerns, failure modes - connections are high on list of reliability issues.
2. ____ Address "Dry" circuits - low voltage, film buildup (low current may = gold plating).
3. ____ Consider insertion force.
4. ____ Avoid IC sockets.
5. ____ Account for voltage drops, intermittent connections, aging (increased resistance).
6. ____ Address fretting corrosion, and sealing requirements.

5.2.4 Printed Circuit Boards (PCB's), General

1. ____ Address reliability concerns, failure modes - opens, shorts, flexing/warpage.
2. ____ Avoid use of edge connectors (if applicable) to wiring harness, reliability subject to many parameters (e.g., plating uniformity, tolerances).
3. ____ Determine material and copper thickness (1oz, 2oz, 3oz) required to meet current and thermal requirements.
4. ____ Maximum temp of PCB and solder joints must not be exceeded.
5. ____ Address thermal considerations - e.g., max temp rating, matching of thermal expansions, localized heating = delamination.
6. ____ Address manufacturability constraints, allow for process cleanliness (shunt resistance).

7. ____ Address EMC layout criteria (see section 5.8.2).
8. ____ Address dendritic growth mitigation.

5.2.4.1 Through Hole Technology (TH)

NOTE: In the following layout rules, specific values listed are a starting point (will vary between different OEM's, vendors and processes).

NOTE: 1 mil = 0.001 inch.

1. ____ For single sided PCB, conductor width = 12 mils minimum (conservative), 8 mil (realistic).
2. ____ For double sided PCB, power/ground conductor width = 16 mil minimum. Signal conductor width = 12 mil minimum (conservative), 8 mil (realistic).
3. ____ Plated through hole (PTH) pad diameter = or > 2 x hole diameter.
4. ____ PTH diameter = or > 40 % of material thickness.
5. ____ PTH double sided - hole diameter 10 to 28 mil > lead diameter.
6. ____ PTH single sided - hole diameter 5 to 20 mil > lead diameter.
7. ____ Do not use sharp corners for conductor traces - stress concentration point.
8. ____ Web between holes - for punched holes = 60 mil minimum or 1.5 times hole diameter whichever is greater. For drilled holes = 35 mil minimum.
9. ____ Warpage - balance copper density within 30 % both sides. For large copper areas (e.g., ground plane), use voids at random intervals.
10. ____ Use thermal relief around component holes in large copper areas.
11. ____ Auto insertion - hole diameter > 15 mil over lead diameter min.
12. ____ Lead formed double kink parts for PTH - euroform type preferred, stress relief, trapped gas in PTH area.
13. ____ For clinched leads, use tear drop pads (more bonding area).
14. ____ Solder mask - types (screened, dry film).

5.2.4.2 SMD Technology

Type 1 - All SMD's

Type 2 - SMD's and/or TH on top, SMD's and/or TH on bottom of PCB

Type 3 - TH on top, SMD's on bottom of PCB.

1. ____ Vias, test pads not part of attachment pad.
2. ____ Lead coplanarity (flatness) < 4 mil
3. ____ Underside leaded component clearance > 10 mil for solvent action.
4. ____ Component orientation relative to soldering direction.
5. ____ Tombstoning prevention.

5.2.5 Thick film substrates

1. ____ Address reliability concerns, failure modes.
2. ____ Address thermal considerations - e.g., max temp rating, matching of thermal expansions.
3. ____ Address manufacturability constraints.
4. ____ Address EMC layout criteria (see section 5.8.2).
5. ____ Resistors - 10 to 200 ppm/C, $\pm 15\%$ tolerance typical (untrimmed). Top hat resistors more susceptible to high voltage arcover.
6. ____ Conductor - palladium silver = 0.035 ohms/sq., 0.08 with solder coating, 250 - 800 ppm/ °C.
7. ____ Conductor signal width/spacing normally 0.5 mm.
8. ____ Component attachment pad configuration.
9. ____ Minimize crossovers and number of resistive paste values.
10. ____ Conductor concerns
11. ____ Silver migration - silver + electrolyte + moisture = dendritic growth of silver (.020 " gap in minutes with 0.5V bias). Preventive measures = cleaning, potting.
12. ____ Galvanic action - Alum + electrolyte + moisture = battery with palladium or silver (2.5 to 2.8V). Preventive measures = cleaning, potting.
13. ____ Intermetallics - Palladium + tin = poor adhesion of pal silver films (conductor adhesion). Control solder.

5.2.6 Transistors, Diodes, MOSFET's

1. ____ Address reliability concerns, failure modes
2. ____ Consider tolerances - initial, aging, temp
3. ____ Consider diode/zenor response time to transients.
4. ____ Use within Safe Operating Area (SOA) - derate for voltage, current, power dissipation, temperature.
5. ____ Diodes connected to battery must have minimum of 200V rating.
6. ____ Use transistor base to emitter resistor - ensures stable off state.
7. ____ Consider collector to housing stray capacitance for switching circuits - may cause radiated emissions.
8. ____ Limit base/gate drive - fast drive into saturation creates noise, balance Electromagnetic Interference (EMI) with heat dissipation.
9. ____ Consider ESD on MOSFET's - one of major failure modes.

5.2.7 Linear (Op Amps, etc)

1. ____ Consider single supply limitations - input range usually does not include power supply rails, output loading determines voltage range.
2. ____ Do not overdrive inputs - may drive output to power supply rail (transmits power supply noise).

3. ____ High gain amplifier - stability, oscillations, stray capacitance and inductance varies with temperature/sample.
4. ____ Use Bode gain/phase plot analysis to determine stability margin.
5. ____ Differential amps - consider all sources of unbalance to ground, DC and AC (e.g., capacitors, source impedance).
6. ____ Differential amps limited in rejection of common mode signals at higher frequencies.
7. ____ Use op amp internal compensation capacitor, if accessible, for filtering (acts as non linear filter).
8. ____ Voltage follower latch up - input levels too high.
9. ____ Avoid high impedances ($> 100k \Omega$).

5.2.8 Digital (microprocessors, etc.)

1. ____ Consider fanout limitations - e.g., loading affects propagation delays especially for CMOS.
2. ____ Verify logic levels compatible over min. & max. temperature/specification limits.
3. ____ Maximize logic levels margins (e.g., $V_{low \max}$ and $V_{high \min}$).
4. ____ CMOS - latchup when input $>$ power supply or $<$ ground.
5. ____ Microprocessor clock - verify operation, including start up, under all temperature and power supply transitions.
6. ____ Microprocessor - address reset, low voltage inhibit, I/O pin assignment, A/D inputs, interrupts, timer/PWM.
7. ____ Be aware of any differences that may exist between devices used for development and production.
8. ____ Verify outputs remain in predetermined state through all power up-down sequence.

5.3 Circuit Design Checklist

5.3.1 General

1. ____ Implement Design Process (see section 4)
2. ____ Identify critical characteristics from customer perspective - Quality Functional Deployment (QFD).
3. ____ Conduct Fault Tree Analysis - Module, Subsystem, System (before circuit design).
4. ____ Conduct Failure Modes and Effects (FMEA) analysis - Module, Subsystem, System level (after circuit design).
5. ____ Conduct criticality analysis (severity/probability of occurrence) - module, subsystem, system level.
6. ____ Define limited operation strategy (e.g., powertrain limp home).
7. ____ Consider that wiring harness/connector reliability greatly affects module warranty.
8. ____ Address design for manufacturability.
9. ____ Address design for testability.
10. ____ Consider that breadboards may aggravate problems - long leads, poor ground(s).
11. ____ Determine use of discrete vs. custom circuits - cost, reliability, volume tradeoffs. For custom circuits, use pessimistic cost/timing.

12. ____ Determine redundancy requirements for critical circuits.
13. ____ Use bookshelf circuits where possible.
14. ____ Maximize use of proven circuits.
15. ____ Minimize number of parts.
16. ____ Maximize use of standard parts and widest tolerances.
17. ____ Use slowest speed technology consistent with function.
18. ____ Where possible, include hysteresis on analog/digital circuits.
19. ____ Terminate unused inputs to I.C.'s.
20. ____ Consider relay precautions - e.g., diode increases dropout time, contact arcing, transients, contact sticking.
21. ____ Determine potting, conformal coating requirements - where used, types, limitations. Subject to manufacturing variability if not carefully controlled.
22. ____ Limit standby (idle) current – beware of sneak paths when installed in vehicle..
23. ____ Determine load power management strategy - when different loads turned on/off as voltage varies.
24. ____ For calculating maximum power/ground currents consider lamp inrush, motor stalls, motor reversing, load dump, etc.
25. ____ Allow for impedance buildup during system life.
26. ____ Is module tolerant to “hot plugging” (ref 2.3.4).
27. ____ Tolerance to “soft shorts” (e.g., 0.5 Ω instead of 0 Ω).
28. ____ Define load power management (how system/module should respond in various voltage ranges from less than 6V to over 24V).

5.3.2 Module Inputs

1. ____ Protect for shorts to ground/power.
2. ____ Switch requirements - consider contact material/pressure, type of connector, minimum voltage/current for oxidation burn through (dry circuits).
3. ____ Allow for contact resistance, shunt resistance on mechanical switches (e.g., series = 50 Ω , parallel = 50k Ω). Also address values for elastomeric and solid state switches.
4. ____ Allow mechanical switch bounce time of 50-100 ms.
5. ____ Maximize input thresholds for noise immunity.
6. ____ Maximize input filtering considering maximum signal information delay, minimum signal pulse width to be recognized, fastest signal rate of change (dV/dT).
7. ____ Verify shared sensors compatible between systems - i.e., one sensor to multiple modules.

5.3.3 Module Outputs

1. ____ Protect for shorts to ground/power.
2. ____ Verify inductive driver transient protection.
3. ____ Output driver current source vs. current sink considerations - current source has same failure mode (wiring short or open).
4. ____ Limit high current actuator transition times (without overheating) - generates noise, wiring harness ringing.
5. ____ H - Bridge driver - ensure both drivers in each leg not on simultaneously during transitions.

5.3.4 Power Supply Related

1. ____ Verify circuits compatible with run - start - run cycle (starting) et al.
2. ____ Verify power up/down sequence over temperature.
3. ____ Consider overvoltage, under voltage, reverse voltage, load dump.
4. ____ Address power supply protection schemes.
5. ____ Address power supply regulator response time - not too fast or may be noise sensitive.
6. ____ Verify stability over temp - step response on input and output load.
7. ____ Verify stability with chosen output cap over temp (test to failure with physical resistance in series with cap)
8. ____ Power supply capacitor design - e.g., aluminum electrolytic voltage/temperature, ripple calculations, aging.
9. ____ Avoid voltage divider circuits, if used consider worst case power supply voltages.
10. ____ Minimum current draw may deregulate power supply.
11. ____ Consider that two power supplies may cause latch up if not tracking.
12. ____ For mixed technologies (e.g., CMOS, TTL), power up/down may produce errors due to different valid/invalid levels.

5.3.5 Electrical overstress

1. ____ Address ignition arc over design considerations for underhood applications.
2. ____ Address transient protection - Resistor, Capacitor, R/C, clamps (e.g., MOV, zener, diode).
3. ____ All circuits connected to main power, or through loads to main power, must withstand electrical overstress.
4. ____ Shutdown circuits must have fast response.
5. ____ Load dump, often overdesigned if other parallel loads (e.g., inductive loads, other modules) not considered during validation testing.
6. ____ Address ESD protection: Often misanalyzed as electrical overstress. Part (e.g., IC) protection limited - too slow (ESD < 5 ns.). Use Resistor, Capacitor, R/C, clamps - consider high peak voltage.
7. ____ Part ESD part rating does not relate to module test – completely different setup and coupling mechanism. Must test in circuit configuration.

8. ____ Verify minimum part parameter shift after ESD test.
9. ____ Do ESD before environmental testing - ESD creates walking wounded that may fail when exposed to other stress.

5.3.6 Circuit Tolerance/Analysis

1. Conduct circuit/tolerance analysis:
 - Use combination of Worst Case Analysis (WCA), Probabilities, Sensitivities, Risk Assessment and Design
 - Centering.
 - Monte Carlo method - determines "likely" performance, useful for complex circuits.
 - Design of Experiments, Taguchi methods.
2. Determine simulation requirements - Realistic assumptions, must correlate with bench, not substitute for analysis.
3. Determine how to address reliability prediction/estimation (ref 3.6) if customer requires.
4. Conduct sneak circuit analysis.

5.4 Software

1. ____ Use modularization.
2. ____ Optimize decoupling with other software modules.
3. ____ Design for testability.
4. ____ Determine documentation requirements.
5. ____ Allow sufficient time for testing and debug - can be as much as design and coding.
6. ____ Determine software module testing - simulation on mainframe.
7. ____ Define static (change inputs manually) bench testing of system (total program).
8. ____ Define dynamic (many combinations of inputs) design verification.
9. ____ Address fault tolerance - e.g., inputs within realistic limits (e.g., dV/dT, dFreq./dT, edges, change in A/D counts), revert to old data, ignore, try again.
10. ____ Define watchdog timer strategy and implementation.
11. ____ Define low voltage reset strategy.
12. ____ Define software noise immunity strategies and limitations.
13. ____ Define switch contact bounce strategy.
14. ____ Determine software development tools - portable engineering and calibration consoles.
15. ____ Determine vehicle testing program.

5.5 Diagnostics

1. ____ Determine what functions to check - assign probability/severity index.
2. ____ Determine diagnostic troubleshooting procedures - philosophy, documentation.
3. ____ Diagnostics considered in warranty analysis.
4. ____ Define built in monitor circuits.
5. ____ Determine warning indicator requirements - e.g., instrument panel light.
6. ____ Address intermittents - how to precipitate, store in non volatile memory.
7. ____ Define self test methodology - factory and field service.
8. ____ Determine test equipment requirements.
9. ____ Define software memory allocation.

5.6 Repairability

1. ____ Determine level (module replace vs. sub-module replace).
2. ____ Consider module partitioning for repair.
3. ____ Consider cost models based on warranty forecasting.
4. ____ Factor accessibility - harder to replace item within system will have better warranty.
5. ____ Address, remanufacturing (if applicable), rework considerations, including vehicle In-Plant repair.

5.7 Environmental (Non EMC)

5.7.1 General

The most important thing to consider in this category is to focus the testing on the weak points identified in the design review. In addition, it should be realized that just meeting specification only provides a minimal amount of information. Testing should use the robustness validation philosophy to find the design margins.

5.7.2 Thermal Considerations (Components/Assemblies)

1. ____ Temperature has a major effect on reliability. In fact, as the temperature of a system rises, thermal failures almost completely overweigh failures from other causes.
2. ____ Conduct mission profile of thermal environment (underhood, passenger compartment, etc.) - start temperature (heat, cold soak), warm up time, operational temperature (range, rate of temperature change, frequency of change), number of cycles, cooling effects.
3. ____ Determine assembly (module) temperature environment vs. reliability - field experiences.
4. ____ Conduct component (resistor, capacitor, transistor, diode, etc) thermal analysis - worst case analysis (electrical loading, environment), heat sinking, derating (safety margins).
5. ____ Conduct assembly (module) thermal analysis - worst case analysis (electrical loading, environment), heat sinking, derating (safety margins).
6. ____ Consider that thermal analysis using thermal resistance values is best case - does not consider non linearity (hot spots), interface bonds < 100 % of area.

7. ____ Conduct thermal testing evaluation - e.g., thermocouple critical areas in module and test under worst case electrical loading and environment in temperature chamber. Vehicle evaluation shall also be done (temperature chamber, wind tunnel, etc).
8. ____ Consider different expansion coefficient stresses - potting, conformal coating, Surface Mount Devices (SMD's), Leadless Chip Carriers (LCC's), PCB interfaces, etc.
9. ____ Define rules (thermal) for mounting components.
10. ____ Define rules (thermal) for mounting assemblies (modules).
11. ____ Address thermal shock (splash, cold start) - typical failure modes.
12. ____ Identify critical thermal components and their special requirements.
13. ____ Define thermal stress test for Development, Design/Production Validation, Conformity (ref 4.2 to 4.6).
14. ____ Appendix A gives example of accelerated thermal cycle test.
15. ____ Consider that combined thermal stress with other tests (e.g., thermal, vibration, humidity, voltage) more realistic.
16. ____ Define testing sample size (ref 3.5).

5.7.3 Vibration/Shock Considerations (Components/Assembly)

1. ____ Conduct mission profile of vibration/shock environment (underhood, passenger compartment, etc.) - conditions (bumps/potholes, road vibration, handling, rail shock), type (sine, random, complex), frequency range, amplitude/Power Spectral Density (PSD), axis, duration.
2. ____ Address stresses on components, bonds, mounting brackets, etc. - concerns, typical failure modes.
3. ____ Define rules for mounting components - e.g., part size/mass vs. mounting technique.
4. ____ Conduct CAE modeling prior to testing.
5. ____ Define module mounting techniques - consider mounting bracket effects (e.g., resonances).
6. ____ Consider resonances - conduct resonant search, failure modes, determine solutions.
7. ____ Define vibration test for Development, Design/Production Validation, Conformity (ref 4.2 to 4.6)..
8. ____ Define shock test for Development, Design/Production Validation, Conformity (ref 4.2 to 4.6).
9. ____ Conduct vibration/shock testing before climatic testing (if done separately).
10. ____ Consider that vibration/shock combined with temperature cycling, humidity more realistic.
11. ____ Define testing sample size (ref 3.5).

5.7.4 Humidity/Splash/Dust Considerations (Components/Assemblies)

1. ____ Address component/assembly sealing - gasketing, potting, etc.
2. ____ Address connector integrity - type of connector (open, sealed, greased, etc).
3. ____ Determine failure modes - shunt or series impedance.
4. ____ Define thermal stress test for Development, Design/Production Validation, Conformity (ref 4.2 to 4.6).

5. ____ Consider that more realistic if combined with temperature cycling, vibration.
6. ____ Define testing sample size (ref 3.5).

5.7.5 Burn In *

1. ____ Determine need, component vs. assembly or both - field correlation, experiences, cost analysis.
2. ____ Determine component burn-in requirements - which ones, more stress than assembly, minimizes rework. If ppm failure rates low, burn-in may make worse (handling, ESD).
3. ____ Determine assembly burn-in requirements - facilities, thermal mass test considerations.
4. ____ Define test conditions - elevated temperature and voltage accelerates failure modes (different times for different failure modes). Static, dynamic operation.
5. ____ Determine optimum burn-in empirically - time vs. temperature/voltage failure rates.
6. ____ Consider combined powered thermal cycle and burn-in.

* Burn-in, as we know it from the past, is no longer a general key for getting rid of early failures.

But today's memories, at least for automotive, do need a so called run-in for about 20hrs to bring weak memory cells to break-down. The largest memory suppliers, have hundreds of ovens for this step, which includes the final test of the devices.

5.8 Electromagnetic Compatibility (EMC)

5.8.1 Component (Module) Level

1. ____ Define Radiated Immunity requirements:
 - a. Low RF level (25 volts/meter) - represents low power (<10 watts) transmitters located in/near vehicle. Also Radio, TV, Amateur, Land Mobile, etc in vicinity of vehicle
 - b. Moderate RF level (50 volts/meter) - represents nearby transmitters (30-100 watts), low power on-board transmitters in close proximity to electronics
 - c. High RF level (100 volts/meter) - represents high power (100 watt) on-board transmitters or transmitters very close to module (e.g., cell phone near center stack display).
 - d. Test procedures - SAE J1113, ISO 11452, OEM
2. ____ Define Conducted Immunity requirements:
 - a. Normally operation range = 10 to 16V (at battery) - Note charging system voltage vs. temp.
 - b. Reverse battery = -14V, includes servicing and vehicle assembly plant conditions.
 - c. Overvoltage - Failed alternator regulator (19-20v), double voltage jump start (24V).
 - d. Cold start = Dips to 5 to 6V (low impedance)
 - e. Voltage dropouts - Contact bounce, ignition switch rotation, intermittent connections (high impedance)
 - f. Vehicle electrical system noise (e.g., Alternator ripple, load dump, switch arcing, inductive transients, groundshifts).